NOVATEK
聯 詠 科 技

Data Sheet

NT51008M

1536 ch Source Driver with LVDS TCON

For 1024RGBx768/600 TFT LCD

V0.1

Preliminary Spec

INDEX

Revision History

NT51008M Specification Revision History			
Version	**Content**	**PAGE**	**Date**
0.1	New release	All	2013/03/31

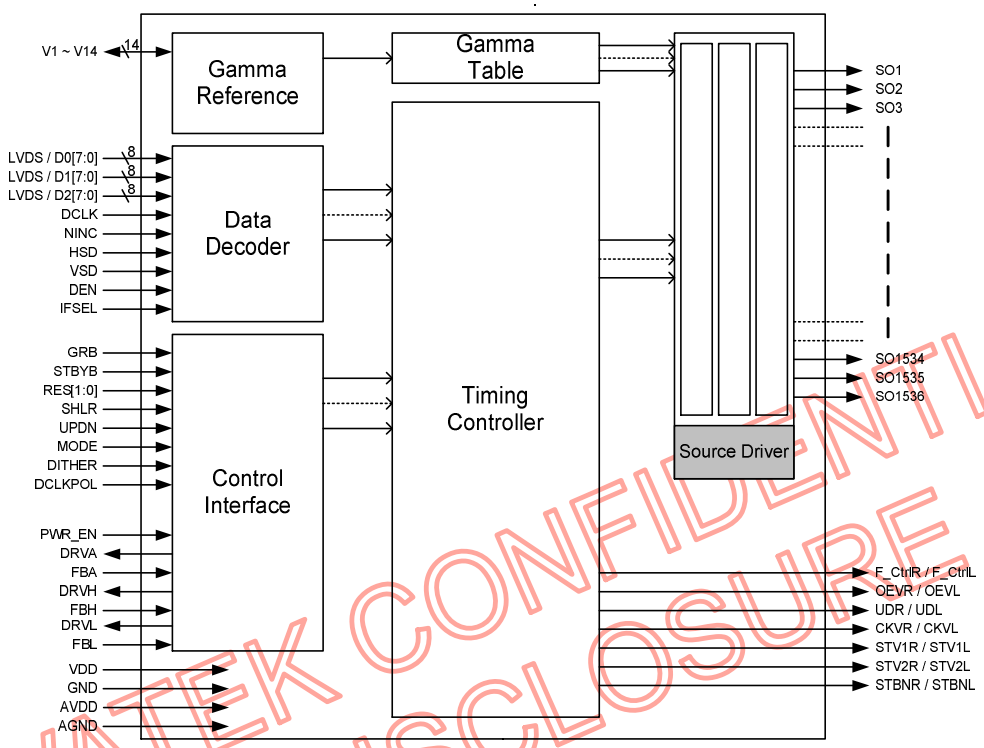
Features

- Special design for 1024RGBx600 TFT LCD Panel with LVDS/TTL interface
- Integrate 1536 channel source driver with single or dual gate function
- Support cascade function with bidirectional shift control (CMOS signal)
- Support panel resolution (HxV) : 1024(RGB) x 768 , 1024(RGB) x 600 , 800(RGB) x 600 , 800(RGB) x 480
- 8-bit resolution 256 gray-scale with Dithering (6 bits DAC + 2 bit FRC or HFRC)
- Support Pin Control function for Up/Down, Left/Right … control
- Power for digital circuit(VDD): 2.3V ~ 3.6V
- Power for analog circuit(AVDD): 8V ~ 13.5V
- Operating frequency : 71 MHz (Max.)
- Embedded Gamma Table for special custom request
- V1~V14 for adjusting Gamma correction
- 1 + 2 dot inversion architecture
- Built-In PWM controller for AVDD , Charge pump for VGH / VGL , and VCOM buffer
- Built-In CABC function
- Built-In AUTO pattern
- Built-In SDRRS function
- Support no_clock detection
- COG package
- Chip size = 25000um x 700um
- Output bump pitch = 15um

General Description

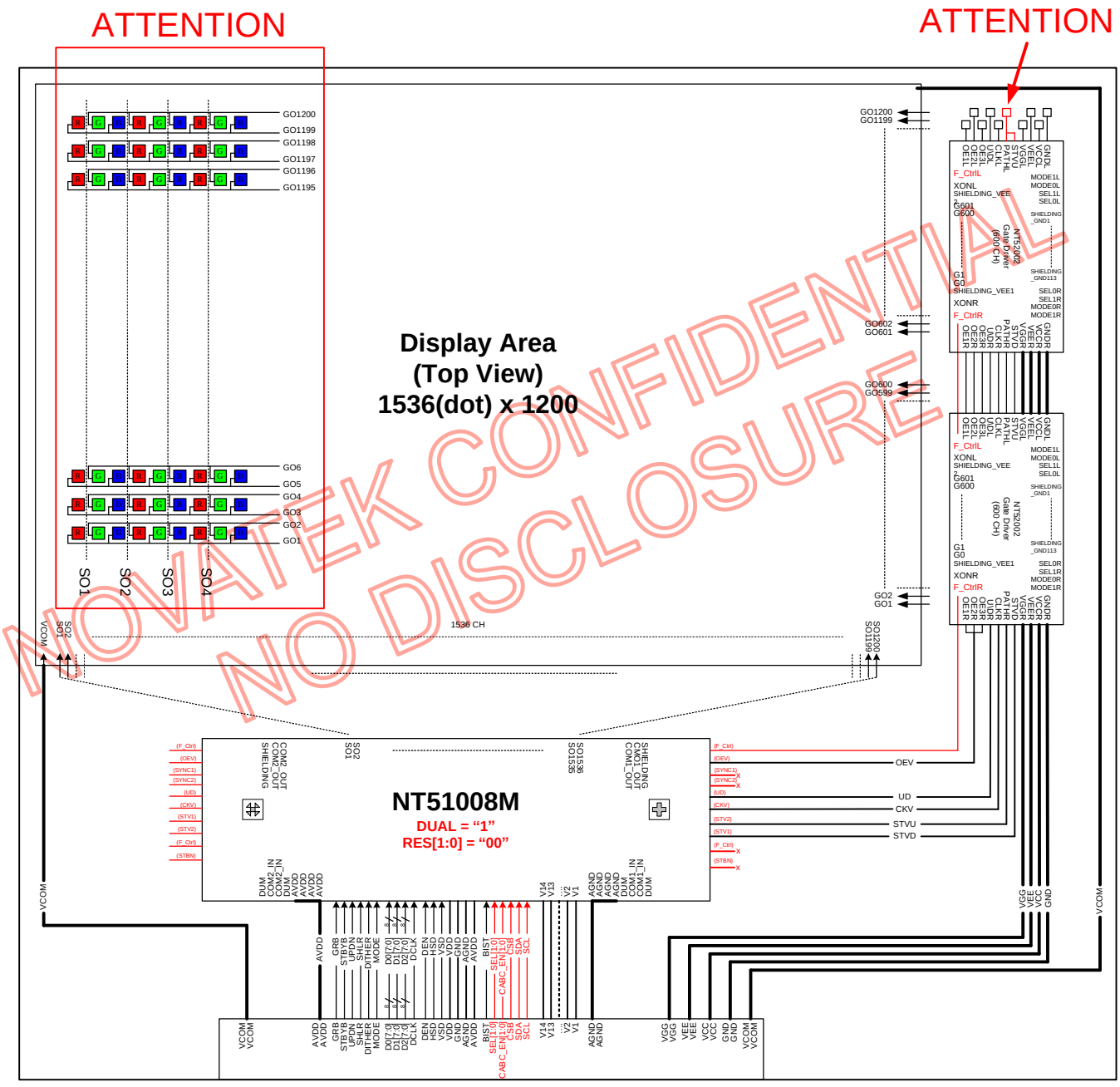
The NT51008M is a highly integrated solution for small size to middle size a-Si TFT-LCD panels. This chip integrates 1536ch dual gate mode source driver with LVDS and parallel RGB input interface . This chip is special designed for low cost UMPC application.

Function Block Diagram

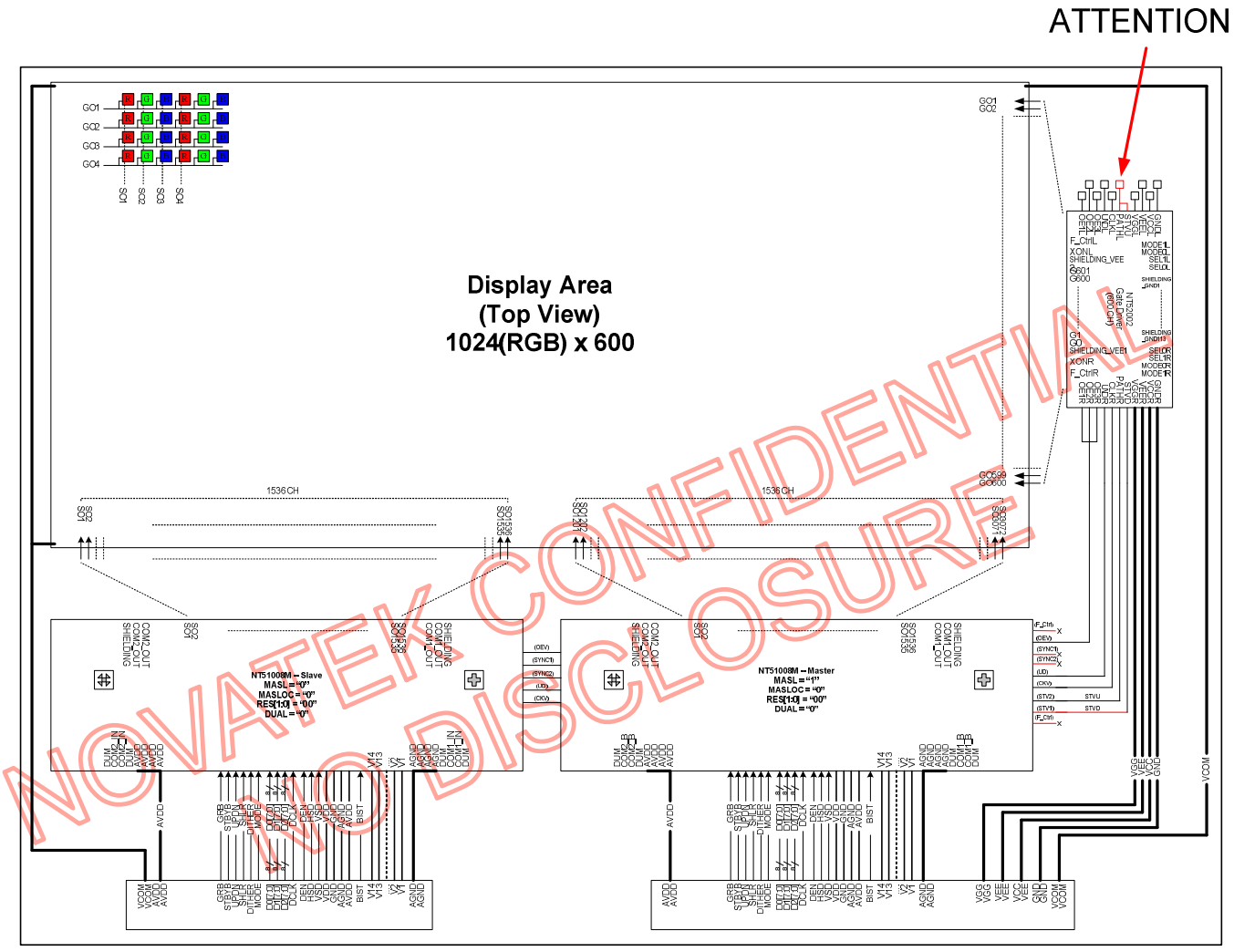


Application Block Diagram

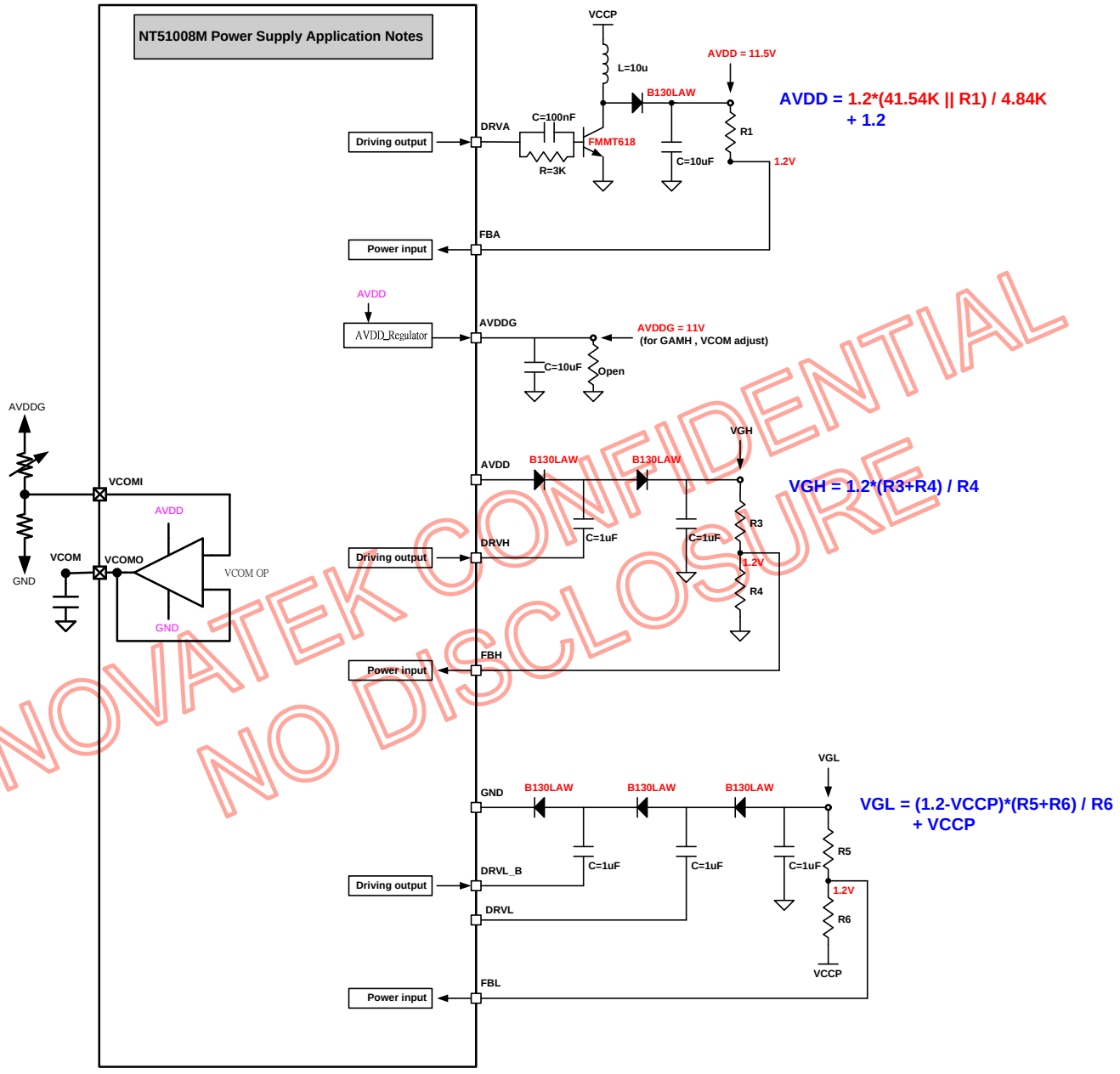
1. Dual Gate



2. Cascade with Two-FPC

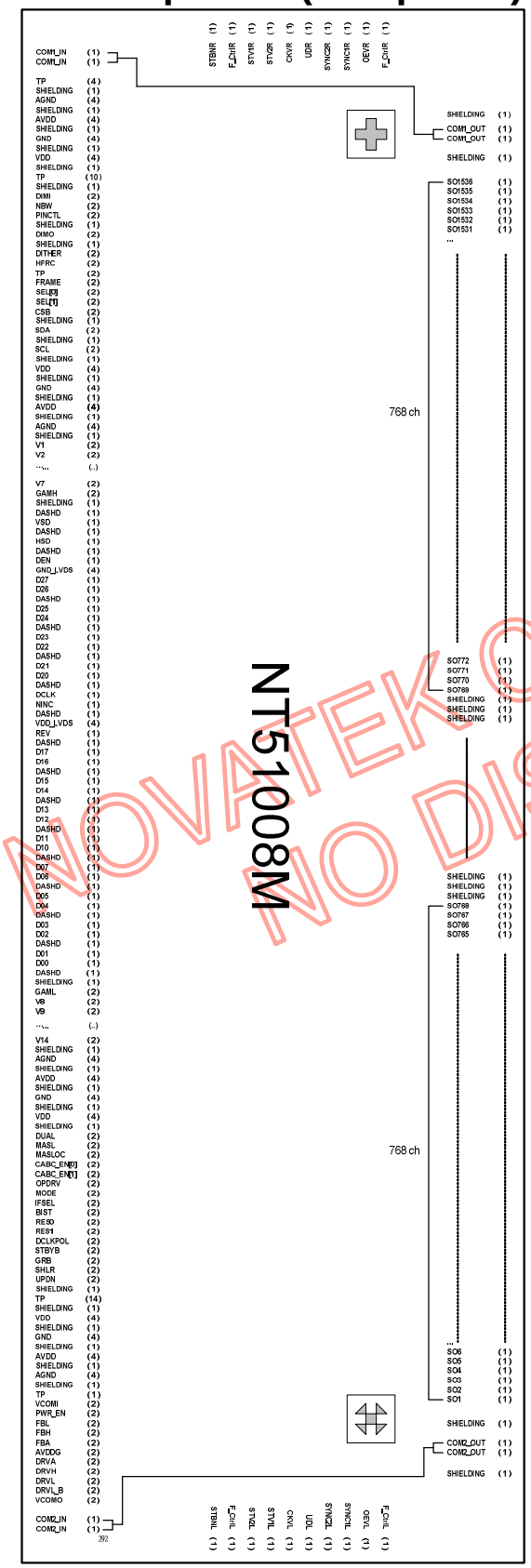


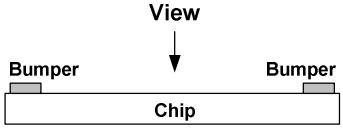
Application Power Circuit



Note : 1. VCCP must be 3V~5V and bigger than VDD
2. The value of R1~R6 is suggested to be more than 10K ohm

Pad Sequence (bump side)





Pin Descriptions

<table>
<tr><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>D07~D00
D17~D10
D27~D20</td><td>I</td><td>LVDS or Parallel RGB data Input. Select by “IFSEL” pin.
<table>
<tr><th>Pin name</th><th>TTL input mode
IFSEL = L</th><th>LVDS input mode
IFSEL = H</th></tr>
<tr><td>D2[0], D2[1]</td><td>B[0], B[1]</td><td>NIND0, PIND0</td></tr>
<tr><td>D2[2], D2[3]</td><td>B[2], B[3]</td><td>NIND1, PIND1</td></tr>
<tr><td>D2[4], D2[5]</td><td>B[4], B[5]</td><td>NIND2, PIND2</td></tr>
<tr><td>D2[6], D2[7]</td><td>B[6], B[7]</td><td>NIND3, PIND3</td></tr>
</table>
LVDS 6 bit data input : PIND[2:0], NIND[2:0].
D[07:00] = R[7:0] data; D[17:10] = G[7:0] data; D[27:20] = B[7:0] data.
For TTL 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to GND.
Note : D07~D00 → SO1 , SO4 … SO1531 , SO1534
D17~D10 → SO2 , SO5 … SO1532 , SO1535
D27~D20 → SO3 , SO6 … SO1533 , SO1536
Please note the relation between RGB data and Color Filter sequence</td></tr>
<tr><td>DCLK</td><td>I</td><td>Clock Input pin for LVDS or TTL mode. Select by “IFSEL” pin.
<table>
<tr><th>Pin name</th><th>TTL input mode
IFSEL = L</th><th>LVDS input mode
IFSEL = H</th></tr>
<tr><td>DCLK</td><td>DCLK</td><td>PINC</td></tr>
</table></td></tr>
<tr><td>NINC</td><td>I</td><td>Negative LVDS differential clock input.</td></tr>
<tr><td>HSD</td><td>I</td><td>Horizontal Sync input for TTL mode. Negative polarity.
(In LVDS interface , used as 6-bit/8-bit input select .
Connected to FPC and pull low
HSD = L , 8-bit ; HSD = H , 6-bit)</td></tr>
<tr><td>VSD</td><td>I</td><td>Vertical Sync input for TTL mode. Negative polarity.
(In LVDS interface , connected to FPC and pull low)</td></tr>
<tr><td>DEN</td><td>I</td><td>Data Input Enable. Active High to enable the data input bus under “DE Mode”.
Normally pull low.</td></tr>
<tr><td>MODE</td><td>I</td><td>DE / SYNC mode select under TTL mode. Normally pull high
H : DE mode. L : HSD/VSD mode.</td></tr>
<tr><td>IFSEL</td><td>I</td><td>TTL and LVDS Interface selection. Normally pull low
IFSEL = L : TTL interface
IFSEL = H : LVDS interface</td></tr>
<tr><td>RES[1:0]</td><td>I</td><td>Display resolution selection. Normally pull low
RES[1:0] = “01”, for 1024(RGB)*768 display resolution(dual or cascade)
RES[1:0] = “00”, for 1024(RGB)*600 display resolution(dual or cascade) (Default)
RES[1:0] = “10”, for 800(RGB)*600 display resolution(dual or cascade)
(601~936 channel disable)
RES[1:0] = “11”, for 800(RGB)*480 display resolution(dual or cascade)
(601~936 channel disable)</td></tr>
<tr><td>DITHER</td><td>I</td><td>Dithering function enable control. Normally pull low.
In LVDS 6-bit mode , IC don’t care DITHER and HFRC setting.
DITHER = “1”, Enable internal dithering function
DITHER = “0”, Disable internal dithering function. If in LVD 8-bit mode or TTL mode, IC will bypass D01/D00 , D11/D10 , D21/D20 .</td></tr>
</table>

HFRC	I	H-FRC selection. Normally pull low HFRC = H : H-FRC enable HFRC = L : H-FRC disable If DITHER = "0" , disable dithering function(H-FRC and FRC disable)
DCLKPOL	I	Input clock edge selection. Normally pull low CLKPOL = "1", Latch data at DCLK rising edge. CLKPOL = "0", Latch data at DCLK falling edge. (Default)
DUAL	I	Dual Gate function enables control. Normally pull high DUAL = "1", Enable Dual Gate Function. (Default) DUAL = "0", Disable Dual Gate Function Note: Cascade function will be disabled under "dual gate" mode!!
V1 ~ V14	I	When INTERNAL Gamma Table is used, GAMH tied to AVDDG via resistor for PWR_EN = H , enable PWM or tied to AVDD for PWR_EN = L , disable PWM GAML tied to GND and V1~V14 pad are un-used. When using external gamma voltage, GAMH and GAML are floaging , and V1~V14 are the external gamma correction points. The voltage of these pins must be: AGND<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1< AVDD .
GAMH	I	When INTERNAL Gamma Table is used, GAMH tied to AVDDG via resistor for PWR_EN = H , enable PWM or tied to AVDD for PWR_EN = L , disable PWM. Otherwise floating.
GAML	I	When using INTERNAL Gamma Table , tied to GND . Otherwise floating.
GRB	I	Global reset pin. Active Low to enter Reset State. Normally pull high. Suggest to connecting with an RC reset circuit for stability.
STBYB	I	Standby mode, Normally pulled high. STBYB = "1", normal operation STBYB = "0", timing controller, source driver will turn off, all output are High-Z
MASL	I	Master and Slave Mode selection. Normally pull high. MASL = "H", for Master mode. (Default Mode) MASL = "L", for Slave mode. Only the Master chip will issue the Gate and Cascade control signal.
MASLOC	I	Master location definition pin. Normally pull low. MASLOC = "L", Master locate on right side (Panel top view). (Default Mode) MASLOC = "H", Master locate on left side (Panel top view).
SHLR	I	Source Right or Left sequence control. Normally pull high. SHLR = "L", shift left: last data = S1←S2←S3.....←S1536 = first data. SHLR = "H", shift right: first data = S1→S2→S3.....→S1536 = last data.
UPDN	I	Gate Up or Down scan control. Normally pull low. UPDN = "L", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. UPDN = "H", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
BIST	I	Normal Operation/BIST pattern select. Normally pull low BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation
NBW	I	Normally black or normally white setting. Normally pulled low. NBW = H : Normally black NBW = L : Normally white
REV	I	Controls whether the data of D00~D27 are inverted or not, normally pulled low. When "REV"=1 these data will be inverted. EX. "00" → " 3F", "07"→ " 38", "15"→ "2A", and so on.

<table>
<tr><td>FRAME</td><td>I</td><td>Frame inverse or not select. Normally pulled low
FRAME = “1”, Uniform
FRAME = “0”, Frame inverse (Default)</td></tr>
<tr><td>SEL[1:0]</td><td>I</td><td>Gate on sequence select. Normally pull low
<table>
<tr><th>SEL[0]</th><th>SEL[1]</th><th>Pin control function</th></tr>
<tr><td>1</td><td>1</td><td>Z+ Ƨ</td></tr>
<tr><td>1</td><td>0</td><td>Ƨ</td></tr>
<tr><td>0</td><td>1</td><td>⧹</td></tr>
<tr><td>0</td><td>0</td><td>Z</td></tr>
</table></td></tr>
<tr><td>OEVR/OEVL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>SYNC1R/SYNC1L</td><td>O</td><td>CABC and BIST sync control</td></tr>
<tr><td>SYNC2R/SYNC2L</td><td>O</td><td>CABC and BIST sync control</td></tr>
<tr><td>UDR/UDL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>CKVR/CKVL</td><td>O</td><td>Gate driver control signal (CABC and BIST sync control)</td></tr>
<tr><td>STV1R/STV1L</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>STV2R/STV2L</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>STBNR/STBNL</td><td>O</td><td>Gate driver control signal</td></tr>
<tr><td>F_CtrlR/F_CtrlL</td><td>O</td><td>Gate driver control signal (For special Gate on sequence).
NOTE : In Cascade structure , let this pin floating
In Dual Gate structure , connect this pin to gate driver’s F_Ctrl .
And setting gate driver’s SEL[1:0] to “00”.</td></tr>
<tr><td>CABC_EN[1:0]</td><td>I</td><td>CABC H/W enable pin. Normally pull low.
When CABC_EN=”00”, CABC OFF. (Default mode)
When CABC_EN=”01”, User interface Image.
When CABC_EN=”10”, Still Picture.
When CABC_EN=”11”, Moving Image.</td></tr>
<tr><td>DIMI</td><td>I</td><td>Brightness control signal. Normally pull high</td></tr>
<tr><td>DIMO</td><td>O</td><td>Backlight dimmer signal for external controller.
DIMO = “0”, Turn off external backlight controller
DIMO = “1”, Logical control signal to turn on external backlight controller
NOTE : If CABC OFF , DIMO = DIMI . Else DIMO is controlled by CABC</td></tr>
<tr><td>PINCTL</td><td>I</td><td>Enable pin control function. Normally pull high
PINCTL=”0”, Disable pin control function and enable 3-wire control register.
Following pin setting will be inactive:
MODE, RES[1:0], DITHER, HFRC, DCLKPOL, SHLR, UPDN, BIST, NBW, FRAME, SEL[1:0], CABC_EN[1:0], OPDRV, PWR_EN
PINCTL=”1”, Enable pin control function.
NOTE: The related 3-wire control register bit control will be disabled under PINCTL=”1”.</td></tr>
<tr><td>OPDRV</td><td>I</td><td>Source OP driving selection. Normally pull low
OPDRV = H : 133%
OPDRV = L : normal</td></tr>
<tr><td>CSB</td><td>I</td><td>Serial communication chip select. Normally pull low</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Serial communication data input. Normally pull low</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial communication clock input. Normally pull low</td></tr>
<tr><td>AVDD</td><td>PI</td><td>Power supply for analog circuits</td></tr>
<tr><td>AGND</td><td>PI</td><td>Ground pins for analog circuits</td></tr>
<tr><td>VDD</td><td>PI</td><td>Power supply for digital circuits</td></tr>
</table>

GND	PI	Ground pins for digital circuits
VDD_LVDS	PI	LVDS power
GND_LVDS	PI	LVDS ground
PWR_EN	I	POWER enable. Normally pull low PWR_EN = H , enable PWM , Charge pump and VCOM buffer PWR_EN = L , disable PWM , Charge pump and VCOM buffer
FBA	VI	PWM controller feedback input. (for AVDD)
DRVA	O	PWM output driver signal for the boost converter (for AVDD)
FBH	VI	Charge Pump controller feedback input. (for VGH)
DRVH	O	Charge Pump driver signal for the boost converter (for VGH)
FBL	VI	Charge Pump controller feedback input. (for VGL)
DRVL	O	Charge Pump driver signal for the boost converter (for VGL)
DRVL_B	O	Inverse of DRVL(for VGL)
VCOMI	I	VCOM buffer in
VCOMO	O	VCOM buffer out
AVDDG	O	AVDD regulate output
SO1~SO1536	O	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
COM1_IN COM1_OUT	S	Internal link together between input side and output side.
COM2_IN COM2_OUT	S	Internal link together between input side and output side.
TP	T	Test pin for Novatek only. Float these pins for normal operation.
SHIELDING	SH	IC Shielding pads. Those pins are internally connected to the AGND. DO NOT connect to any WOA on the panel.
DASHD	SH	Data Bus Shielding pad. Those pins are internally connected to the GND. RECOMMAND to add shielding lines on the FPC to reduce EMI.
DUM	D	Dummy pads. Those pins are floating pads.

Note:
I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, I / O: Input / Output, PS: Power Setting, C: Capacitor pin.

NT51008M Pass Line Description:

Pass Line No:	Pad Name	
1	COM1_IN	COM1_OUT
2	COM2_IN	COM2_OUT

Value of Wiring Resistance

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pin Name	Wiring resistance value(Ω)	Pin Name	Wiring resistance value(Ω)
AVDD	<5	RES0	<100
AGND	<5	RES1	<100
VDD	<5	SHLR	<100
GND	<5	UPDN	<100
V1~V14	<5	BIST	<100
DRVx	<5	MODE	<100
FBx	<5	DCLKPOL	<100
VCOMI	<5	DIMO	<100
VCOMO	<5	IFSEL	<100
D00~D07	<5	F_Ctrlx	<500
D10~D17	<5	OEVx	<500
D20~D27	<5	UDx	<500
DCLK	<5	CKVx	<500
NINC	<5	STV1x	<500
VSD	<20	STV2x	<500
HSD	<20	STBNx	<500
DEN	<20		
GRB	<100		
STBYB	<100		
DITHER	<100		

3-Wire Serial Port Interface

1. 3-Wire Command Format

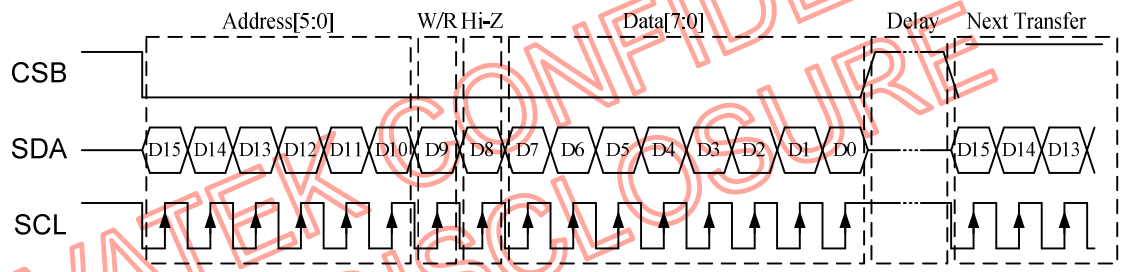
NT51008M use the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. NT51008M 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing Diagram” for the detail timing.



3-Wire Command Format:

Bit	Description
D15-D10	Register Address [5:0].
D9	W/R control bit. “0” for Write; “1” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	X	DATA (Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	Hi-Z	DATA (Issue by 3-Wire engine)							

2. 3-Wire Control Registers

Following table list all the 3-Wire control registers and bit name definition for NT51008M. Refer to the next section for detail register function description, please.

Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

R0: System Control Register

Designation	Address	Description
MODE	R0[0]	DE / SYNC mode select. MODE="0", HSD/VSD mode. MODE="1", DE mode. (Default)
DCLKPOL	R0[1]	DCLK polarity control bit. DCLKPOL="0": Data sampling at DCLK falling edge. (Default) DCLKPOL="1": Data sampling at DCLK rising edge.
GRB	R0[2]	Global reset bit. GRB="0", The controller is in reset state. GRB="1", Normal operation. (Default)
STBYB	R0[3]	Standby mode selection bit. STBYB="0", Timing control, driver and DC-DC converter, are off, and all outputs are High-Z. STBYB="1", Normal operation. (Default)
UPDN	R0[4]	G Gate Up or Down scan control. UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (Default) UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
SHLR	R0[5]	Right/Left sequence control of source driver. SHLR="0", Shift left: Last data=S1<-S2<-S3 … <-S960=First data. SHLR="1", Shift right: First data=S1->S2->S3 … ->S960=Last data. (Default)
	R0[6]	Reserved
PWR_EN	R0[7]	POWER enable. PWR_EN = H , enable PWM , Charge pump and VCOM buffer PWR_EN = L , disable PWM , Charge pump and VCOM buffer (Default)

R1: System Control Register

Designation	Address	Description
		Reserved
RES[1:0]	R1[2:1]	Display resolution selection. RES[1:0] = "01", for 1024(RGB)*768 display resolution(dual or cascade) RES[1:0] = "00", for 1024(RGB)*600 display resolution(dual or cascade) (Default) RES[1:0] = "10", for 800(RGB)*600 display resolution(dual or cascade) (601~936 channel disable) RES[1:0] = "11", for 800(RGB)*480 display resolution(dual or cascade) (601~936 channel disable)
BIST	R1[3]	Normal Operation/BIST pattern select. BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation (Default)
DITHER	R1[4]	Dithering function enable control. DITHER = "1", Enable internal dithering function DITHER = "0", Disable internal dithering function (Default)
HFRC	R1[5]	H-FRC selection. HFRC = H : H-FRC enable HFRC = L : H-FRC disable (Default) If DITHER = "0" , disable dithering function(H-FRC and FRC disable)
CABC_EN[1:0]	R1[7:6]	CABC H/W enable pin. Normally pull low. When CABC_EN="00", CABC OFF. (Default mode) When CABC_EN="01", User interface Image. When CABC_EN="10", Still Picture. When CABC_EN="11", Moving Image.

R2: System Control Register

Designation	Address	Description
		Reserved
NBW	R2[6]	Normally black or normally white setting. NBW = H : Normally black NBW = L : Normally white (Default)
INVSEL	R2[7]	One dot or Two dot inversion selection. Refer to Note1. INVSEL = ”0”, 1+2 dot inversion. (Default) INVSEL = ”1”, two line dot inversion.

R3: Gate on sequence Controller Register

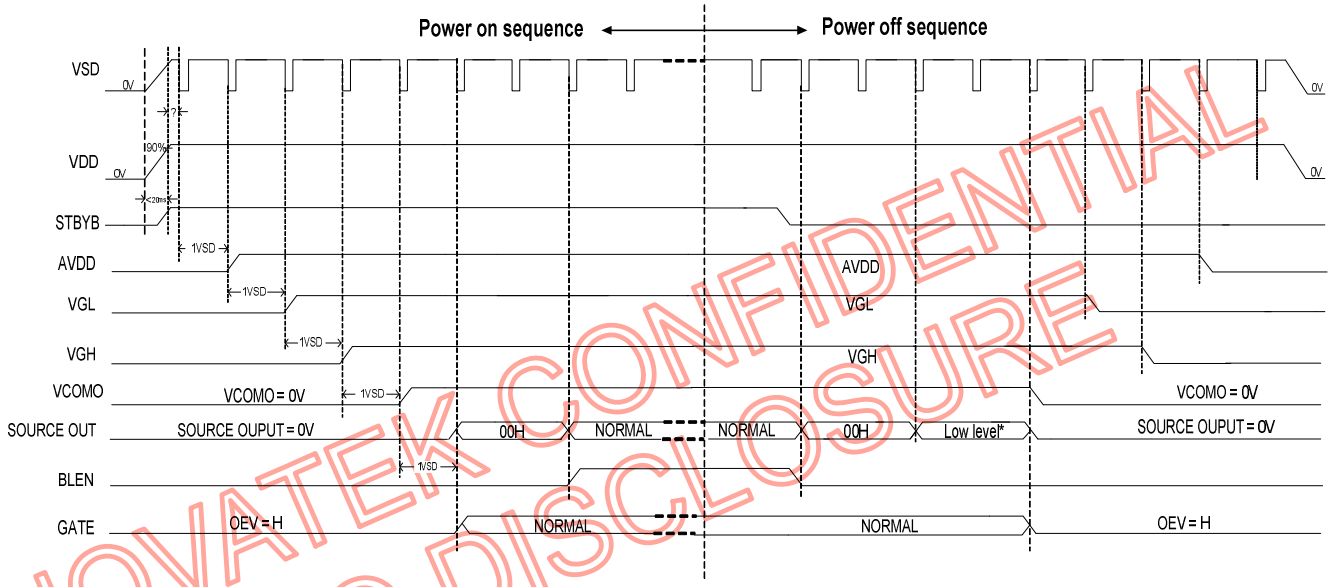
Designation	Address	Description
SEL[1:0]	R3[1:0]	Gate on sequence select SEL[0] / SEL[1] / Pin control function 1 / 1 / Z+2 1 / 0 / 2 0 / 1 / ⧵ (GIP also work) 0 / 0 / Z(Default) (GIP also work)
FRAME	R3[2]	Frame inverse or not select. FRAME = “1”, Uniform FRAME = “0”, Frame inverse (Default)
		Reserved

Function Description

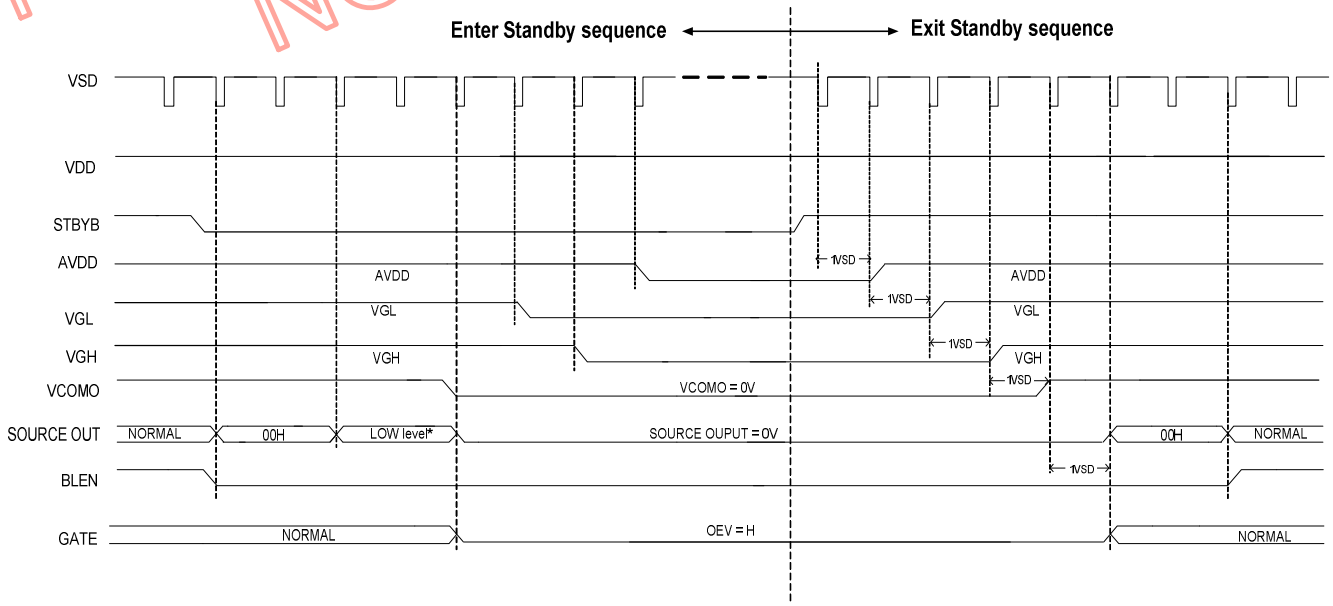
1. Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (T_{POR}) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

Power-On/Off Timing Sequence:



Enter and Exit Standby Mode Sequence:



***Note :** Low level = 3FH , when NBW = L (Normally white)
Low level = 00H , when NBW = H (Normally black)

2. Input Data VS Output Channels

1. DUAL="0"

(1) SHLR="1" , right shift

Output	SO1	SO2	SO3	- - -	SO1534	SO1535	SO1536
Order	First data			→	Last data		
Odd Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20

(2) SHLR="0", left shift

Output	SO1	SO2	SO3	- - -	SO1534	SO1535	SO1536
Order	Last data			←	First data		
Odd Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20
Even Line	D07~D00	D17~D10	D27~D20	- - -	D07~D00	D17~D10	D27~D20

2. DUAL="1"

(1) SHLR="1" , right shift

Output	SO1	SO2	SO3	- - -	SO1534	SO1535	SO1536
Order	First data			→	Last data		
Odd Line /Gn	D07~D00	D27~D20	D17~D10	- - -	D07~D00	D27~D20	D17~D10
Odd Line /Gn+1	D17~D10	D07~D00	D27~D20	- - -	D17~D10	D07~D00	D27~D20
Even Line /Gn	D07~D00	D27~D20	D17~D10	- - -	D07~D00	D27~D20	D17~D10
Even Line /Gn+1	D17~D10	D07~D00	D27~D20	- - -	D17~D10	D07~D00	D27~D20

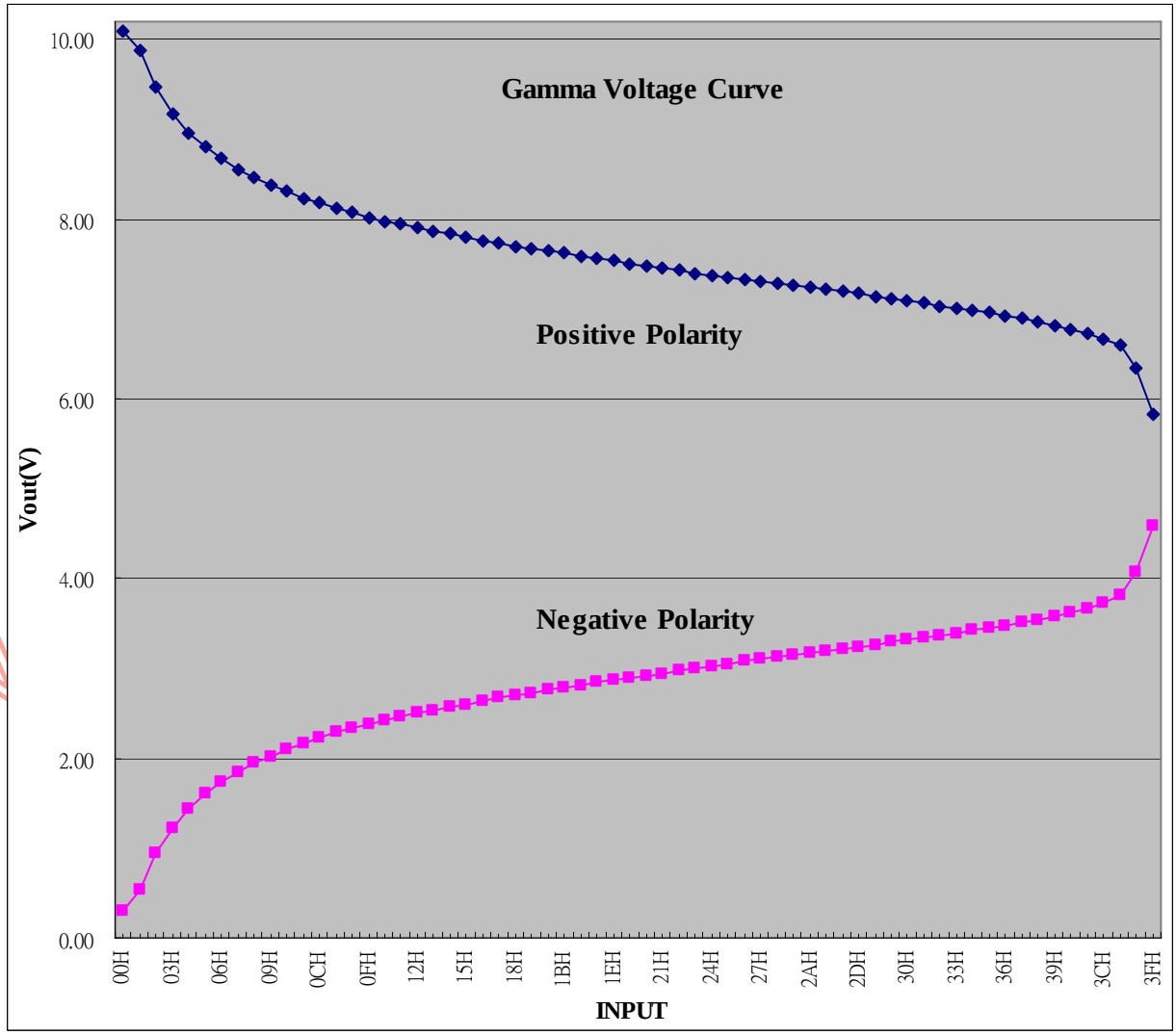
(2) SHLR="0", left shift

Output	SO1	SO2	SO3	- - -	SO1534	SO1535	SO1536
Order	Last data			←	First data		
Odd Line /Gn	D07~D00	D27~D20	D17~D10	- - -	D07~D00	D27~D20	D17~D10
Odd Line /Gn+1	D17~D10	D07~D00	D27~D20	- - -	D17~D10	D07~D00	D27~D20
Even Line /Gn	D07~D00	D27~D20	D17~D10	- - -	D07~D00	D27~D20	D17~D10
Even Line /Gn+1	D17~D10	D07~D00	D27~D20	- - -	D17~D10	D07~D00	D27~D20

3. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.

Gamma Tables very for each customer. Contact Novatek for more detail information.



Remark:

AVDD-0.1V ≥ V1 ≥ V2≥ V3 ≥ V4 ≥ V5 ≥ V6 ≥ V7; V8 ≥ V9 ≥ V10 ≥ V11 ≥ V12 ≥ V13 ≥ V14 ≥ AGND+0.1V

4. Input Data and Output Voltage Reference Table

Note: Gamma Tables vary for each custom. Contact Novatek for more detailed information.

@AVDD=11V

Chip Version	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	[unit]
NT51008M	10.242	9.99	8.542	8.057	7.719	7.354	6.014	5.497	4.608	3.609	3.097	2.494	0.553	0.165	V

Negative Polarity

Data	Negative Polarity
3FH	AVDD X 0.500
3EH	AVDD X 0.419
3DH	AVDD X 0.402
3CH	AVDD X 0.390
3BH	AVDD X 0.381
3AH	AVDD X 0.374
39H	AVDD X 0.368
38H	AVDD X 0.363
37H	AVDD X 0.358
36H	AVDD X 0.353
35H	AVDD X 0.348
34H	AVDD X 0.344
33H	AVDD X 0.340
32H	AVDD X 0.336
31H	AVDD X 0.332
30H	AVDD X 0.328
2FH	AVDD X 0.325
2EH	AVDD X 0.322
2DH	AVDD X 0.319
2CH	AVDD X 0.315
2BH	AVDD X 0.314

Data	Negative Polarity
2AH	AVDD X 0.310
29H	AVDD X 0.307
28H	AVDD X 0.304
27H	AVDD X 0.301
26H	AVDD X 0.298
25H	AVDD X 0.296
24H	AVDD X 0.293
23H	AVDD X 0.290
22H	AVDD X 0.287
21H	AVDD X 0.284
20H	AVDD X 0.282
1FH	AVDD X 0.279
1EH	AVDD X 0.276
1DH	AVDD X 0.273
1CH	AVDD X 0.270
1BH	AVDD X 0.266
1AH	AVDD X 0.263
19H	AVDD X 0.260
18H	AVDD X 0.257
17H	AVDD X 0.254
16H	AVDD X 0.250

Data	Negative Polarity
15H	AVDD X 0.247
14H	AVDD X 0.243
13H	AVDD X 0.239
12H	AVDD X 0.235
11H	AVDD X 0.231
10H	AVDD X 0.227
0FH	AVDD X 0.222
0EH	AVDD X 0.216
0DH	AVDD X 0.211
0CH	AVDD X 0.204
0BH	AVDD X 0.198
0AH	AVDD X 0.191
09H	AVDD X 0.183
08H	AVDD X 0.175
07H	AVDD X 0.165
06H	AVDD X 0.154
05H	AVDD X 0.141
04H	AVDD X 0.126
03H	AVDD X 0.107
02H	AVDD X 0.083
01H	AVDD X 0.050
00H	AVDD X 0.015

Positive Polarity

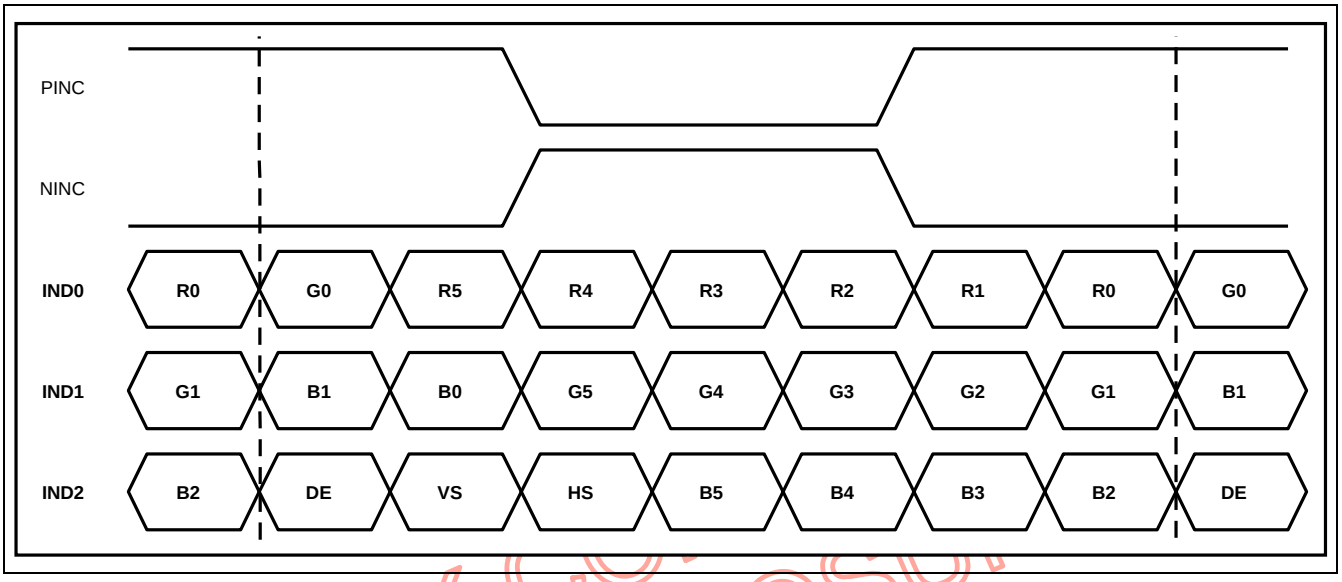
Data	Positive Polarity
00H	AVDD X 0.931
01H	AVDD X 0.908
02H	AVDD X 0.884
03H	AVDD X 0.865
04H	AVDD X 0.850
05H	AVDD X 0.838
06H	AVDD X 0.828
07H	AVDD X 0.820
08H	AVDD X 0.813
09H	AVDD X 0.807
0AH	AVDD X 0.801
0BH	AVDD X 0.796
0CH	AVDD X 0.792
0DH	AVDD X 0.788
0EH	AVDD X 0.783
0FH	AVDD X 0.780
10H	AVDD X 0.777
11H	AVDD X 0.773
12H	AVDD X 0.770
13H	AVDD X 0.766
14H	AVDD X 0.763

Data	Positive Polarity
15H	AVDD X 0.760
16H	AVDD X 0.757
17H	AVDD X 0.754
18H	AVDD X 0.751
19H	AVDD X 0.749
1AH	AVDD X 0.746
1BH	AVDD X 0.743
1CH	AVDD X 0.741
1DH	AVDD X 0.739
1EH	AVDD X 0.737
1FH	AVDD X 0.735
20H	AVDD X 0.732
21H	AVDD X 0.730
22H	AVDD X 0.728
23H	AVDD X 0.726
24H	AVDD X 0.724
25H	AVDD X 0.722
26H	AVDD X 0.720
27H	AVDD X 0.718
28H	AVDD X 0.716
29H	AVDD X 0.715

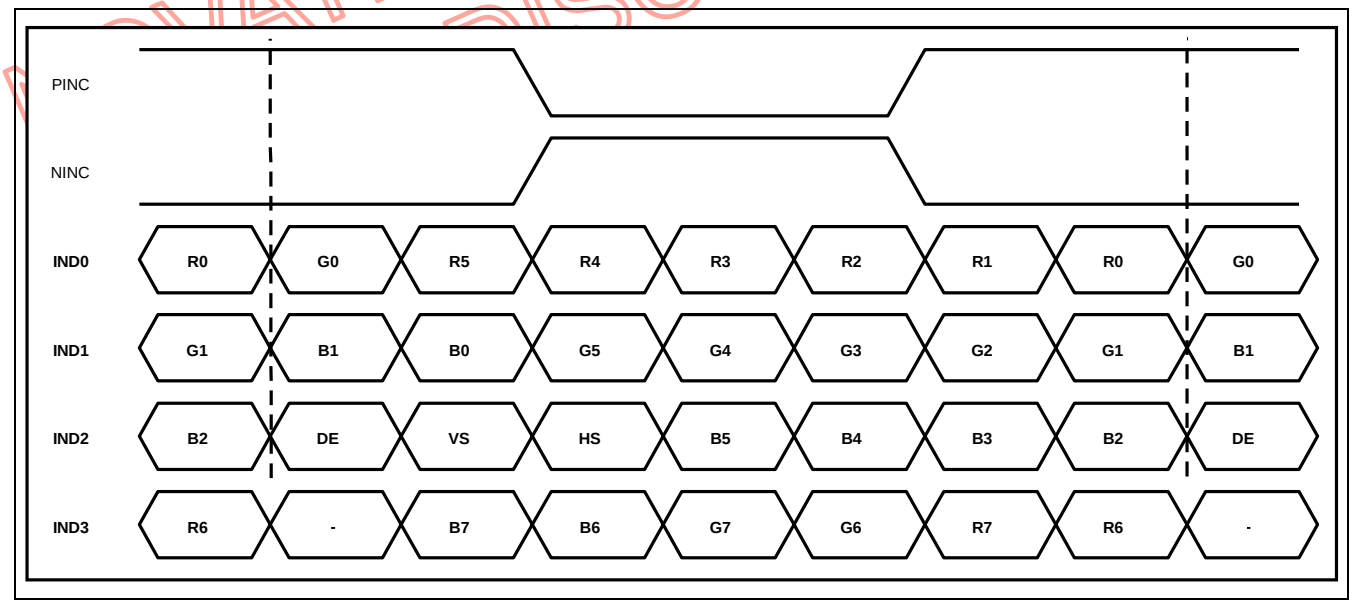
Data	Positive Polarity
2AH	AVDD X 0.713
2BH	AVDD X 0.712
2CH	AVDD X 0.709
2DH	AVDD X 0.708
2EH	AVDD X 0.706
2FH	AVDD X 0.704
30H	AVDD X 0.702
31H	AVDD X 0.701
32H	AVDD X 0.700
33H	AVDD X 0.698
34H	AVDD X 0.696
35H	AVDD X 0.695
36H	AVDD X 0.694
37H	AVDD X 0.693
38H	AVDD X 0.691
39H	AVDD X 0.689
3AH	AVDD X 0.686
3BH	AVDD X 0.684
3CH	AVDD X 0.682
3DH	AVDD X 0.677
3EH	AVDD X 0.669
3FH	AVDD X 0.547

Data Input Format for LVDS

6bit LVDS input

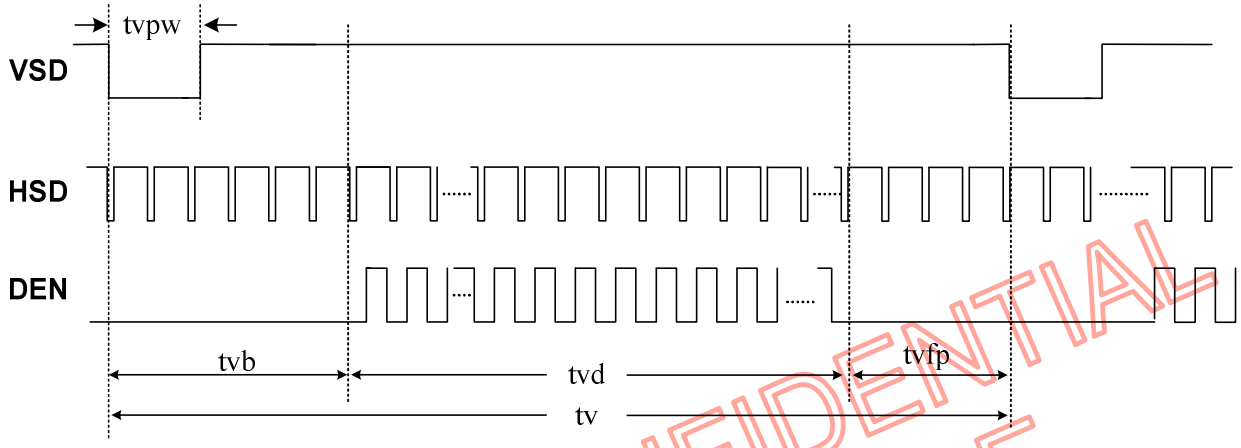


8-bit LVDS input (HSD='L')

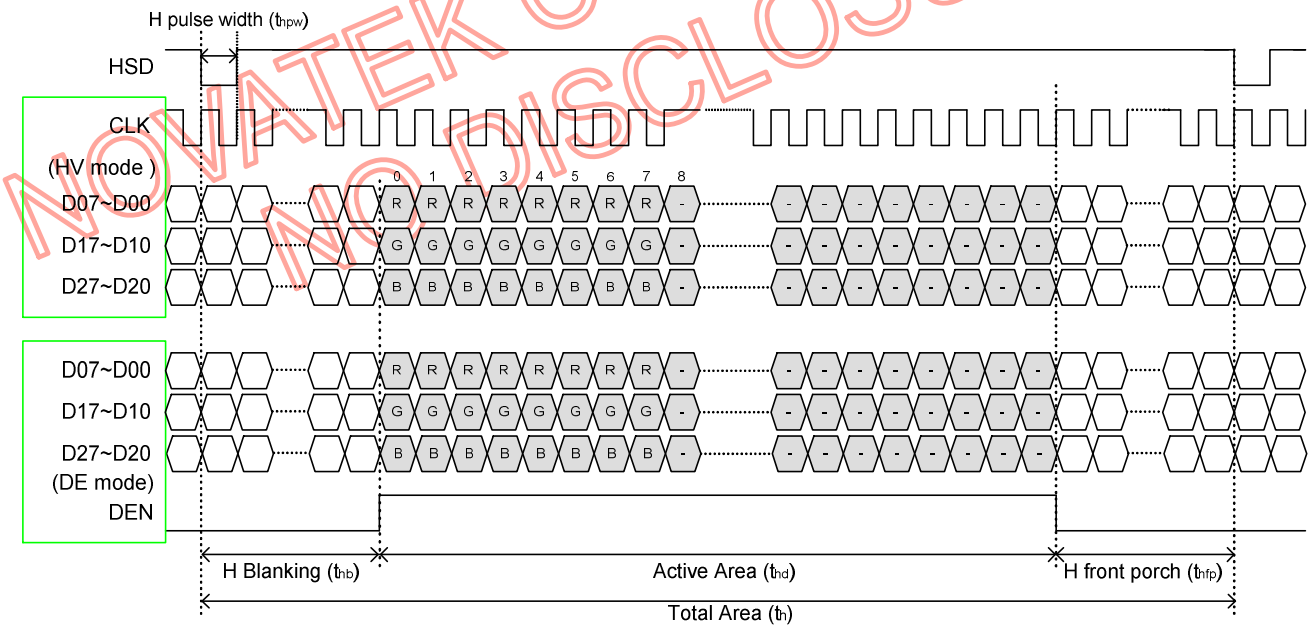


Data Input Format for TTL

Vertical input timing



Horizontal input timing



Parallel RGB input timing table

For 1024x768 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	52	65	71	MHz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		768		H
VSYNC period time	tv	778	806	845	H
VSYNC blanking	tvb+tvfp	10	38	77	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		1024		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			57	65	70.5	MHz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			140		
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		768		H
VSYNC period time	tv	792	806	840	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC Blanking (tvb)	tvb	23	23	23	H
VSYNC Front porch (tvfp)	tvfp	1	15	49	H

For 1024x600 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	40.8	51.2	67.2	MHz
Horizontal display area	thd		1024		DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	635	800	H
VSYNC blanking	tvb+tvfp	10	35	200	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		1024		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			44.9	51.2	63	MHz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			140		
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	624	635	750	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC Blanking (tvb)	tvb	23	23	23	H
VSYNC Front porch (tvfp)	tvfp	1	12	127	H

For 800x600 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	32.6	39.6	62.4	MHz
Horizontal display area	thd		800		DCLK
HSYNC period time	th	890	1000	1300	DCLK
HSYNC blanking	thb+thfp	90	200	500	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tv	610	660	800	H
VSYNC blanking	tvb+tvfp	10	60	200	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		800		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			34.5	39.6	50.4	MHz
1 Horizontal Line		th	900	1000	1200	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			40		
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	112	312	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	640	660	700	H
VSYNC pulse width	tvpw	1	-	20	H
VSYNC Blanking (tvb)	tvb	39	39	39	H
VSYNC Front porch (tvfp)	tvfp	1	21	61	H

For 800x480 panel

DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @ Frame rate = 60Hz	fclk	26.2	29.2	54.6	MHz
Horizontal display area	thd		800		DCLK
HSYNC period time	th	890	928	1300	DCLK
HSYNC blanking	thb+thfp	90	128	500	DCLK
Vertical display area	tvd		480		H
VSYNC period time	tv	490	525	700	H
VSYNC blanking	tvb+tvfp	10	45	220	H

HV mode

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		800		DCLK
DCLK frequency @ Frame rate = 60Hz		fclk	Min.	Typ.	Max.	
			27.7	29.2	39.6	MHz
1 Horizontal Line		th	900	928	1100	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			40		
HSYNC blanking		thb	88	88	88	
HSYNC front porch		thfp	12	40	212	

Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		480		H
VSYNC period time	tv	513	525	600	H
VSYNC pulse width	tvpw	1	-	3	H
VSYNC Blanking (tvb)	tvb	32	32	32	H
VSYNC Front porch (tvfp)	tvfp	1	13	88	H

Absolute Maximum Ratings

	MIN.	MAX.	UNIT
Logic supply voltage, VDD **Digital input voltage**	-0.5	5	V
Analog supply voltage, AVDD **Gamma voltage , V1~V14** **OUT1 ~ OUT1536**	-0.5	15	V

TEMPREATURE

	MIN.	MAX.	UNIT
Operating temperature	-20	85	°C
Storage temperature	-55	125	°C

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

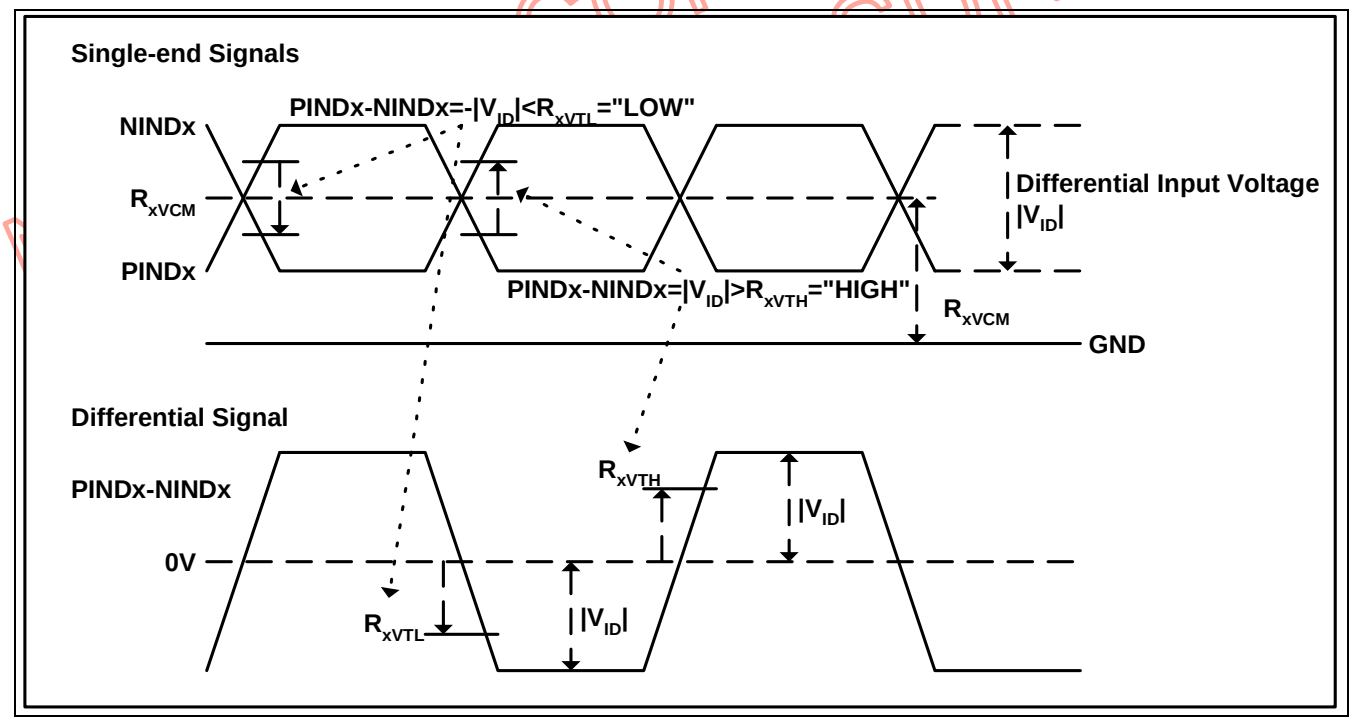
DC Electrical Characteristics

(VDD= 2.3 to 3.6V, AVDD= 8 to 13.5V, GND=AGND= 0V, TA= -20 to +85°C)
TTL mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Low level input voltage	Vil	0	-	0.3xVDD	V	For the digital circuit
High level input voltage	Vih	0.7xVDD	-	VDD	V	For the digital circuit
Input leakage current	Ii	-	-	±1	μA	For the digital circuit
High level output voltage	Voh	VDD-0.4	-	-	V	Ioh= -400μA
Low level output voltage	Vol	-	-	GND+0.4	V	Iol= +400μA
Pull low/high resistor	Ri	200K	250K	300K	ohm	For the digital input pin @ VDD=3.3V
Digital Operating Current	Idd	-	15	25	mA	Fclk=65 MHz, FLD=50KHz, VDD=3.3V
Digital Stand-by Current	Ist1	-	10	50	μA	Clock & all functions are stopped
Analog Operating Current	Idda	-	10	12	mA	No load, Fclk=65MHz, FLD=50KHz @ AVDD=10V,V1=8V, V14=0.4V
Analog Stand-by Current	Ist2	-	10	50	μA	No load, Clock & all functions are stopped
Input level of V1 ~ V7	Vref1	0.4* AVDD	-	AVDD-0.1	V	Gamma correction voltage input
Input level of V8 ~ V14	Vref2	0.1	-	0.6* AVDD	V	Gamma correction voltage input
Output Voltage deviation	Vod1	-	±20	±35	mV	Vo = AGND+0.1V ~ AGND+0.5V & Vo = AVDD-0.5V ~ AVDD-0.1V
Output Voltage deviation	Vod2	-	±15	±20	mV	Vo = AGND+0.5V ~ AVDD-0.5V
Output Voltage Offset between Chips	Voc	-	-	±20	mV	Vo = AGND+0.5V ~ AVDD-0.5V
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	SO1 ~ SO1536
Sinking Current of Outputs	IOLy	80	-	-	uA	SO1 ~ SO1536; Vo=0.1V v.s 1.0V , AVDD=13.5V
Driving Current of Outputs	IOHy	80	-	-	uA	SO1 ~ SO1536; Vo=13.4V v.s 12.5V , AVDD=13.5V
Resistance of Gamma Table	Rg	0.7*Rn	1.0*Rn	1.3*Rn	ohm	Rn: Internal gamma resistor

LVDS mode (Receiver Differential Input: PIND0~PIND3, NIND0~NIND3, PINC, NINC)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	R_{xVTH}			+0.1	V	R_{xVCM} =1.2V
Differential input low threshold voltage	R_{xVTL}	-0.1			V	
Input voltage range (singled-end)	R_{XVIN}	0		2.4	V	
Differential input common mode voltage	R_{xVCM}	$\|V_{ID}\|/2$		2.4-$\|V_{ID}\|/2$	V	
Differential input voltage	$\|V_{ID}\|$	0.2		0.6	V	
Differential input leakage current	RV_{xliz}	-10		+10	μA	
LVDS Digital Operating Current	Iddlvds	-	40	50	mA	Fclk=65 MHz, VDD=3.3V
LVDS Digital Stand-by Current	Istlvds	-	10	50	μA	Clock & all Functions are stopped



Power

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
DRV output voltage for PWM	VDRV	0	-	VDD	V	
Feedback voltage for PWM	VFB	1.1	1.2	1.3	V	
Duty cycle maximum	Dmax	-	-	85	%	
VCOM buffer input voltage	VCOMI	3	5	7	V	
VCOM buffer output voltage	VCOMO	VCOMI – 0.2	VCOMI	VCOMI+ 0.2	V	
AVDDG output variation	VAVDDG	10.9	11	11.1	V	AVDD = 11.5V , No load

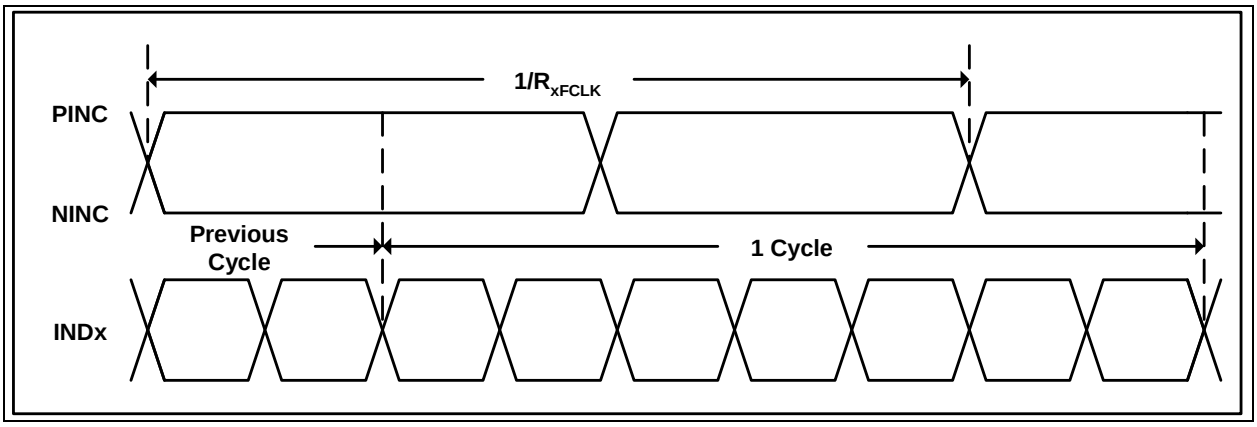
AC Electrical Characteristics

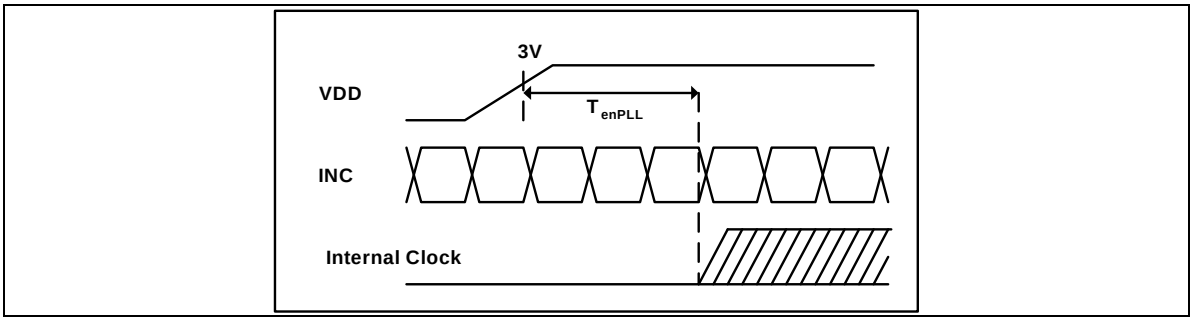
(VDD= 2.3 to 3.6V, AVDD= 8 to 13.5V, GND=AGND= 0V, TA= -20 to +85°C)
TTL mode

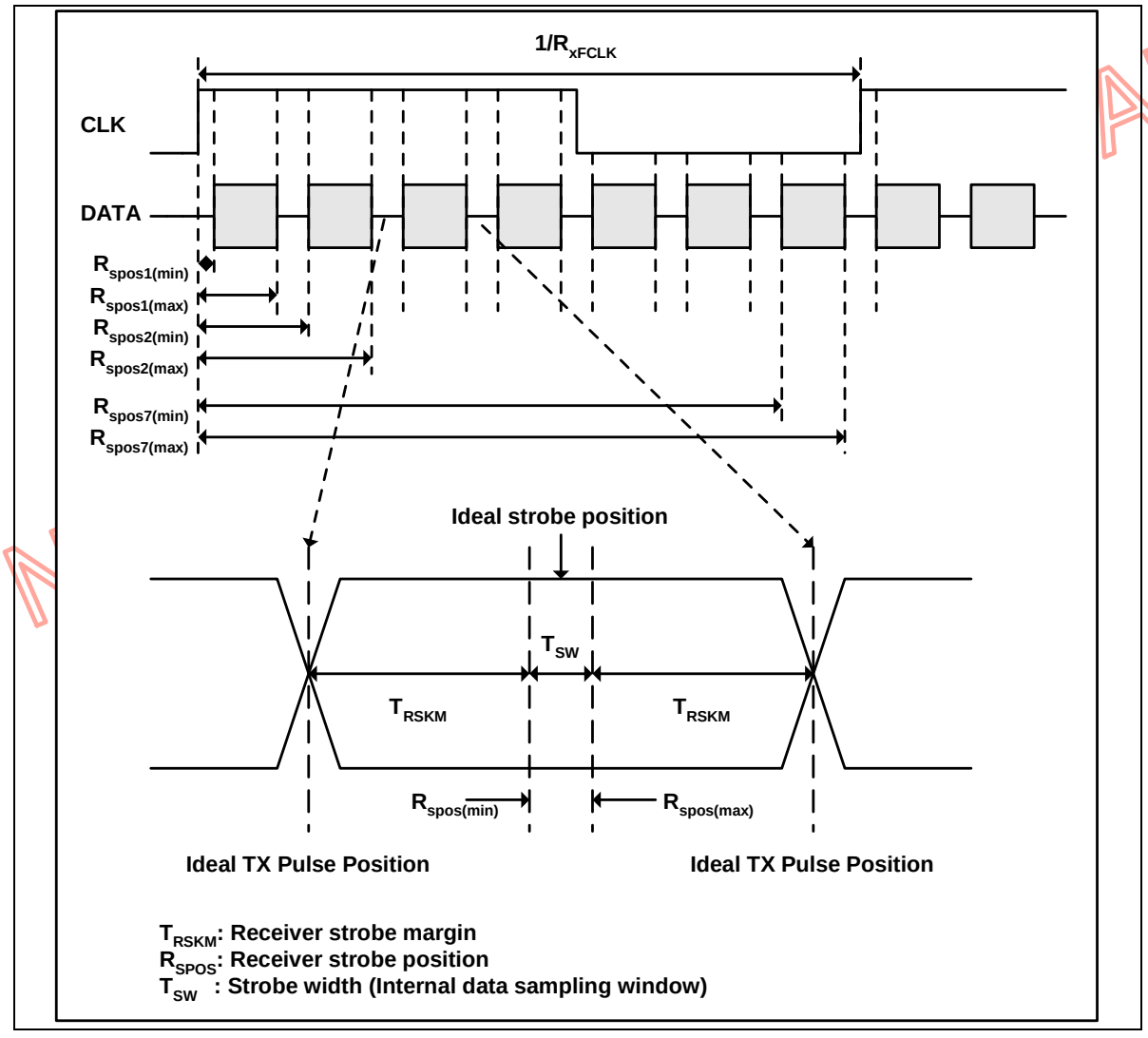
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power On Slew rate	T_{POR}	-	-	20	ms	From 0V to 90% VDD
RSTB pulse width	T_{Rst}	50	-	-	us	DCLK = 65MHz
DCLK cycle time	Tcph	14			ns	
DCLK pulse duty	Tcwh	40	50	60	%	
VSD setup time	Tvst	5	-	-	ns	
VSD hold time	Tvhd	5	-	-	ns	
HSD setup time	Thst	5	-	-	ns	
HSD hold time	Thhd	5	-	-	ns	
Data set-up time	Tdsu	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
Data hold time	Tdhd	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
DE setup time	Tesu	5	-	-	ns	
DE hold time	Tehd	5	-	-	ns	
Output stable time	Tsst	-	-	6	us	10% to 90% target voltage. CL=90pF, R=10K ohm (Cascade)
				3		Dual gate

LVDS mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency	R_{xFCLK}	20		71	MHz	
Input data skew margin	T_{RSKM}	500			pS	$\|V_{ID}\|$ = 400mV R_{xVCM} = 1.2V R_{xFCLK} = 71 MHz
Clock high time	T_{LVCH}		4/(7* R_{xFCLK})		ns	
Clock low time	T_{LVCL}		3/(7* R_{xFCLK})		ns	
PLL wake-up time	T_{enPLL}			150	uS	







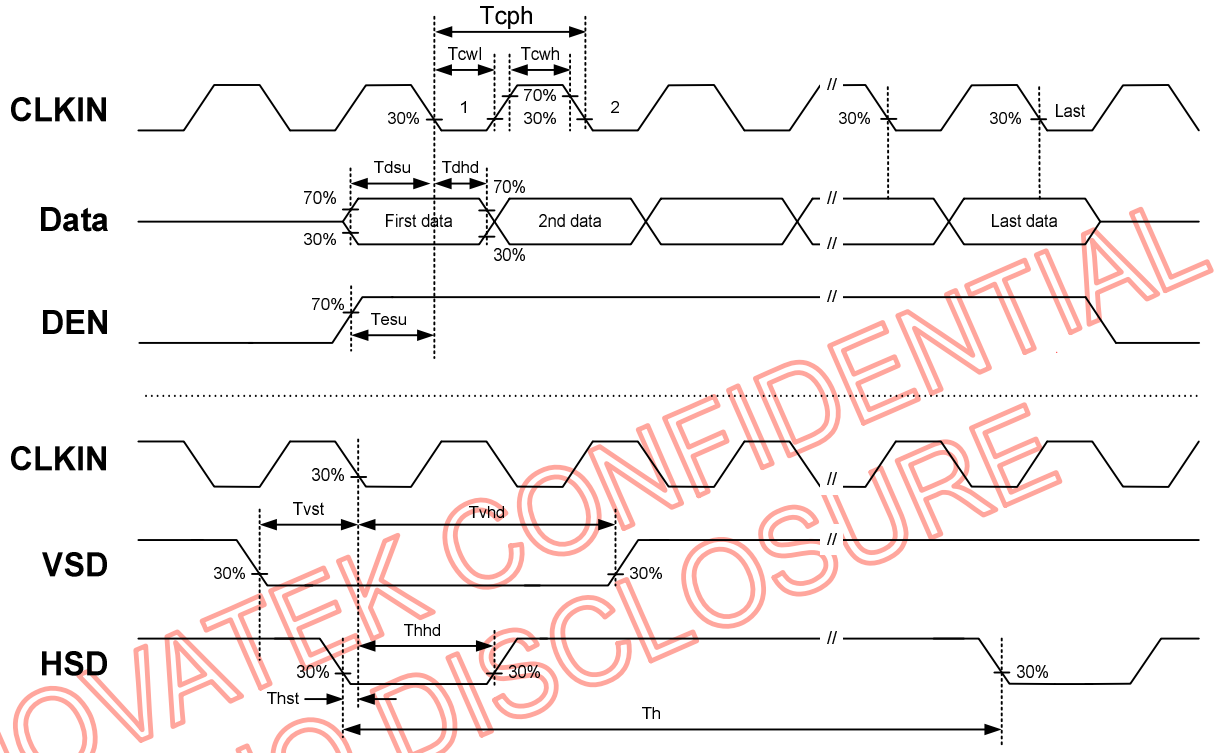
SSC torence of LVDS receiver						
Symbol	**parameter**	**condition**	**Min.**	**Typ.**	**Max.**	**Units**
SSC_{MF}	Modulation Frequency		23		93	KHz
SSC_{MR}	Modulation Rate	LVDS clock = 71MHz center spread			±3	%

Output Timing Table

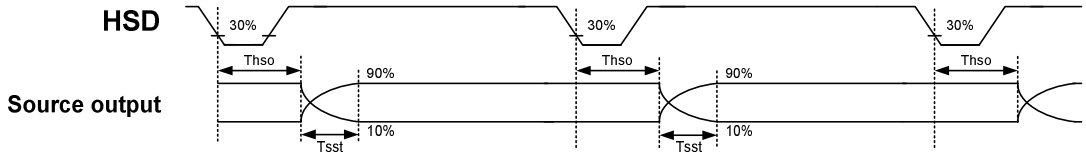
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCLK Frequency	Fclk	-	65	71	MHz	VDD = 2.3V ~3.6V
DCLK Cycle Time	Tclk	14.1	15.4	-	ns	
DCLK Pulse Duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso	-	64	-	DCLK	
Time from HSD to LD	Thld	-	64	-	DCLK	
Time from HSD to STV	Thstv	-	2	-	DCLK	
Time from HSD to CKV	Thckv	-	20	-	DCLK	
Time from HSD to OEV	Thoev	-	4	-	DCLK	
LD Pulse Width	Twld	-	10	-	DCLK	
CKV Pulse Width	Twckv	-	66	-	DCLK	
OEV Pulse Width	Twoev	-	74	-	DCLK	

Timing Diagram

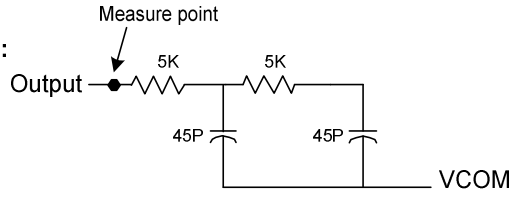
1. Input Clock and Data Timing Diagram



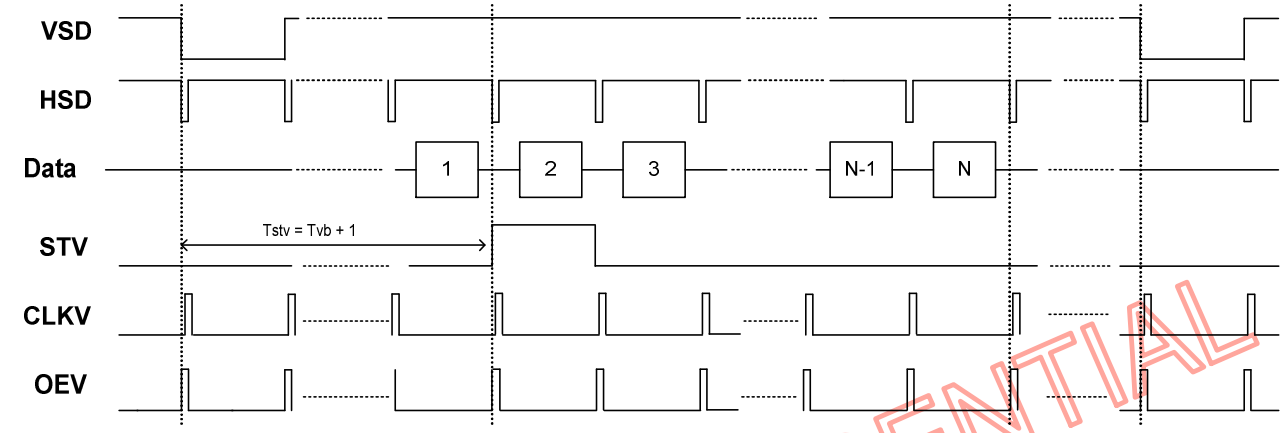
2. Source Output Timing Diagram (Cascade)



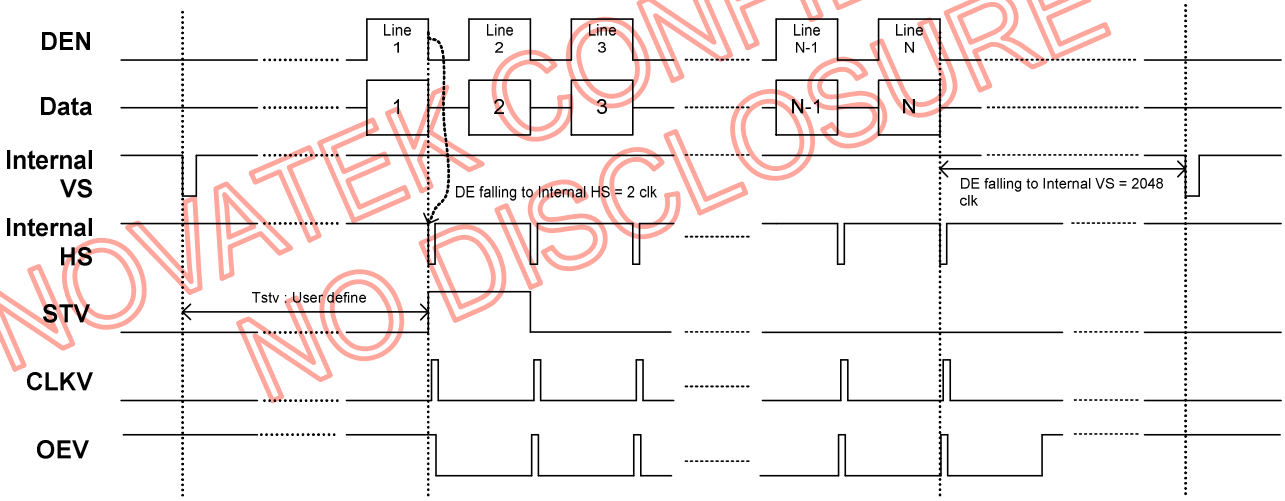
Output load condition :



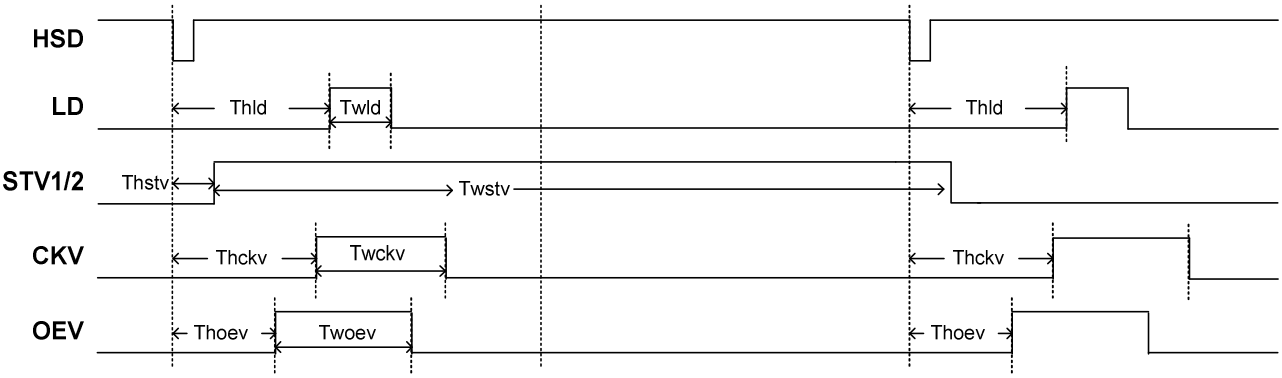
3. Vertical Timing Diagram HV (Cascade)



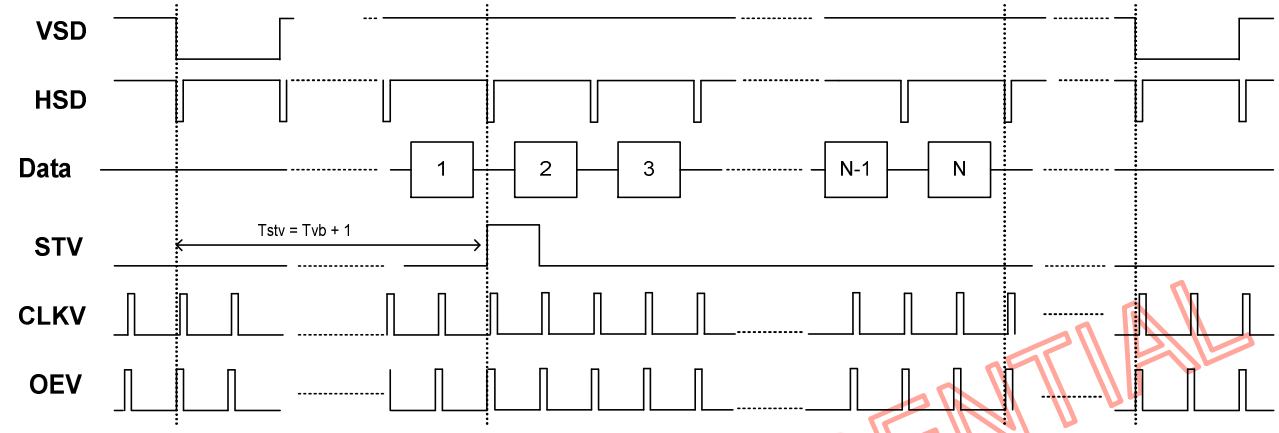
4. Vertical Timing Diagram DE (Cascade)



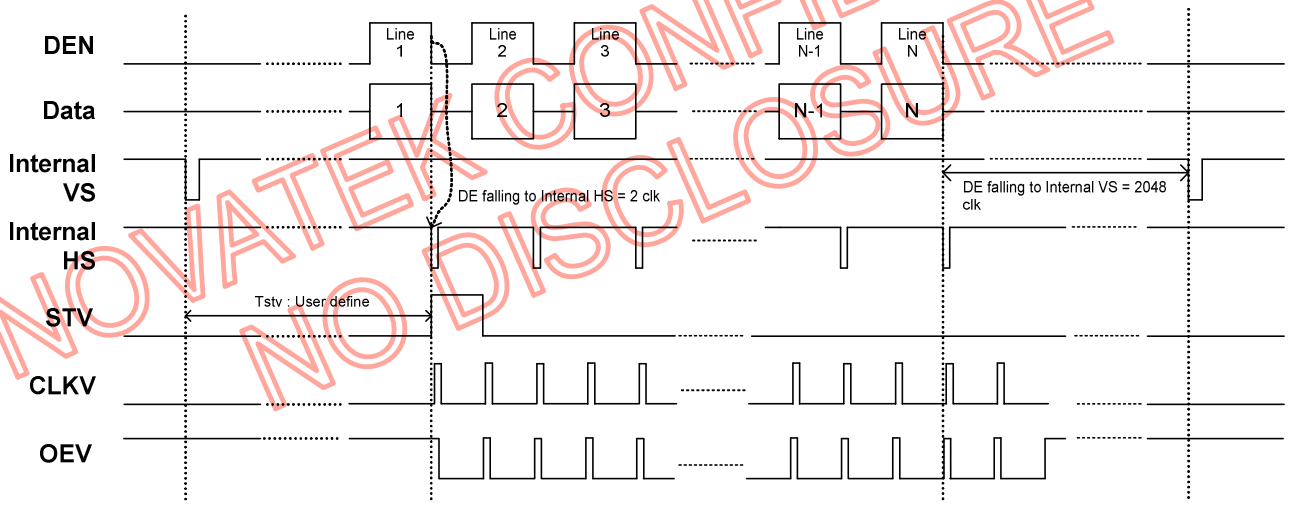
5. Gate output timing diagram (Cascade)



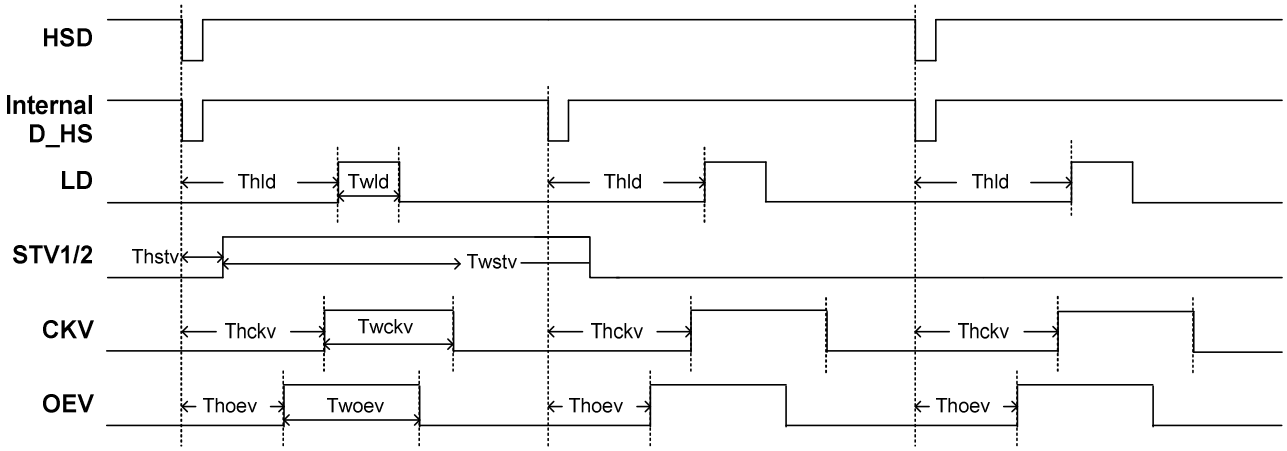
6. Vertical Timing Diagram HV (Dual Gate)



7. Vertical Timing Diagram DE (Dual Gate)



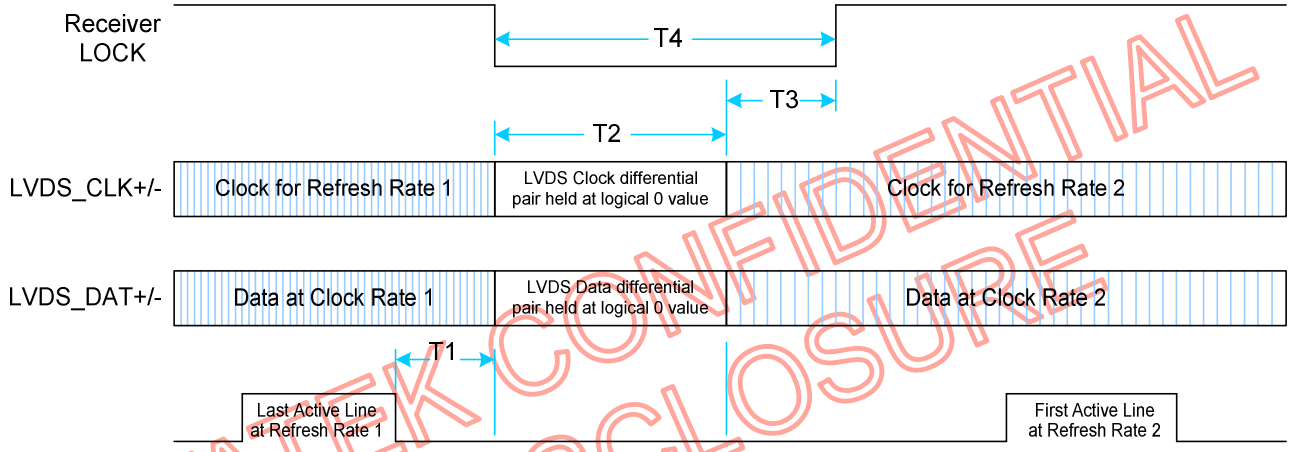
8. Gate output timing diagram (Dual Gate)



9. SDRRS timing diagram

SDRRS (seamless display refresh rate switching)

When Showing the still picture, it is accept to reduce the refresh rate from 60Hz to low refresh rate (for example 40Hz). The purpose is mainly for power saving. INTEL defined a timing chart switch between different refresh rate. Following this timing chart, the switch between different refresh rates is seamless for end user.



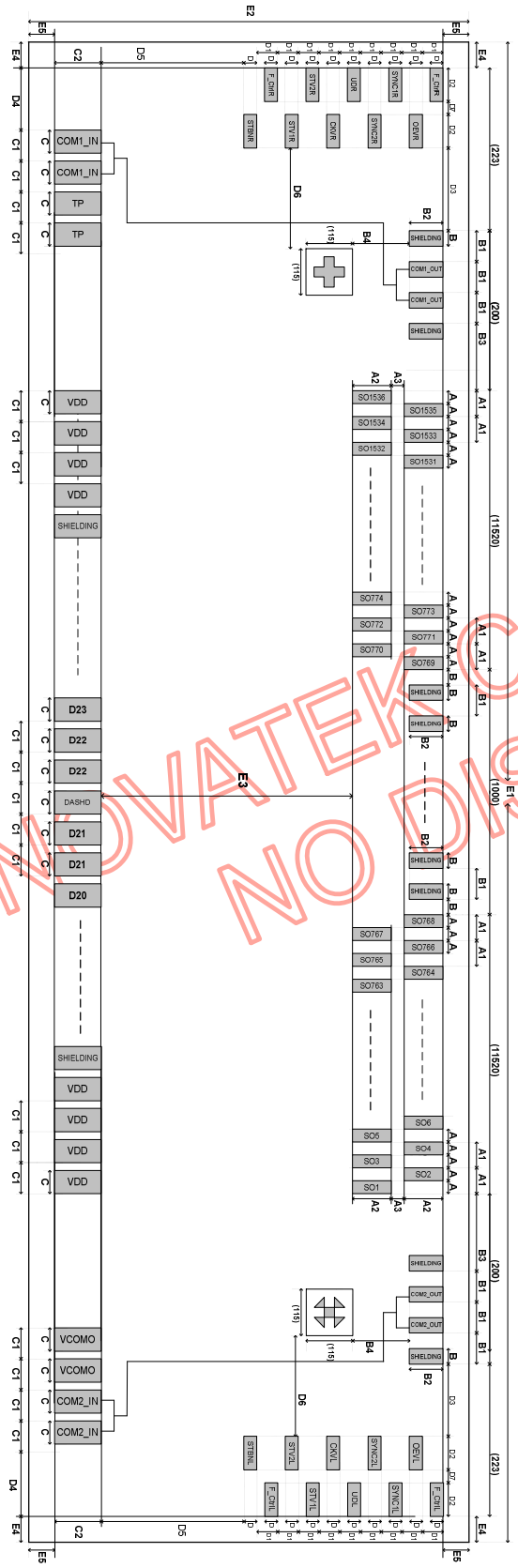
T1 - Min delay from start of vert blank to start of timing change: 2 lines (HSYNC periods)

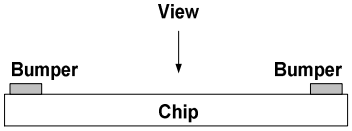
T2 - Max delay for clock to transition to new frequency: 100us

T3 - Max receiver lock delay from stable clock: Display specific (TBD)

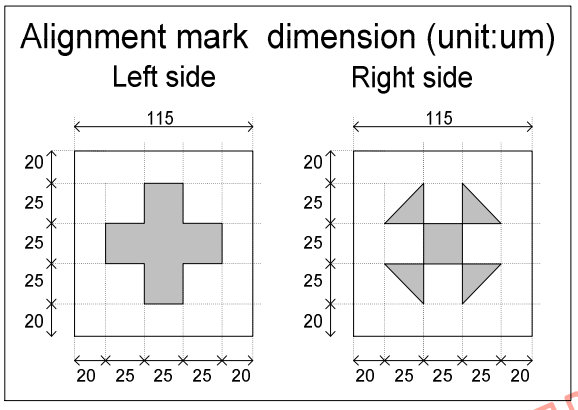
T4 - Max period during which panel maintains display (T2+T3): Display specific (TBD)

Chip Outline Dimensions





Alignment Mark



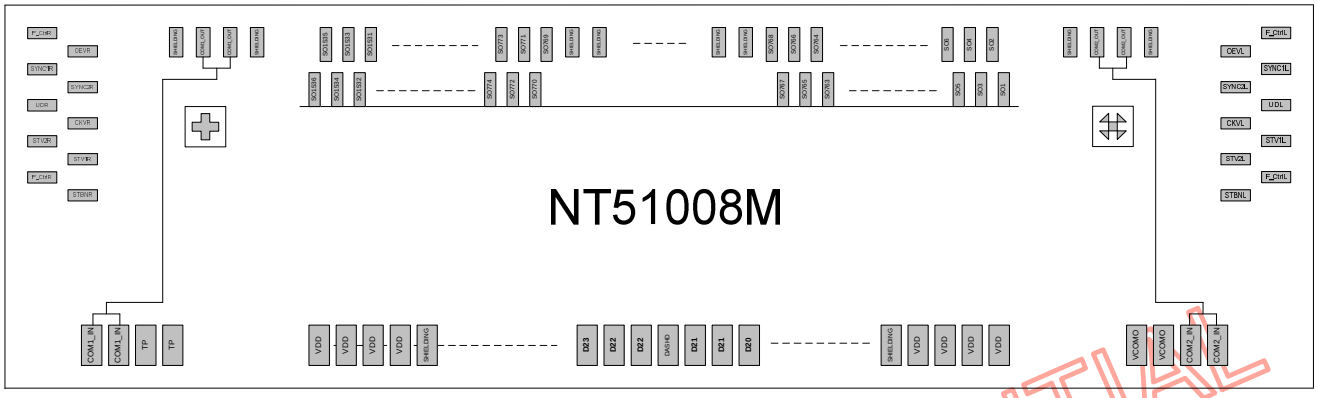
Pad Information

Symbol	Dimension (um)
A	15
A1	30
A2	100
A3	30
B	30
B1	50
B2	70
B3	50
B4	50
C	65
C1	85
C2	100

Symbol	Dimension (um)
D	30
D1	40
D2	80
D3	43
D4	33
D5	96
D6	74
D7	20
E1	25000
E2	700
E3	256
E4	57(max)
E5	57(max)

***Note: Chip dimension includes scribe line.**

Pad Coordinate



Pad	TextName	CX	CY
1	COM1_IN	-12377.5	-243
2	COM1_IN	-12292.5	-243
3	TP	-12207.5	-243
4	TP	-12122.5	-243
5	TP	-12037.5	-243
6	TP	-11952.5	-243
7	SHIELDING	-11867.5	-243
8	AGND	-11782.5	-243
9	AGND	-11697.5	-243
10	AGND	-11612.5	-243
11	AGND	-11527.5	-243
12	SHIELDING	-11442.5	-243
13	AVDD	-11357.5	-243
14	AVDD	-11272.5	-243
15	AVDD	-11187.5	-243
16	AVDD	-11102.5	-243
17	SHIELDING	-11017.5	-243
18	GND	-10932.5	-243
19	GND	-10847.5	-243
20	GND	-10762.5	-243
21	GND	-10677.5	-243
22	SHIELDING	-10592.5	-243
23	VDD	-10507.5	-243
24	VDD	-10422.5	-243
25	VDD	-10337.5	-243
26	VDD	-10252.5	-243
27	SHIELDING	-10167.5	-243
28	TP	-10082.5	-243
29	TP	-9997.5	-243
30	TP	-9912.5	-243
31	TP	-9827.5	-243
32	TP	-9742.5	-243
33	TP	-9657.5	-243
34	TP	-9572.5	-243
35	TP	-9487.5	-243
36	TP	-9402.5	-243
37	TP	-9317.5	-243
38	SHIELDING	-9232.5	-243
39	DIMI	-9147.5	-243
40	DIMI	-9062.5	-243
41	NBW	-8977.5	-243
42	NBW	-8892.5	-243
43	PINCTL	-8807.5	-243
44	PINCTL	-8722.5	-243
45	SHIELDING	-8637.5	-243
46	DIMO	-8552.5	-243
47	DIMO	-8467.5	-243
48	SHIELDING	-8382.5	-243
49	DITHER	-8297.5	-243
50	DITHER	-8212.5	-243
51	HFRC	-8127.5	-243
52	HFRC	-8042.5	-243
53	TP	-7957.5	-243
54	TP	-7872.5	-243
55	FRAME	-7787.5	-243
56	FRAME	-7702.5	-243
57	SEL[0]	-7617.5	-243
58	SEL[0]	-7532.5	-243
59	SEL[1]	-7447.5	-243
60	SEL[1]	-7362.5	-243
61	CSB	-7277.5	-243
62	CSB	-7192.5	-243
63	SHIELDING	-7107.5	-243
64	SDA	-7022.5	-243
65	SDA	-6937.5	-243
66	SHIELDING	-6852.5	-243
67	SCL	-6767.5	-243
68	SCL	-6682.5	-243
69	SHIELDING	-6597.5	-243
70	VDD	-6512.5	-243
71	VDD	-6427.5	-243
72	VDD	-6342.5	-243
73	VDD	-6257.5	-243
74	SHIELDING	-6172.5	-243
75	GND	-6087.5	-243
76	GND	-6002.5	-243
77	GND	-5917.5	-243
78	GND	-5832.5	-243
79	SHIELDING	-5747.5	-243
80	AVDD	-5662.5	-243
81	AVDD	-5577.5	-243
82	AVDD	-5492.5	-243
83	AVDD	-5407.5	-243
84	SHIELDING	-5322.5	-243
85	AGND	-5237.5	-243
86	AGND	-5152.5	-243
87	AGND	-5067.5	-243
88	AGND	-4982.5	-243
89	SHIELDING	-4897.5	-243
90	V1	-4812.5	-243
91	V1	-4727.5	-243
92	V2	-4642.5	-243
93	V2	-4557.5	-243
94	V3	-4472.5	-243
95	V3	-4387.5	-243
96	V4	-4302.5	-243
97	V4	-4217.5	-243
98	V5	-4132.5	-243
99	V5	-4047.5	-243
100	V6	-3962.5	-243
101	V6	-3877.5	-243
102	V7	-3792.5	-243
103	V7	-3707.5	-243
104	GAMH	-3622.5	-243
105	GAMH	-3537.5	-243
106	SHIELDING	-3452.5	-243
107	DASHD	-3367.5	-243
108	VSD	-3282.5	-243
109	DASHD	-3197.5	-243
110	HSD	-3112.5	-243
111	DASHD	-3027.5	-243
112	DEN	-2942.5	-243
113	GND_LVDS	-2857.5	-243
114	GND_LVDS	-2772.5	-243
115	GND_LVDS	-2687.5	-243
116	GND_LVDS	-2602.5	-243
117	D27	-2517.5	-243
118	D26	-2432.5	-243
119	DASHD	-2347.5	-243
120	D25	-2262.5	-243
121	D24	-2177.5	-243
122	DASHD	-2092.5	-243
123	D23	-2007.5	-243
124	D22	-1922.5	-243
125	DASHD	-1837.5	-243

126	D21	-1752.5	-243
127	D20	-1667.5	-243
128	DASHD	-1582.5	-243
129	DCLK	-1497.5	-243
130	NINC	-1412.5	-243
131	DASHD	-1327.5	-243
132	VDD_LVDS	-1242.5	-243
133	VDD_LVDS	-1157.5	-243
134	VDD_LVDS	-1072.5	-243
135	VDD_LVDS	-987.5	-243
136	REV	-902.5	-243
137	DASHD	-817.5	-243
138	D17	-732.5	-243
139	D16	-647.5	-243
140	DASHD	-562.5	-243
141	D15	-477.5	-243
142	D14	-392.5	-243
143	DASHD	-307.5	-243
144	D13	-222.5	-243
145	D12	-137.5	-243
146	DASHD	-52.5	-243
147	D11	32.5	-243
148	D10	117.5	-243
149	DASHD	202.5	-243
150	D07	287.5	-243
151	D06	372.5	-243
152	DASHD	457.5	-243
153	D05	542.5	-243
154	D04	627.5	-243
155	DASHD	712.5	-243
156	D03	797.5	-243
157	D02	882.5	-243
158	DASHD	967.5	-243
159	D01	1052.5	-243
160	D00	1137.5	-243
161	DASHD	1222.5	-243
162	SHIELDING	1307.5	-243
163	GAML	1392.5	-243
164	GAML	1477.5	-243
165	V8	1562.5	-243
166	V8	1647.5	-243
167	V9	1732.5	-243
168	V9	1817.5	-243
169	V10	1902.5	-243
170	V10	1987.5	-243
171	V11	2072.5	-243
172	V11	2157.5	-243
173	V12	2242.5	-243
174	V12	2327.5	-243
175	V13	2412.5	-243
176	V13	2497.5	-243
177	V14	2582.5	-243
178	V14	2667.5	-243
179	SHIELDING	2752.5	-243
180	AGND	2837.5	-243
181	AGND	2922.5	-243
182	AGND	3007.5	-243
183	AGND	3092.5	-243
184	SHIELDING	3177.5	-243
185	AVDD	3262.5	-243
186	AVDD	3347.5	-243
187	AVDD	3432.5	-243
188	AVDD	3517.5	-243
189	SHIELDING	3602.5	-243
190	GND	3687.5	-243
191	GND	3772.5	-243
192	GND	3857.5	-243
193	GND	3942.5	-243
194	SHIELDING	4027.5	-243
195	VDD	4112.5	-243
196	VDD	4197.5	-243
197	VDD	4282.5	-243
198	VDD	4367.5	-243
199	SHIELDING	4452.5	-243
200	DUAL	4537.5	-243
201	DUAL	4622.5	-243
202	MASL	4707.5	-243
203	MASL	4792.5	-243
204	MASLOC	4877.5	-243
205	MASLOC	4962.5	-243
206	CABC_EN[0]	5047.5	-243
207	CABC_EN[0]	5132.5	-243
208	CABC_EN[1]	5217.5	-243
209	CABC_EN[1]	5302.5	-243
210	OPDRV	5387.5	-243
211	OPDRV	5472.5	-243
212	MODE	5557.5	-243
213	MODE	5642.5	-243
214	IFSEL	5727.5	-243
215	IFSEL	5812.5	-243
216	BIST	5897.5	-243
217	BIST	5982.5	-243
218	RES[0]	6067.5	-243
219	RES[0]	6152.5	-243
220	RES[1]	6237.5	-243
221	RES[1]	6322.5	-243
222	DCLKPOL	6407.5	-243
223	DCLKPOL	6492.5	-243
224	STBYB	6577.5	-243
225	STBYB	6662.5	-243
226	GRB	6747.5	-243
227	GRB	6832.5	-243
228	SHLR	6917.5	-243
229	SHLR	7002.5	-243
230	UPDN	7087.5	-243
231	UPDN	7172.5	-243
232	SHIELDING	7257.5	-243
233	TP	7342.5	-243
234	TP	7427.5	-243
235	TP	7512.5	-243
236	TP	7597.5	-243
237	TP	7682.5	-243
238	TP	7767.5	-243
239	TP	7852.5	-243
240	TP	7937.5	-243
241	TP	8022.5	-243
242	TP	8107.5	-243
243	TP	8192.5	-243
244	TP	8277.5	-243
245	TP	8362.5	-243
246	TP	8447.5	-243
247	SHIELDING	8532.5	-243
248	VDD	8617.5	-243
249	VDD	8702.5	-243
250	VDD	8787.5	-243
251	VDD	8872.5	-243
252	SHIELDING	8957.5	-243
253	GND	9042.5	-243
254	GND	9127.5	-243
255	GND	9212.5	-243
256	GND	9297.5	-243
257	SHIELDING	9382.5	-243
258	AVDD	9467.5	-243
259	AVDD	9552.5	-243
260	AVDD	9637.5	-243
261	AVDD	9722.5	-243
262	SHIELDING	9807.5	-243
263	AGND	9892.5	-243
264	AGND	9977.5	-243
265	AGND	10062.5	-243
266	AGND	10147.5	-243
267	SHIELDING	10232.5	-243
268	TP	10317.5	-243
269	VCOMI	10402.5	-243
270	VCOMI	10487.5	-243
271	PWR_EN	10572.5	-243
272	PWR_EN	10657.5	-243
273	FBL	10742.5	-243
274	FBL	10827.5	-243
275	FBH	10912.5	-243
276	FBH	10997.5	-243
277	FBA	11082.5	-243
278	FBA	11167.5	-243
279	AVDDG	11252.5	-243
280	AVDDG	11337.5	-243
281	DRVA	11422.5	-243
282	DRVA	11507.5	-243
283	DRVH	11592.5	-243
284	DRVH	11677.5	-243
285	DRVL	11762.5	-243
286	DRVL	11847.5	-243
287	DRVL_B	11932.5	-243
288	DRVL_B	12017.5	-243
289	VCOMO	12102.5	-243
290	VCOMO	12187.5	-243
291	COM2_IN	12272.5	-243
292	COM2_IN	12357.5	-243
293	STBNL	12303	-82
294	F_CtrlL	12403	-42
295	STV2L	12303	-2
296	STV1L	12403	38
297	CKVL	12303	78
298	UDL	12403	118
299	SYNC2L	12303	158
300	SYNC1L	12403	198
301	OEVL	12303	238
302	F_CtrlL	12403	278
303	SHIELDING	12205	258
304	COM2_OUT	12155	258
305	COM2_OUT	12105	258
306	SHIELDING	12055	258
307	SO1	12012.5	113
308	SO2	11997.5	243
309	SO3	11982.5	113
310	SO4	11967.5	243
311	SO5	11952.5	113
312	SO6	11937.5	243
313	SO7	11922.5	113
314	SO8	11907.5	243
315	SO9	11892.5	113
316	SO10	11877.5	243
317	SO11	11862.5	113
318	SO12	11847.5	243
319	SO13	11832.5	113
320	SO14	11817.5	243
321	SO15	11802.5	113
322	SO16	11787.5	243
323	SO17	11772.5	113

324	SO18	11757.5	243
325	SO19	11742.5	113
326	SO20	11727.5	243
327	SO21	11712.5	113
328	SO22	11697.5	243
329	SO23	11682.5	113
330	SO24	11667.5	243
331	SO25	11652.5	113
332	SO26	11637.5	243
333	SO27	11622.5	113
334	SO28	11607.5	243
335	SO29	11592.5	113
336	SO30	11577.5	243
337	SO31	11562.5	113
338	SO32	11547.5	243
339	SO33	11532.5	113
340	SO34	11517.5	243
341	SO35	11502.5	113
342	SO36	11487.5	243
343	SO37	11472.5	113
344	SO38	11457.5	243
345	SO39	11442.5	113
346	SO40	11427.5	243
347	SO41	11412.5	113
348	SO42	11397.5	243
349	SO43	11382.5	113
350	SO44	11367.5	243
351	SO45	11352.5	113
352	SO46	11337.5	243
353	SO47	11322.5	113
354	SO48	11307.5	243
355	SO49	11292.5	113
356	SO50	11277.5	243
357	SO51	11262.5	113
358	SO52	11247.5	243
359	SO53	11232.5	113
360	SO54	11217.5	243
361	SO55	11202.5	113
362	SO56	11187.5	243
363	SO57	11172.5	113
364	SO58	11157.5	243
365	SO59	11142.5	113
366	SO60	11127.5	243
367	SO61	11112.5	113
368	SO62	11097.5	243
369	SO63	11082.5	113
370	SO64	11067.5	243
371	SO65	11052.5	113
372	SO66	11037.5	243
373	SO67	11022.5	113
374	SO68	11007.5	243
375	SO69	10992.5	113
376	SO70	10977.5	243
377	SO71	10962.5	113
378	SO72	10947.5	243
379	SO73	10932.5	113
380	SO74	10917.5	243
381	SO75	10902.5	113
382	SO76	10887.5	243
383	SO77	10872.5	113
384	SO78	10857.5	243
385	SO79	10842.5	113
386	SO80	10827.5	243
387	SO81	10812.5	113
388	SO82	10797.5	243
389	SO83	10782.5	113
390	SO84	10767.5	243
391	SO85	10752.5	113
392	SO86	10737.5	243
393	SO87	10722.5	113
394	SO88	10707.5	243
395	SO89	10692.5	113
396	SO90	10677.5	243
397	SO91	10662.5	113
398	SO92	10647.5	243
399	SO93	10632.5	113
400	SO94	10617.5	243
401	SO95	10602.5	113
402	SO96	10587.5	243
403	SO97	10572.5	113
404	SO98	10557.5	243
405	SO99	10542.5	113
406	SO100	10527.5	243
407	SO101	10512.5	113
408	SO102	10497.5	243
409	SO103	10482.5	113
410	SO104	10467.5	243
411	SO105	10452.5	113
412	SO106	10437.5	243
413	SO107	10422.5	113
414	SO108	10407.5	243
415	SO109	10392.5	113
416	SO110	10377.5	243
417	SO111	10362.5	113
418	SO112	10347.5	243
419	SO113	10332.5	113
420	SO114	10317.5	243
421	SO115	10302.5	113
422	SO116	10287.5	243
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1567	SO1252	-7752.5	113
1568	SO1253	-7767.5	243
1569	SO1254	-7782.5	113
1570	SO1255	-7797.5	243
1571	SO1256	-7812.5	113
1572	SO1257	-7827.5	243
1573	SO1258	-7842.5	113
1574	SO1259	-7857.5	243
1575	SO1260	-7872.5	113
1576	SO1261	-7887.5	243
1577	SO1262	-7902.5	113
1578	SO1263	-7917.5	243
1579	SO1264	-7932.5	113
1580	SO1265	-7947.5	243
1581	SO1266	-7962.5	113
1582	SO1267	-7977.5	243
1583	SO1268	-7992.5	113
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1585	SO1270	-8022.5	113
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1587	SO1272	-8052.5	113
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1590	SO1275	-8097.5	243
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1592	SO1277	-8127.5	243
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1596	SO1281	-8187.5	243
1597	SO1282	-8202.5	113
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1600	SO1285	-8247.5	243
1601	SO1286	-8262.5	113
1602	SO1287	-8277.5	243
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1604	SO1289	-8307.5	243
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1609	SO1294	-8382.5	113
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1611	SO1296	-8412.5	113
1612	SO1297	-8427.5	243
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1623	SO1308	-8592.5	113
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1625	SO1310	-8622.5	113
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1627	SO1312	-8652.5	113
1628	SO1313	-8667.5	243
1629	SO1314	-8682.5	113
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1631	SO1316	-8712.5	113
1632	SO1317	-8727.5	243
1633	SO1318	-8742.5	113
1634	SO1319	-8757.5	243
1635	SO1320	-8772.5	113
1636	SO1321	-8787.5	243
1637	SO1322	-8802.5	113
1638	SO1323	-8817.5	243
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1651	SO1336	-9012.5	113
1652	SO1337	-9027.5	243
1653	SO1338	-9042.5	113
1654	SO1339	-9057.5	243
1655	SO1340	-9072.5	113
1656	SO1341	-9087.5	243
1657	SO1342	-9102.5	113
1658	SO1343	-9117.5	243
1659	SO1344	-9132.5	113
1660	SO1345	-9147.5	243
1661	SO1346	-9162.5	113
1662	SO1347	-9177.5	243
1663	SO1348	-9192.5	113
1664	SO1349	-9207.5	243
1665	SO1350	-9222.5	113
1666	SO1351	-9237.5	243
1667	SO1352	-9252.5	113
1668	SO1353	-9267.5	243
1669	SO1354	-9282.5	113
1670	SO1355	-9297.5	243
1671	SO1356	-9312.5	113
1672	SO1357	-9327.5	243
1673	SO1358	-9342.5	113
1674	SO1359	-9357.5	243
1675	SO1360	-9372.5	113
1676	SO1361	-9387.5	243
1677	SO1362	-9402.5	113
1678	SO1363	-9417.5	243
1679	SO1364	-9432.5	113
1680	SO1365	-9447.5	243
1681	SO1366	-9462.5	113
1682	SO1367	-9477.5	243
1683	SO1368	-9492.5	113
1684	SO1369	-9507.5	243
1685	SO1370	-9522.5	113
1686	SO1371	-9537.5	243
1687	SO1372	-9552.5	113
1688	SO1373	-9567.5	243
1689	SO1374	-9582.5	113
1690	SO1375	-9597.5	243
1691	SO1376	-9612.5	113
1692	SO1377	-9627.5	243
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1694	SO1379	-9657.5	243
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1696	SO1381	-9687.5	243
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1699	SO1384	-9732.5	113
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1708	SO1393	-9867.5	243
1709	SO1394	-9882.5	113

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1729	SO1414	-10182.5	113
1730	SO1415	-10197.5	243
1731	SO1416	-10212.5	113
1732	SO1417	-10227.5	243
1733	SO1418	-10242.5	113
1734	SO1419	-10257.5	243
1735	SO1420	-10272.5	113
1736	SO1421	-10287.5	243
1737	SO1422	-10302.5	113
1738	SO1423	-10317.5	243
1739	SO1424	-10332.5	113
1740	SO1425	-10347.5	243
1741	SO1426	-10362.5	113
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1746	SO1431	-10437.5	243
1747	SO1432	-10452.5	113
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1751	SO1436	-10512.5	113
1752	SO1437	-10527.5	243
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1754	SO1439	-10557.5	243
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1756	SO1441	-10587.5	243
1757	SO1442	-10602.5	113
1758	SO1443	-10617.5	243
1759	SO1444	-10632.5	113
1760	SO1445	-10647.5	243
1761	SO1446	-10662.5	113
1762	SO1447	-10677.5	243
1763	SO1448	-10692.5	113
1764	SO1449	-10707.5	243
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1767	SO1452	-10752.5	113
1768	SO1453	-10767.5	243
1769	SO1454	-10782.5	113
1770	SO1455	-10797.5	243
1771	SO1456	-10812.5	113
1772	SO1457	-10827.5	243
1773	SO1458	-10842.5	113
1774	SO1459	-10857.5	243
1775	SO1460	-10872.5	113
1776	SO1461	-10887.5	243
1777	SO1462	-10902.5	113
1778	SO1463	-10917.5	243
1779	SO1464	-10932.5	113
1780	SO1465	-10947.5	243
1781	SO1466	-10962.5	113
1782	SO1467	-10977.5	243
1783	SO1468	-10992.5	113
1784	SO1469	-11007.5	243
1785	SO1470	-11022.5	113
1786	SO1471	-11037.5	243
1787	SO1472	-11052.5	113
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1790	SO1475	-11097.5	243
1791	SO1476	-11112.5	113
1792	SO1477	-11127.5	243
1793	SO1478	-11142.5	113
1794	SO1479	-11157.5	243
1795	SO1480	-11172.5	113
1796	SO1481	-11187.5	243
1797	SO1482	-11202.5	113
1798	SO1483	-11217.5	243
1799	SO1484	-11232.5	113
1800	SO1485	-11247.5	243
1801	SO1486	-11262.5	113
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1803	SO1488	-11292.5	113
1804	SO1489	-11307.5	243
1805	SO1490	-11322.5	113
1806	SO1491	-11337.5	243
1807	SO1492	-11352.5	113
1808	SO1493	-11367.5	243
1809	SO1494	-11382.5	113
1810	SO1495	-11397.5	243
1811	SO1496	-11412.5	113
1812	SO1497	-11427.5	243
1813	SO1498	-11442.5	113
1814	SO1499	-11457.5	243
1815	SO1500	-11472.5	113
1816	SO1501	-11487.5	243
1817	SO1502	-11502.5	113
1818	SO1503	-11517.5	243
1819	SO1504	-11532.5	113
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1826	SO1511	-11637.5	243
1827	SO1512	-11652.5	113
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1834	SO1519	-11757.5	243
1835	SO1520	-11772.5	113
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1842	SO1527	-11877.5	243
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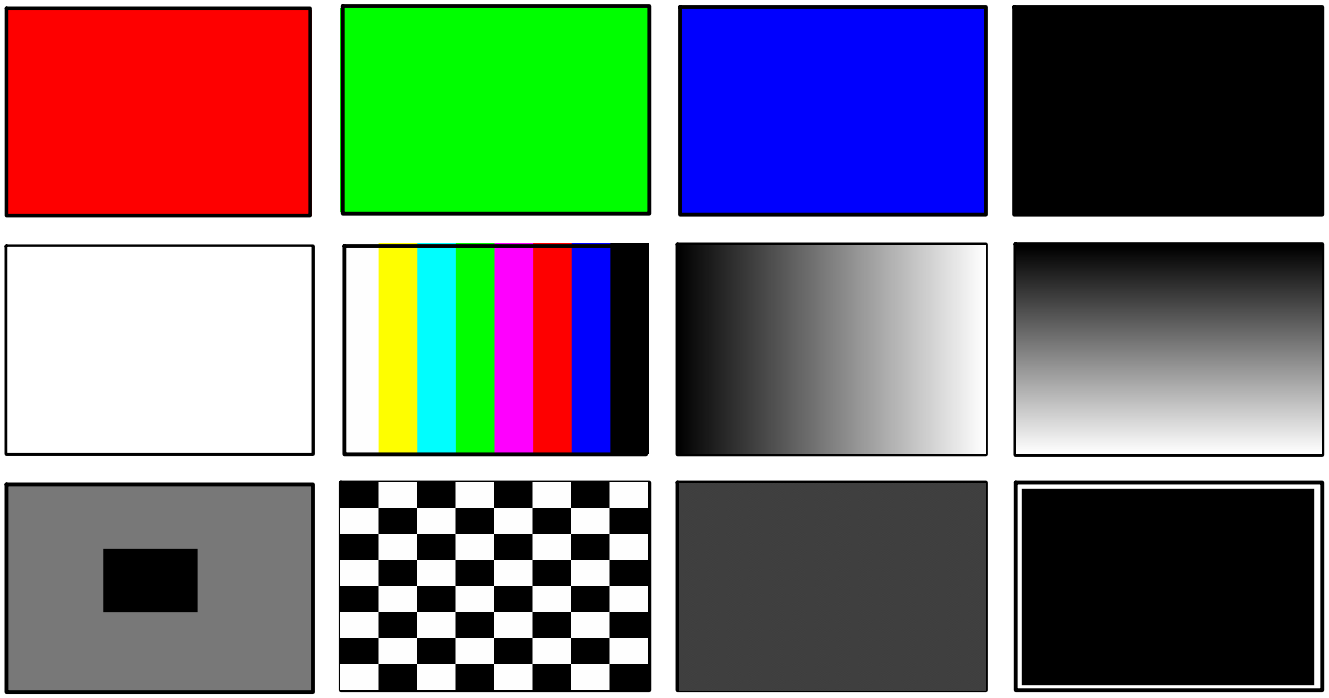
1847	SO1532	-11952.5	113
1848	SO1533	-11967.5	243
1849	SO1534	-11982.5	113
1850	SO1535	-11997.5	243
1851	SO1536	-12012.5	113
1852	SHIELDING	-12055	258
1853	COM1_OUT	-12105	258
1854	COM1_OUT	-12155	258
1855	SHIELDING	-12205	258
1856	F_CtrlR	-12403	278
1857	OEVR	-12303	238
1858	SYNC1R	-12403	198
1859	SYNC2R	-12303	158
1860	UDR	-12403	118
1861	CKVR	-12303	78
1862	STV2R	-12403	38
1863	STV1R	-12303	-2
1864	F_CtrlR	-12403	-42
1865	STBNR	-12303	-82
	ALIGNMENT_MARK_L	-12131.5	115.5
	ALIGNMENT_MARK_R	12131.5	115.5

Appendix A : BIST pattern

R→ G → B → Black → White → Color Bar → Horizontal 256 gray scale → Vertical 256 gray scale → Crosstalk pattern → Chess board (L255/L0) → Flicker pattern → Black background with white out frame



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