ILI2130

Single Chip Capacitive Touch Panel Controller

Data Sheet

(Preliminary)

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1. Introduction

ILI2130 is a high performance capacitive touch panel controller. It integrates I2C interfaces and Flash memory into a QFN-56 package. ILI2130 has 43 touch sensor channels, it can support out-cell and on-cell touch sensors.

With ILITEK's unique driving technology and algorithm, ILI2130 has excellent noise immunity ability and acheave high signal to noise ratio. For noise immunity, ILI2130 can support IEC-61000-4-6 CS 10Vrms requirement. ILI2130 is an optimal touch solution for Tablet, Appliance, HMI, POS applications.

2. Features

2.1 Driving and Sensing Channels for Capacitive Touch Panel

- 5 TX driving channels
- 22 RX sensing channels
- 16 TRX channels
- 1 Guarding (GR) channel
- Integrated x5 AVDD_CP charge pump controller and support 10V driving voltage for driving heavy RC loading touch panel.
- Support mutual-cap and self-cap driving/sensing technology
- Support G/G (DITO), G/G (SITO), OGS, GFF, GF2, FFF and On-Cell touch panel stack up (approved by ILITEK or ILITEK qualified touch panel maker)
- Support both of direct bonding and air bonding with TFT and IPS LCD module (LCM)
- Support Ag nano wire (AgNW), metal mesh (copper or Ag), printing copper and ITO conductive material
- Support Diamond and proprietary sensor patterns (approved by ILITEK or ILITEK qualified touch panel maker)
- Support PET and glass cover lens
  - Plastic 0.2mm to 4mm, depends on panel size, touch size, panel stack up and performance requirements
  - Glass 0.4mm to 8mm, depends on panel size, touch size, panel stack up and performance requirements

2.2 Host Interface

- I2C
  - Support 100kHz standard mode and 400kHz fast mode clock rate
  - I2C slave clock stretching function
  - Support Windows HID over I2C protocol

2.3 Reset

- Support chip enable/disable input
- Support power on reset (POR) function
- Support low voltage detection (LVD) function

2.4 Power Supply

- Input voltage for Analog (AVDD_CP) and Digital (PVDD), nominal 3.3V
- On-chip 1.2V regulator output for Digital core (VDD), nominal 1.2V
- On-chip X2 charge pump controller output (PVDD_MVCP), nominal 2*AVDD_CP
- On-chip programmingable MV regulator output for internal Analog circuit (AVDD)
- On-chip X5 charge pump controller and regulator output (HVDD), nominal 10V

2.5 General Purpose I/O (GPIO)

- 4.9V general purpose I/O, up to 23 pin (Multi-function with Rx channel and RX_GR)

2.6 Package

- 56-pin, QFN-56, 6 × 6 × 0.75 mm, pitch 0.35 mm.
- EPAD, IC ground, please connect to ground.

2.7 Operating Temperature

- -40℃ to +85℃

2.8 Storage temperature

- -55~125°C

3. Device Overview

3.1. Block Diagram

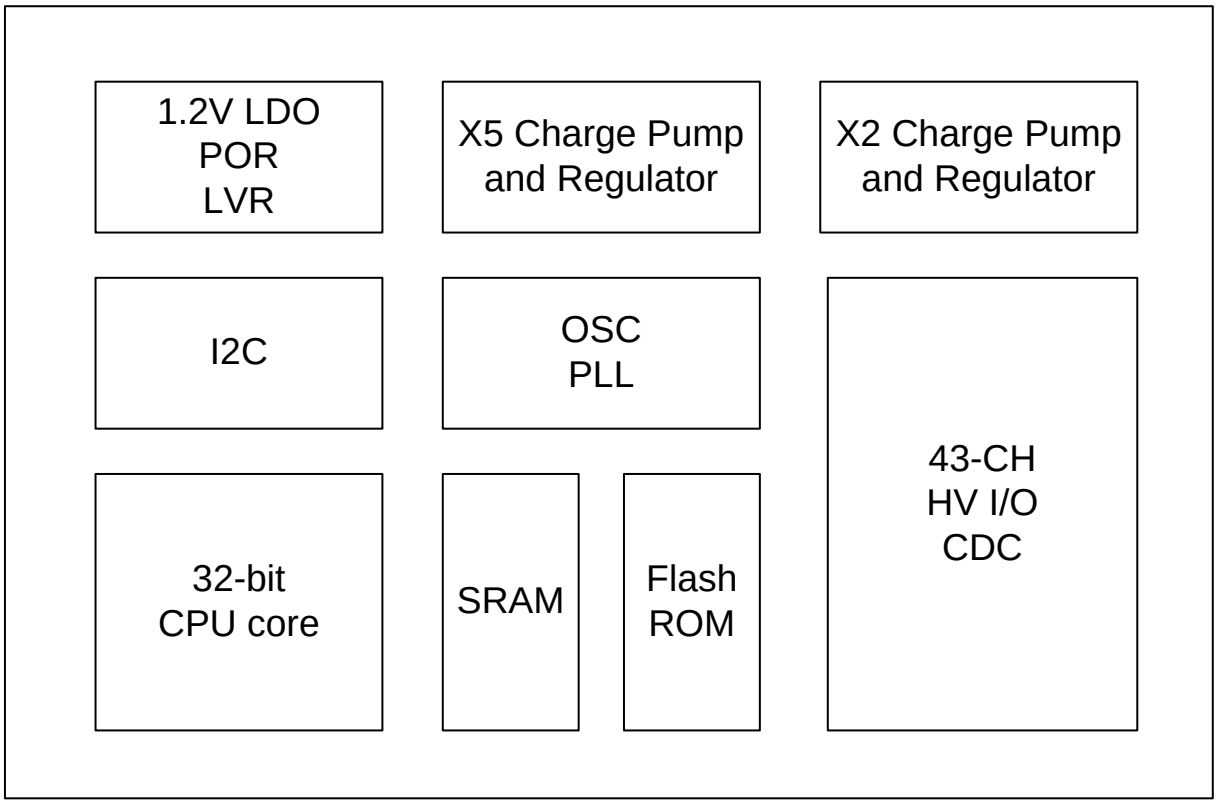


Figure 1. ILI2130 Block Diagram

3.2. Pin Configuration

3.2.1. QFN-56 (Top View)

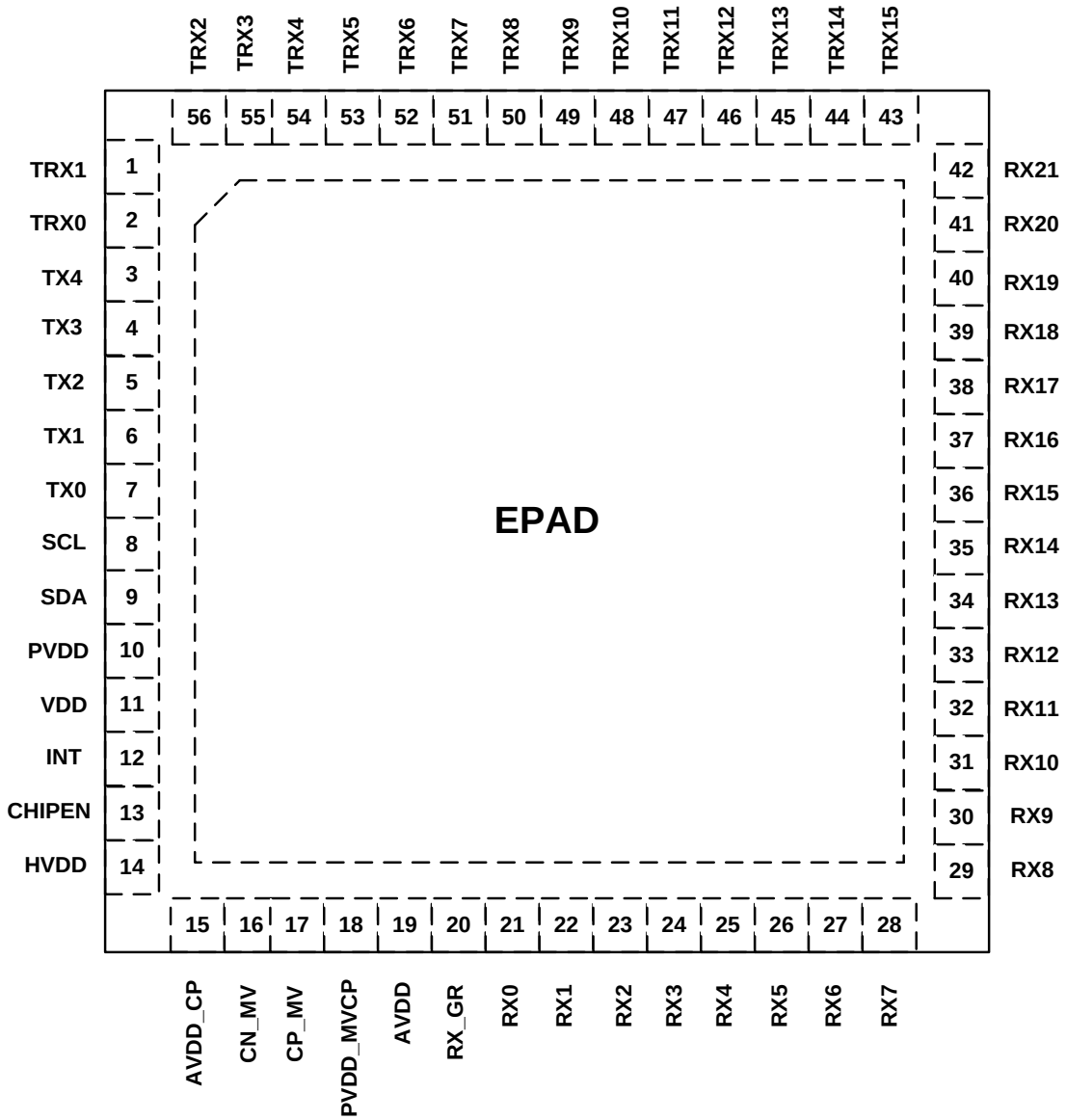


Figure 2. ILI2130 Pin Configuration

3.2.2. Pin Definition

Pin	Name	Type	Description	If Unused...
1 ~ 2	TRX1 ~ TRX0	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
3 ~ 7	TX4 ~ Tx0	I/O	TX driving channels	Leave open
8	SCL	I	I2C Mode: Serial Clock.	--
9	SDA	I/O	I2C Mode: Serial Data.	--
10	PVDD	P	Input power supply, typical 3.3V. Connect to a 1uF/10V/X5R bypass capacitor.	--
11	VDD	P	On-chip 1.2V regulator output, typical 1.2V. Connect to a 1uF/10V/X5R bypass capacitor.	--
12	INT	I/O	Multi-function I/O. It can be programming as INT signal or UART TXD signal. INT: Interrupt signal to Host. Normal: High, Active: Low UART TXD: UART transmit data channel	--
13	CHIPEN	I	Chip reset signal. Normal: High, Active Reset: Low	--
14	HVDD	P	Input power supply for TX driving channel. Connect to a 2.2uF/25V/X5R bypass capacitor. HVDD internal mode: On-chip programmingable HV regulator output. Output Level : 8V to 10 V External mode : Input Level : 10V to 25V	--
15	AVDD_CP	I	Input power supply, typical 3.3V. Connect to a 1uF/10V/X5R bypass capacitor.	--
16	CN_MV	P	Fly capacitor output of On-chip AVDD_CP x2 charge pump controller. Connect a 2.2uF/10V/X5R fly capacitor to CP_MV.	--
17	CP_MV	P	Fly capacitor output of On-chip AVDD_CP x2 charge pump controller. Connect a 2.2uF/10V/X5R fly capacitor to CN_MV.	--
18	PVDD_MVCP	P	On-chip AVDD_CP x2 charge pump controller output. Connect to a 2.2uF/10V/X5R bypass capacitor.	--
19	AVDD	P	On-chip programmingable MV regulator output. Connect to a 2.2uF/10V/X5R bypass capacitor.	--
20	RX_GR	I/O	Multi-function I/O. It can be programming as Guarding (GR) channel or INT signal. INT: Interrupt signal to Host. Normal: High, Active: Low GR: Guarding (GR) signal for TX and RX channels.	--
21 ~ 42	RX0 ~ RX21	I/O	RX sensing channel	Leave open
43 ~ 56	TRX15 ~ TRX2	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
--	EPAD	P	IC Ground.	--

Pin Type:

P: Power or Ground

I: Input only

O: Output only

I/O: Input or Output

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Item	Symbol	Unit	Value
Input Power Supply 1	PVDD	V	-0.3 ~ +3.4
Input Power Supply 2	AVDD_CP	V	-0.3 ~ +3.4
Input Power Supply 3	HVDD	V	-0.3 ~ +25
Parameters maximum writes		Cycle	10,000
ESD target for Human Body Model	HBM	V	4000
ESD target for Machine Model	MM	V	400
Maximum junction temperature	Tj	℃	125
Operating temperature	Topr	℃	-40 ~ +85
Storage temperature	Tstg	℃	-55 ~ +125

CAUTION:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanently damage to the device. These are stresses ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the device.

4.2. Recommended Operating Conditions

Item	Symbol	Unit	Recommended Value
Input Power Supply 1	PVDD	V	3.3 ± 3%
Input Power Supply 2	AVDD_CP	V	3.3 ± 3%
Input Power Supply 3	HVDD	V	10 (For Internal mode) 20 (For External mode)
Operating Temperature	Topr	℃	-40 ~ +85
Storage Temperature	Tstg	℃	-55 ~ +125
Temperature Slew Rate			10℃/min

4.3. Input Power Supply and GPIO Characteristics

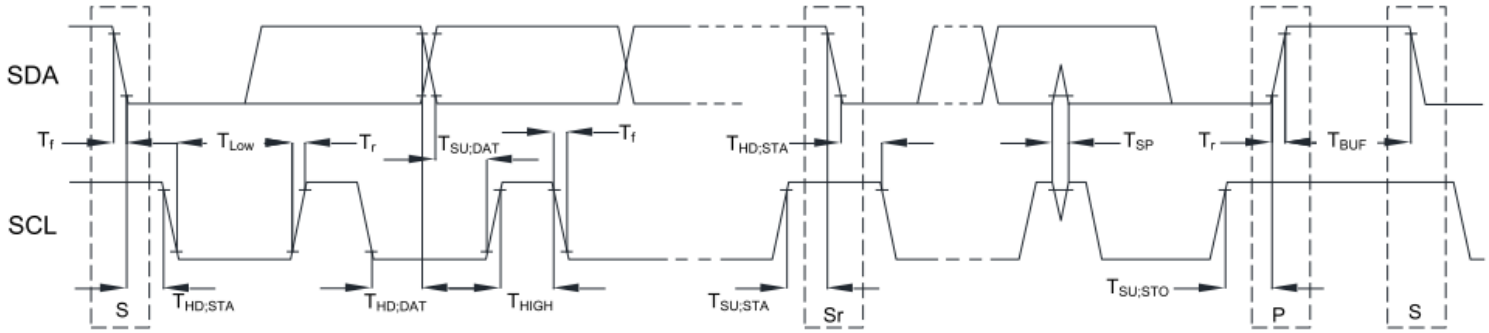
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Power Supply 1	PVDD	2.97	3.3	3.4	V	
Input Power Supply 2	AVDD_CP	2.97	3.3	3.4	V	
Input Power Supply 3	HVDD	-	8	10	V	Internal mode
		10	20	25	V	External mode
On-Chip 1.2V Regulator	VDD	1.08	1.2	1.32	V	
Operating Current	PVDD		90		mA	1
Idle Current	PVDD		20		mA	1
Low Input Logic Level	VIL			0.3*PVDD	V	
High Input Logic Level	VIH	0.7*PVDD			V	

Note 1: The configuration values listed as below table were used in the ILITEK's Bench Board to validate the interfaces and derive the operating current.

Test Configuration Table

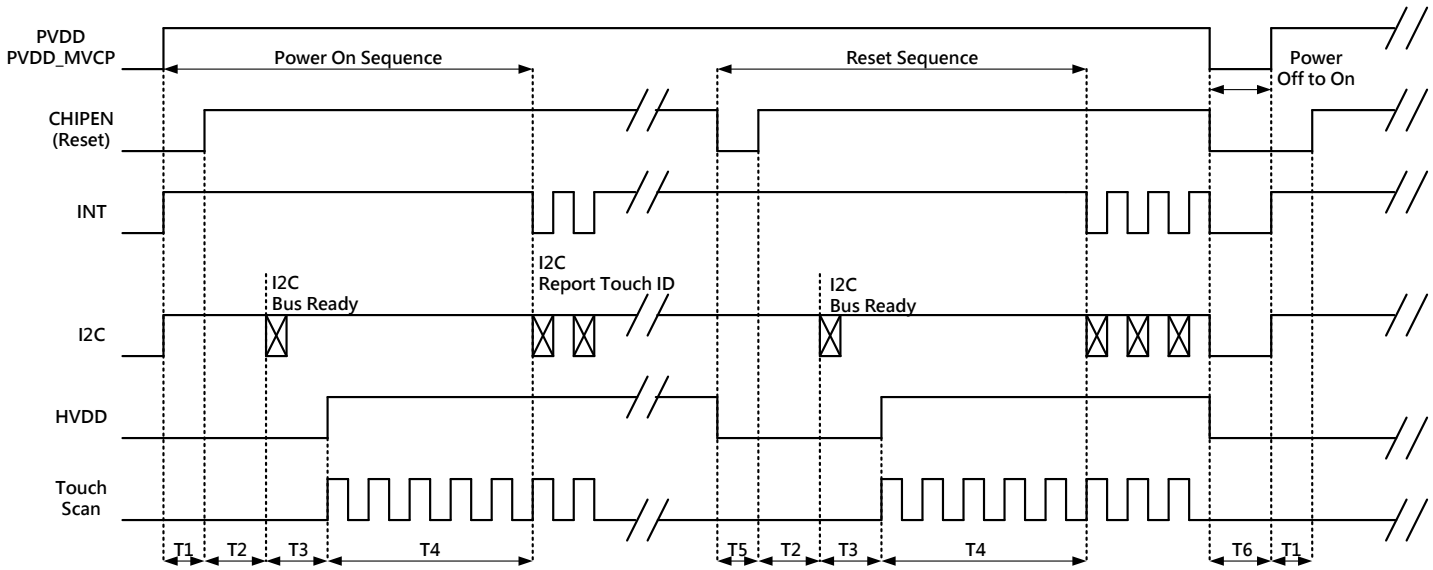
Item	Value	Note
HVDD	10V	HVDD Internal mode.
Active Mode Report Rate	125Hz	ILI2130 report Touch ID to ILITEK's I2C to USB Bridge Board.
Report Touch ID Number	10	
I2C SCL Clock Rate	400kHz	Fast mode
I2C Idle Mode	Idle time: 30ms	Support Touch Wake Up function

4.4. I2C AC Characteristics



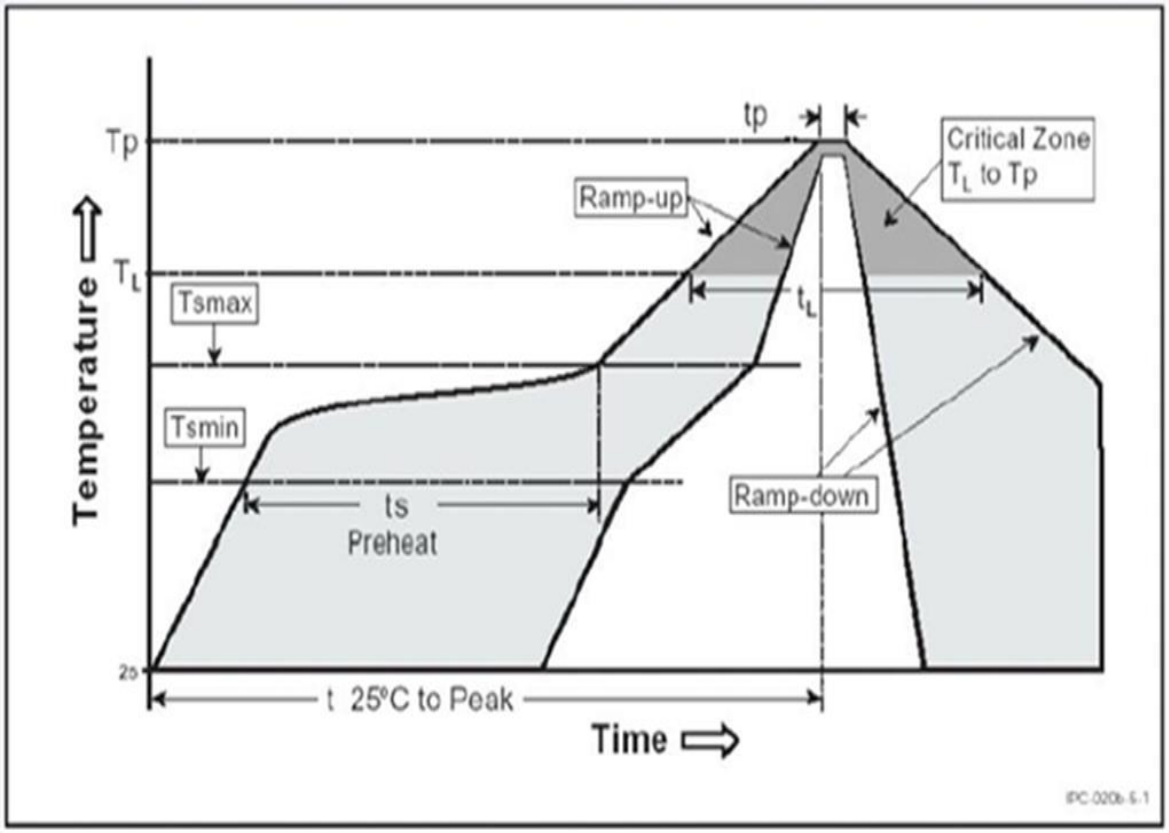
Item	Symbol	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
SCL standard mode clock frequency	FSCL	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock is generated.	THD;STA	4	--	0.6	--	us
LOW period of the SCL clock	TLOW	4.7	--	1.3	--	us
HIGH period of the SCL clock	THIGH	4	--	0.6	--	us
Setup time for a repeat START condition.	TSU;STA	4.7	--	0.6	--	us
Data hold time	THD;DAT	0	--	0	--	us
Data setup time	TSU;DAT	250	--	100	--	ns
Rising time of both SDA and SCL signals	Tr	--	1000	--	300	ns
Falling time of both SDA and SCL signals	Tf	--	300	--	300	ns
Setup time for STOP condition.	TSU;STO	4	--	0.6	--	us
Free time between STOP and START condition	TBUF	4.7	--	1.3	--	us
Pulse width of spikes which must be suppressed by input filter	TSP	--	--	0	50	ns

4.5. Power Sequence



Symbol	Description	Min.	Max.	Unit.
T1	Input Power Supply PVDD, PVDD_MVCP, Power on Reset time. Host need to control Reset time to be larger than 10ms.	10	--	ms
T2	Chip initial time		400	ms
T3	HVDD start up time		300	ms
T4	Chip report Touch ID preparation time		400	ms
T5	Chip Reset and HVDD discharge time. Host need to control Reset time to be larger than 10ms.	10		ms
T6	Input Power Supply PVDD, PVDD_MVCP, and HVDD Power off discharge time. Host need to control discharge time to be larger than 100ms.	100		ms

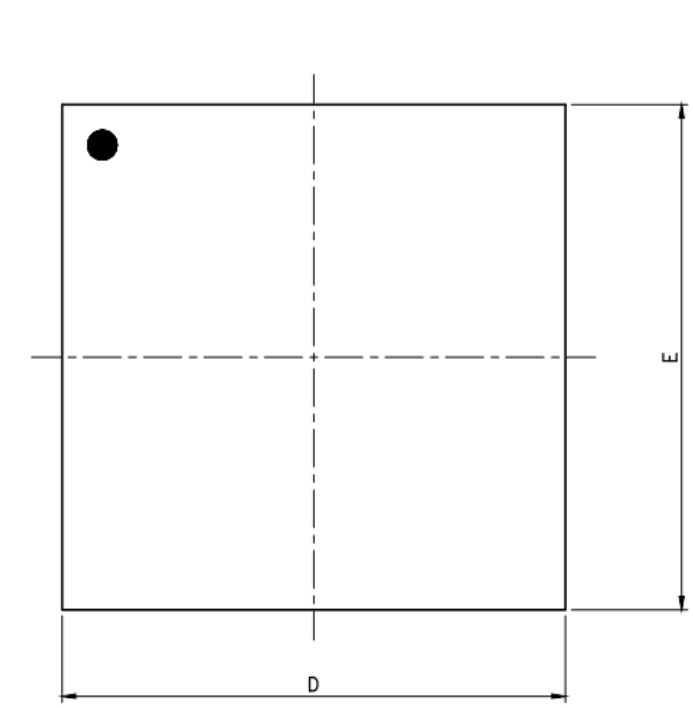
5. SMT IR Reflow Profile

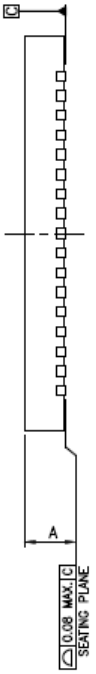


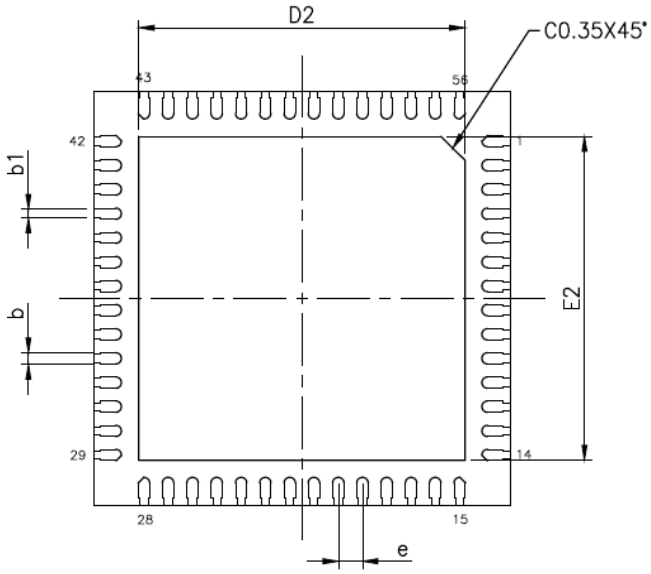
Profile Feature	Pb-Free Assemble
Average ramp-up rate (TL to Tp)	3℃/Second max
Preheat -Temperature Min (Tsmim) -Temperature Max(Tsmax) -Time (min to max)(ts)	 150℃ 200℃ 60-120 Seconds
Time maintained above -Temperature(TL) -Time(tL)	 217℃ 60-150 Seconds
Peak Temperature(Tp)	245 +0/-5℃
Time within 5℃ of actual Peak Temperature(tp)	20-40 Seconds
Ramp-down Rate	3℃ /Second max
Time 25℃ to Peak Temperature	8 minutes max

6. Package Information

6.1. QFN-56 Package Dimension



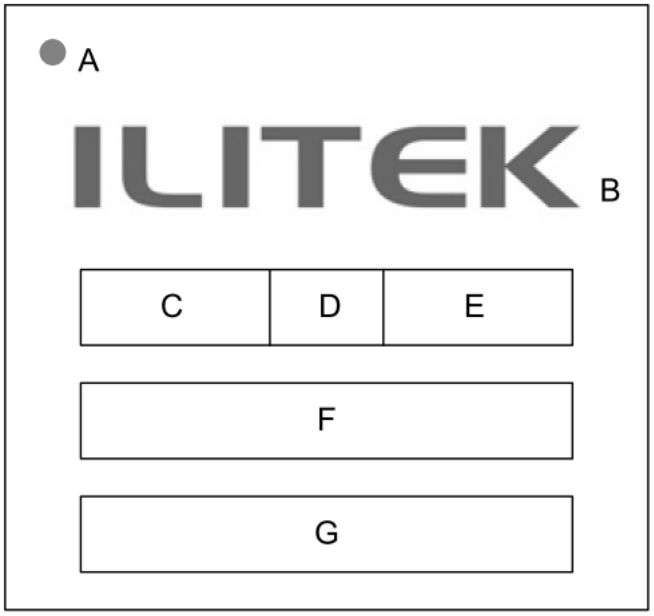




	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X656)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D	6.00 BSC		
E	6.00 BSC		
e	0.35 BSC		

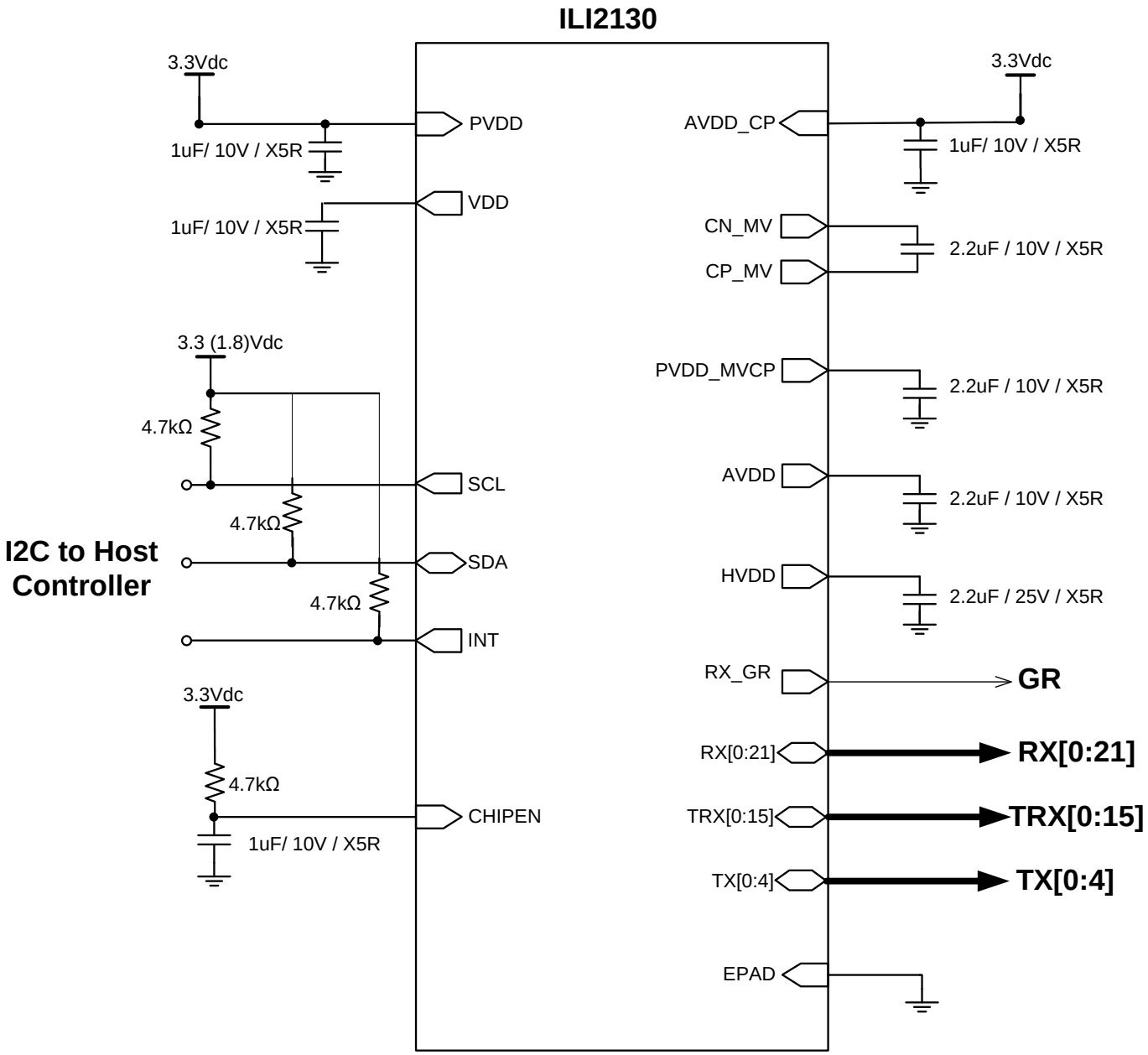
PAD SIZE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
193X19 MIL	4.65	4.70	4.75	4.65	4.70	4.75

6.2. Marking Information



Item	Description
A	Pin 1 Indication
B	ILITEK logo
C	IC Model Name: ILI2130
D	Blank
E	Blank
F	Assembly Lot No.: The code will be updated by production control (1st code is A)
G	Wafer Lot No.: The code will be updated by production control (1st code is A)

7. Typical Application Circuit



8. Revision History

Version No.	Date	Page	Description
V001	2020/03/20	All	Initial release
V002	2020/03/20	4	4.9V general purpose I/O, up to ~~32~~ 26 pin (Multi-function with Rx channel)
V003	2020/05/14	8	Recommand Input Voltage
V004	2020/06/16	5 6, 7-11 12 15	Modify Block Diagram Modify Pin Configuration Figure, Re-edit page 7-11 Add SMT IR Reflow Profile Add Typical Application Circuit