深圳市思迪科科技有限公司
SHENZHEN CDTECH ELECTRONICS

Product Specification

Model Name	S070HWX91NN
Description	800(RGB)x1280 Dots 7" TFT LCD
Date	2022/03/01
Revision	1.0

Approved by/Date	**Check by/Date**	**Prepared by/Date**
ZHP 2022/03/01	HZX 2022/03/01	ZWF 2022/03/01

Customer Approval	
Date	

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1. Record of Revision

Rev	Issued Date	Description	Editor
1.0	2022/03/11	First Release.	ZWF

2 General Specifications

Feature		Spec
Characteristics	Size	7 inch
	Resolution	800(Horizontal)*1280(Vertical)
	Interface	MIPI
	Connect type	Connector
	Color Depth	16.7M
	Technology type	a-Si
	Display Spec. Pixel pitch (mm)	0.117(H)×0.117(V)
	Pixel Configuration	R.G.B. Vertical Stripe
	Display Mode	Normally Black
	Driver IC	HX8260-A
	Viewing Direction	full view
Mechanical	LCM (W x H x D) (mm)	103.46(W)*162.03(H)*2.5(D)
	Active Area(mm)	94.2(H)x 150.72(V)
	With /Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	20 LEDs

Note 1: Viewing direction is follow the data which measured by optics equipment.
Note 2: Requirements on Environmental Protection: RoHS
Note 3: LCM weight tolerance: +/- 5%

3 Input/Output Terminals

LCD PIN-MAP

No	Symbol	Description
1	NC	No connect
2	GND	GROUND
3	MIPI_3N	MIPI Negative data signal(-)
4	MIPI_3P	MIPI Positeve data signal(+)
5	GND	GROUND
6	MIPI_D0N	MIPI Negative data signal(-)
7	MIPI_D0P	MIPI Positeve data signal(+)
8	GND	GROUND
9	MIPI_CKN	MIPI Negative clock signal(-)
10	MIPI_CKP	MIPI Positeve clock signal(+)
11	GND	GROUND
12	MIPI_D1N	MIPI Negative data signal(-)
13	MIPI_D1P	MIPI Positeve data signal(+)
14	GND	GROUND
15	MIPI_D2N	MIPI Negative data signal(-)
16	MIPI_D2P	MIPI Positeve data signal(+)
17	GND	GROUND
18	NC	No connect
19	RESET	Device reset signal
20	GND	GROUND
21	DIMO	CABC PWM output
22	GND	GROUND
23	NC	No connect
24	VDD(1.8V)	Power supply for logic operation
25	AVDD+5.5V	Positive LDO output for Driver IC usage.
26	VDD(1.8V)	Power supply for logic operation
27	AVEE-5.5V	Negative LDO output for Driver IC usage.
28	NC	No connect
29	NC	No connect

30	VDD(1.8V)	Power supply for logic operation
31	TE	LVDS mode(IF_SEL=1):TE output signal
32	GND	GROUND
33	VDD(1.8V)	Power supply for logic operation
34	VDD(1.8V)	Power supply for logic operation
35	LED-K	Power supply for LED(Cathode)
36	LED-K	Power supply for LED(Cathode)
37	NC	No connect
38	LED-A	Power supply for LED(Anode)
39	LED-A	Power supply for LED(Anode)

4 Absolute Maximum Ratings

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	VDD	-0.3	-	3.3	V	-
Analog power supply voltage	AVDD	3.6		6.5	V	
	AVEE	-6.5		-3.6	V	
Operating Temperature	TOPR	-20	-	70	℃	-
Storage Temperature	TSTG	-30	-	80	℃	
Humidity	RH	-	-	90%(Max 60 °C)	RH	

5 Electrical Characteristics

5.1 Driving TFT LCD Panel

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	VDD	1.75	1.8	1.9	V	-
Supply voltage for logic	AVDD	5.0	5.5	6.0	V	
Supply voltage for logic	AVEE	-5.0	-5.5	-3.6	V	
Current of power supply	I_{VDD}	-	80	130	mA	
Input voltage “H”level	VIH	0.7VDD	-	VDD	V	-
Input voltage “L”level	VIL	0	-	0.3VDD	V	

5.2 Driving Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	30	-	mA	
Forward Voltage	V_F	27.0	-	34.0	V	
Backlight Power consumption	W_{BL}	0.81	-	1.02	W	
LED Lifetime		-	30000	-	Hrs	

Note 1: Each LED : IF =20 mA, VF =2.7-3.4V.
Note 2: Optical performance should be evaluated at Ta=25℃ only.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced.Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

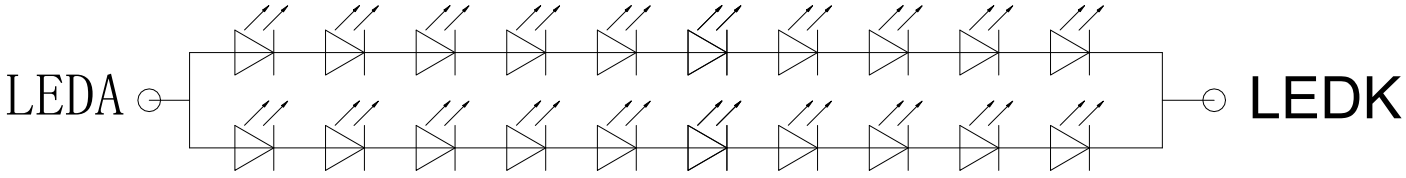
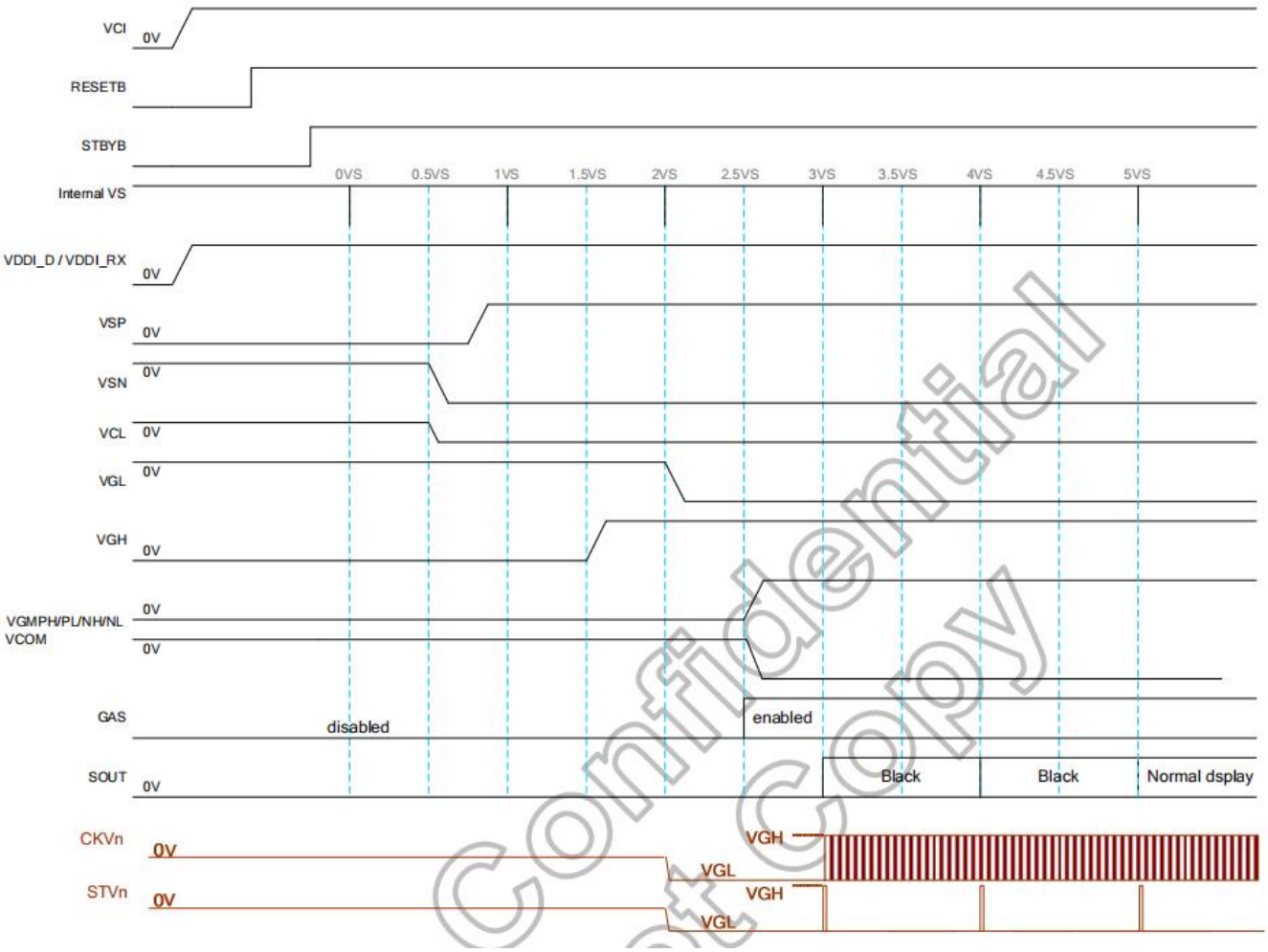


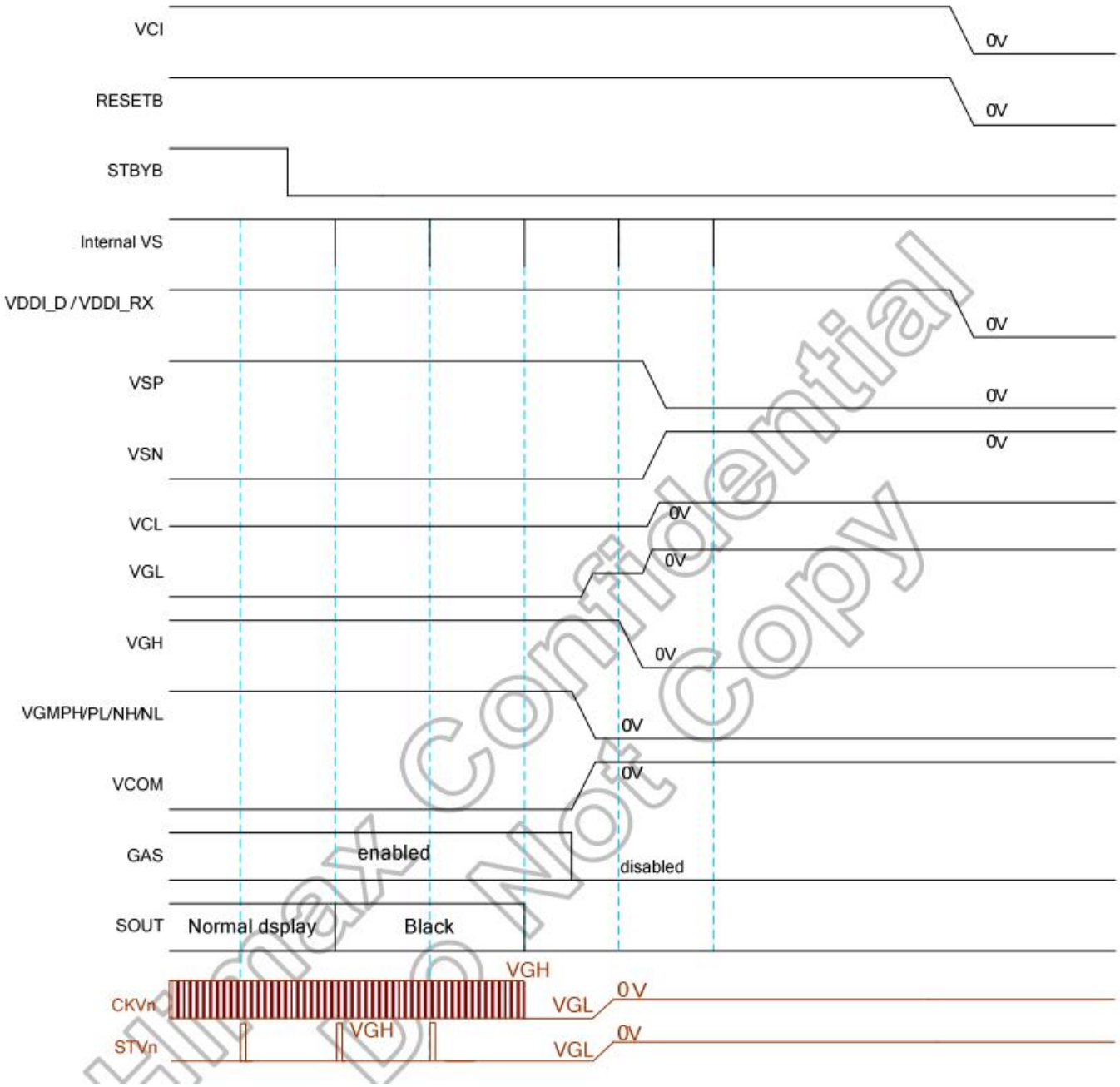
Figure : LED connection of backlight

5.2 POWER SEQUENCE

5.2.1 POWER ON SEQUENCE



5.2.2 POWER OFF SEQUENCE



5.5 RESET TIMING CHARACTERISTICS

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

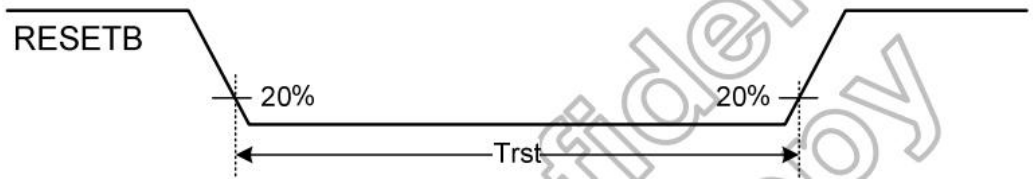
However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(VDDI_D=1.7V~1.9V, VSS=0V, T_A=-20℃~+85℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

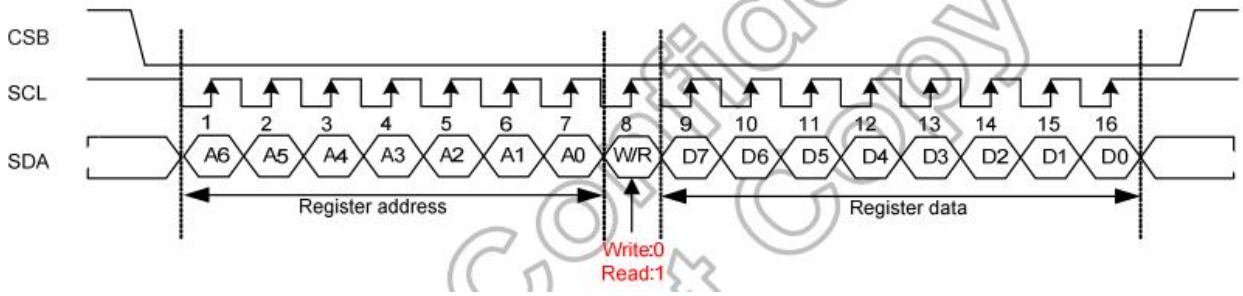
Table 13.6: Reset timing



5.6 Timing CHARACTERISTCS

5.6.1 SPI Timing

For the MIPI mode 3-wire SPI pin are "MIPI_CSB, MIPI_SCK and MIPI_SD"
For the LVDS mode 3-wire SPI pin are ""LNSW_CSB, PNSW_SCL, MIPITE_SDA"



5.6.2 MIPI DC Timing

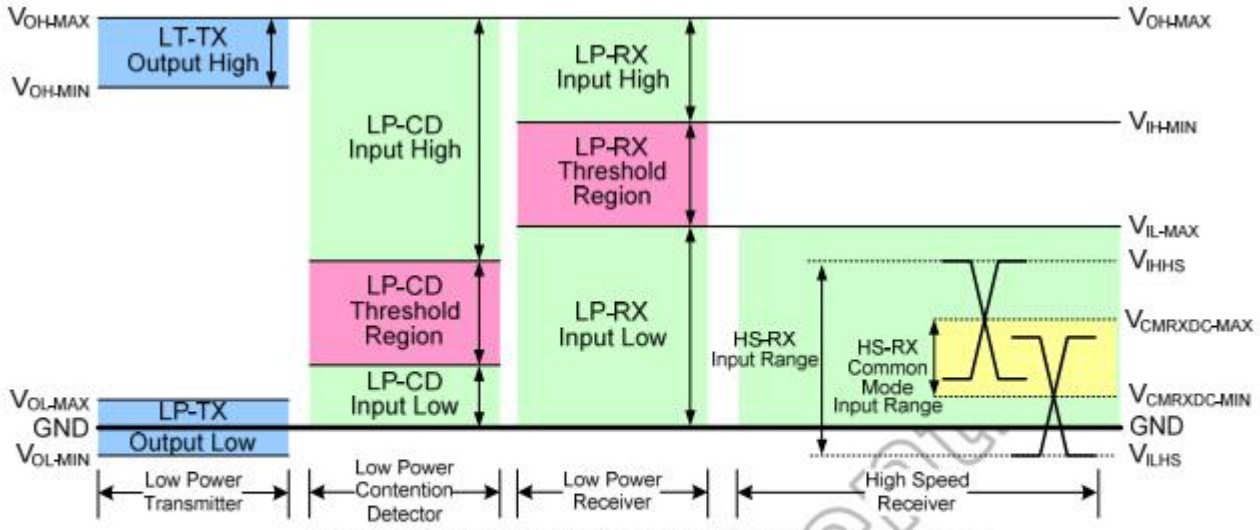


Figure 12.1: MIPI signaling and contention voltage levels

DC characteristics for MIPI LP mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage	V_{IL}	0	-	550	mV
Logic 1 output voltage	V_{OH}	1.1	1.2	1.3	V
Logic 0 output voltage	V_{OL}	-50	-	50	mV

DC characteristics for MIPI HS mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Common-mode voltage HS Receive mode	V_{CMRXDC}	70	-	330	mV
Differential input high threshold	V_{IDTH}	-	-	70	mV
Differential input low threshold	V_{IDTL}	70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Differential input impedance	Z_{ID}	80	100	125	Ω
HS transmit differential voltage **(VDP-VDN)**	|VOD|	140	200	270	mV

Note: (1) V_{IDTH} and V_{IDTL} only for reference, related to power and ground noise, this spec need to check on panel performance to fine tune

5.6.3 MIPI AC Timing

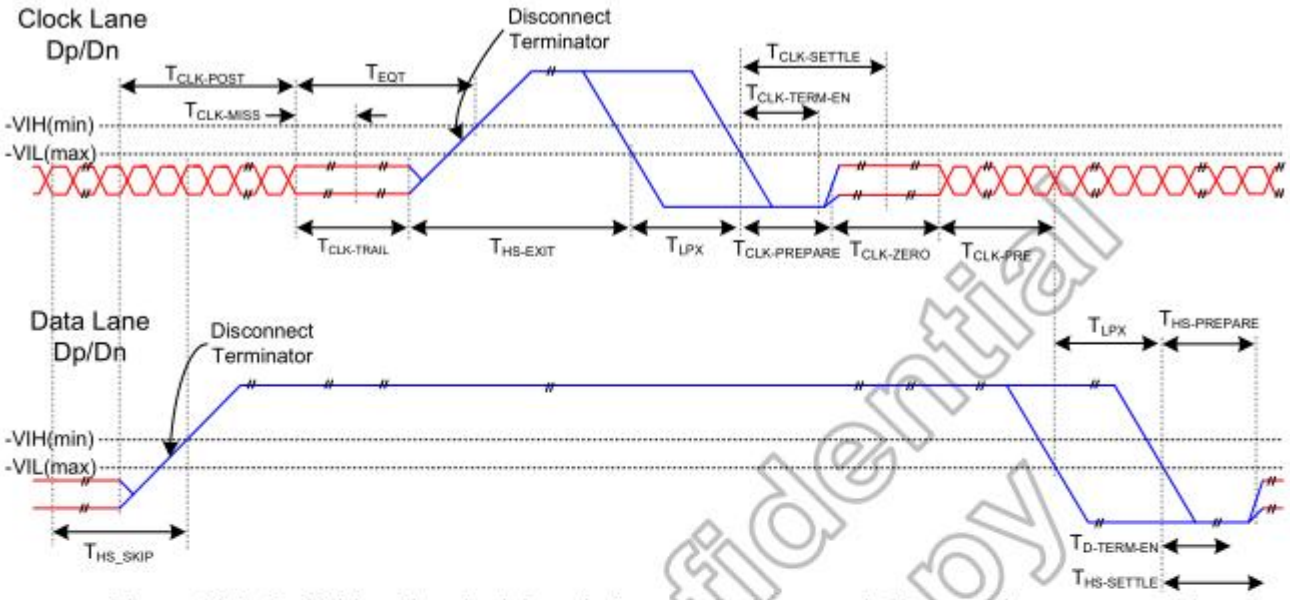


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

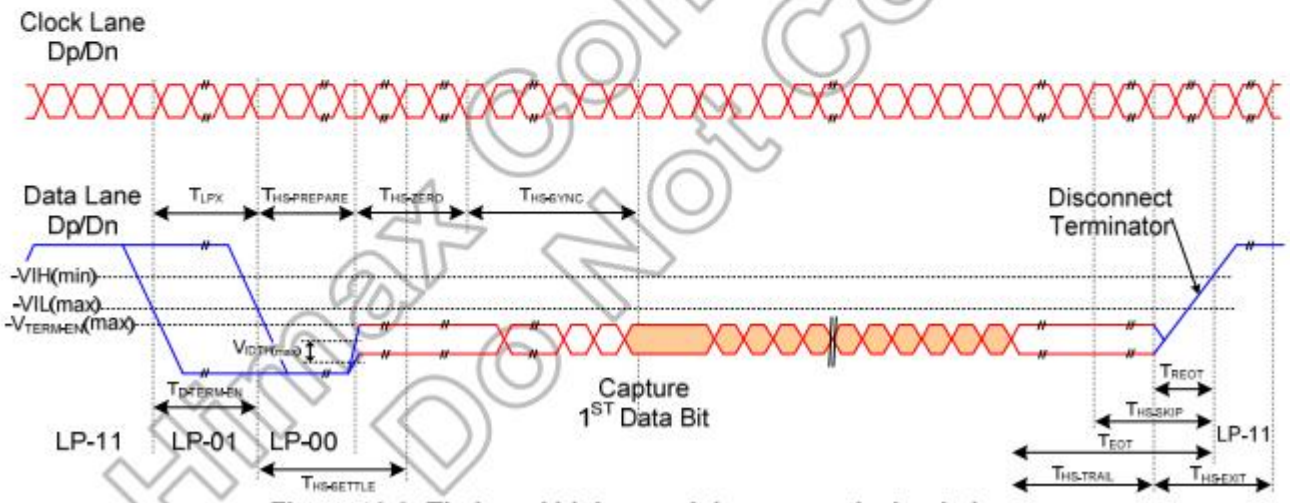


Figure 13.2: Timing of high-speed data transmission in bursts

Parameter	Description	Spec.			Unit
		Min	Typ	Max	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI **(For DCS)**	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX		$5*T_{LPX}$		ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request		$4*T_{LPX}$		ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

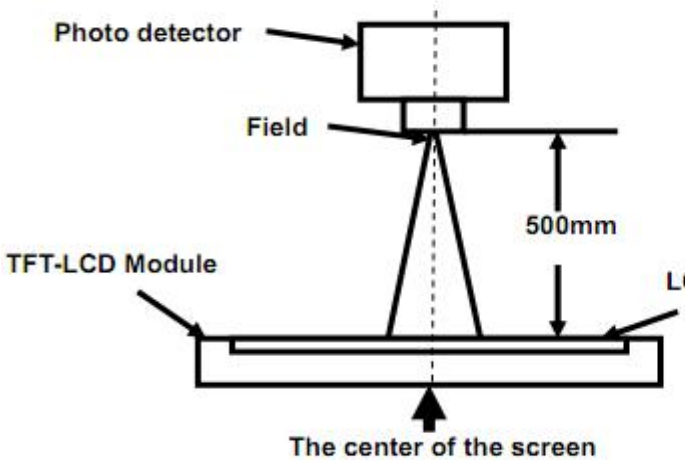
Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

6 Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angles		θ_T	Center CR≥10	80	85	-	Degree.	Note2
		θ_B		80	85	-		
		θ_L		80	85	-		
		θ_R		80	85	-		
Contrast Ratio		CR	Θ =0	600	800	-	-	Note1, Note3
Response Time		T_{ON}	25°C	-	30	40	ms	Note1, Note4
		T_{OFF}						
Chromaticity	White	X_W	Backlight is on	0.263	0.313	0.363	-	Note1, Note5
		Y_W		0.273	0.320	0.373	-	
	Red	X_R		0.603	0.653	0.703	-	
		Y_R		0.280	0.330	0.380	-	
	Green	X_G		0.274	0.324	0.374	-	
		Y_G		0.522	0.572	0.622	-	
	Blue	X_B		0.084	0.134	0.184	-	
		Y_B		0.068	0.118	0.168	-	
Luminance Uniformity		LU		70	75	-	%	Note1, Note6
Luminance		L		270	320		cd/m2	Note1, Note7

Test Conditions:
1. IF= 20mA(one channel),the ambient temperature is 25°C.
2. The test systems refer to Note 1 and Note 2.

Note 1:Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

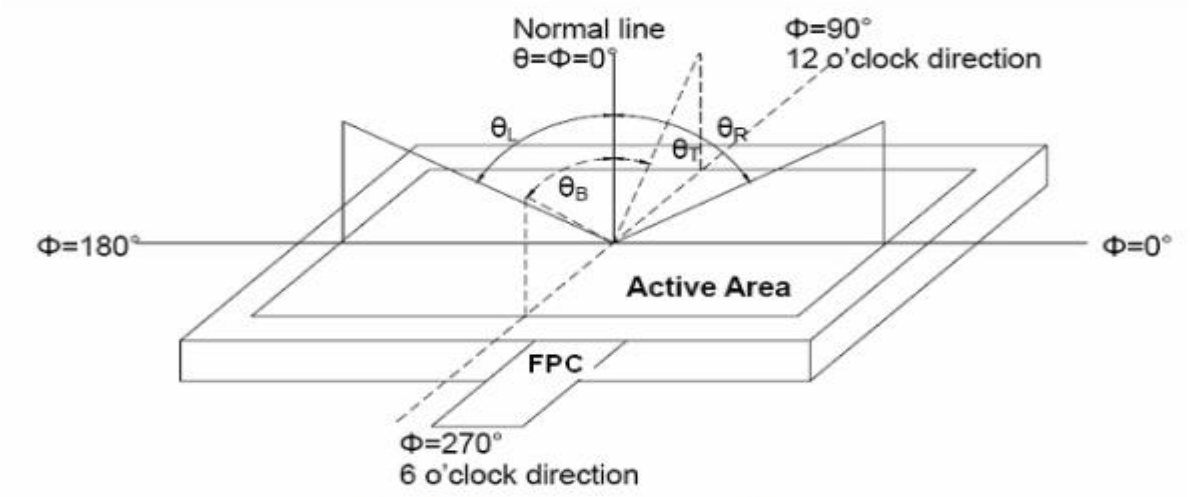


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

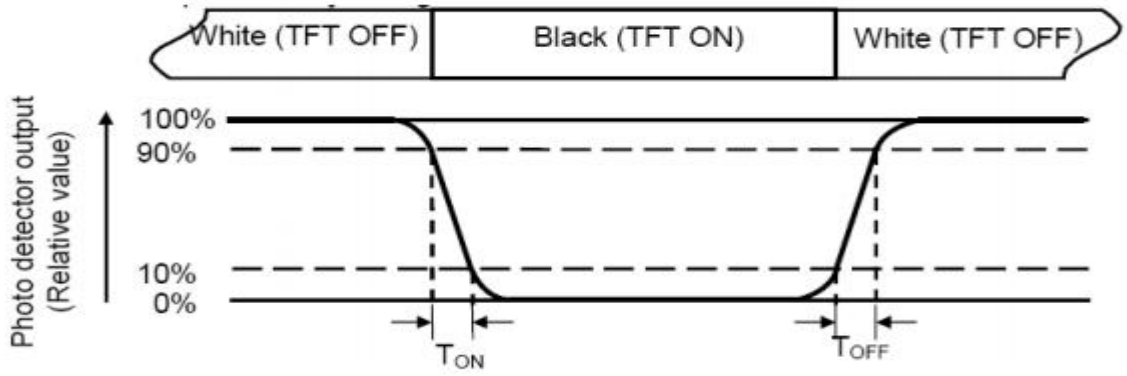
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.
Note 6: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax X100%
L-------Active area length W----- Active area width

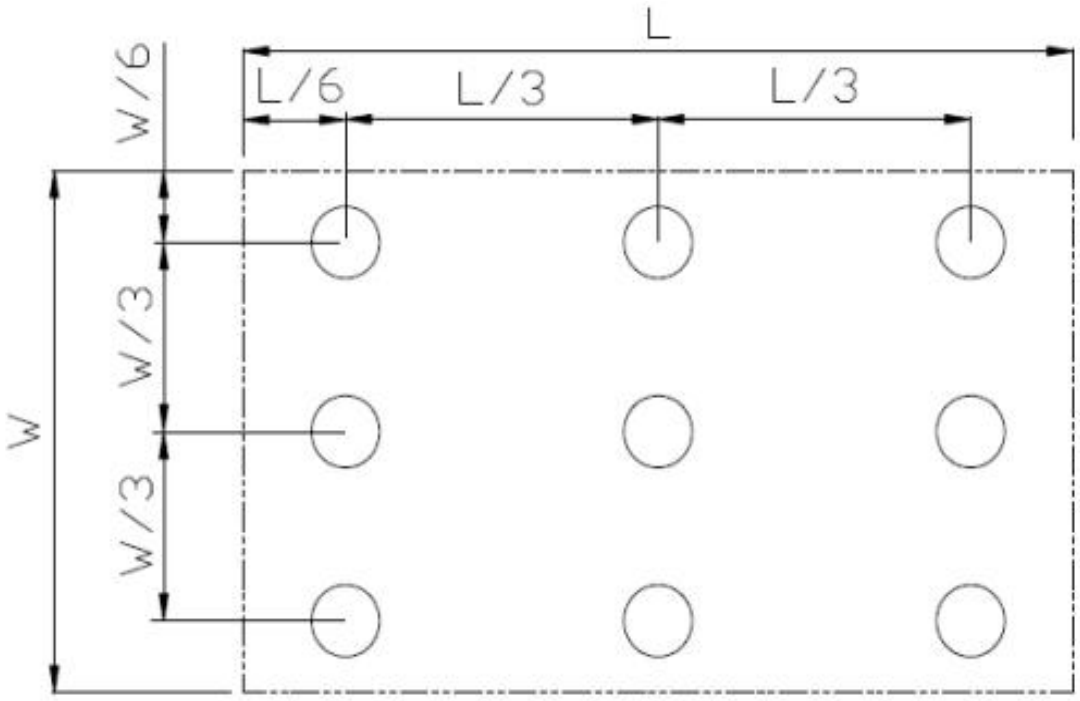


Fig. 2 Definition of uniformity
Lmax: The measured maximum luminance of all measurement position.
Lmin: The measured minimum luminance of all measurement position.

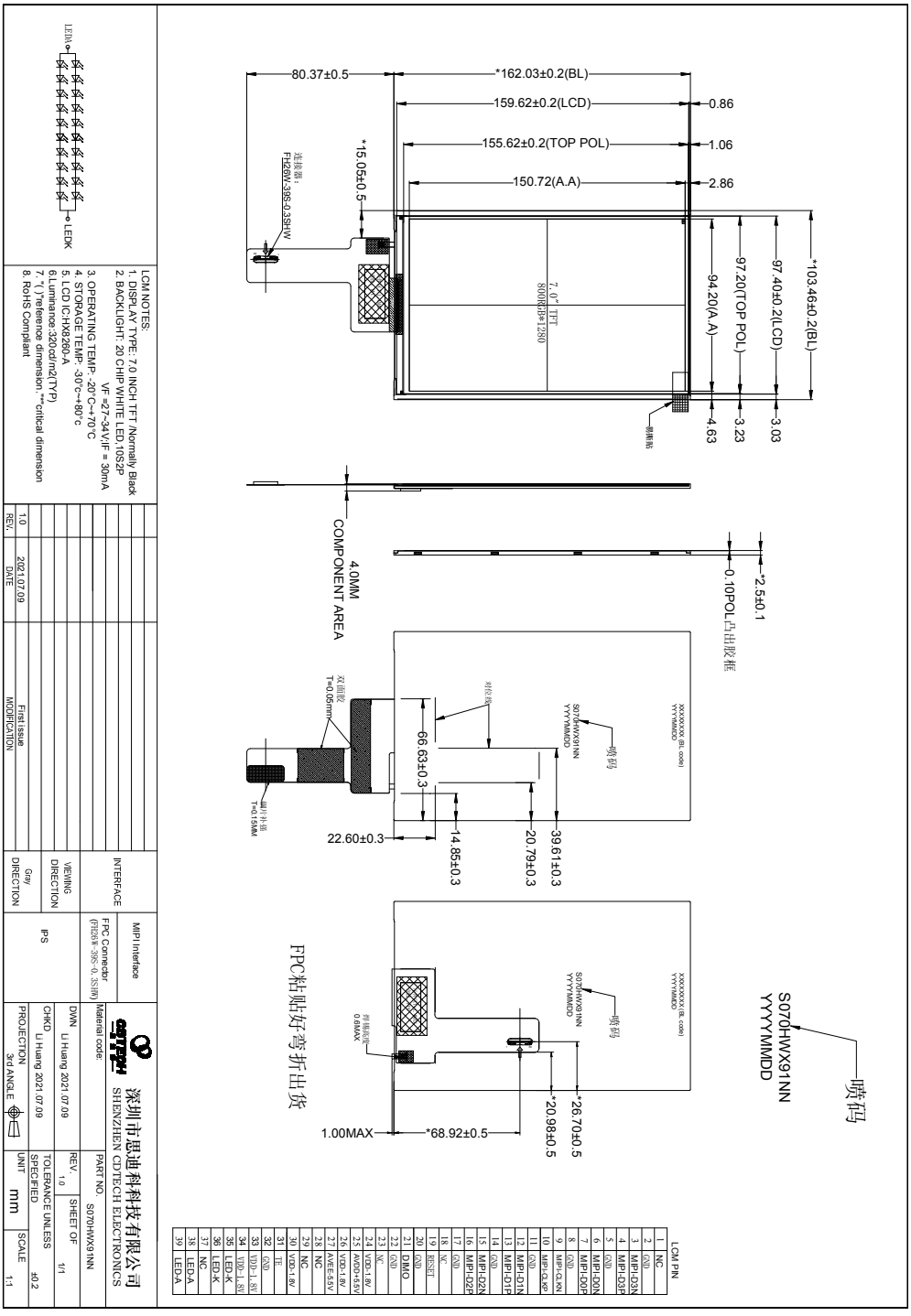
Note 7: Definition of Luminance :
Measure the luminance of white state at center point.

7 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	IEC60068-2-1:2007 GB2423. 2-2008
2	Low Temperature Operation	Ta= -20℃, 96hrs	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta= +80℃,96hrs	IEC60068-2-1:2007 GB2423. 2-2008
4	Low Temperature Storage	Ta= -30℃, 96hrs	IEC60068-2-1:2007 GB2423.1-2008
5	High Temperature & Humidity Operation	Ta= +60℃, 90% RH max,96 hours	IIEC60068-2-78:2001 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 20 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14:1984, GB2423.22-2002
7	ESD	C=150pF, R=330 Ω, 5 points/panel , Air:±8KV, 5 times Contact: ±4KV, 5 times (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2:2001 GB/T17626.2-2006
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.5mm , Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (6 hours for total)	IEC60068-2-6:1982 GB/T2423.10-1995
9	Mechanical Shock (Non-operation)	Half Sine Wave 60G ,6ms,±X,±Y,±Z 3times for each direction	IEC60068-2-27:1987 GB/T2423.5—1995
10	Package Drop Test	Height: 60 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32:1990 GB/T2423.8-1995

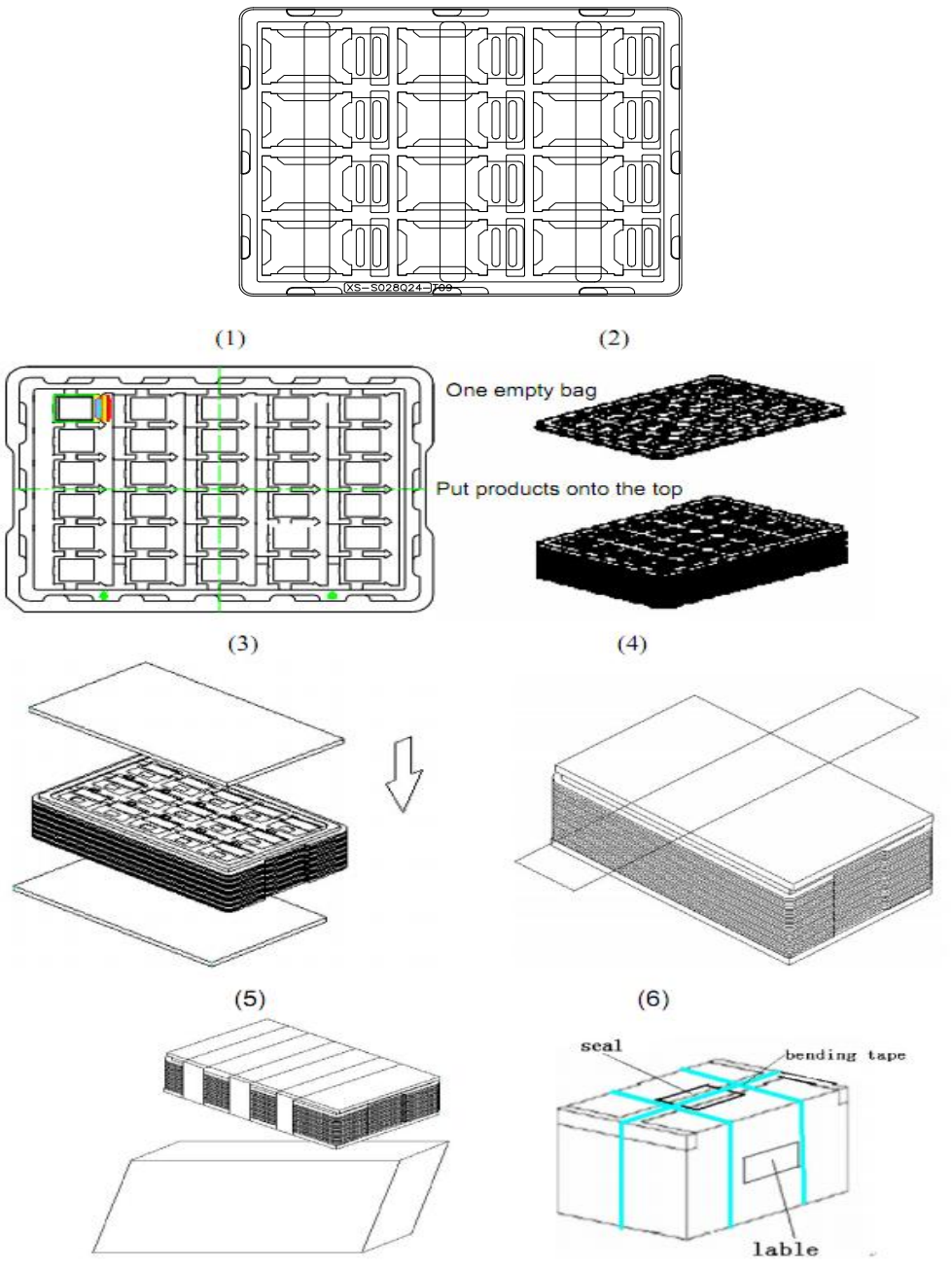
Notes:
1. The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:
1).Air bubble in the LCD;
2).Seal leak
3).Non-display
4).missing segments
5).Glass crack
6).CR reduction >40%
7).IDD increase >100%
8).Brightness reduction >50%
9).Color coordinate tolerance >0.05
2.≤7.0 inch：The size of sample is 5pcs；
　＞7.0 inch：The size of sample is 2pcs；
3. One test sample must complete each test item;
4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5.In the test of High Temperature Operation and High Temperature & Humidity Operation ,the operation temperature is the surface temperature of module.

8 Mechanical Drawing



9 Packing

Packing Method



1. Put module into tray cavity:
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above:
4. Fix the cardboard to the tray stack with adhesive tape:
5. Put the tray stack into carton.
6. Carton sealing with adhesive tap

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.