

Product Specification

Model Name	S040HWV09NN
Description	Standard LCD Module 4.0" WVGA 480(RGB)x480 Dots
Date	2019/9/12
Version	1.0

Approved by/Date	Check by/Date	Prepared by/Date
ZHP 2019/9/12	HZX 2019/9/12	Yigui.Han 2019/9/12

Customer Approval	
Date	

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1. Record of Revision

Rev	Issued Date	Description	Editor
1.0	2019/9/12	First Release.	Yigui.Han

2. General Specifications

	Feature	Spec
Characteristics	Size	4.0 inch
	Resolution	480(horizontal)*480(Vertical)
	Interface	MIPI 2Lane
	Connect type	Connector
	Display Colors	16.7M
	Technology type	a-Si
	Pixel pitch (mm)	0.149*0.146
	Pixel Configuration	R.G.B-Stripe
	Display Mode	Normally Black
	LCD Driver IC	ST7701S-G5
	Viewing Direction	Full view
Mechanical	LCM (W x H x D) (mm)	77.66*78.97*2.3
	Active Area(mm)	71.86 x70.18
	With /Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	10 LEDs

Note 1: Requirements on Environmental Protection: RoHs

Note 2: LCM weight tolerance: +/- 5%

3. Input/Output Terminals

No.	Symbol	Description
1	VLED+	Backlight LED Anode.
2~3	VLED-	Backlight LED Cathode
4	VCI	Power supply 3.3V
5	IOVCC	Power supply 1.8V
6	RESET	Reset signal pin
7	TE	Tearing effect signal is used to synchronize MCU to frame memory
8	LED-PWM	The PWM frequency output for LCD driver control.
9	GND	Ground
10	MIPI_D0P	MIPI Negative data signal(+)
11	MIPI_D0N	MIPI Positive data signal(-)
12	GND	Ground
13	MIPI_D1P	MIPI Negative data signal(+)
14	MIPI_D1N	MIPI Positive data signal(-)
15	GND	Ground
16	MIPI_CKP	MIPI Negative clock signal(+)
17	MIPI_CKN	MIPI Positive clock signal(-)
18	GND	Ground
19~20	NC	No connect
21	GND	Ground
22~23	NC	No connect
24	GND	Ground
25	CTP (INT)NC	Interrupt request to the host (NC)
26	CTP (SDA)NC	I2C data input and output (NC)
27	CTP (SCL)NC	I2C clock input (NC)
28	CTP (RST)NC	Reset Pin for CTP (NC)
29	CTP (VCI)NC	Power supply for CTP (NC)
30	CTP (GND)NC	Ground CTP (NC)

4. Absolute Maximum Rating

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	VDD	-0.5	-	5	V	-
Operating Temperature	TOPR	-20	-	70	°C	-
Storage Temperature	TSTG	-30	-	80	°C	

5. Electrical Characteristics

5.1 Driving TFT LCD Panel

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		VDD	3.0	3.3	3.6	V	
Input Signal Voltage	Low Leve	V _{IL}	GND	-	0.3x VDD	V	
	High Level	V _{IH}	0.7x VDD	-	VDD	V	
Output Signal Voltage	Low Leve	V _{IL}	GND	-	VDD+0.4	V	
	High Level	V _{IH}	VDD-0.4	-	VDD	V	
(Panel+LSI) Power Consumption		Black Mode (60Hz)	-	74		nW	
		Standby	-	50	-	uW	

Item	Symbol	Min.	Typ.	Max.	Unit	Note
TFT Gate ON Voltage	V _{GH}	--	(15)	--	V	*1,*2
TFT Gate OFF Voltage	V _{GL}	--	(-10)	--	V	
TFT Common Voltage	V _{com}	--	(0)	--	V	
Data (RGB signal) Voltage	V _{sig}	(-5)	--	(5)	V	

Note:

*1. V_{GH} is TFT Gate operating Voltage.

*2. V_{GL} is TFT Gate operating Voltage.

The storage structure of this model is C_{ST}(Storage on Common)

*3. V_{com} must be adjusted to optimize display quality _Cross talk, Contrast Ratio and etc.

5.2 LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I _F	-	40	-	mA	
Forward Voltage	V _F	14.4	15	15.6	V	
Backlight Power consumption	W _{BL}	-	0.6	-	W	
LED Lifetime		-	30000	-	Hrs	

Note 1: Each LED: $I_F = 20 \text{ mA}$, $V_F = 3.2 \pm 0.2 \text{ V}$.

Note 2: Optical performance should be evaluated at $T_a = 25^\circ\text{C}$ only.

Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

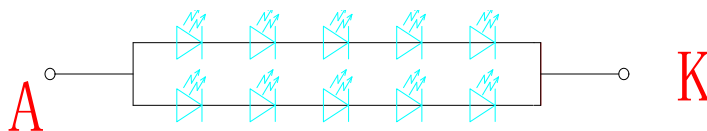
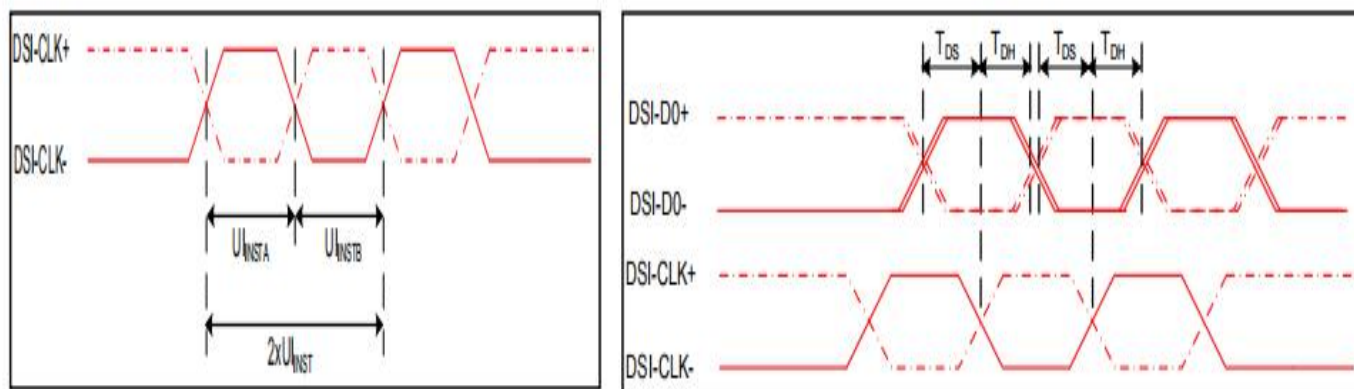


Figure: LED connection of backlight(Constant Current)

6. Interface Timing

6.1 MIPI Interface Characteristics:

High Speed Mode

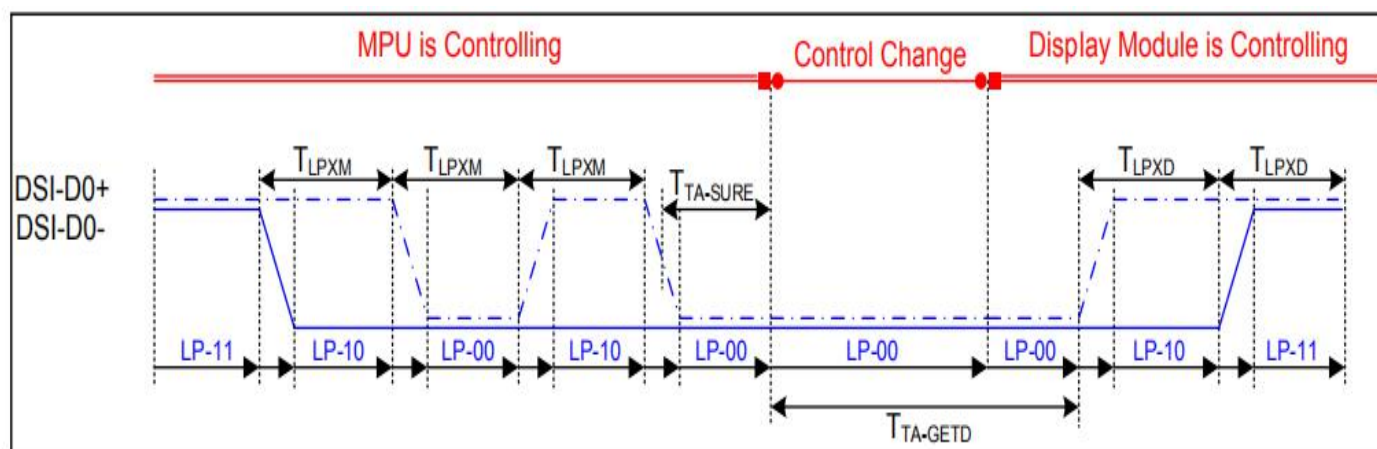


DSI clock channel timing

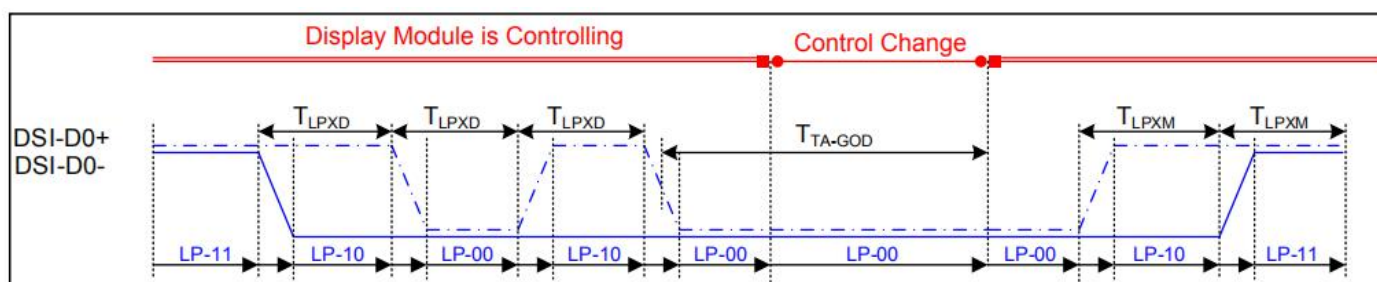
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halves	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	UI	

Mipi Interface- High Speed Mode Timing Characteristics

6.2 Low Power Mode



Turnaround (BTA) from display module to MPU Timing



Turnaround (BTA) from MPU to display module Timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5 \times T_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4 \times T_{LPXD}$		ns	Output

Mipi Interface Low Power Mode Timing Characteristics

The diagram illustrates the timing for DSI0+ and DSI0- signals across three operational modes:

- Low Power Mode, Disable RX Line Termination:** This mode is active during the LP-11, LP-01, and LP-00 phases. The DSI0+ signal is shown as a high-level signal, and the DSI0- signal is shown as a low-level signal. The signal levels are defined by the VIHLPRX(Min) and VIHLPRX(Max) thresholds.
- High Speed Mode, Enable Rx Line Termination:** This mode is active during the HS-PREPREPARE, HS-ZERO, and HS-SYNC phases. The DSI0+ signal transitions to a high-level signal, and the DSI0- signal transitions to a low-level signal. The signal levels are defined by the VIHLPRX(Min) and VIHLPRX(Max) thresholds. The HS-PREPREPARE phase is marked by the T_{HS-TERM-EN} and T_{HS-SETTLE} timing parameters. The HS-ZERO phase is marked by the T_{HS-ZERO} timing parameter. The HS-SYNC phase is marked by the T_{HS-SYNC} timing parameter. The HS-PREPREPARE phase is also marked by the T_{HS-TERM-EN} and T_{HS-SETTLE} timing parameters.
- Low Power Mode, Disable Rx Line Termination:** This mode is active during the LP-11 phase. The DSI0+ signal transitions to a high-level signal, and the DSI0- signal transitions to a low-level signal. The signal levels are defined by the VIHLPRX(Min) and VIHLPRX(Max) thresholds. The LP-11 phase is marked by the T_{HS-TRAIL} and T_{HS-EXIT} timing parameters. The LP-11 phase is also marked by the T_{HS-SKIP} and T_{EOT} timing parameters.

Key timing parameters shown include:

- T_{LPX}: Low Power Mode exit time.
- T_{HS-TERM-EN}: High Speed Mode termination enable time.
- T_{HS-SETTLE}: High Speed Mode settle time.
- T_{HS-ZERO}: High Speed Mode zero time.
- T_{HS-SYNC}: High Speed Mode sync time.
- T_{HS-SKIP}: High Speed Mode skip time.
- T_{EOT}: End of transmission time.
- T_{HS-TRAIL}: High Speed Mode trail time.
- T_{HS-EXIT}: High Speed Mode exit time.

The diagram also shows the DSI0+ and DSI0- signals, the VIHLPRX(Min) and VIHLPRX(Max) thresholds, and the "Capture 1st Data Bit" point. A "Disconnect Terminator" is indicated at the end of the HS-SYNC phase.

The diagram illustrates the timing relationships for the DSI HS-0/1, HS-0, LP-11, LP-01, LP-00, HS-0, and HS-0/1 states. The top section shows the DSI-CLK+ and DSI-CLK- signals, which are differential clock signals. The bottom section shows the DSI-D0+ and DSI-D0- signals, which are differential data signals. The diagram includes various timing parameters such as T_{EOT} , $T_{CLK-MISS}$, $T_{CLK-SETTLE}$, $T_{CLK-TERM-EN}$, $T_{CLK-POST}$, $T_{CLK-TRAIL}$, $T_{HS-EXIT}$, T_{LPX} , $T_{CLK-PREPARE}$, $T_{CLK-ZERO}$, $T_{CLK-PRE}$, T_{LPX} , $T_{HS-PREPARE}$, $T_{HS-SKIP}$, $VIHLPRX(\text{Min})$, and $VIHLPRX(\text{Max})$. The diagram also shows the transition from HS-0/1 to HS-0, LP-11, LP-01, LP-00, HS-0, and back to HS-0/1. A blue arrow labeled "Disconnect Terminator" points to the DSI-D0+/- signals during the HS-0 state.

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Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

6.4 Reset Timing

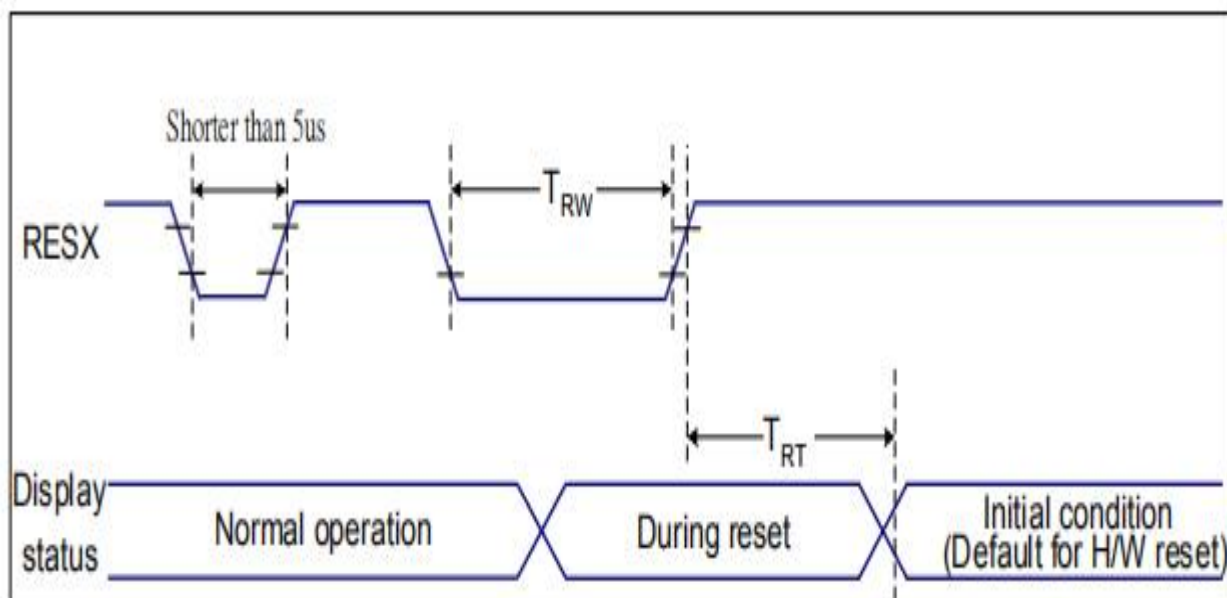


Figure 9 Reset Timing

$VDDI=1.8, VDD=2.8, AGND=DGND=0V, T_a=25\text{ }^{\circ}\text{C}$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

7. Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	-	-	25	35	ms	FIG.1	Note4
Contrast Ratio		CR		500	700	-	-	FIG.2	Note1
Surface luminance		LV	$\theta = 0^\circ$	-	350	-	cd/m2	FIG.2	Note2
Luminance uniformity		Yu	$\theta = 0^\circ$	70	80	-	%	FIG.2	Note3
NTSC		-	$\theta = 0^\circ$	-	50	-	%	FIG.2	Note5
Viewing angle		θ_T	Center CR ≥ 10	-	80	-	deg	FIG.3	Note6
		θ_B		-	80	-	deg	FIG.3	
		θ_L		-	80	-	deg	FIG.3	
		θ_R		-	80	-	deg	FIG.3	
Chromaticity	Red	R _X	$\theta = 0^\circ$ $\phi = 0^\circ$ Ta=25 $^\circ$	0.5784	0.6284	0.6784	-	FIG.2 CIE1931	Note5
		R _Y		0.3046	0.3546	0.4046	-		
	Green	G _X		0.2914	0.3414	0.3914	-		
		G _Y		0.5068	0.5568	0.6068	-		
	Blue	B _X		0.0952	0.1452	0.1952	-		
		B _Y		0.0297	0.0797	0.1298	-		
	White	W _X		0.2511	0.3011	0.3511	-		
		W _Y		0.2526	0.3026	0.3526	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON' s BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3,,Pn)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_r) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_f) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity, The x,y value is determined by screen active area center position P5. For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers' s ConoScope or DMS series Instruments or compatible.

FIG.1.The definition of response Time

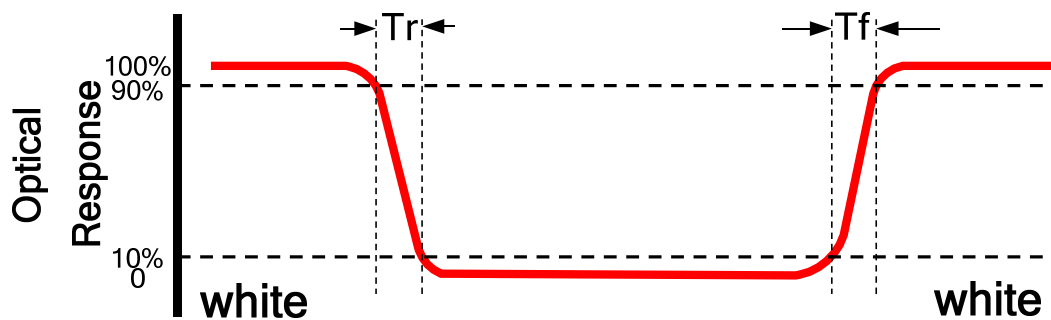


FIG.2. Measuring method for contrast ratio, surface luminance,

luminance uniformity, CIE (x,y) chromaticity

Size : $S \leq 5"$ (see Figure a) A : 5 mm B : 5 mm

H,V : Active area

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

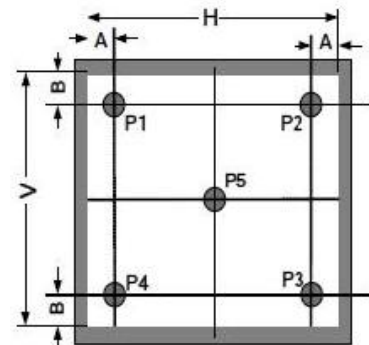


Figure a

Size : $5'' < S \leq 12.3''$ (see Figure b) H,V : Active area

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

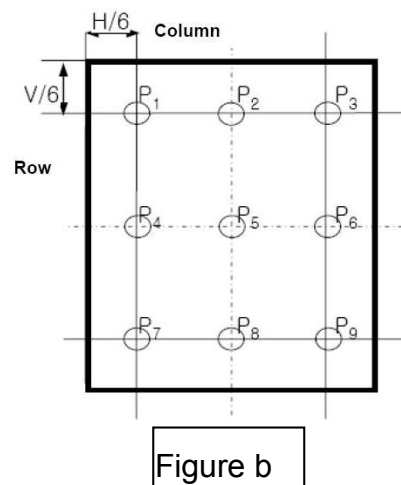
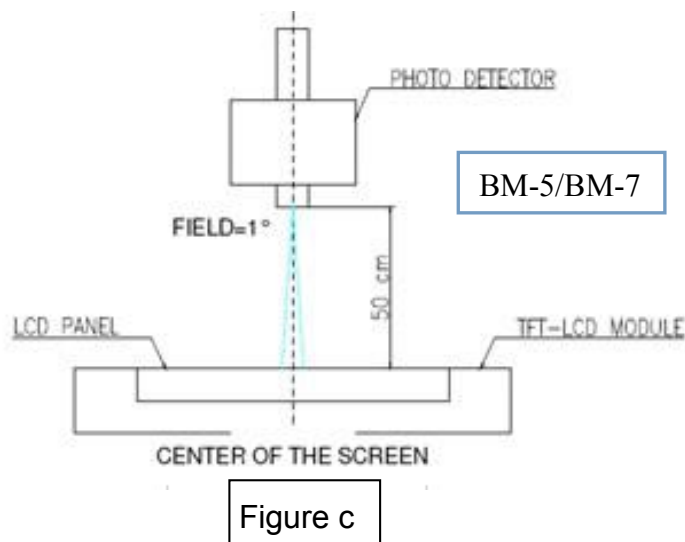
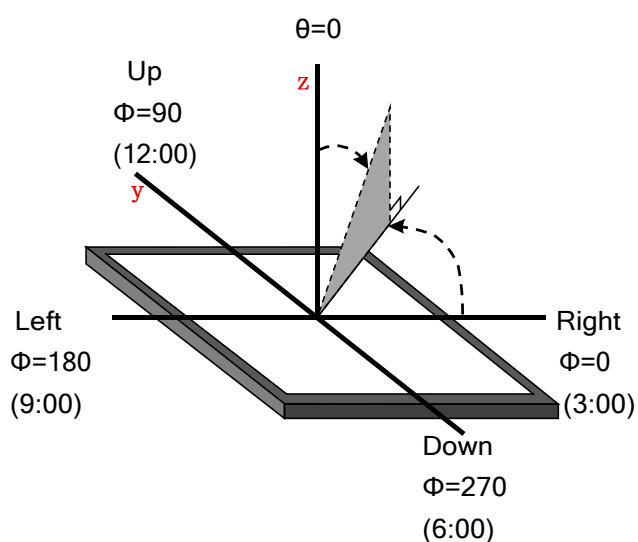


FIG.3.The definition of viewing angle



8. Environmental / Reliability Tests

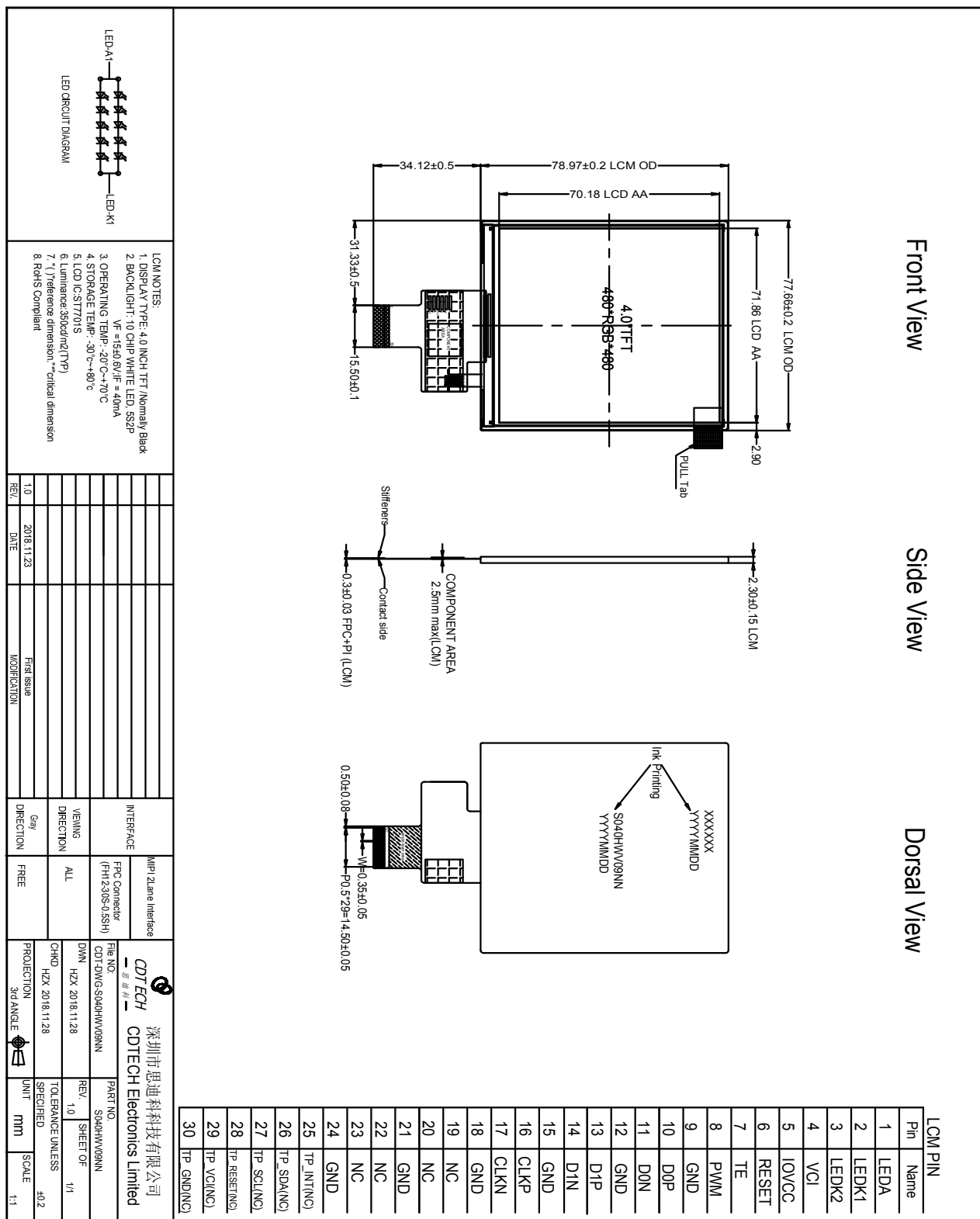
No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 120hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 120hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +70℃, 90% RH max,120 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-20℃ 30 min ~ +70℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Discharge (Operation) Static	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. Ts is the temperature of panel's surface.

2. Ta is the ambient temperature of sample.

3. The size of sample is 5pcs.

9. Mechanical Drawing



10. Packing

Packing Method

TBD

11. TFT-LCD Module Inspection Criteria

11.1 Scope

The incoming inspection standards shall be applied to TFT – LCD Modules (hereinafter Called "Modules") that supplied by CDTech Technology LTD.

11.2 Incoming Inspection

The customer shall inspect the modules within twenty calendar days of the delivery date (the “inspection period”) at its own cost. The result of the inspection (acceptance or rejection) shall be recorded in writing, and a copy of this writing will be promptly sent to The seller, If the results of the inspecting from buyer does not send to the seller within twenty Calendar days of the delivery date. The modules shall be regards as acceptance. Should the customer fail to notify the seller within the inspection period, the buyers Right to reject the modules shall be lapsed and the modules shall be deemed to have Been accepted by the buyer

11.3 Inspection Sampling

- 3.1. Lot size: Quantity per shipment lot per model
 - 3.2. Sampling type: Normal inspection, Single sampling
 - 3.3. Inspection level: II
 - 3.4. Sampling table: MIL-STD-105E
 - 3.5. Acceptable quality level (AQL)
- Major defect: AQL=0.65 Minor defect: AQL=1.00

11.4 Inspection Conditions

4.1 Ambient conditions:

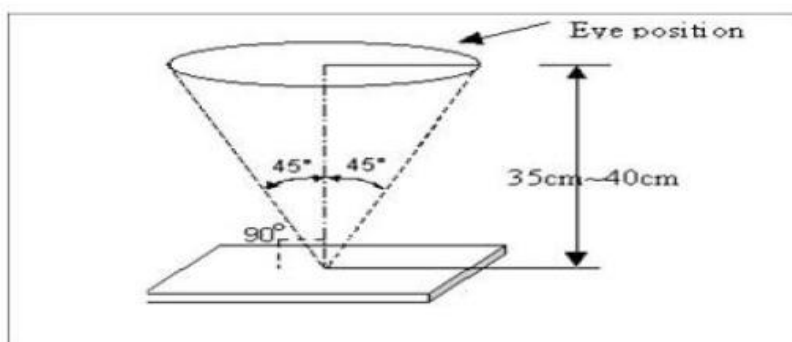
- a. Temperature: Room temperature $25 \pm 5^{\circ}\text{C}$
- b. Humidity: $(60 \pm 10) \% \text{RH}$
- c. Illumination: Single fluorescent lamp non-directive (300 to 700 Lux)

4.2 Viewing distance

The distance between the LCD and the inspector's eyes shall be at least $35 \pm 5 \text{ cm}$.

4.3 Viewing Angle

U/D: $45^{\circ} / 45^{\circ}$, L/R: $45^{\circ} / 45^{\circ}$



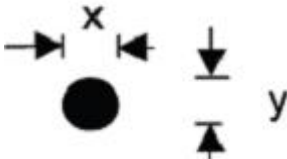
11.5 Inspection Criteria

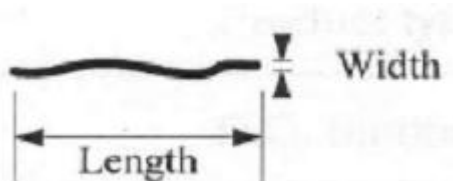
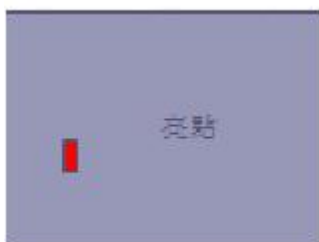
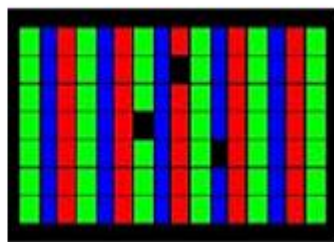
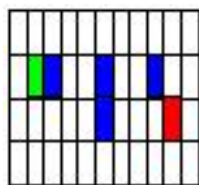
Defects are classified as major defects and minor defects according to the degree of Defectiveness defined herein.

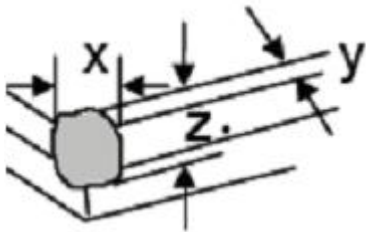
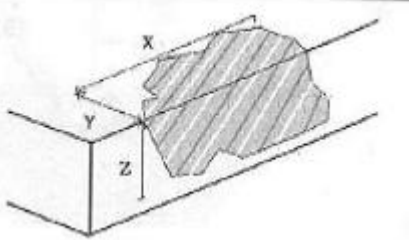
11.5.1 Major defect

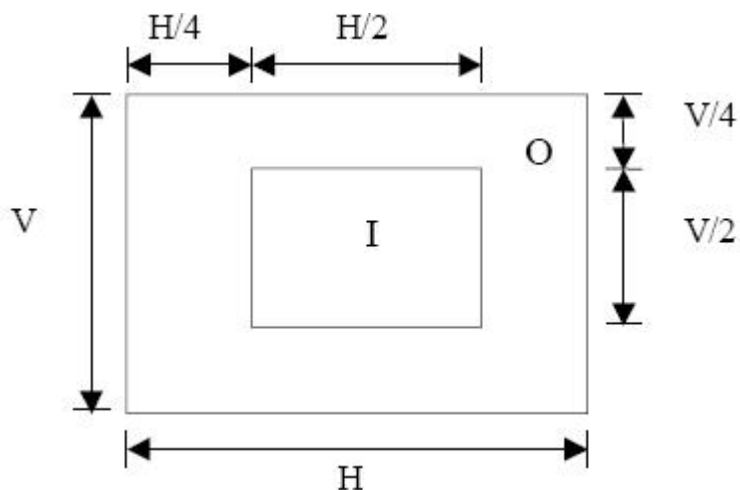
Item No	Items to be inspected	Inspection Standard
5.1.1	All functional defects	1) No display 2) Display abnormally 3) Short circuit 4) line defect
5.1.2	Missing	Missing function component
5.1.3	Crack	Glass Crack

11.5.2 Minor defect

Item No	Items to be inspected	Inspection standard	
5.2.1	Spot Defect Including Black spot White spot Pinhole Foreign particle Polarizer dirt	For dark/white spot is defined $\phi = (x+y) / 2$ 	
		Size ϕ (mm)	Acceptable Quantity
		$\phi \leq 0.2$	Ignore
		$0.2 < \phi \leq 0.5$	3
		$0.5 < \phi$	Not allowed

5.2.2	Line Defect Including Black line White line Scratch	Define: 				
		Width(mm) Length(mm)		Acceptable Quantity		
		W≤0.05		Ignore		
		0.05 < W≤0.1 L≤2.5		3		
		0.1 < W, or L>2.5		Not allowed		
5.2.3	Polarizer Dent/Bubble	Sizeφ(mm)		Acceptable Quantity		
		φ ≤0.2		Ignore		
		0.2 < φ ≤0.3		2		
		0.3 < φ ≤0.5		1		
		0.5 < φ		Not allowed		
		Total QTY		3		
5.2.4	Electrical Dot Defect	Bright and Black dot define:   and 				
		Two Adjacent Dot				
		Inspection pattern: Full white、Full black、Red、green and blue screens				
		Item		Acceptable Quantity		
				I	O	Note
		Black dot defect		2		φ ≤0.15 (5mm≤Distance)
		Bright dot defect		1		
		Total Dot		1		

5.2.5	Glass defect	 <p>1. Corner Fragment:</p>	
		Size(mm)	Acceptable Quantity
		$X \leq 3\text{mm}$ $Y \leq 1\text{mm}$ $Z \leq T$	Ignore T: Glass thickness X: Length Y: Width Z: thickness
		<p>2. Side Fragment:</p> 	
		Size(mm)	Acceptable Quantity
		$X \leq 5.0\text{mm}$ $Y \leq 1\text{mm}$ $Z \leq T$	T: Glass thickness X: Length Y: Width Z: thickness



I area & O area

- Note:
- 1). Dot defect is defined as the defective area of the dot area is larger than 50% of the dot area.
 - 2). The distance between two bright dot defects (red, green, blue, and white) should be larger than 15mm.
 - 3). The distance between black dot defects or black and bright dot defects should be more than 5mm apart.
 - 4). Polarizer bubble is defined as the bubble appears on active display area. The defect of polarizer bubble shall be ignored if the polarizer bubble appears on the outside of active display area.

11.6 Mechanics specification

As for the outside dimension, weight of the modules, please refer to product specification
For more details

12. Precautions for Use of LCD modules

12.1 Handling Precautions

12.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

12.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

12.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

12.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

12.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

12.1.6. Do not attempt to disassemble the LCD Module.

12.1.7. If the logic circuit power is off, do not apply the input signals.

12.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

12.1.8.1. Be sure to ground the body when handling the LCD Modules.

12.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

12.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

12.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

12.2 Storage Precautions

12.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

12.2.2. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0°C ~ 40°C Relatively humidity: ≤80%

12.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

12.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.