# CDTech(H.K.)Electronics Limited

## Product Specification

| | |
|---|---|
| **Model Name** | S035CHV67NS |
| **Description** | TFT LCD Module<br>3.5" HVGA<br>320(RGB)x480 Dots |
| **Date** | 2019/07/20 |
| **Version** | 1.0 |

| **Approved by/Date** | **Check by/Date** | **Prepared by/Date** |
|---|---|---|
| ZHP 2019/07/20 | HZX 2019/07/20 | Yigui.Han 2019/07/20 |

| **Customer Approval** | |
|---|---|
| | |
| **Date** | |

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## 1. Record of Revision

| Rev | Issued Date | Description | Editor |
|---|---|---|---|
| 1.0 | 2018/07/20 | First Release. | Yigui.Han |
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## 2. General Specifications

| Feature | | Spec |
|---|---|---|
| Characteristics | Size | 3.5 inch |
| | Resolution | 320(horizontal)*480(Vertical) |
| | Interface | RGB 18 bit |
| | Connect type | Connector |
| | Technology type | a-Si |
| | Pixel pitch (mm) | 0.051*0.153 |
| | Pixel Configuration | R.G.B.-Stripe |
| | Display Mode | Normally Black |
| | Driver IC | ILI9488 |
| | Viewing Direction | ALL |
| Mechanical | LCM (W x H x D) (mm) | 54.76*83.58*2.50 |
| | Active Area(mm) | 48.96*73.44 |
| | With /Without TSP | Without TSP |
| | Weight (g) | TBD |
| | LED Numbers | 6 LEDS |

Note 1: Requirements on Environmental Protection: RoHs
Note 2: LCM weight tolerance: +/- 5%

## 3. Input/Output Terminals

| No. | Symbol | Description |
|---|---|---|
| 1 | YU(NC) | No connection |
| 2 | XL(NC) | No connection |
| 3 | YD(NC) | No connection |
| 4 | XR(NC) | No connection |
| 5 | GND | System Ground |
| 6 | IOVCC | A supply voltage to the digital circuit(1.8V) |
| 7 | VCC | A supply voltage to the analog circuit2.8V) |
| 8 | /CS | Chip select input signal. |
| 9 | SDI | Serial data input/output.. |
| 10 | GND | System Ground |
| 11 | SCLK | SCL pin as Serial Clock. |
| 12 | GND | System Ground |
| 13-18 | B0-B5 | Data bus. |
| 19-24 | G0-G5 | Data bus. |
| 25-30 | R0-R5 | Data bus |
| 31 | GND | System Ground |
| 32 | PCLK | Dot clock signal input. |
| 33 | DE | Data enable input. |
| 34 | HSYNC | Horizontal sync input. Negative polarity. |
| 35 | VSYNX | Vertical sync input. Negative polarity. |
| 36 | RESET | Reset signal. |
| 37 | LEDA | Backlight LED Anode. |
| 38 | LEDA | Backlight LED Anode. |
| 39 | LEDK | Backlight LED Cathode. |
| 40 | LEDK | Backlight LED Cathode. |

## 4. Absolute Maximum Rating

| Item | Symbol | MIN | Typ | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.3 | - | 5.0 | V | - |
| Operating Temperature | $T_{OPR}$ | -20 | - | 70 | ℃ | - |
| Storage Temperature | $T_{STG}$ | -30 | - | 80 | ℃ | |

# 5. Electrical characteristics

## 5.1 Driving TFT LCD Panel

| Item | | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{cc}$ | 2.5 | 2.8 | 3.3 | V | |
| | | IOVCC | 1.65 | 1.8 | 3.3 | | |
| Input Signal Voltage | Low Leve | $V_{IL}$ | -0.3 | - | 0.3x IOVCC | V | |
| | High Level | $V_{IH}$ | 0.7x IOVCC | - | IOVCC | V | |
| Output Signal Voltage | Low Leve | $V_{OL}$ | 0 | - | 0.2*IOVCC | V | |
| | High Level | $V_{OH}$ | 0.8*IOVCC | - | IOVCC | V | |

## 5.2 LED Driving Conditions

| Item | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Forward Current | $I_F$ | - | 120 | - | mA | |
| Forward Voltage | $V_F$ | 2.8 | 3.2 | 3.6 | V | |
| Backlight Power consumption | $W_{BL}$ | - | 0.36 | - | W | |
| LED Lifetime | | - | 30000 | - | Hrs | |

Note 1: Each LED: IF =20 mA, VF =3.2+/0.4V.
Note 2: Optical performance should be evaluated at Ta=25℃ only.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

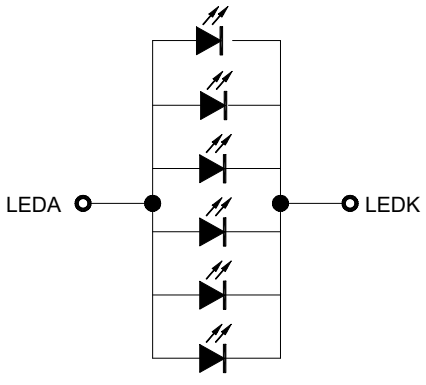



Figure: LED connection of backlight(Constant Current)

# 6 Interface Timing

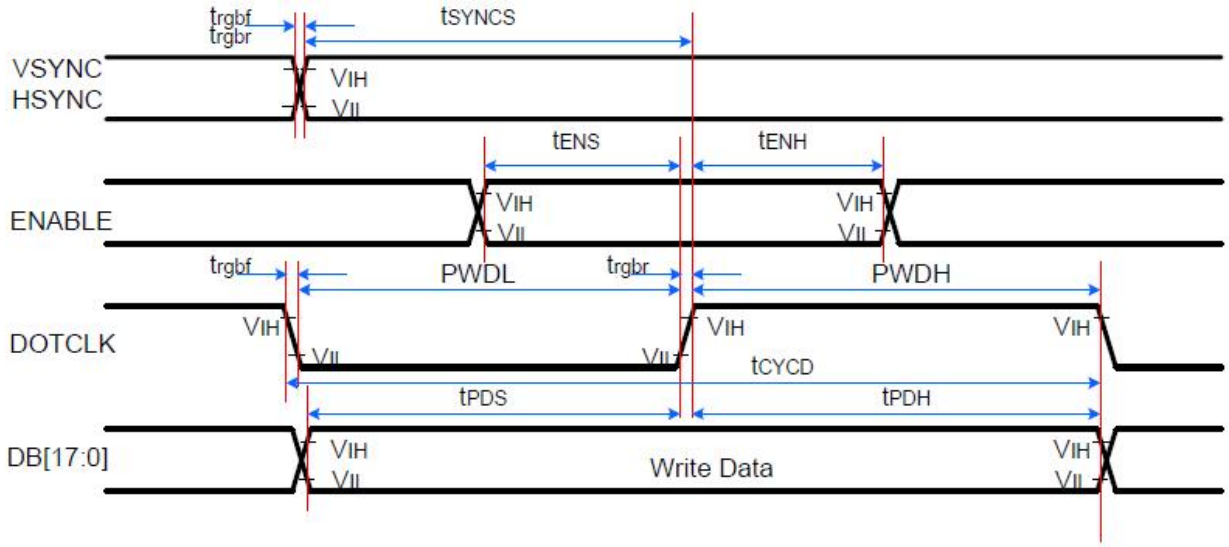
## 6.1 DC Characteristics for Panel Driving

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| **Power & Operation Voltage** | | | | | | | |
| Analog operating voltage | VCI | - | 2.5 | 2.8 | 3.3 | V | |
| Logic operating voltage | IOVCC | - | 1.65 | 1.8 | 3.3 | V | Note 1, 2 |
| OTP Supply voltage | DDVDH | - | - | 7 | - | V | Note 1 |
| Logic High level input voltage | VIH | - | 0.7*IOVCC | | IOVCC | V | Note 1 |
| Logic Low level input voltage | VIL | - | -0.3 | | 0.3*IOVCC | V | Note 1 |
| Logic High level output voltage TE, SDO (SDA) , CABC_PWM_OUT | VOH | IOH = -1.0mA | 0.8*IOVCC | | IOVCC | V | Note 1 |
| Logic Low level output voltage TE, SDO (SDA) , CABC_PWM_OUT | VOL | IOL = +1.0mA | 0 | | 0.2*IOVCC | V | Note 1 |
| Gate Driver High Voltage | VGH | - | 10.0 | - | 20 | V | |
| Gate Driver Low Voltage | VGL | - | -15.0 | - | -6.0 | V | |
| Driver Supply Voltage | - | \|VGH-VGL\| | 16 | - | 32 | V | |
| **Input and Output** | | | | | | | |
| Logic High Level Input Voltage | VIH | - | 0.7*IOVCC | - | IOVCC | V | |
| Logic Low Level Input Voltage | VIL | - | DGND | - | 0.3*IOVCC | V | |
| **VCOM Operation** | | | | | | | |
| DC VCOM Amplitude Voltage | VCOM | - | -2.0 | - | -0.06 | V | Note 3 |
| **Source Driver** | | | | | | | |
| Source Output Range | VSOUT | - | 0.1 | - | VREG1OUT-0.1 | V | Note 4 |
| Positive Gamma Reference Voltage | VREG1OUT | - | 3.625 | - | 5.5 | V | |
| Negative Gamma Reference Voltage | VREG2OUT | - | -5.5 | - | -3.625 | V | |
| Source Output Setting Time | Tr | Below with 99% precision | - | 10 | - | uS | Note 3. 4 |
| Output Deviation Voltage (Source Output channel) | Vdev | Sout>=4.2V Sout<=0.8V | - | - | 20 | mV | Note 3 |
| | | 4.2V>Sout>0.8V | - | - | 15 | mV | - |
| Output Offset Voltage | VOFFSET | - | - | - | 35 | mV | Note 3 |
| **Booster Operation** | | | | | | | |
| Booster (VCIx2) Voltage | DDVDH | - | | | 6 | V | |
| Booster (VCIx2) Voltage | DDVDL | - | -6 | | | V | |
| Booster (VCIx2 Drop Voltage) | VCI1x2 drop | loading=1mA | - | - | 5 | % | |
| Gate Driver High Voltage | VGH | - | 10.0 | - | 20 | V | |
| Gate Driver Low Voltage | VGL | - | -15.0 | - | -6.0 | V | |
| **Standby mode current consumption (Ta = 25℃, Interface: DBI and DPI)** | | | | | | | |
| Sleep in mode | VCI | VCI=2.8V IOVCC=1.8V | - | 100 | - | uA | |
| Deep Standby mode | VCI | | - | 1 | - | uA | |

**Notes:**

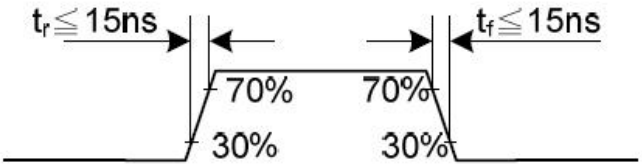
1. Ta = -30 to 70 ℃ (no damage up to 85℃ (at maximum)), IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, DGND=0V.
2. Supply the digital IOVCC voltage equal to or less than the analog VCI voltage.
3. Source channel loading = 10KΩ,30pF/channel
4. The maximum value is between 10KΩ,30pF/channel and Gamma setting value.

## 6.2 DPI Parallel Interface (RGB Interface) Characteristics




| Signal | Symbol | Parameter | min | max | Unit | Description |
|---|---|---|---|---|---|---|
| VSYNC/ HSYNC | $t_{SYNCS}$ | VSYNC/HSYNC setup time | 15 | - | ns | |
| | $t_{SYNCH}$ | VSYNC/HSYNC hold time | 15 | - | ns | |
| ENABLE | $t_{ENS}$ | ENABLE setup time | 15 | - | ns | |
| | $t_{ENH}$ | ENABLE hold time | 15 | - | ns | |
| DB [23:0] | $t_{POS}$ | Data setup time | 15 | - | ns | 16-/18-/24-bit bus RGB interface mode |
| | $t_{PDH}$ | Data hold time | 15 | - | ns | |
| DOTCLK | PWDH | DOTCLK high-level period | 20 | - | ns | |
| | PWDL | DOTCLK low-level period | 20 | - | ns | |
| | $t_{CYCD}$ | DOTCLK cycle time | 50 | - | ns | |
| | $t_{rgbr}$ , $t_{rgbf}$ | DOTCLK,HSYNC,VSYNC rise/fall time | - | 15 | ns | |

**Note:** Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V



## 6.3 DPI Parallel Interface (RGB Interface) Timing

The DPI can display moving pictures by two ways: rewrite into the GRAM and transmit directly to the shift register. The selection is set by the register BPGRAM (bypass GRAM) and RM bit. The RM bit selects an interface for the access operation of the Frame Memory. For the DPI, RM should be set as 1.

| BPGRAM | Display Data Path |
|---|---|
| 1 | Direct to shift register |
| 0 | Write into Memory |
| **RM** | **Interface for RAM access** |
| 0 | System interface |
| 1 | RGB interface |

The DM bit selects the clock operation mode. It allows switching between display operations in synchronization with the internal oscillation clock. If DM = 1, the external DOTCLK cannot be stopped unless it enters the Sleep-In mode.

| DM | RGB Interface Operating Clock Selection |
|---|---|
| 0 | Internal system clock |
| 1 | RGB interface (DOTCLK) |

### 4.5.1. RGB Interface Selection

The DPI can be selected by the RCM bit. When the RCM is set to 0, the DE mode is selected by VSYNC, HSYNC, DOTCLK, ENABLE, and DB [23:0] pins. When RCM is set to 1, the SYNC mode is selected by VSYNC, HSYNC, DOTCLK, and DB [23:0] pins. It supports several pixel formats that can be selected by DPI [2:0] bits in Pixel Format Set (R3Ah) command. The selection of a given interface is done by DPI [2:0], as shown in Table 6 and Figure 17.

**Table 6: DPI Interface Selection**

| RCM | DPI [2:0] | | | RGB Interface Mode | RGB Mode | Used Pins |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 24-bit RGB interface (16.7M colors) | **DE Mode** Valid data is determined by the ENABLE signal. | VSYNC, HSYNC, ENABLE, DOTCLK, DB [23:0] |
| 0 | 1 | 1 | 0 | 18-bit RGB interface (262K colors) | | VSYNC, HSYNC, ENABLE, DOTCLK, DB [17:0] |
| 0 | 1 | 0 | 1 | 16-bit RGB interface (65K colors) | | VSYNC, HSYNC, ENABLE, DOTCLK, DB [15:0] |
| 1 | 1 | 1 | 1 | 24-bit RGB interface (16.7M colors) | **SYNC Mode** In the SYNC mode, ENABLE signal is ignored; blanking porch is determined by B5h command. | VSYNC, HSYNC, DOTCLK, DB [23:0] |
| 1 | 1 | 1 | 0 | 18-bit RGB interface (262K colors) | | VSYNC, HSYNC, DOTCLK, DB [17:0] |
| 1 | 1 | 0 | 1 | 16-bit RGB interface (65K colors) | | VSYNC, HSYNC, DOTCLK, DB [15:0] |

24-bit DPI interface connection (DB [23:0] is used): set pixel format DPI [2:0] = 3'h7

| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] |

18-bit DPI interface connection (DB [17:0] is used): set pixel format DPI [2:0] = 3'h6

| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] |

16-bit DPI interface connection (DB [15:0] is used): set pixel format DPI [2:0] = 3'h5

| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | R[4] | R[3] | R[2] | R[1] | R[0] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[4] | B[3] | B[2] | B[1] | B[0] |

**Figure 17: DPI Interface 24/18/16 Pixel Format Selection**

The Pixel clock (DOTCLK) runs all the time without stop. It is used to enter VSYNC, HSYNC, ENABLE and DB [23:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as the internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to indicate when a new frame of the display is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to indicate when a new line of the frame is received. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Data Enable (ENABLE) is used to indicate when the RGB information that should be transferred in the display is received. This is a high enable, and its state is read to the display module by a rising edge of the DOTCLK signal.

DB [23:0] is used to indicate what is the information of the image that is transferred on the display (when ENABLE = 0 (low) and there is a rising edge of DOTCLK). DB [23:0] can be 0 (low) or 1 (high). These lines are read by a rising edge of the DOTCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs the corresponding source voltage according to the gray data from GRAM.

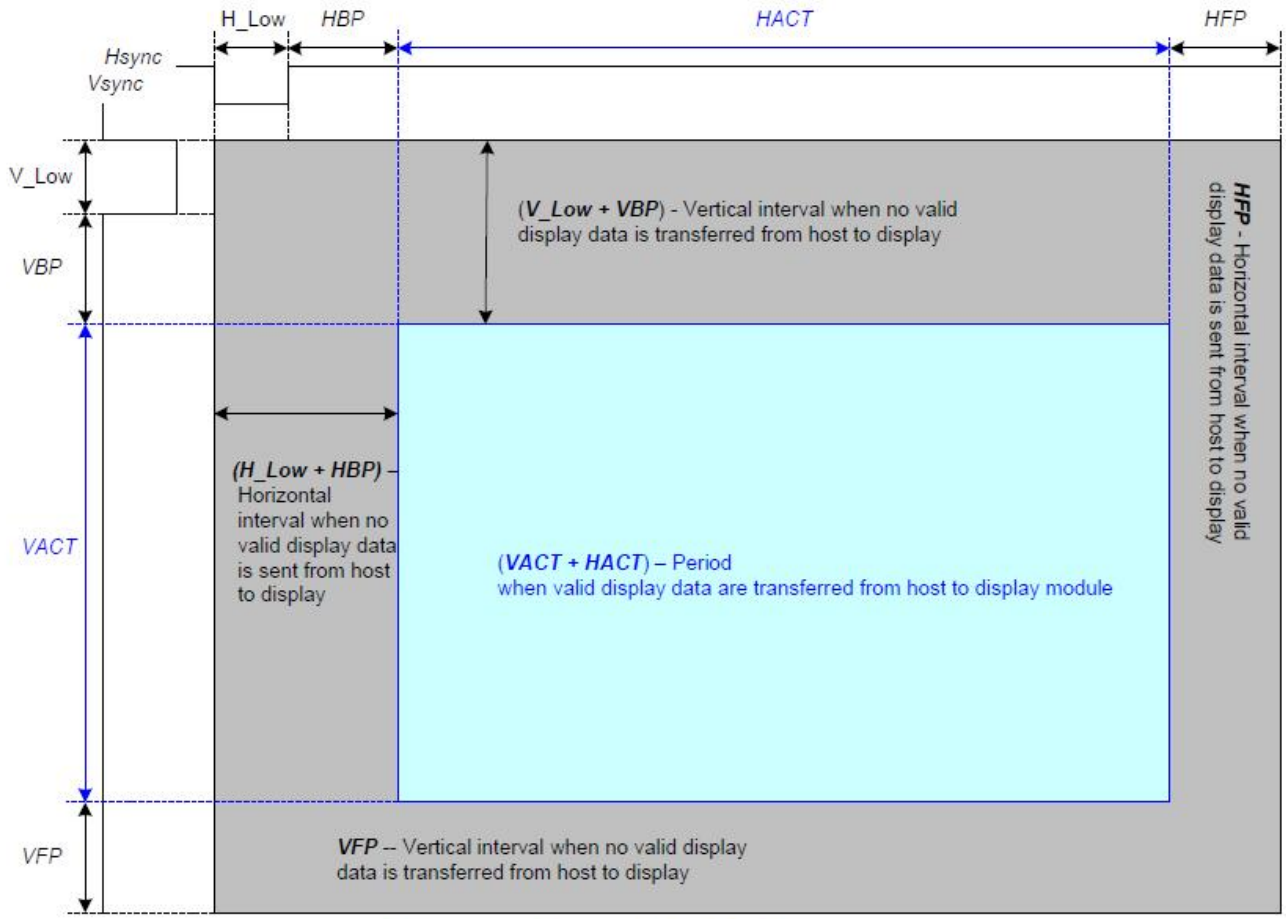



**Figure 18: General DPI Timing Diagram**

| Parameters | Symbols | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Horizontal Synchronization | H_Low | 3 | - | - | DOTCLK |
| Horizontal Back Porch | HBP | 3 | - | - | DOTCLK |
| Horizontal Address | HACT | - | 320 | - | DOTCLK |
| Horizontal Front Porch | HFP | 3 | - | - | DOTCLK |
| Horizontal Frequency | | - | - | 33 | KHz |
| Vertical Synchronization | V_Low | 1 | - | - | Line |
| Vertical Back Porch | VBP | 2 | - | - | Line |
| Vertical Address | VACT | - | 480 | - | Line |
| Vertical Front Porch | VFP | 2 | - | - | Line |
| Vertical Frequency | | 60 | - | 70 | Hz |
| DOTCLK cycle | | 100 | - | 50 | ns |
| DOTCLK Frequency | | 10 | - | 20 | MHz |

Example：DOTCLK = 20Mhz, TE=70Hz, V_Low+VBP=2, VFP=2, H_Low+HBP=100, HFP=170.

The timing chart of 16-/18-/24-bit DPI interface mode is illustrated in Figure 19.

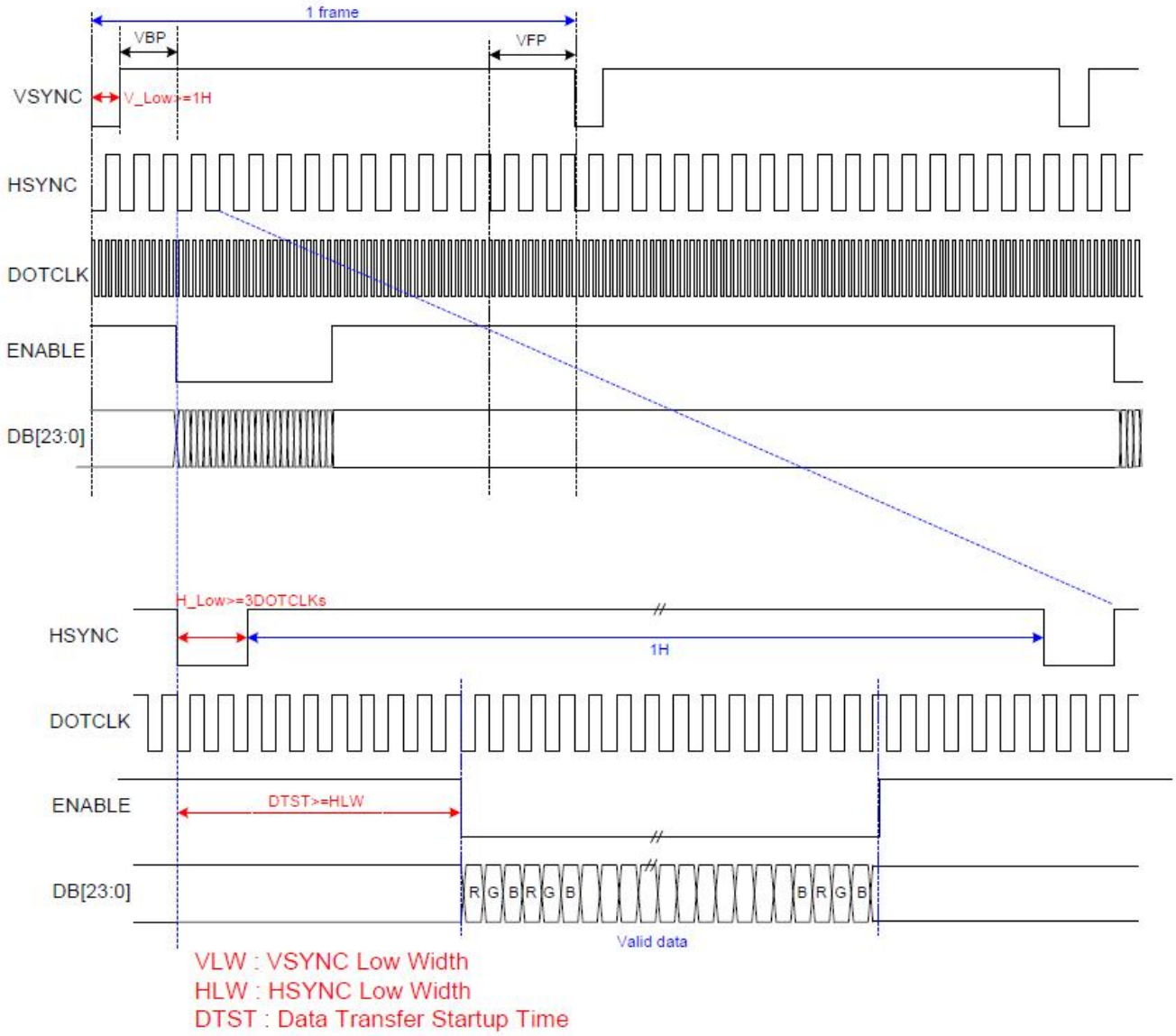



**Figure 19: DPI Interface Timing Diagram**

**Note:** VSPL = 0, HSPL = 0, DPL = 0 and EPL = 0 of Interface Mode Control B0h command.

## 7 Optical Characteristics

| Items | | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark | Note |
|---|---|---|---|---|---|---|---|---|---|
| Response time | | Tr+Tf | - | - | 30 | - | ms | FIG.1 | Note4 |
| Contrast Ratio | | CR | | - | 700 | - | - | FIG.2 | Note1 |
| Surface luminance | | LV | θ =0° | - | 260 | - | cd/m2 | FIG.2 | Note2 |
| Luminance uniformity | | Yu | θ =0° | 80 | - | - | % | FIG.2 | Note3 |
| NTSC | | - | θ =0° | - | 50 | - | % | FIG.2 | Note5 |
| Viewing angle | | θ Cr>10 | ∅=90° | - | 80 | - | deg | FIG.3 | Note6 |
| | | | ∅=270° | - | 80 | - | deg | FIG.3 | |
| | | | ∅=0° | - | 80 | - | deg | FIG.3 | |
| | | | ∅=180° | - | 80 | - | deg | FIG.3 | |
| Chromaticity | Red | $R_X$ | θ =0° ∅=0° Ta=25° | TBD | TBD | TBD | - | FIG.2 CIE1931 | Note5 |
| | | $R_Y$ | | TBD | TBD | TBD | - | | |
| | Green | $G_X$ | | TBD | TBD | TBD | - | | |
| | | $G_Y$ | | TBD | TBD | TBD | - | | |
| | Blue | $B_X$ | | TBD | TBD | TBD | - | | |
| | | $B_Y$ | | TBD | TBD | TBD | - | | |
| | White | $W_X$ | | TBD | TBD | TBD | - | | |
| | | $W_Y$ | | TBD | TBD | TBD | - | | |

**Note1. Definition of contrast ratio**

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON’s BM-5 or BM-7 photo detector or compatible.

**Note2. Definition of surface luminance.**

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ......,Pn)

**Note3. Definition of luminance uniformity**

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

**Note4. Definition of response time**

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (Tr) is the time between photo detector output intensity changed from 90% to 10%. And fall time (Tf) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

**Note5. Definition of color chromaticity (CIE1931)**

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

**Note6. Definition of viewing angle**

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers’s ConoScope or DMS series Instruments or compatible.

**FIG.1.The definition of response Time**

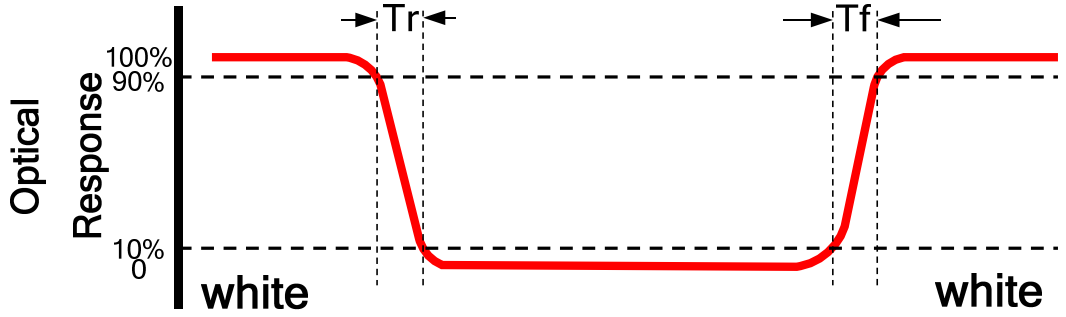



**FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity**

Size : S≤5"(see Figure a) A : 5 mm B : 5 mm
H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure a.
measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

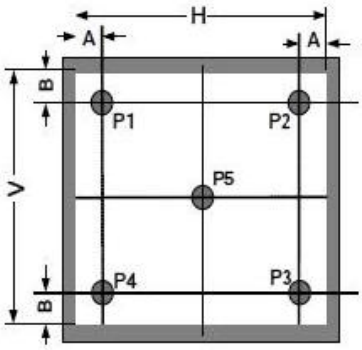



Figure a

Size : 5"＜S≤12.3"(see Figure b) H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure b.
measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

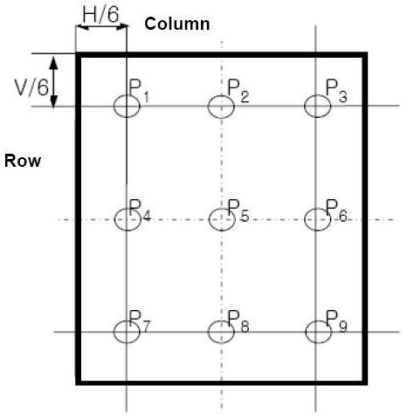



Figure b

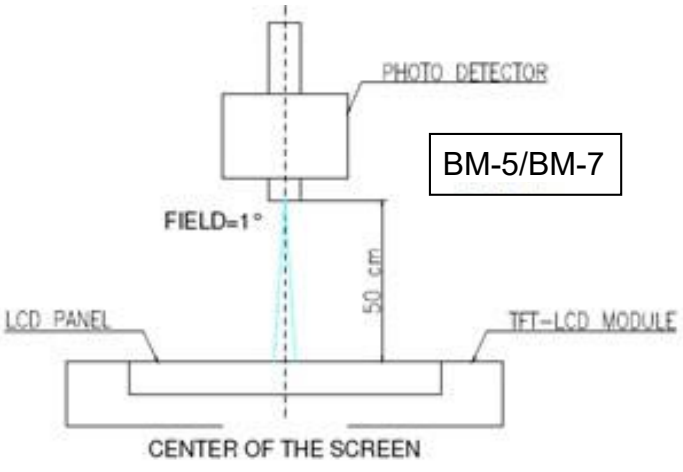
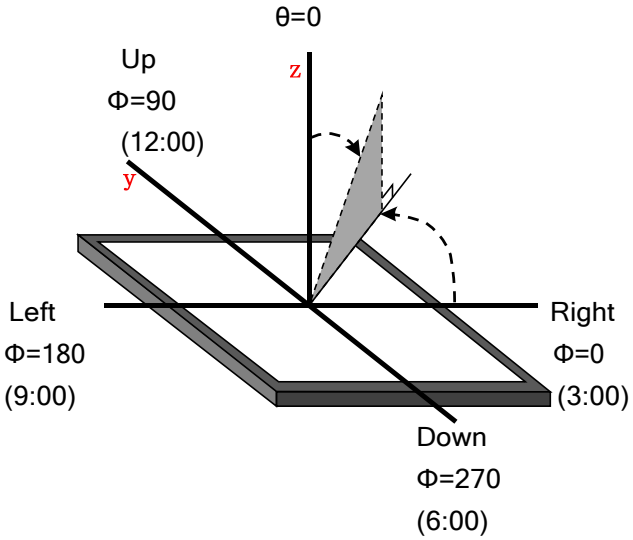



Figure c

**FIG.3.The definition of viewing angle**

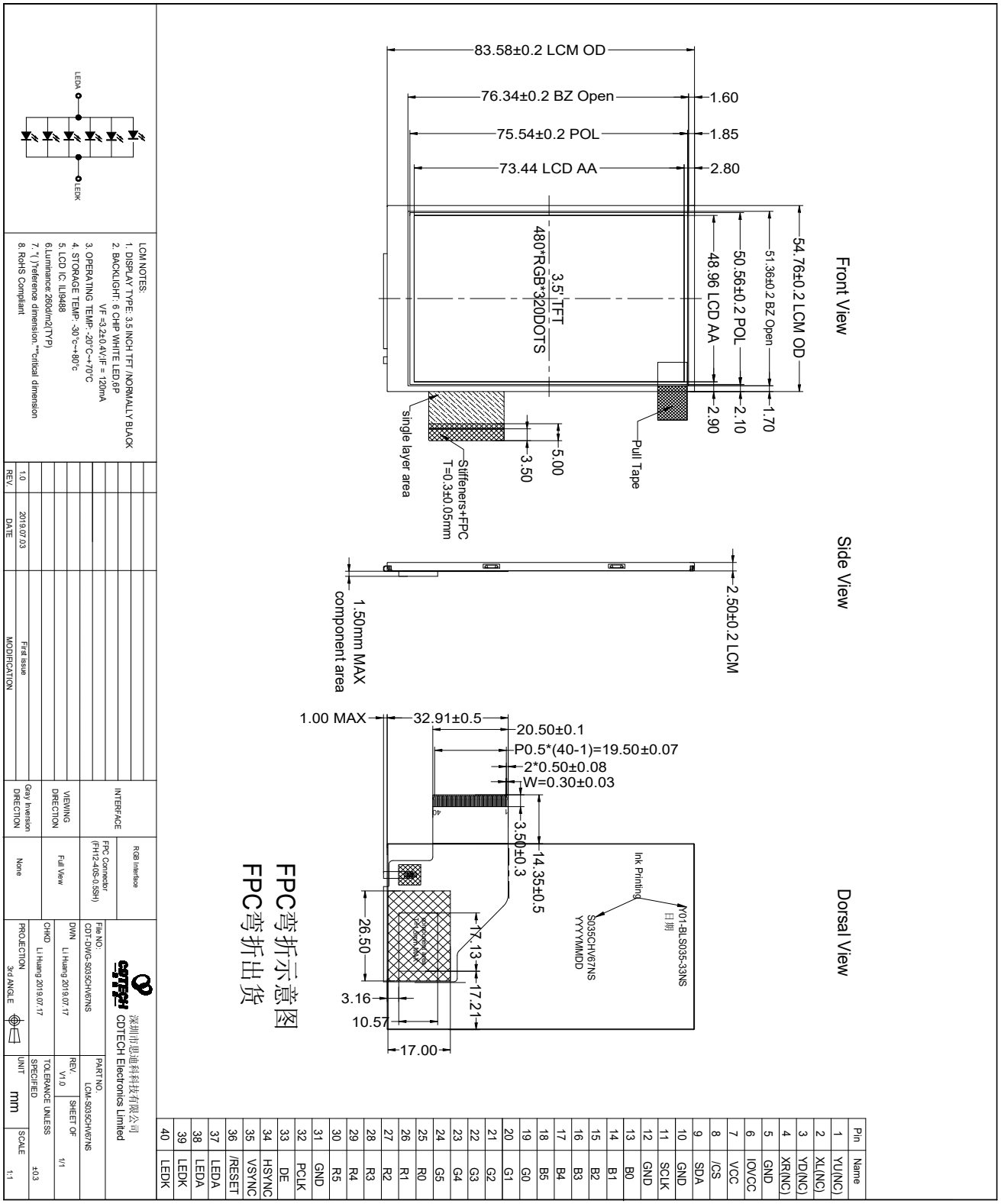


## 8 Environmental / Reliability Tests

| No | Test Item | Condition | Remarks |
|---|---|---|---|
| 1 | High Temperature Operation | Ts= +70℃, 96hrs | Note 1 IEC60068-2-2, GB2423. 2-89 |
| 2 | Low Temperature Operation | Ta= -20℃, 96hrs | Note 2 IEC60068-2-1 GB2423.1-89 |
| 3 | High Temperature Storage | Ta= +80℃, 120hrs | IEC60068-2-2 GB2423. 2-89 |
| 4 | Low Temperature Storage | Ta= -30℃, 120hrs | IEC60068-2-1 GB/T2423.1-89 |
| 5 | High Temperature & Humidity Storage | Ta= +60℃, 90% RH max,120 hours | IEC60068-2-3 GB/T2423.3-2006 |
| 6 | Thermal Shock (Non-operation) | -20℃ 30 min ~ +60℃ 30 min Change time: 5min, 30 Cycle | Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87 |
| 7 | Electro Static Discharge (Operation) | C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa) | IEC61000-4-2 GB/T17626.2-1998 |
| 8 | Vibration (Non-operation) | Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition) | IEC60068-2-6 GB/T2423.5-1995 |
| 9 | Shock (Non-operation) | 60G 6ms, ± X, ±Y , ± Z 3 times for each direction | IEC60068-2-27 GB/T2423.5-1995 |
| 10 | Package Drop Test | Height: 80 cm, 1 corner, 3 edges, 6 surfaces | IEC60068-2-32 GB/T2423.8-1995 |

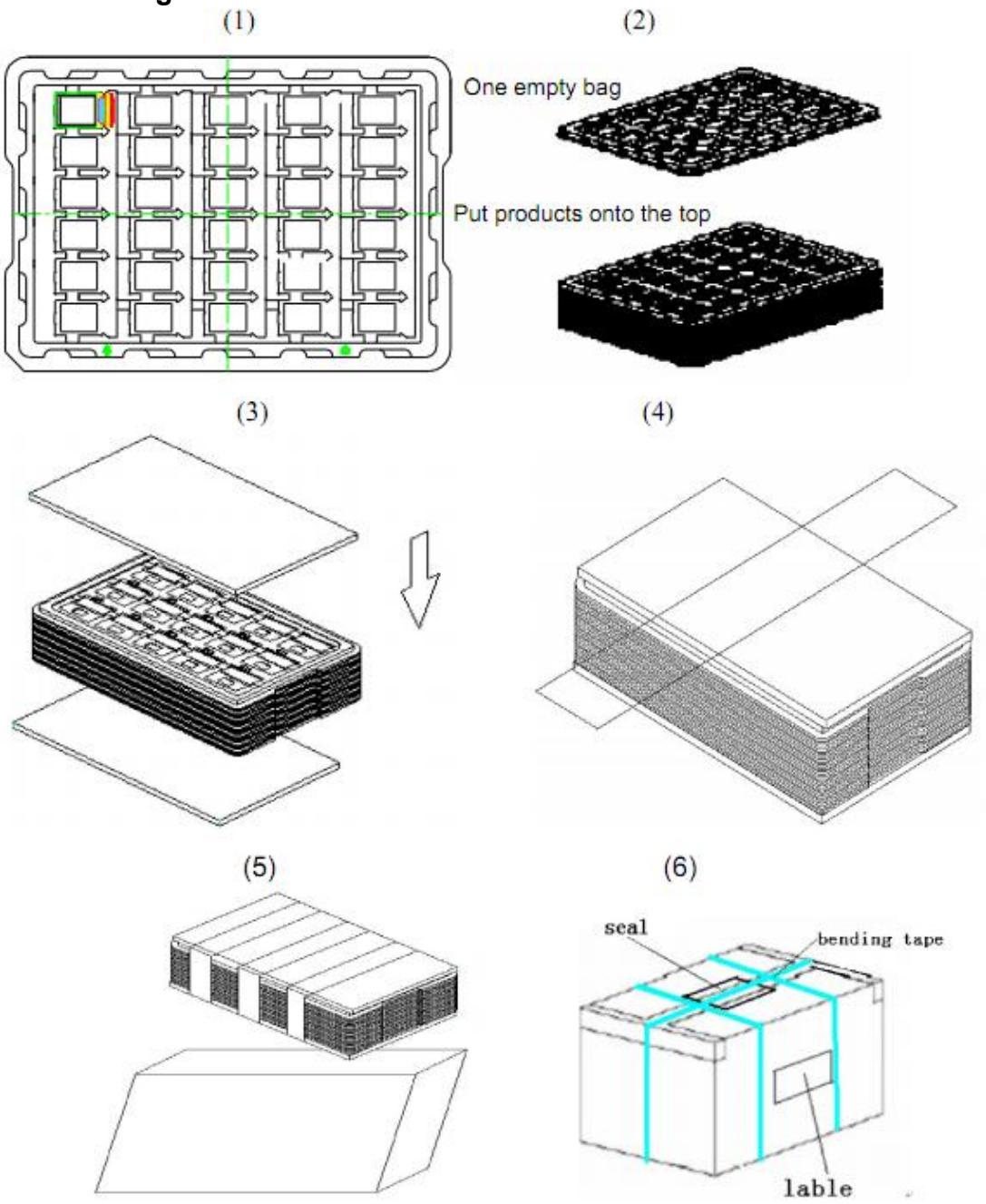
Note:1. Ts is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.
3. The size of sample is 5pcs.

# 9 Mechanical Drawing



# 10 Packing

**Packing Method**




1. Put module into tray cavity:
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above:
4. Fix the cardboard to the tray stack with adhesive tape:
5. Put the tray stack into carton.
6. Carton sealing with adhesive tape.

# 11.Precautions for Use of LCD modules

## 11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

## 11.2 Storage Precautions

11.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

## 11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.