PRODUCT SPECIFICATION

CDTECH Model: **S123HWU14EP**

CUSTOMER Model: -

Description: **12.3 ” TFT-LCD Module**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2025.3.18	2025.3.18	2025.3.18

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
1.0	2025-3-18	First Release	-

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1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	12.3	inch
Number of Pixels	720 (H) RGB x 1920 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Free	-
Interface	MIPI	-
Display Colors	16.7M	colors
Outline Dimension	121.66 (H) x 304.36 (V) x 5.64 (D)	mm
Active Area	109.51 (H) x 292.03 (V)	mm
Pixel Pitch	0.1521 (H) x 0.1521 (V)	mm
Driver IC	HX83102-E	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VCC	-0.3	5.0	V	Note 1
Digital supply voltage	IOVCC	-0.3	1.95	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

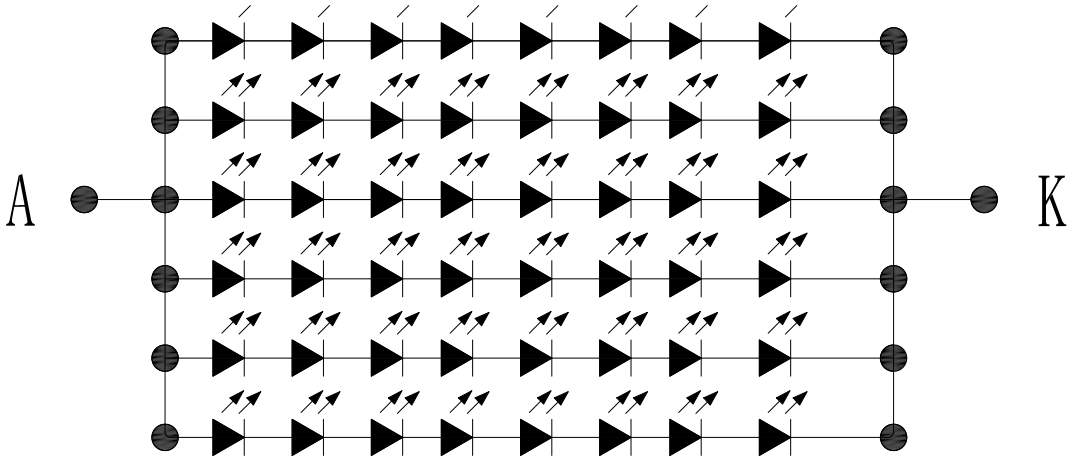
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VCC	3.0	3.3	3.6	V	
Analog supply current	I_{VCC}	55	85	115	mA	VCC=3.3V（PHOTO）
Logic supply voltage	IOVCC	1.65	1.8	3.3	V	
Logic supply current	I_{IOVCC}	15	30	35	mA	IOVCC=1.8V
Logic input voltage	VIH	0.7*IOVCC	-	IOVCC	V	
	VIL	GND	-	0.3*IOVCC	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	270	-	mA	
Driving Voltage	V_F	21.6	-	27.2	V	
Power consumption	W_{BL}	5.832	-	7.344	W	
LED Life-Time	N/A	-	50,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



4. Interface Pin Assignment

4.1 LCM Pin Assignment

No.	Symbol	Description
1	NC	No connection
2	VCC	Power supply
3	VCC	Power supply
4	NC	No connection
5	IOVCC	Power supply
6	IOVCC	Power supply
7	NC	No connection
8	BIST_EN	BiSTmode enable, high active.(It is weak pull-low inside IC).
9	RESET	Global reset pin
10	NC	No connection
11	GND	Ground
12	MIPI_TDN0	MIPI Negative data signal(-)
13	MIPI_TDP0	MIPI Positive data signal(+)
14	GND	Ground
15	MIPI_TDN1	MIPI Negative data signal(-)
16	MIPI_TDP1	MIPI Positive data signal(+)
17	GND	Ground
18	MIPI_TCN	MIPI Negative clock signal(-)
19	MIPI_TCP	MIPI Positive clock signal(+)
20	GND	Ground
21	MIPI_TDN2	MIPI Negative data signal(-)
22	MIPI_TDP2	MIPI Positive data signal(+)
23	GND	Ground
24	MIPI_TDN3	MIPI Negative data signal(-)
25	MIPI_TDP3	MIPI Positive data signal(+)
26	GND	Ground
27	NC	No connection
28	NTC-(NC)	No connection
29	NC	No connection
30	NTC+(NC)	No connection
31	NC	No connection
32	LED-	Power for LED backlight (Cathode)
33	LED-	Power for LED backlight (Cathode)
34	NC	No connection
35	NC	No connection
36	GND	Ground
37	GND	Ground
38	NC	No connection
39	LED+	Power for LED backlight (Anode)
40	LED+	Power for LED backlight (Anode)

5. Interface Characteristics

5.1 Power Sequence

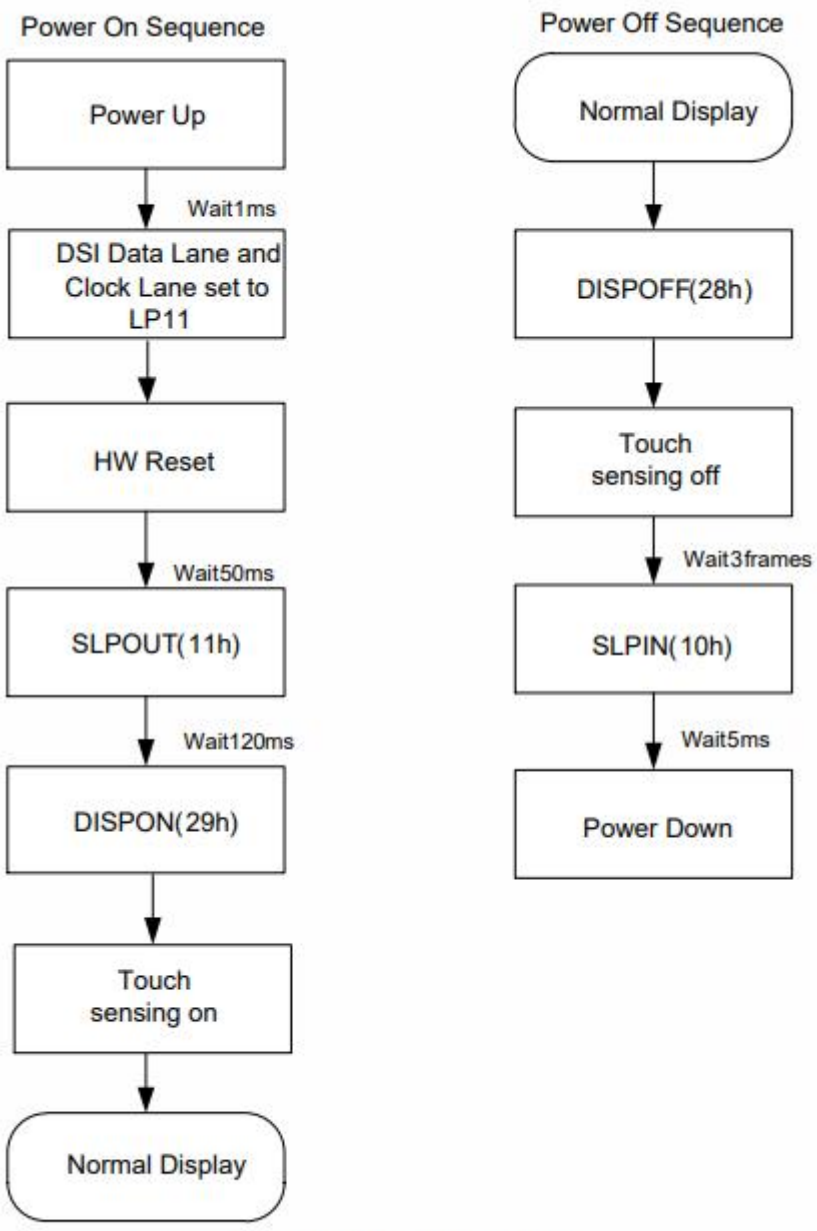
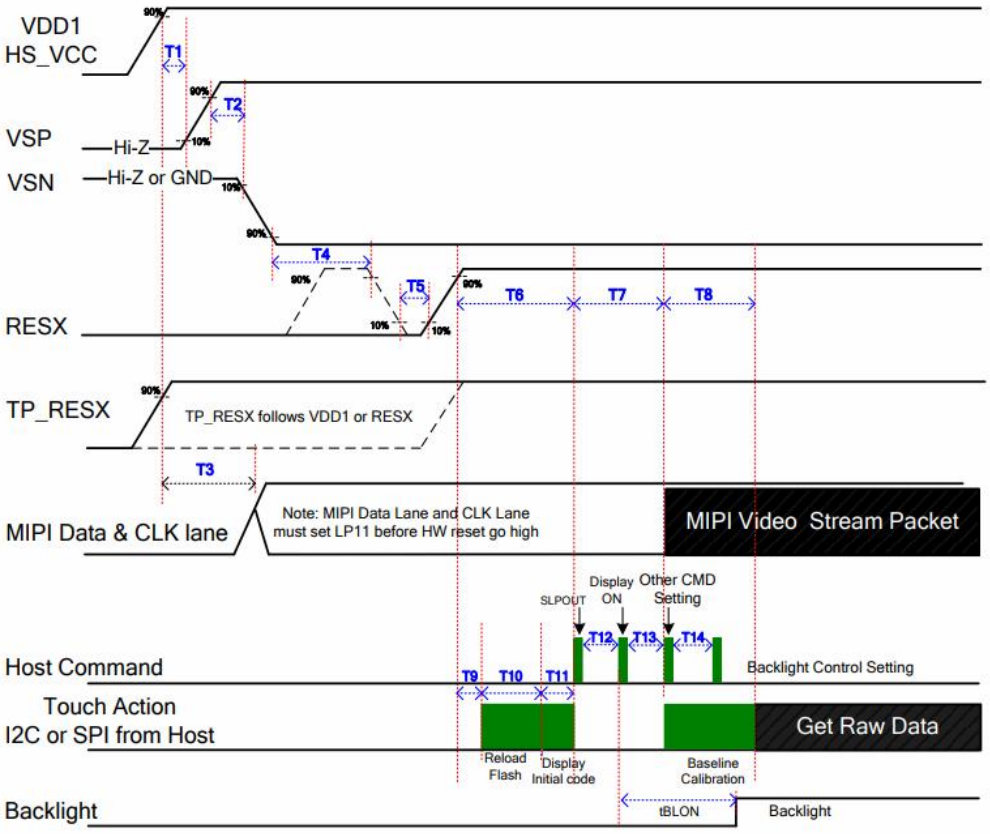


Figure 5.13: Power on/off sequence

5.1.1 Power on sequence

Symbol	Description	Min	Unit	Note
T1	VDD1 to VSP	1	ms	
T2	VSP to VSN	1	ms	
T3	VDD1 to MIPI Lane	1	ms	
T4	Power Ready to Global Reset	1	ms	
T5	Global Reset Keep Low	15	us	TP Reset is the same
T6	Global Reset to Sleep Out	150	ms	
T7	Sleep Out to Light On	140	ms	
T8	Touch Baseline Calibration	24	ms	
T9	Reset to Flash Reload	4	ms	
T10	Flash Reload Time	25	ms	Default: 6MHz
T11	Display initial code by FW	1	ms	
T12	Sleep Out to Display On	120	ms	
T13	Display On to IC Ready	20	ms	
T14	Other CMD Setting to Backlight Control Setting	0	ms	
tBLON	Display On Command to BL On time	40	ms	



Note1: If initial code upload by external flash

Figure 5.14: Power on and DSI signal sequence

5.1.2 Power on with LPWUG sequence

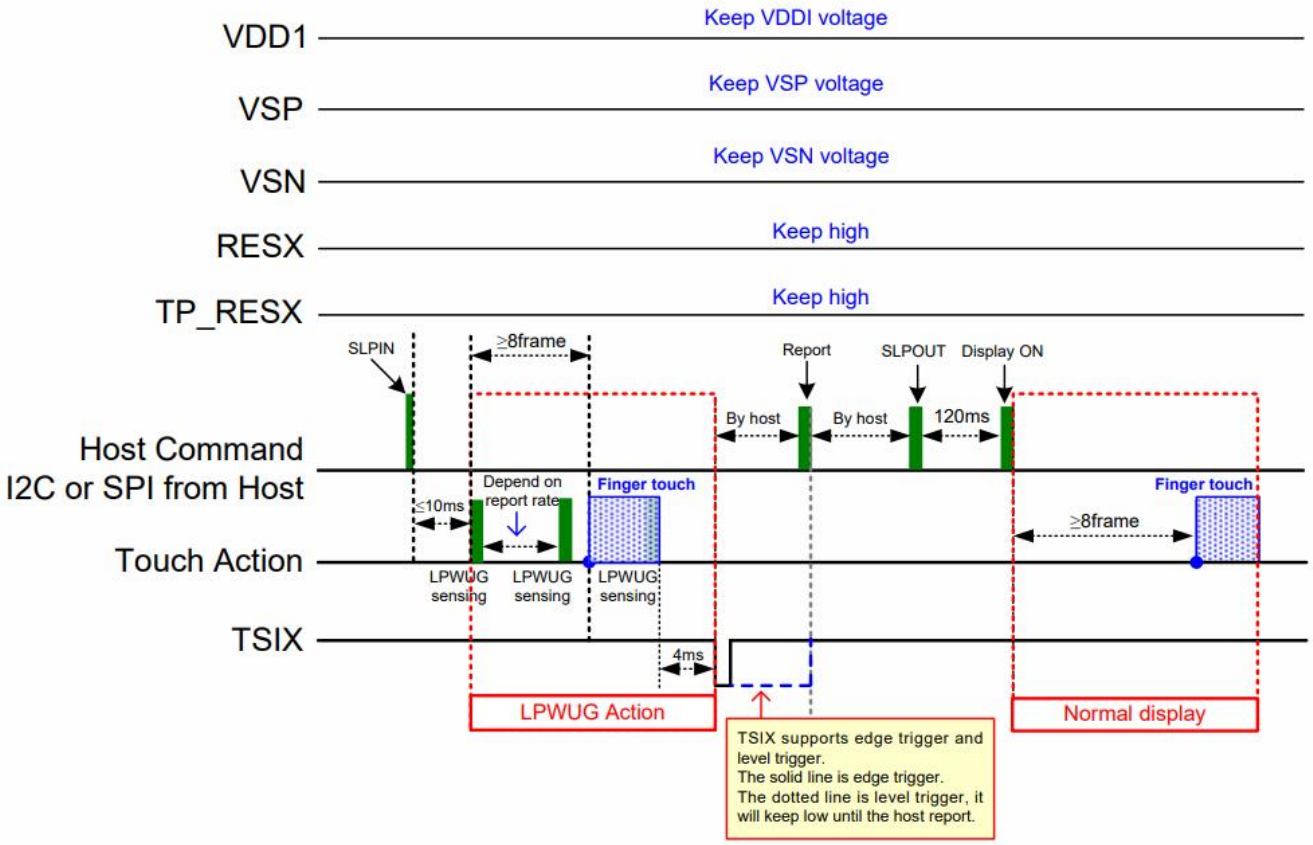
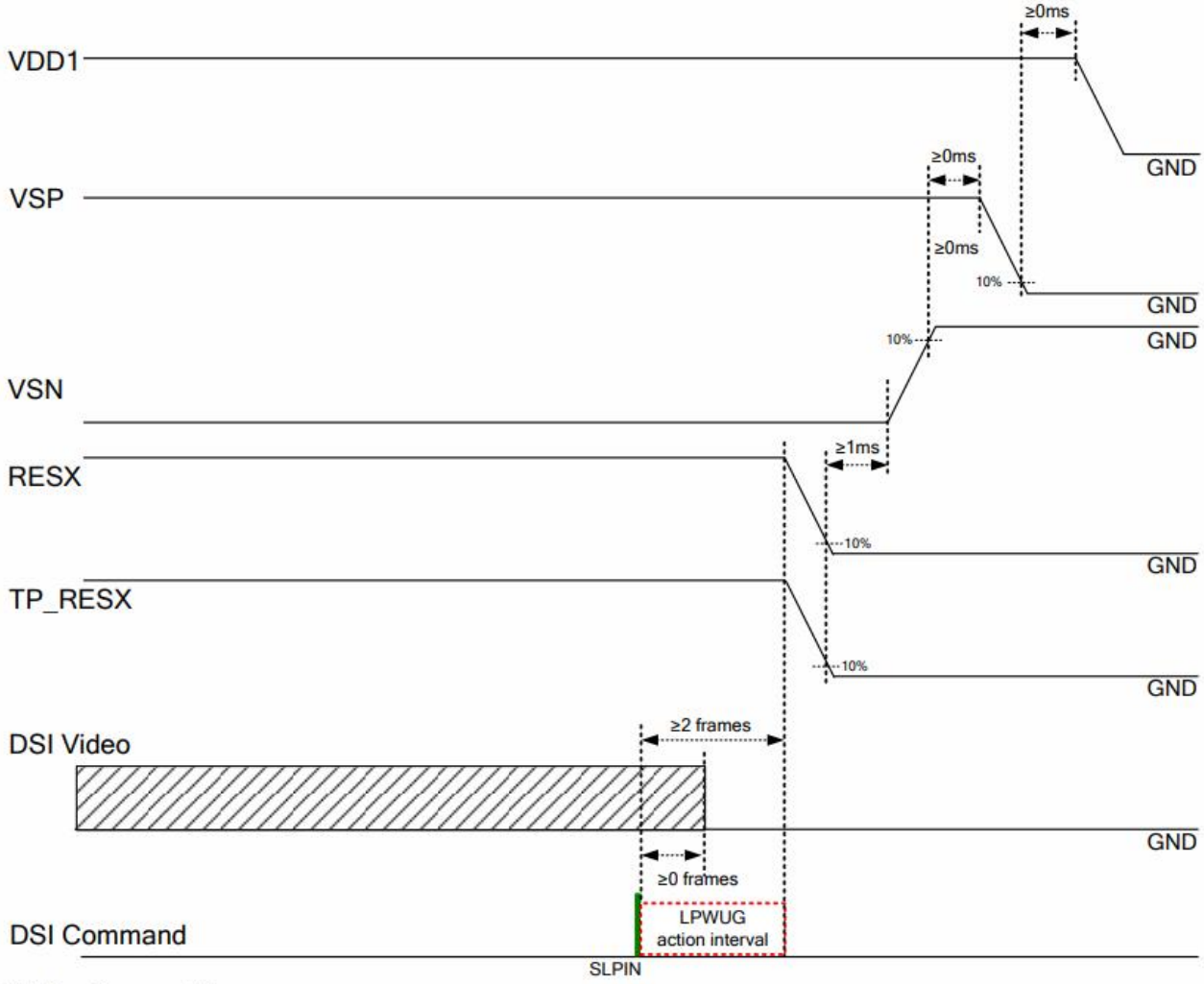


Figure 5.15: LPWUG to normal display for touch sequence

5.1.3 Power off sequence



Note: LPWUG action condition
1. IC enters SLPIN.
2. IC has VDD1/VSP/VSN voltage and TP_RESX/RESX keep high level.

Figure 5.16: Power off and DSI signal sequence

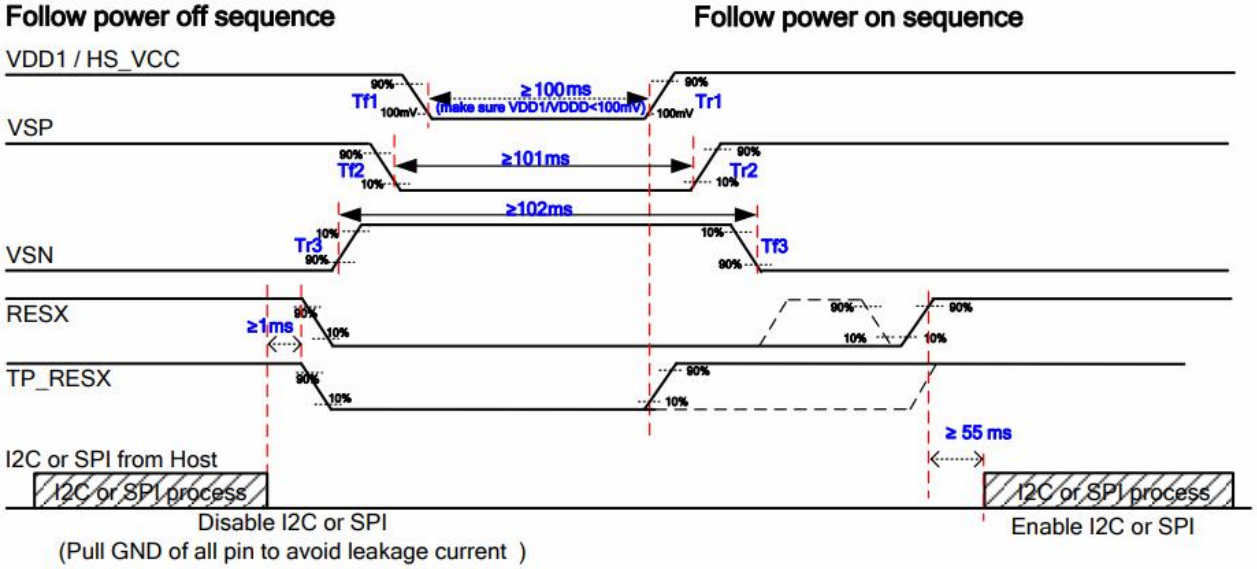


Figure 5.17: VDD1/VSP/VSN input power off to power on sequnence

VDD1/VSP/VSN Power rising and falling timing				
Symbol	**Min**	**Typ**	**Max**	**Descrition**
Tr1	20us	-	2ms	**10% - 90% for VDD1**
Tf1	20us	-	2ms	**90% - 10% for VDD1**
Tr2	100us	-	5ms	**10% - 90% for VSP**
Tf2	100us	-	5ms	**90% - 10% for VSP**
Tr3	100us	-	5ms	**90% - 10% for VSN**
Tf3	100us	-	5ms	**10% - 90% for VSN**

Table 5.8: Power rising and falling timing

5.2 DC Characteristics

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	VDD1= 1.65 ~ 1.95V	0.7 VDD1	-	VDD1	V
Input low voltage	V_{IL}		0	-	0.3 VDD1	V
Output high voltage	V_{OH}	I_{OH} = -1.0 mA	0.8 VDD1	-	VDD1	V
Output low voltage	V_{OL}	VDD1= 1.65 ~ 1.95V I_{OL} = 1.0 mA	0	-	0.2 VDD1	V
Logic High level input current	I_{IH}	All logic input pins	-	-	1	uA
Logic Low level input current	I_{IL}	All logic input pins	-1	-	-	uA
VDD1 current consumption in sleep in mode	$I_{STB(VDD1)}$	VDD1 = 1.8V VSP = 5.5V VSN = -5.5V T_A = 25°C	-	-	450	uA
VSP current consumption in sleep in mode	$I_{STB(VSP)}$		-	-	150	uA
VSN current consumption in sleep in mode	$I_{STB(VSN)}$		-	-	55	uA
VDD1 current consumption in UPS mode	$I_{ULPS(VDD1)}$	VDD1 = 1.8V VSP = 5.5V VSN = -5.5V T_A = 25°C	-	-	425	uA
VSP current consumption in ULPS mode	$I_{ULPS(VSP)}$		-	-	50	uA
VSN current consumption in ULPS mode	$I_{ULPS(VSN)}$		-	-	50	uA
Oscillator tolerance	ΔOSC	T_A =25°C	-3	-	3	%

Table 8.2 : DC characteristic

5.2.1 MIPI DC characteristics

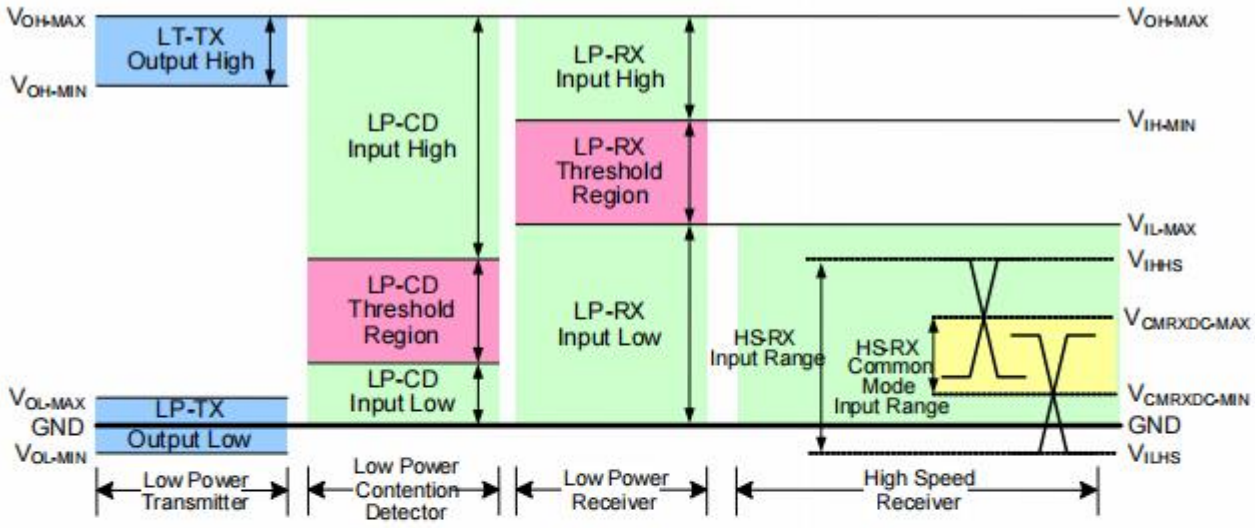


Figure 8.1 : MIPI signaling and contention voltage levels

DC characteristics for MIPI LP mode

Parameter	Symbol	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage	V_{IL}	0	-	550	mV
Logic 1 output voltage	V_{OH}	1.1	1.2	1.3	V
Logic 0 output voltage	V_{OL}	-50	-	50	mV

Table 8.3 : DC characteristics for MIPI LP mode

DC characteristics for MIPI HS mode

Parameter	Symbol	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Common-mode voltage HS Receive mode	V_{CMRXDC}	70	-	330	mV
Differential input high threshold(1)	V_{IDTH}	-	-	70	mV
Differential input low threshold(1)	V_{IDTL}	-70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Differential input impedance	Z_{ID}	80	100	125	Ω
TX HS transmit differential voltage **(VDP-VDN)**	|VOD|	140	200	270	mV

Note: (1) V_{IDTH} and V_{IDTL} only for reference, related to power and ground noise, this spec need to check on panel performance to fine tune

Table 8.4 : DC characteristics for MIPI HS mode

5.3 AC Characteristics

MIPI AC characteristics

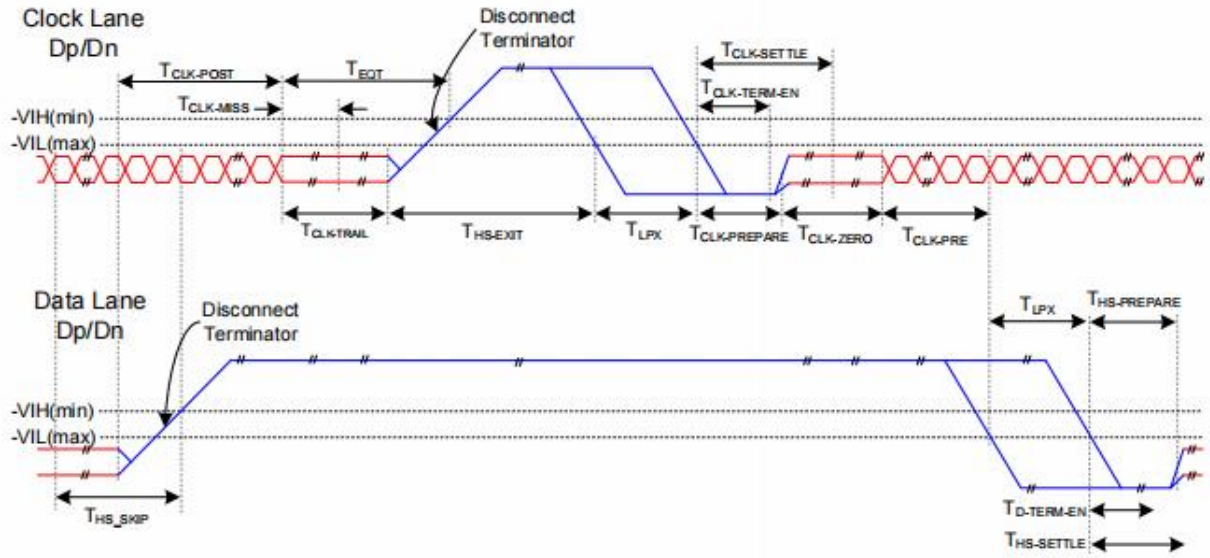


Figure 8.2 : Switching the clock lane between clock transmission and low-power mode

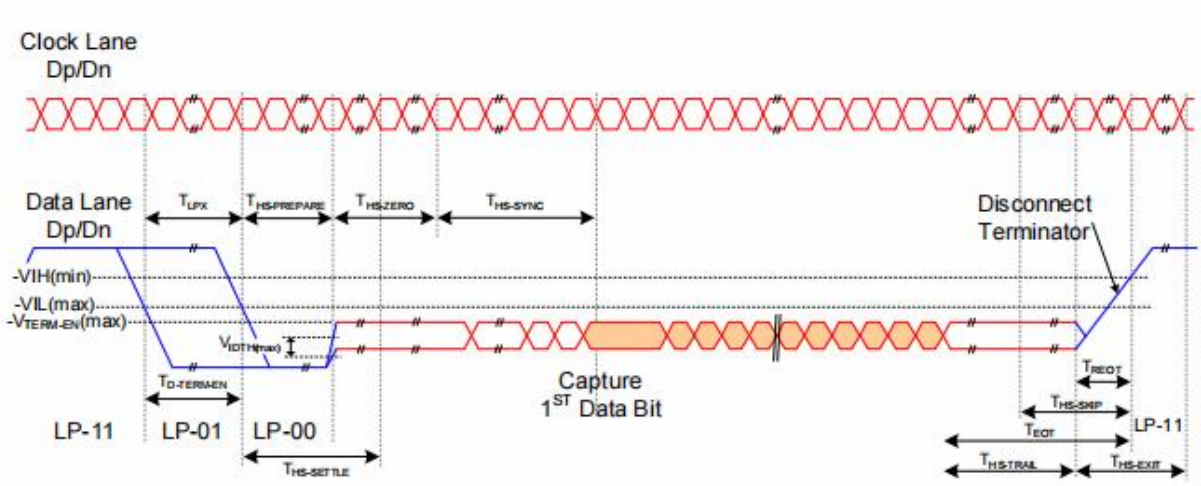


Figure 8.3 : Timing of high-speed data transmission in bursts

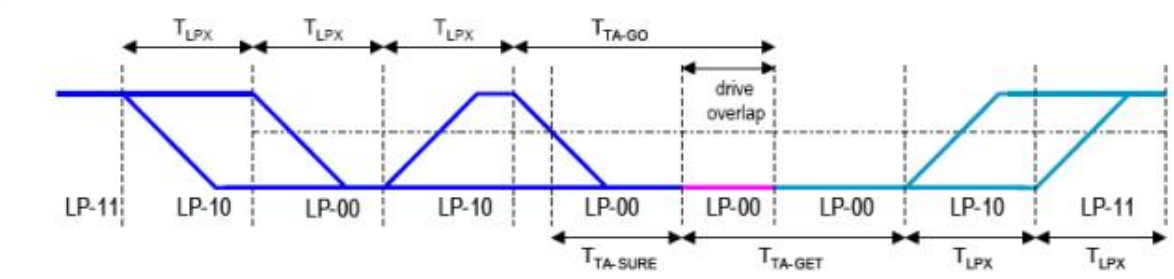


Figure 8.4 : Turnaround Procedure

MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$(1)	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI **(For DCS)**	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	UI
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$(1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	5*T_{LPX}			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	4*T_{LPX}			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	2*T_{LPX}	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

Table 8.5 : MIPI AC characteristics

MIPI data-clock timing specification

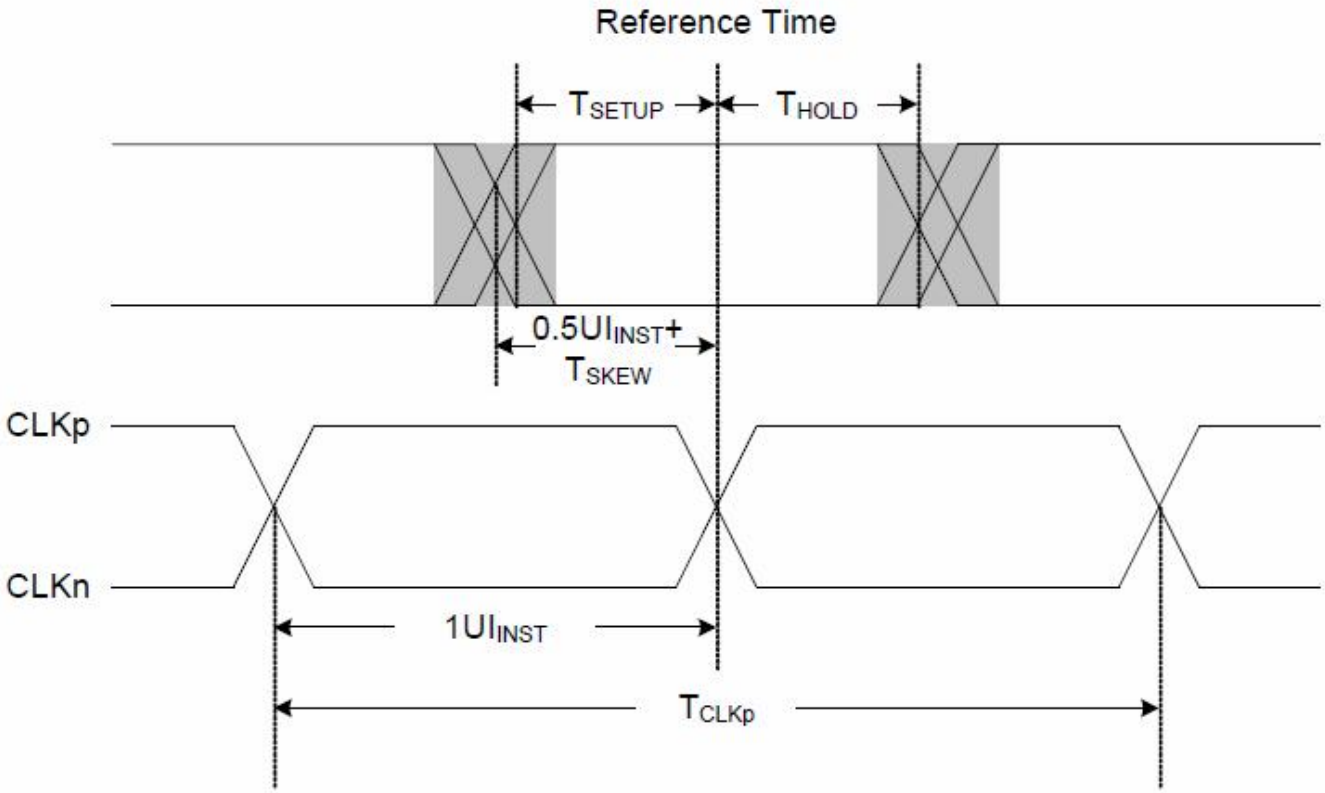


Figure 8.5 : Data to clock timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous	UI_{INST}	0.909	-	12.5(1)	ns
Data to clock setup time	T_{SETUP}	0.15(2)	-	-	UI_{INST}
Data to clock hold time	T_{HOLD}	0.15(2)	-	-	UI_{INST}

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) Total SETUP and HOLD window for receiver of 0.3* UI_{INST}

Timings for DSI video mode

Vertical timings

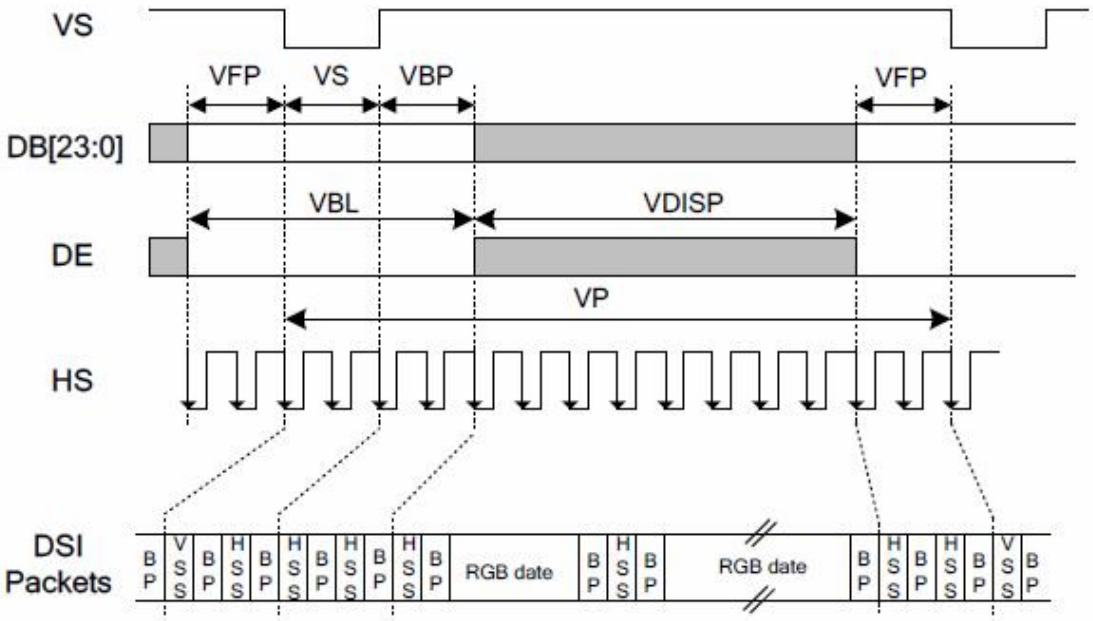


Figure 8.6: Vertical timings for DPI I/F

Resolution=2400channelx1280dot(VSSA=0V, VDD1=1.8V, T_A=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	1286	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSP(STV) and GCK(CLK) timing. The GSP and GCK must be set at corresponding position for LCD normal display.

Table 8.6: Vertical timings for DSI I/F

Horizontal timings

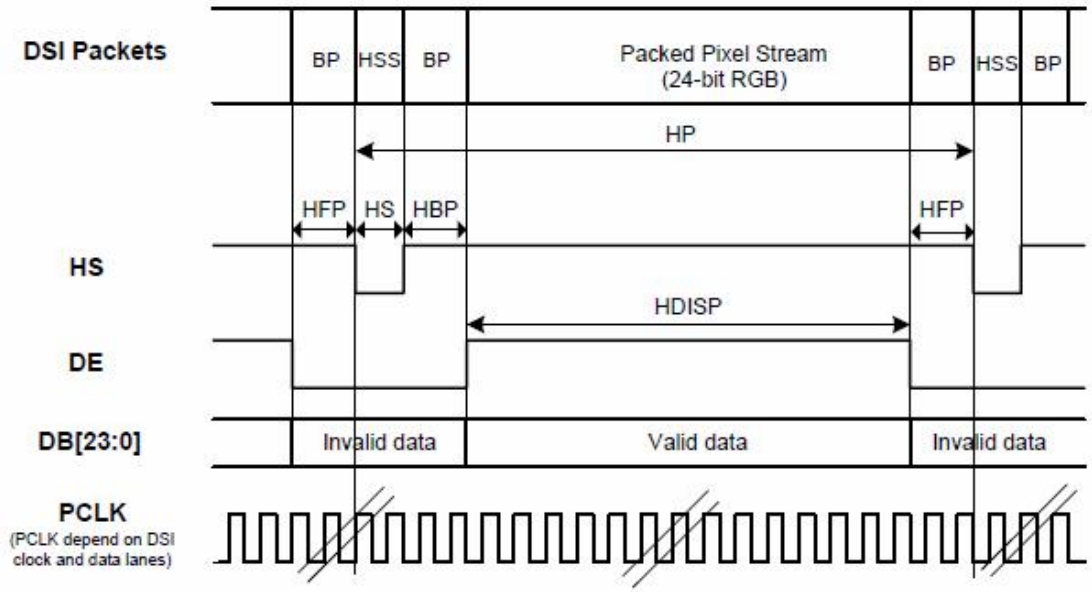


Figure 8.7: Horizontal timing for DSI video mode I/F

Resolution=2400channelx1280dot (VSSA=0V, VDD1=1.8V, T_A=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	-	0.2	-	µs
Horizontal back porch	HBP	-	-	0.2	-	µs
Horizontal front porch	HFP	-	-	0.2	-	µs
Horizontal active area	HDISP	-	-	2400	-	channel
1 line period (720RGB)	1H	HS+HBP+HFP+HDISP	8.3	-	-	µs
1 line period (768RGB)	1H	HS+HBP+HFP+HDISP	8.9	-	-	µs
1 line period (800RGB)	1H	HS+HBP+HFP+HDISP	9.2	-	-	µs

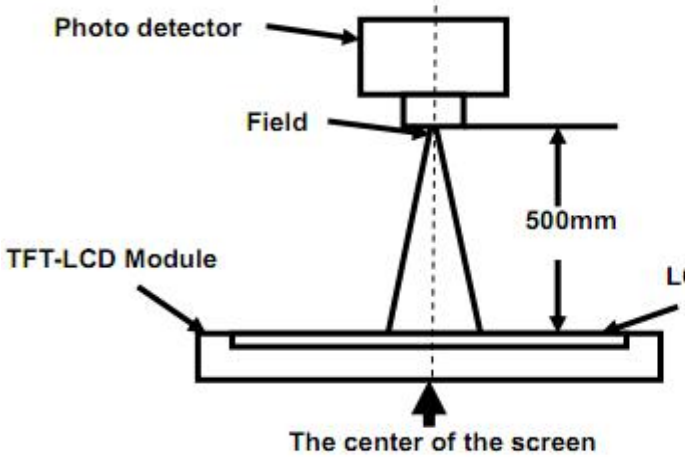
Table 8.7: Horizontal timings for DSI video mode I/F

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	80	85	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	80	85	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	80	85	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	80	85	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	15	17	msec	Note4
	T_{OFF}		-	15	17	msec	Note4
Contrast Ratio	CR		800	1000	-	-	Note1 Note3
Color Chromaticity	W_X		0.2752	0.3052	0.3352	-	Note1 Note5
	W_Y		0.2824	0.3124	0.3424	-	Note1 Note5
Luminance	L		900	1000	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		70	80	-	%	Note1 Note6
NTSC	-		65	70	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Fig 1

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

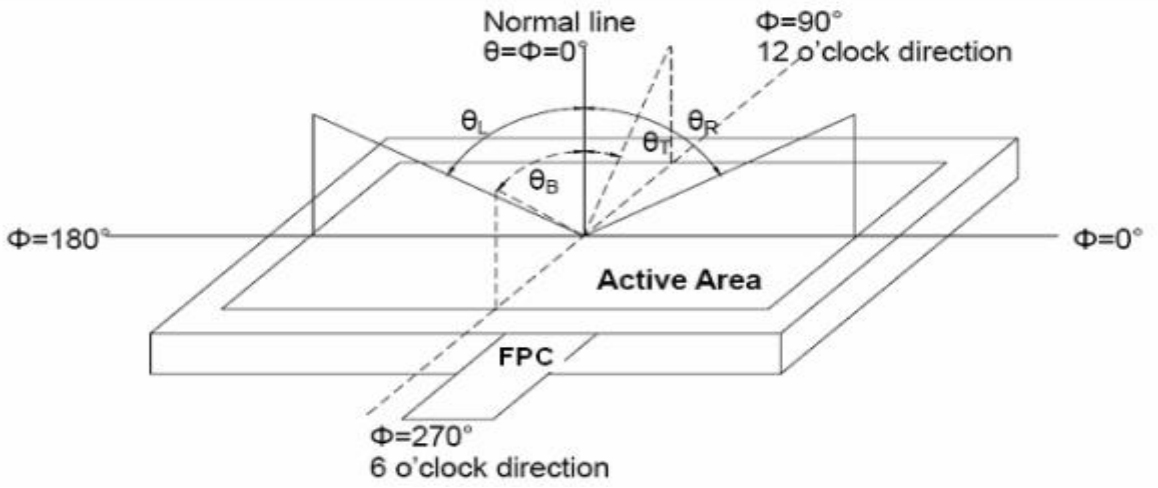


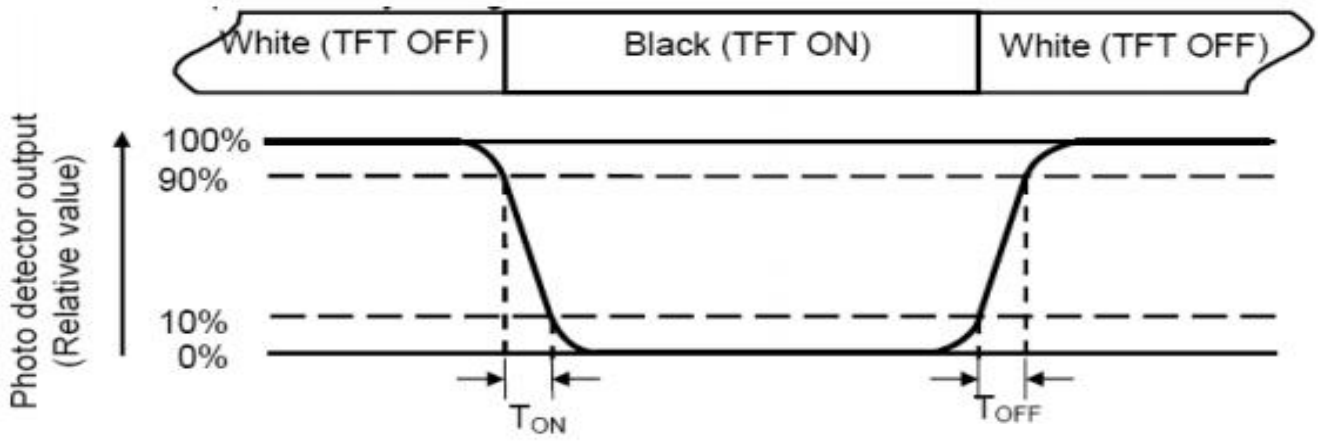
Fig 2 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.3-a/b

Note 7:Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

For more information see FIG.3-a/b

Note 8:

H,V : Active area(see Figure b)

Light spot size ⌀ =5mm(BM-5) or ⌀ =7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens. test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter SR-3A or BM-7 or compatible (see Figure 1).

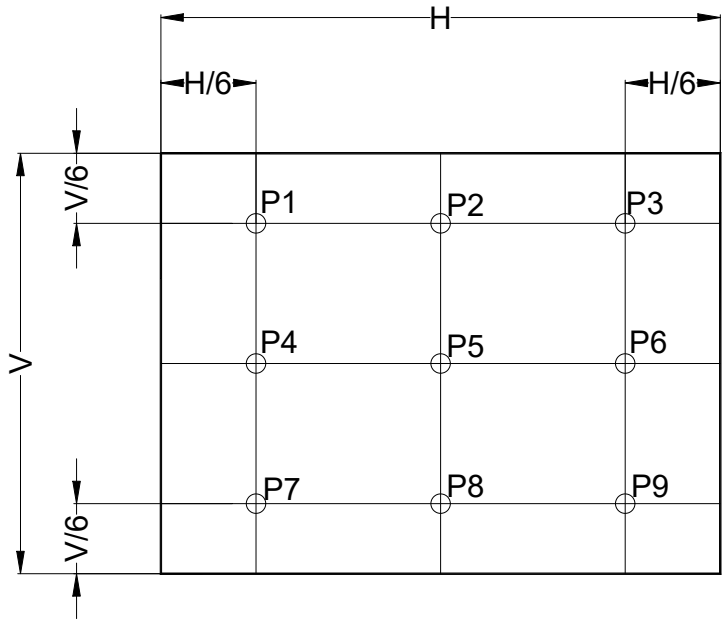


Fig. 3-b Definition of points

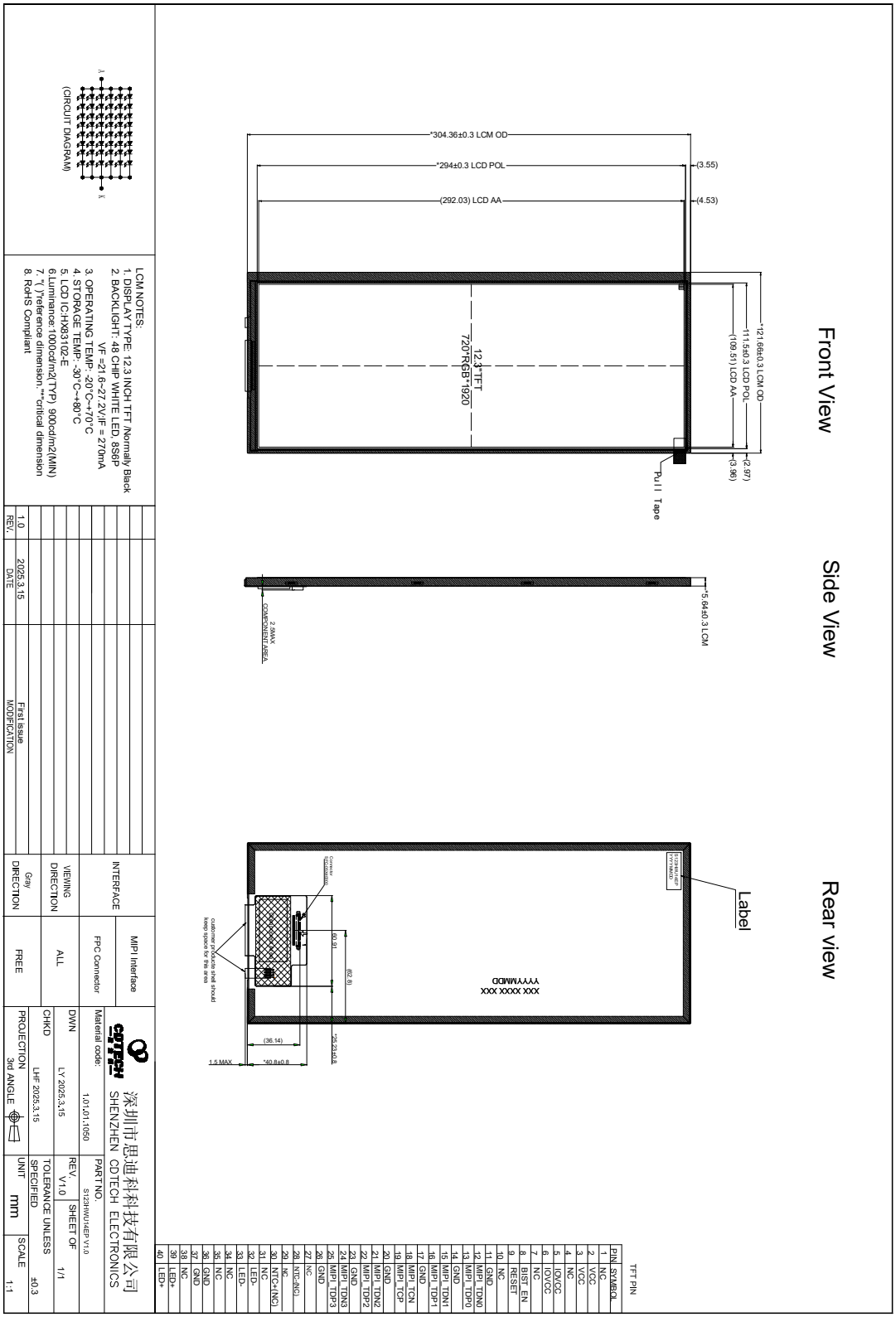
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +80℃	96hrs
Low Temperature Storage	Ta= -30℃	96hrs
High Temperature Operation	Ta= +70℃	96hrs
Low Temperature Operation	Ta= -20℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-20℃/30 min ~ +70℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

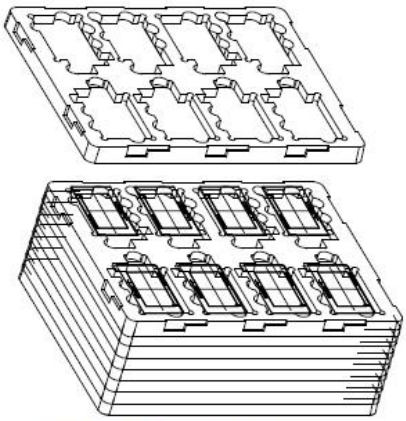
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing

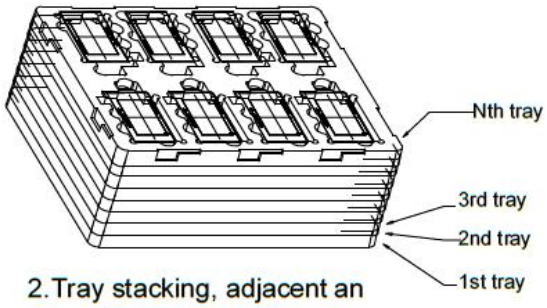


9. Packing

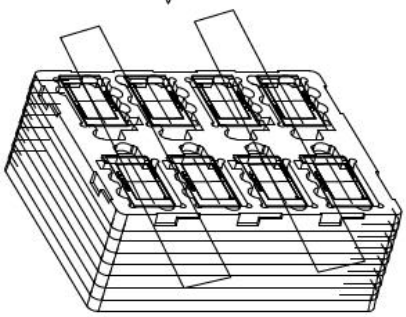
Packing Method



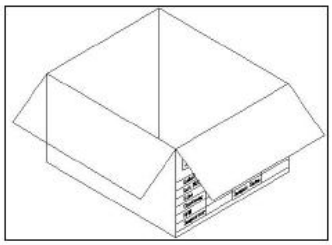
1.Put LCD module into tray cavity



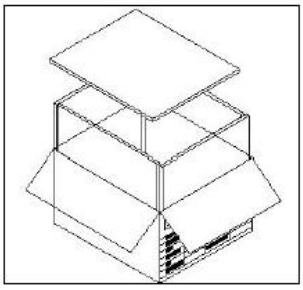
2.Tray stacking, adjacent an upper lower layer with a 180-degree rotation



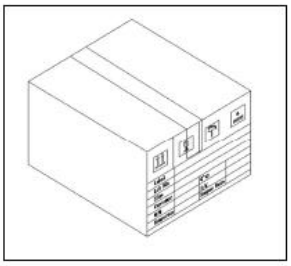
3.Medium Carton: Fix the tray stack with stretch film
Large Carton： Fix the tray stack with stretch film, then place it into a transparent PE antistatic bag



4. put the tray stack into carton



5. 6 sides of white foams inside the box



6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

10.4 Packaging instructions

When the customers using trays, they have to stack the adjacent trays in a 180° staggered to prevent pressure that could cause product damage.