DATA SHEET

(DOC No. HX8272-C01-LT-DS)

HX8272-C01-LT

1441CH TFT LCD Source Driver with TCON

Version 01 April, 2023

Himax Technologies, Inc.
http://www.himax.com.tw

Revision History

April, 2023

Version	Date	Description of changes
01	2023/04/26	New setup.

List of Contents

April, 2023

List of Contents

List of Figures

List of Figures

List of Tables

1. General Description

HX8272-C01-LT is a highly integrated source driver with built-in timing controller for color TFT LCD panels. This driver supports multiple display resolutions, with functions of 1441-channel 8-bit dot-inversion source driver **(SD)**, timing controller **(TCON)**, power circuits, GIP or LTPS switch control, I2C interface **(I2C)** and serial peripheral interface **(SPI)**. This driver is for industrial or automotive products.

2. Features

General

- COG **(Chip on glass)** package
- Support LTPS panel **(MUX1:1/MUX2:4/MUX2:6)**
- Support a-Si TFT Single gate / Dual gate / Triple gate GIP panel structure
- Support traditional gate driver panel structure
- Support Stripe and Zig-Zag type panel
- Support Normally Black and Normally White panels
- 8-bit per color true resolution **(16.7million colors)**
- Cascade mode for high resolution
- Closed loop for IC connection resistance checking
- On-chip OTP **(One-Time-Programming)** memory for all registers
- OTP for 3-set gamma setting
- External EEPROM for all registers
- GAS function **(Gate all select)** for preventing image sticking when abnormal power off
- Touch panel synchronization signals TP_SYNC[2:1]
- AEC-Q100 compliant for automotive applications
- Operation temperature: -40°C to +105°C

Timing controller

- Panel resolution **(Before panel development, it is necessary to confirm the panel RC load of all resolutions)**
  - 2560xRGBx960 **(Except MUX1:1 / Single gate)**
  - 2400xRGBx900 **(Except MUX1:1 / Single gate)**
  - 1920xRGBx1080
  - 1920xRGBx720
  - 1920xRGBx400
  - 1600xRGBx320
  - 1560xRGBx700
  - 1540xRGBx720
  - 1440xRGBx540
  - 1280xRGBx720
  - 1280xRGBx480
  - 1280xRGBx400
  - 960xRGBx2560 **(Only MUX1:1 / Single gate supported)**
  - 960xRGBx540

  - 800xRGBx480
  - 480xRGBx240
- Support 24-bit **(RGB x 8-bit)** or 18-bit **(RGB x 6-bit)** 1-port LVDS / 2-port LVDS / TTL interface
- Support HS+VS mode and DE mode
- 3/4-wire SPI or I2C command setting
- Support digital gamma processing and contrast / brightness control on RGB data separately
- Internal pattern generator with basic patterns in Built-In Self Test **(BIST)** mode
- Provide self-protection function for missing CLK, HS, VS or DE input
- Provide IC fail detection function for LVDS/Source/Power
- Dynamic VCOM/VGH/VGL/VGMPH/VGMPL/VGMNH/VGMNL and analog gamma settings controlled by external temperature sensor with TS_H and TS_L pin setting

Source driver
- Support maximum 1441CH LCD source output
- Source driver output with 8-bit DAC **(256-level)**
- Support Dot / 1+2 Line / 2+4 Line / Column inversion **(Vertical direction)** for MUX1:1, MUX2:4 and MUX2:6
- Support column inversion for Zig-Zag type panel
- Support analog gamma
- Maximum ±6.6V output swing
- Right and left shift capability
- 2-layer staggered pad with 14μm pitch

Gate driver
- Provide twenty adjustable control output signals for GIP circuit
- Support LTPS MUX switch control
- Support traditional gate driver signal **(Support pre-scan function)**

Power
- Main power supply VCC=3.0V to 3.6V
- Built-in PFM power control circuit for VSP and VSN
- Built-in regulators for gamma reference, TCON and LVDS power supplies
- Built-in charge pumps for GIP operation voltages VGH and VGL
- Built-in driving circuit for VCOM with SPI / I2C selection

3. Block Diagram, DC/DC and Boost Circuit Construction

3.1. Block diagram

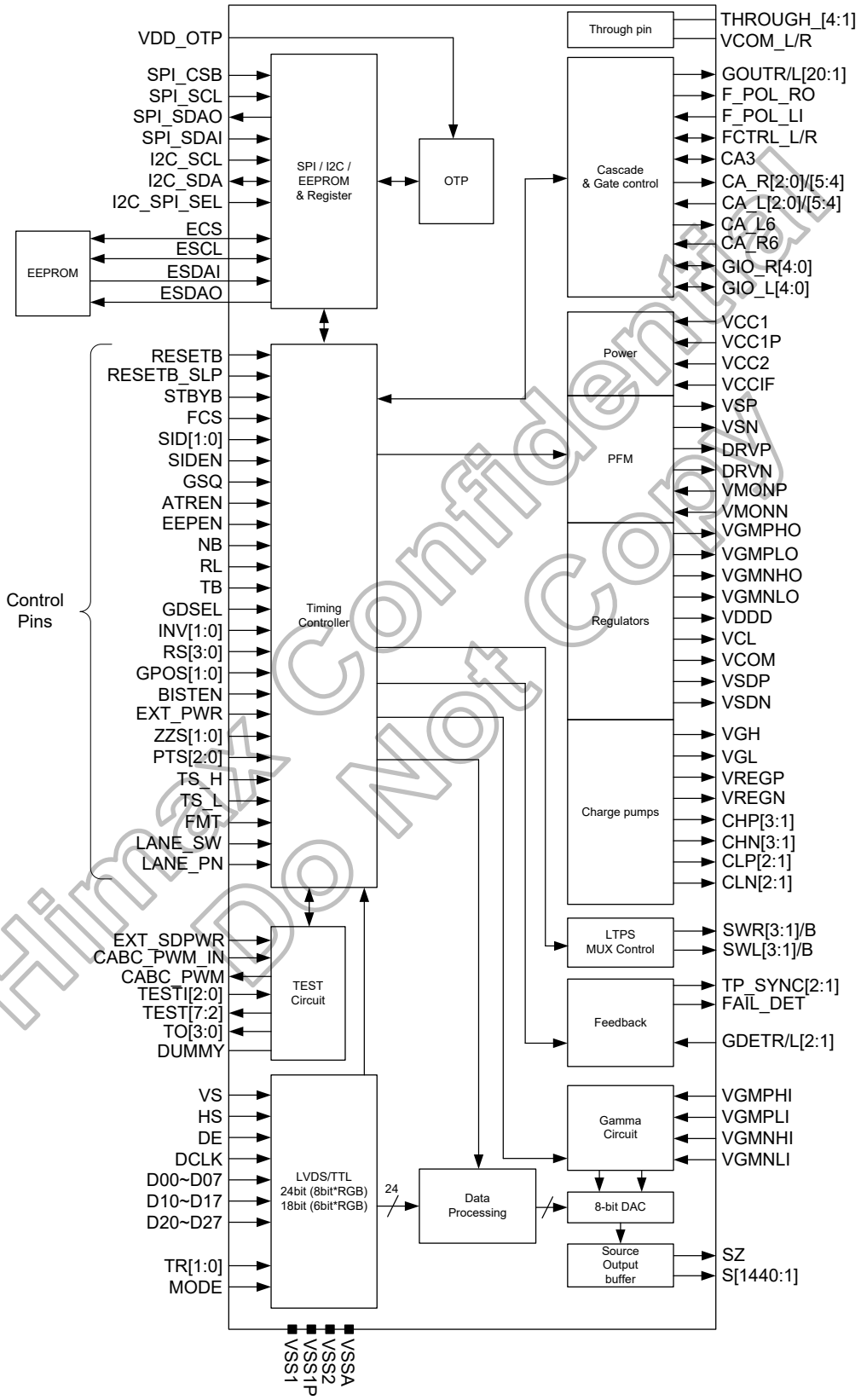


Figure 3.1: Block diagram

3.2. DC/DC voltage construction

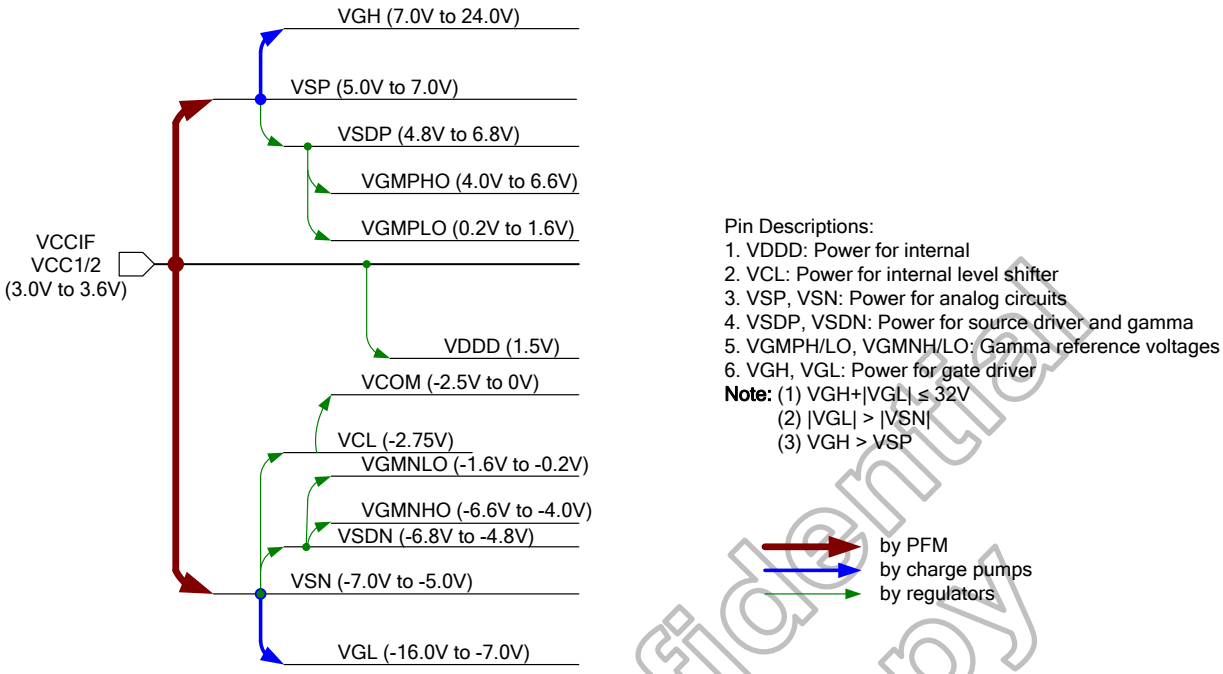


Figure 3.2: DC/DC voltage construction

4. Pin Description

4.1. Pin description

<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td colspan="4">Input interface pins (VCC1/VSS1 level) (Refer to Ch. 4.2. Interface pin connection)</td></tr>
<tr><td>D0[7:0]
D1[7:0]
D2[7:0]</td><td>I</td><td>-</td><td>Data input pins for TTL or LVDS mode.</td></tr>
<tr><td>DCLK</td><td>I</td><td>-</td><td>CLK for TTL mode.</td></tr>
<tr><td>HS</td><td>I</td><td>H</td><td>Horizontal sync signal for TTL mode.</td></tr>
<tr><td>VS</td><td>I</td><td>H</td><td>Vertical sync signal for TTL mode.</td></tr>
<tr><td>DE</td><td>I</td><td>L</td><td>Data enable signal for TTL mode.</td></tr>
<tr><td colspan="4">Input control pins, group 1 (Function controlled) (VCC1/VSS1 level)</td></tr>
<tr><td>RESETB</td><td>I</td><td>H</td><td>Global reset pin, active low.
The chip is in reset state when RESETB=L.</td></tr>
<tr><td>RESETB_SLP</td><td>I</td><td>H</td><td>Reset after power off sequence, active low.
If RESETB_SLP=L, the chip is in sleep in state, and all register will be reset after RESETB_SLP rising edge.
When RESETB_SLP function not used, please connect to VCC1.
(RESETB_SLP function (RESETB_SLP=L) at least needs 7 Frame input timing for Power off sequence.)</td></tr>
<tr><td>STBYB</td><td>I</td><td>H</td><td>Standby mode setting pin, active low.
Timing controller, output buffer, DAC and power circuit all off when STBYB=L.</td></tr>
<tr><td>FCS</td><td>I</td><td>H</td><td>Function control by Hardware/Software selection.
(RL, TB, BISTEN function is the hardware setting “XOR” with register setting when FCS=L.)
<table>
<tr><th>FCS</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Hardware pin (Group 2)</td><td>Default</td></tr>
<tr><td>L</td><td>Software register</td><td>-</td></tr>
</table></td></tr>
<tr><td>SID[1:0]</td><td>I</td><td>LL</td><td>Source driver ID (Position in chain) selection.
<table>
<tr><th>SID[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Master</td><td>Default</td></tr>
<tr><td>LH</td><td>Slave 1</td><td>-</td></tr>
<tr><td>HL</td><td>Slave 2</td><td>-</td></tr>
<tr><td>HH</td><td>Slave 3</td><td>-</td></tr>
</table>
(Refer to Ch. 5.3.1. Driver arrangement on panel.)</td></tr>
<tr><td>SIDEN</td><td>I</td><td>H</td><td>Enable chip ID identification in SPI / I2C.
<table>
<tr><th>SIDEN</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Chip R/W by CHIP ID[1:0] setting</td><td>Default</td></tr>
<tr><td>L</td><td>SPI / I2C writes to all chip, and read from Master only</td><td>-</td></tr>
</table>
(Refer to “Serial interface”.)</td></tr>
<tr><td>GSQ</td><td>I</td><td>L</td><td>Traditional Gate driver type selection.
<table>
<tr><th>GSQ</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Type 2</td><td>-</td></tr>
<tr><td>L</td><td>Type 1</td><td>Default</td></tr>
</table>
(Refer to “Gate driver type definition”.)
(If not Gate driver application, please don’t care GSQ.)</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td>ATREN</td><td>I</td><td>L</td><td>Enable auto reload OTP/EEPROM every 60 Frame. When programming OTP or changing register values by SPI / I2C, ATREN should be kept L.
<table>
<tr><th>ATREN</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Enable auto-reload OTP / EEPROM</td><td>-</td></tr>
<tr><td>L</td><td>Disable auto-reload OTP / EEPROM</td><td>Default</td></tr>
</table>
(If EEPEN=H and ATREN=H, the result is auto reload from EEPROM.)
(If EEPEN=L and ATREN=H, the result is auto reload from OTP.)</td></tr>
<tr><td>EXT_PWR</td><td>I</td><td>L</td><td>External / Internal power supply selection.
<table>
<tr><th>EXT_PWR</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>External VGH / VGL power supply</td><td>-</td></tr>
<tr><td>L</td><td>Internal VGH / VGL power supply</td><td>Default</td></tr>
</table></td></tr>
<tr><td>EEPEN</td><td>I</td><td>L</td><td>EEPROM reload setting enable.
<table>
<tr><th>EEPEN</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Enable</td><td>-</td></tr>
<tr><td>L</td><td>Disable</td><td>Default</td></tr>
</table></td></tr>
<tr><td>I2C_SPI_SEL</td><td>I</td><td>L</td><td>SPI / I2C interface selection.
<table>
<tr><th>I2C_SPI_SEL</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>I2C</td><td>-</td></tr>
<tr><td>L</td><td>SPI</td><td>Default</td></tr>
</table></td></tr>
<tr><td>NB</td><td>I</td><td>H</td><td>The function of NB pin in HX8272-C01-LT is change to polarity change sequence method selection.
<table>
<tr><th>NB</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Disable</td><td>Default</td></tr>
<tr><td>L</td><td>Enable polarity change sequence N frame inversion, N set by POL_INV_FRM[3:0]</td><td>-</td></tr>
</table></td></tr>
<tr><td colspan="4">Input control pins, group 2 (Function controlled by hardware or software setting) (VCC1/VSS1 level)</td></tr>
<tr><td>TR[1:0]</td><td>I</td><td>LL</td><td>Interface selection.
<table>
<tr><th>TR[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>Lx</td><td>TTL</td><td>Default</td></tr>
<tr><td>HL</td><td>1-port LVDS</td><td>-</td></tr>
<tr><td>HH</td><td>2-port LVDS</td><td>-</td></tr>
</table></td></tr>
<tr><td>MODE</td><td>I</td><td>H</td><td>Input timing mode selection.
<table>
<tr><th>MODE</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>HS+VS</td><td>Default</td></tr>
<tr><td>L</td><td>DE only</td><td>-</td></tr>
</table>
(Refer to Figure 6.12: The restriction of input DE variation.)</td></tr>
<tr><td>RL</td><td>I</td><td>H</td><td>Horizontal shift direction (Source output) selection.
(RL function is the hardware setting “XOR” with register setting when FCS=L.)
<table>
<tr><th>RL</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Forward
(S[1]→S[2]→ …→ S[1440])</td><td>Default</td></tr>
<tr><td>L</td><td>Reverse
(S[1440]→S[1439]→ …→ S[1])</td><td>-</td></tr>
</table></td></tr>
<tr><td>TB</td><td>I</td><td>H</td><td>Vertical shift direction (Gate output) selection.
(TB function is the hardware setting “XOR” with register setting when FCS=L.)
<table>
<tr><th>TB</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>Forward, Top→Bottom</td><td>Default</td></tr>
<tr><td>L</td><td>Reverse, Bottom→Top</td><td>-</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td>GDSEL</td><td>I</td><td>L</td><td>Select pin of GIP / Gate driver mode.
<table>
<tr><th>GDSEL</th><th>Function</th><th>Note</th></tr>
<tr><td>L</td><td>GIP</td><td>Default</td></tr>
<tr><td>H</td><td>Traditional Gate driver</td><td>-</td></tr>
</table></td></tr>
<tr><td>INV[1:0]</td><td>I</td><td>HH</td><td>Inversion type selection.
A. When PTS=3’b000/3’b001/3’b010/3’b011 for MUX2:4/MUX2:6/MUX1:1:
<table>
<tr><th>INV[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>LH</td><td>1+2 Line inversion (Vertical)</td><td>-</td></tr>
<tr><td>HL</td><td>2+4 Line inversion (Vertical)</td><td>-</td></tr>
<tr><td>HH</td><td>Column inversion (Vertical)</td><td>Default</td></tr>
</table>
B. When PTS=3’b011 for Single gate:
<table>
<tr><th>INV[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>LH</td><td>1+2 Line inversion (Vertical)</td><td>-</td></tr>
<tr><td>HL</td><td>2+4 Line inversion (Vertical)</td><td>-</td></tr>
<tr><td>HH</td><td>Column inversion (Vertical)</td><td>Default</td></tr>
</table>
C. When PTS=3’b100/3’b110/3’b111 for Dual gate:
<table>
<tr><th>INV[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>1+2 dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>LH</td><td>Reserved</td><td>-</td></tr>
<tr><td>HL</td><td>2-dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>HH</td><td>Column inversion (Vertical)</td><td>Default</td></tr>
</table>
D. When PTS=3’b101 for Triple gate:
<table>
<tr><th>INV[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>LH</td><td>3-dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>HL</td><td>3+6 dot inversion (Vertical)</td><td>-</td></tr>
<tr><td>HH</td><td>Column inversion (Vertical)</td><td>Default</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td>RS[3:0]</td><td>I</td><td>LLLL</td><td>Panel resolution selection.
<table>
<tr><th>RS[3:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LLLL</td><td>2560 x RGB x 960 (Except MUX1:1 / Single gate)</td><td>Default</td></tr>
<tr><td>LLLH</td><td>2400 x RGB x 900 (Except MUX1:1 / Single gate)</td><td>-</td></tr>
<tr><td>LLHL</td><td>1920 x RGB x 1080</td><td>-</td></tr>
<tr><td>LLHH</td><td>1920 x RGB x 720</td><td>-</td></tr>
<tr><td>LHLL</td><td>1920 x RGB x 400</td><td>-</td></tr>
<tr><td>LHLH</td><td>1600 x RGB x 320</td><td>-</td></tr>
<tr><td>LHHL</td><td>1560 x RGB x 700</td><td>-</td></tr>
<tr><td>LHHH</td><td>1540 x RGB x 720</td><td>-</td></tr>
<tr><td>HLLL</td><td>1440 x RGB x 540</td><td>-</td></tr>
<tr><td>HLLH</td><td>1280 x RGB x 720</td><td>-</td></tr>
<tr><td>HLHL</td><td>1280 x RGB x 480</td><td>-</td></tr>
<tr><td>HLHH</td><td>1280 x RGB x 400</td><td>-</td></tr>
<tr><td>HHLL</td><td>960 x RGB x 2560 (Only MUX1:1 / Single gate supported)</td><td>-</td></tr>
<tr><td>HHLH</td><td>960 x RGB x 540</td><td>-</td></tr>
<tr><td>HHHL</td><td>800 x RGB x 480</td><td>-</td></tr>
<tr><td>HHHH</td><td>480 x RGB x 240</td><td>-</td></tr>
</table></td></tr>
<tr><td>GPOS[1:0]</td><td>I</td><td>LL</td><td>Traditional Gate driver location select.
<table>
<tr><th>GPOS[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Left side</td><td>Default</td></tr>
<tr><td>LH</td><td>Right side</td><td>-</td></tr>
<tr><td>HL</td><td>Interlaced driving at dual side</td><td>-</td></tr>
<tr><td>HH</td><td>Progressive driving the same line at dual side</td><td>-</td></tr>
</table>
(Refer to “Gate driver signal definition”.)
(If not Gate driver application, please don’t care GPOS[1:0])</td></tr>
<tr><td>BISTEN</td><td>I</td><td>L</td><td>Enable Built-In Self Test (BIST) function.
(BISTEN function is the hardware setting “XOR” with register setting when FCS=L.)
<table>
<tr><th>BISTEN</th><th>Function</th><th>Note</th></tr>
<tr><td>H</td><td>BIST mode</td><td>-</td></tr>
<tr><td>L</td><td>Normal mode</td><td>Default</td></tr>
</table></td></tr>
<tr><td>ZZS[1:0]</td><td>I</td><td>LL</td><td>Zig-Zag type selection.
<table>
<tr><th>ZZS[1:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LL</td><td>Stripe panel</td><td>Default</td></tr>
<tr><td>LH</td><td>Zig-Zag Type 1</td><td>-</td></tr>
<tr><td>HL</td><td>Zig-Zag Type 2</td><td>-</td></tr>
<tr><td>HH</td><td>Stripe panel</td><td>-</td></tr>
</table></td></tr>
<tr><td>PTS[2:0]</td><td>I</td><td>LHH</td><td>Panel type selection.
<table>
<tr><th>PTS[2:0]</th><th>Function</th><th>Note</th></tr>
<tr><td>LLL</td><td>LTPS MUX2:4</td><td>-</td></tr>
<tr><td>LLH</td><td>LTPS MUX2:6_Type 1</td><td>-</td></tr>
<tr><td>LHL</td><td>LTPS MUX2:6_Type 2</td><td>-</td></tr>
<tr><td>LHH</td><td>LTPS MUX1:1 / Single gate</td><td>Default</td></tr>
<tr><td>HLL</td><td>Dual gate Type 1</td><td>-</td></tr>
<tr><td>HLH</td><td>Triple gate</td><td>-</td></tr>
<tr><td>HHL</td><td>Dual gate Type 2</td><td>-</td></tr>
<tr><td>HHH</td><td>Dual gate Type 3</td><td>-</td></tr>
</table>
(Dual gate Type 3 only support Zig-Zag type panel)</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td>FMT</td><td>I</td><td>L</td><td>TTL or LVDS input data format selection:
If TR[1]=0, select input data order at TTL mode.
<table>
<tr><th>FMT</th><th>Function</th><th>Note</th></tr>
<tr><td>L</td><td>[D07:D00] map DR[7:0];
[D17:D10] map DG[7:0];
[D27:D20] map DB[7:0]</td><td>Default</td></tr>
<tr><td>H</td><td>[D07:D00] map DR[0:7];
[D17:D10] map DG[0:7];
[D27:D20] map DB[0:7]</td><td>-</td></tr>
</table>
If TR[1]=1, select LVDS format.
<table>
<tr><th>FMT</th><th>Function</th><th>Note</th></tr>
<tr><td>L</td><td>JEIDA format</td><td>Default</td></tr>
<tr><td>H</td><td>VESA format</td><td>-</td></tr>
</table></td></tr>
<tr><td>LANE_SW</td><td>I</td><td>L</td><td>LVDS lane swapping selection.
(Please refer to Ch. 4.2. Interface pin connection for lane arrangement.)</td></tr>
<tr><td>LANE_PN</td><td>I</td><td>L</td><td>LVDS lane PN polarity swapping selection.</td></tr>
<tr><td colspan="4">Serial interface pins (VCC1/VSS1 level)</td></tr>
<tr><td>SPI_CSB</td><td>I</td><td>H</td><td>Serial interface chip enable signal for SPI interface.
SPI_CSB=L: Selected (Accessible).
SPI_CSB=H: Not selected (Inaccessible).</td></tr>
<tr><td>SPI_SCL</td><td>I</td><td>L</td><td>Serial interface clock input for SPI interface.</td></tr>
<tr><td>SPI_SDAI</td><td>I</td><td>L</td><td>Serial interface address and data input for SPI interface.</td></tr>
<tr><td>SPI_SDAO</td><td>O</td><td>-</td><td>Serial interface data output for SPI interface.</td></tr>
<tr><td>I2C_SDA</td><td>I/O</td><td>-</td><td>Serial interface address and data input/output for I2C interface.
(I2C interface need external pull high resistance (4.7KΩ).)</td></tr>
<tr><td>I2C_SCL</td><td>I</td><td>L</td><td>Serial interface clock input for I2C interface.</td></tr>
<tr><td colspan="4">EEPROM interface pins (VCC1/VSS1 level)</td></tr>
<tr><td>ECS</td><td>I/O</td><td>L</td><td>Chip select enable signal for EEPROM CS.
ECS=L: Not accessing EEPROM.
ECS=H: Accessing EEPROM.</td></tr>
<tr><td>ESCL</td><td>I/O</td><td>L</td><td>Clock signal for EEPROM CLK.</td></tr>
<tr><td>ESDAI</td><td>I</td><td>L</td><td>Serial data input from EEPROM DO.</td></tr>
<tr><td>ESDAO</td><td>O</td><td>-</td><td>Serial data (Address) output for EEPROM DI.</td></tr>
<tr><td colspan="4">Cascade and gate control pins (Leave these pins open if not used. Refer to Ch. 5.3.2. Cascade and gate driver control interface.)</td></tr>
<tr><td>GIO_L[4:0]</td><td>I/O</td><td>L</td><td>Gate driver control pins at the left side.</td></tr>
<tr><td>FCTRL_L</td><td>I/O</td><td>L</td><td>GIP mode sync pin.</td></tr>
<tr><td>CA_L[2:0]
CA_L[5:4]
CA_R[6]</td><td>I</td><td>L</td><td>Cascade signal input pin.</td></tr>
<tr><td>F_POL_LI</td><td>I</td><td>L</td><td>POL sync control signal.</td></tr>
<tr><td>CA3</td><td>I/O</td><td>L</td><td>Cascade signal pin. (Open drain I/O)</td></tr>
<tr><td>CA_R[2:0]
CA_R[5:4]
CA_L[6]</td><td>O</td><td>-</td><td>Cascade signal output pin.</td></tr>
<tr><td>GIO_R[4:0]</td><td>I/O</td><td>L</td><td>Gate driver control pins at the right side.</td></tr>
<tr><td>FCTRL_R</td><td>I/O</td><td>L</td><td>GIP mode sync pin.</td></tr>
<tr><td>F_POL_RO</td><td>O</td><td>-</td><td>POL sync control signal.</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>Type</th><th>Pulled internally</th><th>Description</th></tr>
<tr><td colspan="4">Special function pins</td></tr>
<tr><td>TP_SYNC[2:1]</td><td>O</td><td>-</td><td>Output frame signal for Touch Panel application.</td></tr>
<tr><td>TS_H
TS_L</td><td>I</td><td>L</td><td>Input temperature status.
<table>
<tr><th>TS_H</th><th>TS_L</th><th>Function</th><th>Note</th></tr>
<tr><td>L</td><td>L</td><td>Room temperature mode.</td><td>Default</td></tr>
<tr><td>L</td><td>H</td><td>Low temperature mode.</td><td>-</td></tr>
<tr><td>H</td><td>L</td><td>High temperature mode.</td><td>-</td></tr>
<tr><td>H</td><td>H</td><td>Reserved</td><td>-</td></tr>
</table></td></tr>
<tr><td>FAIL_DET</td><td>O</td><td>-</td><td>Fail detection signal output.</td></tr>
<tr><td>GDETL[2:1]
GDETR[2:1]</td><td>I</td><td>L</td><td>GIP detect input pin.</td></tr>
<tr><td>TEST4</td><td>O</td><td>-</td><td>TEST4 could output high for PFM_NG fail status.</td></tr>
</table>

Pin name	Type	Description
Source and GIP output pins		
SZ, S[1440:1]	O	Source driver output pins.
GOUTR[20:1]	O	GIP control output pins.
GOUTL[20:1]	O	GIP control output pins.
SWR[3:1] SWR[3:1]B	O	MUX control output pins.
SWL[3:1] SWL[3:1]B	O	MUX control output pins.
Power supply pins: Connected to power supply		
VCC1	P	Power input for main and I/O power **(3.0V to 3.6V)**.
VCC1P	P	Power input pin. Connected to VCC1.
VSS1	P	Ground pin for logic circuit and I/O **(0V)**.
VSS1P	P	Ground pin. Connected to VSS1.
VCC2	P	Power pin for internal references **(3.0V to 3.6V)**.
VSS2	P	Ground pin for internal reference circuit **(0V)**.
VSSA	P	Ground pin for analog circuit **(0V)**.
VCCIF	P	Power pin for LVDS/TTL interface I/O **(3.0V to 3.6V)**.
VSP	P	Power input for source driver and power circuits **(5V to 7V)**.
VSN	P	Power input for source driver and power circuits **(-7V to -5V)**.
VDD_OTP	P	Power input for OTP programming **(8.6V)**. Leave this pin open or connect it to VCC1 when not programming OTP.
Regulator output and voltage reference input pins: Connected to capacitors		
VGMPHO	O	Internal regulator output for positive gamma reference voltage.
VGMPLO	O	Internal regulator output for positive gamma reference voltage.
VGMNHO	O	Internal regulator output for negative gamma reference voltage.
VGMNLO	O	Internal regulator output for negative gamma reference voltage.
VGMPHI	I	Positive gamma reference voltage.
VGMPLI	I	Positive gamma reference voltage.
VGMNHI	I	Negative gamma reference voltage.
VGMNLI	I	Negative gamma reference voltage.
VDDD	O	Internal regulator output for logic power supply **(1.5V)**.
VCOM	O	Internal driving circuit for VCOM **(-2.5V to 0V)**.
VCL	O	Internal regulator output for negative level shifter **(-2.75V)**.
VSDP	O	Internal regulator output for source driver and gamma.
VSDN	O	Internal regulator output for source driver and gamma.
Charge pump and PFM pins: Connected to external components		
VGH	O	Charge pump output for gate driver.
VGL	O	Charge pump output for gate driver.
CHP[3:1] CHN[3:1]	C	Capacitor connection pin for VGH charge pump.
CLP[2:1] CLN[2:1]	C	Capacitor connection pin for VGL charge pump.
VREGP	O	Regulator voltage for VGH charge pump. **(Only for diode connect type)** If not using external diode, let this pin floating.
VREGN	O	Regulator voltage for VGL charge pump. **(Only for diode connect type)** If not using external diode, let this pin floating.
DRVP	O	PFM output control signal for VSP.
DRVN	O	PFM output control signal for VSN.
VMONP	I	Input pin for positive voltage detection for PFM over current detection. When PFM function not used, please connect to GND.
VMONN	I	Input pin for negative voltage detection for PFM over current detection. When PFM function not used, please connect to GND.
Test pins, through pins and dummy pins		
TEST[3:2] TEST[7:5]	O	Logic test pins, leave these pins open.
TESTI[2:0]	I	Logic test pins, leave these pins open. **(Default pull low)**

Pin name	Type	Description
TO[3:0]	O	Internal reference voltage test pin, leave these pins open.
THROUGH_[4:1]	-	These sets of pins can be used for resistance measurement.
VCOM_R VCOM_L	-	These sets of pins can be used for VCOM connection to the panel.
EXT_SDPWR	I	Logic test pin, leave this pin open. **(Default pull low)**
CABC_PWM_IN	I	Test pin, leave this pin open. **(Default pull low)**
CABC_PWM	O	Test pin, leave this pin open.
DUMMY	-	Please let it floating.

4.2. Interface pin connection

Pin name	Pin type	TTL 8-bit		TTL 6-bit(1)		LVDS 2-port	LVDS 1-port	LVDS 2-port	LVDS 1-port	LVDS 1-port
		8-bit		6-bit(2)		8-bit	8-bit	8-bit	8-bit	6-bit(2)
LANE_SW selection		Don't care		Don't care		0		1		0(3)
FMT selection		0	1	0	1	JEIDA(0) / VESA(1)				Don't care
D20	TTL/ Differential	DB0	DB7	VSS	DB5	-	-	-	-	-
D21		DB1	DB6	VSS	DB4	-	-	-	-	-
D22		DB2	DB5	DB0	DB3	-	-	-	-	-
D23		DB3	DB4	DB1	DB2	-	-	-	-	-
D24		DB4	DB3	DB2	DB1	ELV3P	-	ELV0P	-	-
D25		DB5	DB2	DB3	DB0	ELV3N	-	ELV0N	-	-
D26		DB6	DB1	DB4	VSS	ELV2P	-	ELV1P	-	-
D27		DB7	DB0	DB5	VSS	ELV2N	-	ELV1N	-	-
D10		DG0	DG7	VSS	DG5	ELVCLKP	-	ELVCLKP	-	-
D11		DG1	DG6	VSS	DG4	ELVCLKN	-	ELVCLKN	-	-
D12		DG2	DG5	DG0	DG3	ELV1P	-	ELV2P	-	-
D13		DG3	DG4	DG1	DG2	ELV1N	-	ELV2N	-	-
D14		DG4	DG3	DG2	DG1	ELV0P	-	ELV3P	-	-
D15		DG5	DG2	DG3	DG0	ELV0N	-	ELV3N	-	-
D16		DG6	DG1	DG4	VSS	OLV3P	OLV3P	OLV0P	OLV0P	-
D17		DG7	DG0	DG5	VSS	OLV3N	OLV3N	OLV0N	OLV0N	-
D00		DR0	DR7	VSS	DR5	OLV2P	OLV2P	OLV1P	OLV1P	OLV2P
D01		DR1	DR6	VSS	DR4	OLV2N	OLV2N	OLV1N	OLV1N	OLV2N
D02		DR2	DR5	DR0	DR3	OLVCLKP	OLVCLKP	OLVCLKP	OLVCLKP	OLVCLKP
D03		DR3	DR4	DR1	DR2	OLVCLKN	OLVCLKN	OLVCLKN	OLVCLKN	OLVCLKN
D04		DR4	DR3	DR2	DR1	OLV1P	OLV1P	OLV2P	OLV2P	OLV1P
D05		DR5	DR2	DR3	DR0	OLV1N	OLV1N	OLV2N	OLV2N	OLV1N
D06		DR6	DR1	DR4	VSS	OLV0P	OLV0P	OLV3P	OLV3P	OLV0P
D07		DR7	DR0	DR5	VSS	OLV0N	OLV0N	OLV3N	OLV3N	OLV0N
DCLK	TTL	CLK				-	-	-	-	-
HS		HS				-	-	-	-	-
VS		VS				-	-	-	-	-
DE		DE				-	-	-	-	-

Note: (1) In TTL 6-bit mode, unused pins should be connected to ground. Unused pins in other modes can be floating.
(2) When 6-bit mode selected, the data bits would be expanded to 8-bit in TCON circuit. Bit 1 is equal to Bit 7 and Bit 0 is equal to Bit 6.
(3) LVDS 6-bit mode doesn't support lane swap function.

Table 4.1: Interface pin connection

4.3. Recommended wiring resistance values

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pad type	Pad	Resistance
Power supply pins	VCC1	< 5Ω
	VCC1P	< 5Ω
	VSS1	< 5Ω
	VSS1P	< 5Ω
	VCC2	< 5Ω
	VSS2	< 3Ω
	VSSA	< 3Ω
	VCCIF	< 5Ω
	VSP	< 3Ω
	VSN	< 3Ω
	VDD_OTP	< 10Ω
Special function pins	TP_SYNC[2:1]	< 20Ω
	FAIL_DET	
	TEST4	
	TS_L	< 50Ω
	TS_H	
	GDETL[2:1]	< 10KΩ
	GDETR[2:1]	
Regulator output and reference input pins	VGMPHI/VGMPLI	< 20Ω
	VGMNHI/VGMNLI	
	VGMPHO/VGMPLO	
	VGMNHO/VGMNLO	
	VDDD	< 5Ω
	VCOM	< 30Ω
	VCL	< 10Ω
	VSDP	< 3Ω
	VSDN	< 3Ω
SPI/I2C pins	SPI_CSB	< 20Ω
	SPI_SCL	
	SPI_SDAI	
	SPI_SDAO	
	I2C_SDA	
	I2C_SCL	
Cascade pins	CA_R[2:0]	< 100Ω
	CA_R[6:4]	
	CA_L[2:0]	
	CA_L[6:4]	
	CA3	
	GIO_R[4:0]	
	GIO_L[4:0]	
	FCTRL_L	
	FCTRL_R	
	F_POL_LI	
	F_POL_RO	

Pad type	Pad	Resistance
Input interface pins	D0[7:0] D1[7:0] D2[7:0] DCLK	< 20Ω
	HS	
	VS	
	DE	
Input control pins	RESETB/ RESETB_SLP	< 50Ω
	STBYB	
	FCS	< 150Ω
	SID[1:0]	
	SIDEN	
	GSQ	
	ATREN	
	EXT_PWR	
	EEPEN	
	TR[1:0]	
	MODE	
	NB	
	RL	
	TB	
	GDSEL	
	INV[1:0]	
	RS[3:0]	
	GPOS[1:0]	
	BISTEN	
	ZZS[1:0]	
	PTS[2:0]	
	I2C_SPI_SEL	
	FMT	
	LANE_SW	
	LANE_PN	
Through pins	THROUGH_[4:1]	-
	VCOM_R	
	VCOM_L	
EEPROM	ECS	< 20Ω
	ESCL	
	ESDAI	
	ESDAO	
Charge pump and PFM pins	VGH	<10Ω
	VGL	
	CHP[3:1]	< 5Ω
	CHN[3:1]	
	CLP[2:1]	
	CLN[2:1]	
	VREGP/VREGN	< 5Ω
	DRVP/DRVN	< 5Ω
	VMONP/VMONN	< 20Ω

Table 4.2: Recommended wiring resistance values

4.4. Group 2 input pins vs. registers

The following settings can be chosen to be controlled by hardware input pin **(Group 2)** or by values in register Page00h and Page0Ch. When FCS is set to L, the chip is controlled by registers. Otherwise, the chip is controlled by hardware pin.

Pin name	Register address (Page00h)
GPOS[1:0]	Page00h R04h[5:4]
TR[1:0]	Page00h R02h[7:6]
MODE	Page00h R02h[4]
RL(1)	Page00h R03h[7]
TB(1)	Page00h R03h[6]
INV[1:0]	Page00h R03h[5:4]
RS[3:0]	Page00h R03h[3:0]
BISTEN(1)	Page00h R05h[4]
PTS[2:0]	Page00h R01h[6:4]
ZZS[1:0]	Page00h R01h[2:1]
GDSEL	Page00h R01h[0]
Pin name	**Register address (Page0Ch)**
FMT	Page0Ch R01h[4]
LANE_SW	Page0Ch R01h[3]
LANE_PN	Page0Ch R01h[2]

Note: (1) RL, TB, BISTEN function is the hardware setting “XOR” register setting when FCS=L.

Standby operation is controlled by hardware input pin STBYB and register STBYB_CMD **(Page00h R1Eh)** with “AND logic”.

FCS	Hardware pin STBYB	Register value STBYB_CMD (Page00h R1Eh)	Operation state
X	H	Not 55h	Operation
	L		Standby
X	H	Not 55h	Operation
		55h **(Default 00h)**	Standby

Table 4.3: Operation state of STBYB

RL, TB, BISTEN are controlled by hardware input pins and values in register Page00h. When FCS is set to L, the chip is controlled by both with “XOR logic”. Otherwise, the chip is controlled by hardware pin.

FCS	Hardware pin	Register value	Operation state
H	H	X	1
	L		0
L	H	1	0
		0	1
	L	1	1
		0	0

Table 4.4: Operation state of RL, TB and BISTEN

5. Panel Application

5.1. Display resolution configuration

16 typical resolutions are selected with RS[3:0]. Before panel development, it is necessary to confirm the panel RC load of all resolutions.

5.1.1. LTPS MUX1:1 / Single gate structure

The source drivers can be cascaded to support maximum resolution 1920xRGBx1080 with 4-chip, or 960xRGBx2560 with 2-chip.

Resolution		Setting	Source driver	
RGB (X)	Line (Y)	RS[3:0]	Chips cascaded (N)	Channels per chip
2560	960	0000	-	Not supported(1)
2400	900	0001	-	Not supported(1)
1920	1080	0010	4	1440
1920	720	0011	4	1440
1920	400	0100	4	1440
1600	320	0101	4	1200
1560	700	0110	4	1176 / 1176 / 1164 / 1164
1540	720	0111	4	1164 / 1152 / 1152 / 1152
1440	540	1000	3	1440
1280	720	1001	3	1284 / 1284 / 1272
1280	480	1010	3	1284 / 1284 / 1272
1280	400	1011	3	1284 / 1284 / 1272
960	2560	1100	2	1440
960	540	1101	2	1440
800	480	1110	2	1200
480	240	1111	1	1440

Note: (1) Hactive larger than 1920 is not supported.

5.1.2. LTPS MUX2:4 / Dual gate structure

The source drivers can be cascaded to support maximum resolution 2560xRGBx960 with 3-chip.

Resolution		Setting	Source driver	
RGB (X)	Line (Y)(1),(2)	RS[3:0]	Chips cascaded (N)	Channels per chip
2560	960	0000	3	1284 / 1278 / 1278
2400	900	0001	3	1200
1920	1080	0010	2	1440
1920	720	0011	2	1440
1920	400	0100	2	1440
1600	320	0101	2	1200
1560	700	0110	2	1170
1540	720	0111	2	1158 / 1152
1440	540	1000	2	1080
1280	720	1001	2	960
1280	480	1010	2	960
1280	400	1011	2	960
960	2560	1100	-	Not supported
960	540	1101	1	1440
800	480	1110	1	1200
480	240	1111	1	720

Note: (1) The Vactive lines must be even number.
(2) If GDSEL=L for GIP mode with dual gate structure, the Vactive must less than 2000 Line.

5.1.3. LTPS MUX2:6 / Triple gate structure

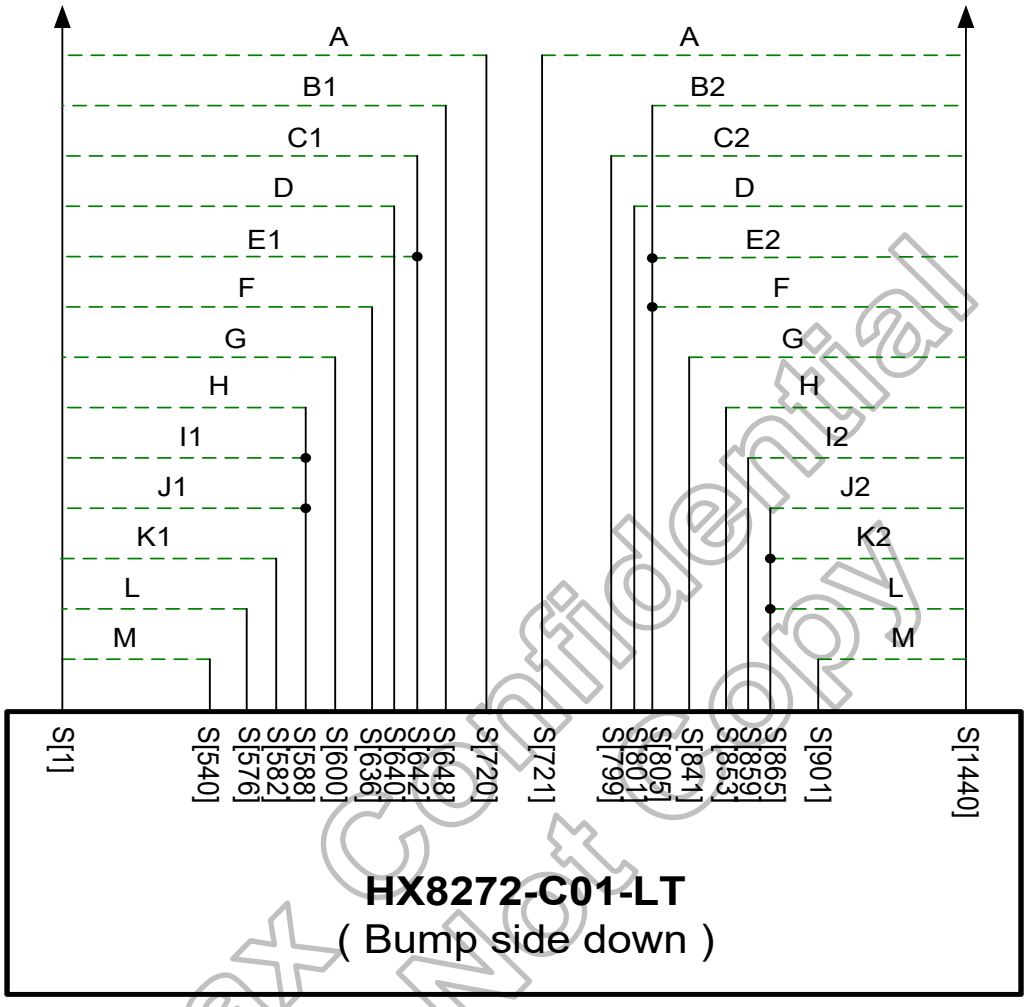
The source drivers can be cascaded to support maximum resolution 2560xRGBx960 with 2-chip.

Resolution		Setting	Source driver	
RGB (X)	Line (Y)(1)	RS[3:0]	Chips cascaded (N)	Channels per chip
2560	960	0000	2	1280
2400	900	0001	2	1200
1920	1080	0010	2	960
1920	720	0011	2	960
1920	400	0100	2	960
1600	320	0101	2	800
1560	700	0110	2	780
1540	720	0111	2	772 / 768
1440	540	1000	1	1440
1280	720	1001	1	1280
1280	480	1010	1	1280
1280	400	1011	1	1280
960	2560	1100	-	Not supported
960	540	1101	1	960
800	480	1110	1	800
480	240	1111	1	480

Note: (1) If GDSEL=L for GIP mode with triple gate structure, the Vactive must less than 1333 Line.

Table 5.1: Resolution table

5.2. Source output channel valid range



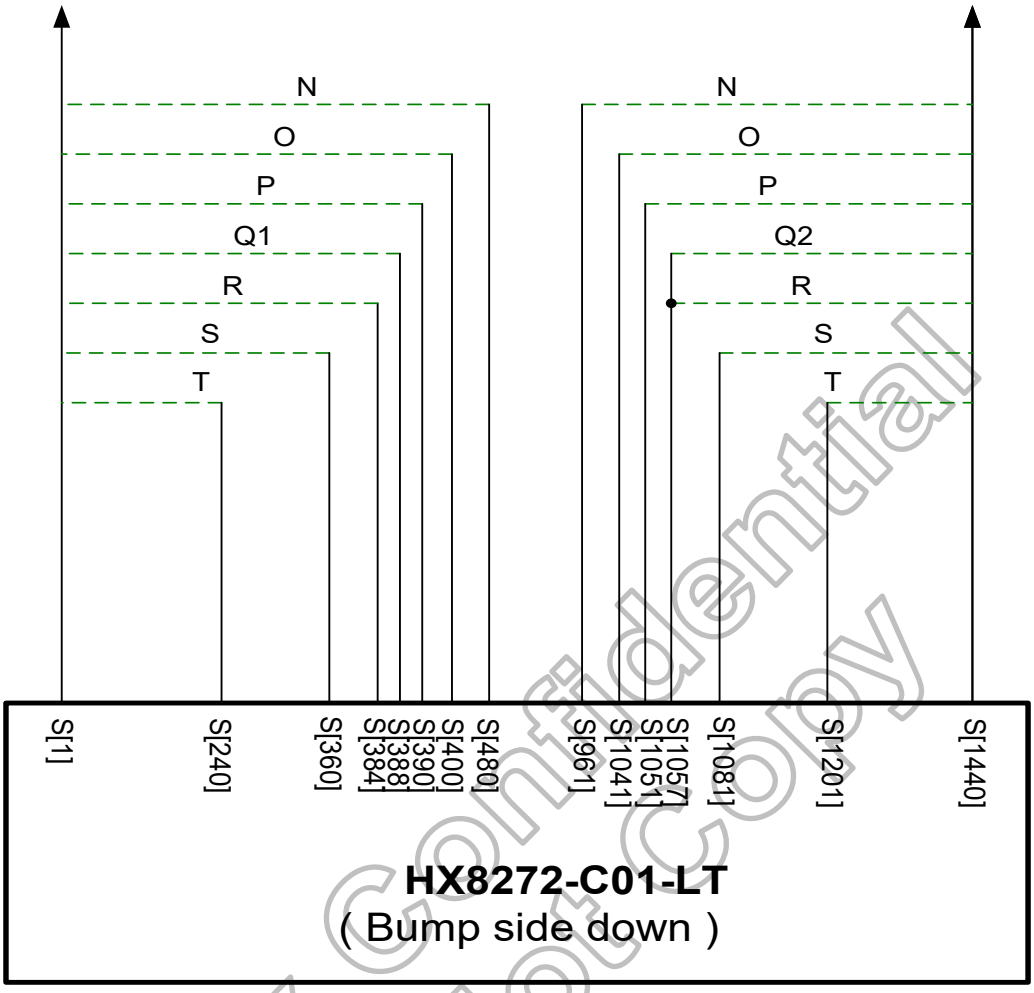


Figure 5.1: Valid source output

Channel			Valid source output	Note
A		1440	S[1]~S[720], S[721]~S[1440]	-
B1	B2	1284	S[1]~S[648], S[805]~S[1440]	MUX1:1 / Single gate
C1	C2	1284	S[1]~S[642], S[799]~S[1440]	MUX2:4 / Dual gate
D		1280	S[1]~S[640], S[801]~S[1440]	-
E1	E2	1278	S[1]~S[642], S[805]~S[1440]	-
F		1272	S[1]~S[636], S[805]~S[1440]	-
G		1200	S[1]~S[600], S[841]~S[1440]	-
H		1176	S[1]~S[588], S[853]~S[1440]	-
I1	I2	1170	S[1]~S[588], S[859]~S[1440]	-
J1	J2	1164	S[1]~S[588], S[865]~S[1440]	-
K1	K2	1158	S[1]~S[582], S[865]~S[1440]	-
L		1152	S[1]~S[576], S[865]~S[1440]	-
M		1080	S[1]~S[540], S[901]~S[1440]	-
N		960	S[1]~S[480], S[961]~S[1440]	-
O		800	S[1]~S[400], S[1041]~S[1440]	-
P		780	S[1]~S[390], S[1051]~S[1440]	-
Q1	Q2	772	S[1]~S[388], S[1057]~S[1440]	-
R		768	S[1]~S[384], S[1057]~S[1440]	-
S		720	S[1]~S[360], S[1081]~S[1440]	-
T		480	S[1]~S[240], S[1201]~S[1440]	-

Table 5.2: Valid source output table

5.3. Cascade connection

5.3.1. Driver arrangement on panel

The below pictures show how source drivers and gate drivers are located on panel. “X” represents output channels per chip.

5.3.1.1. MUX1:1 application

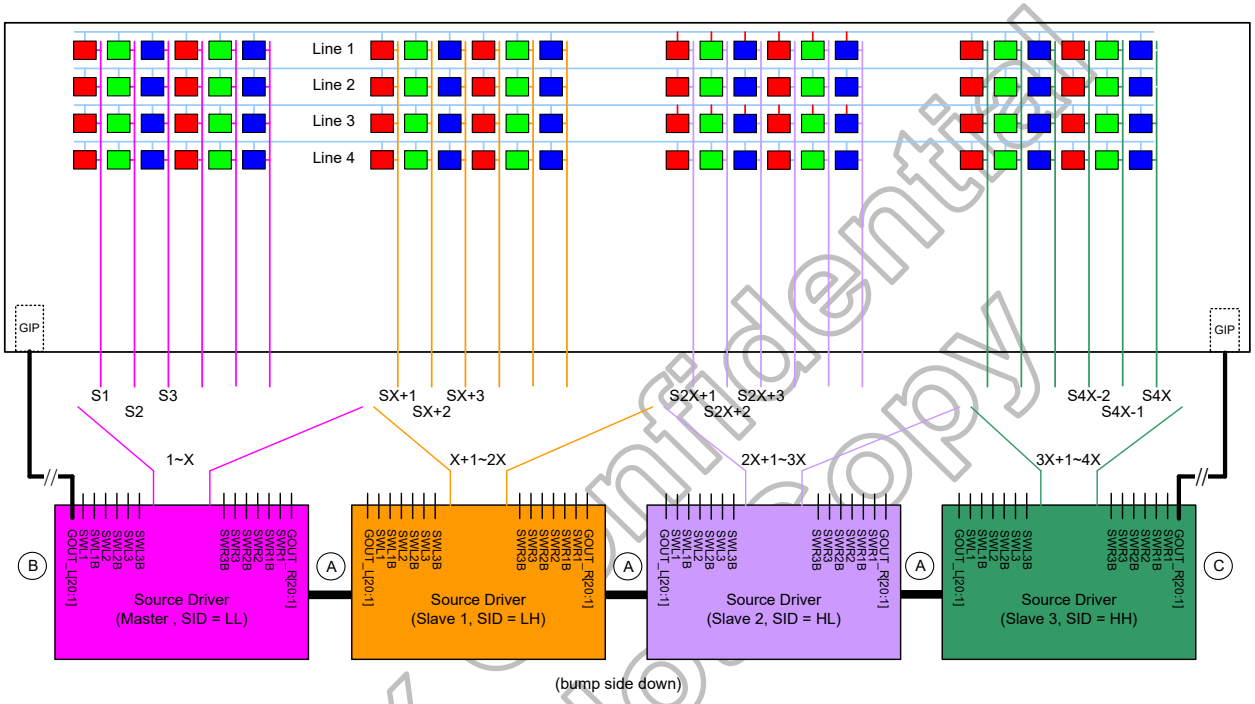


Figure 5.2: MUX1:1 application for Stripe panel (ZZS[1:0]=LL/HH)

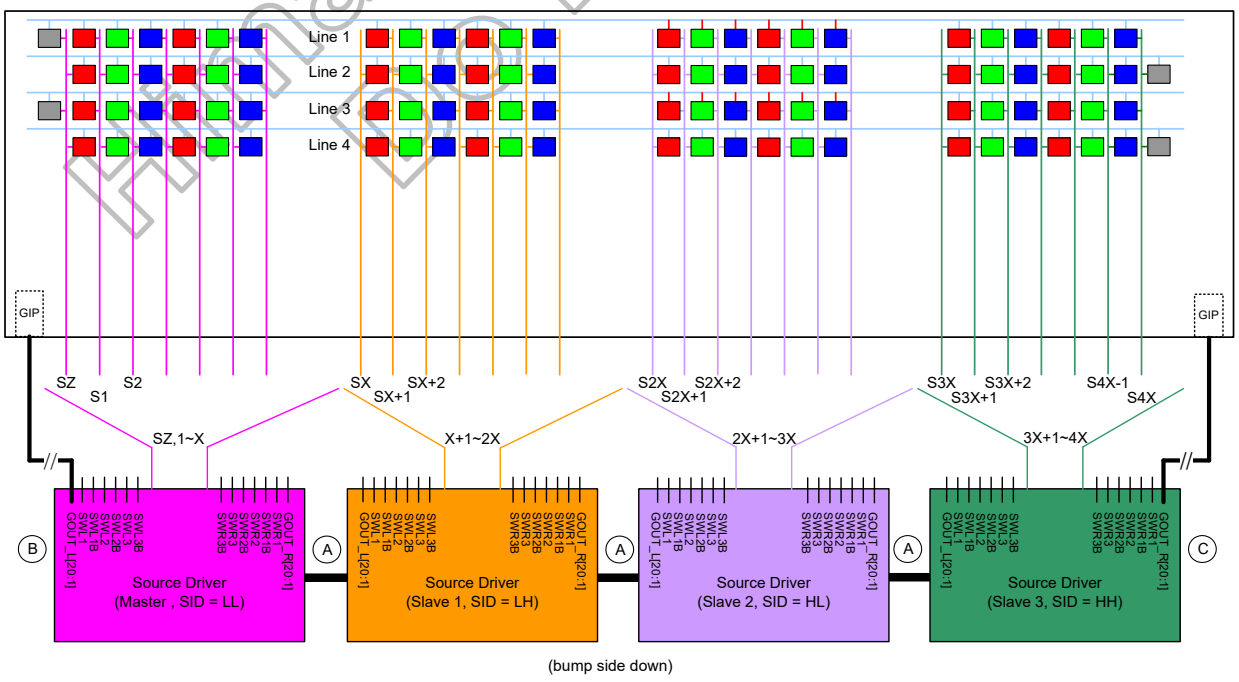


Figure 5.3: MUX1:1 application for Zig-Zag Type 1 panel (ZZS[1:0]=LH)

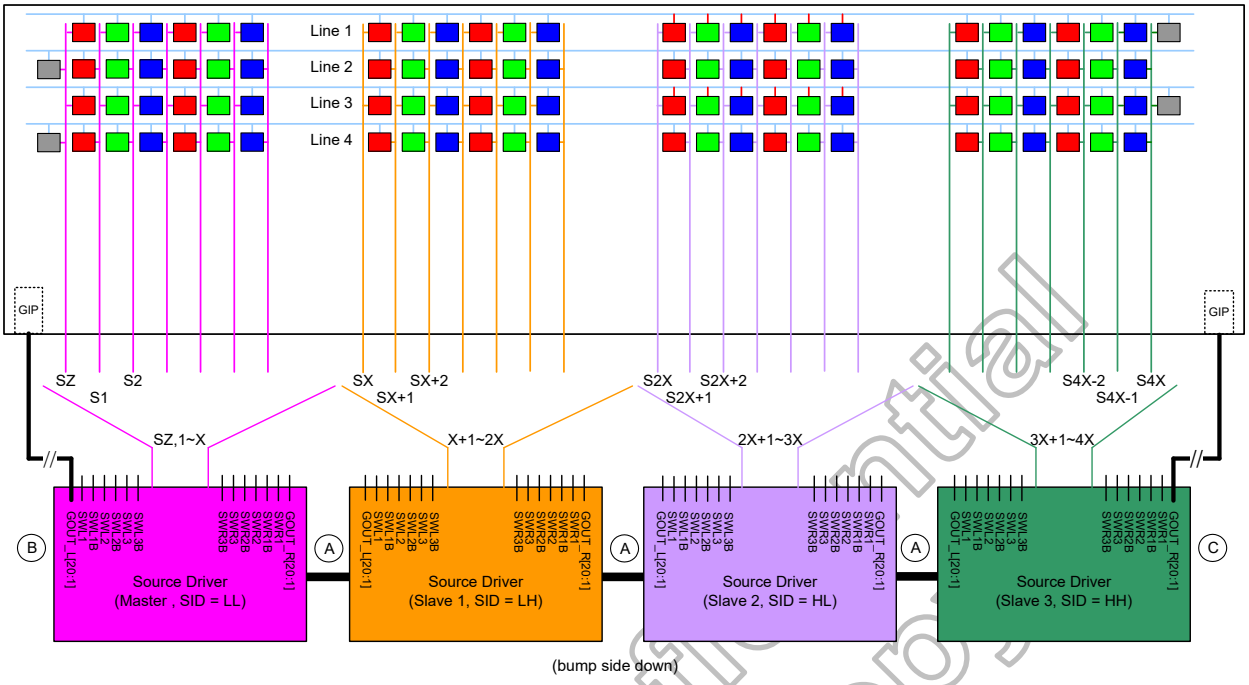


Figure 5.4: MUX1:1 application for Zig-Zag Type 2 panel (ZZS[1:0]=HL)

5.3.1.2. MUX2:4 application

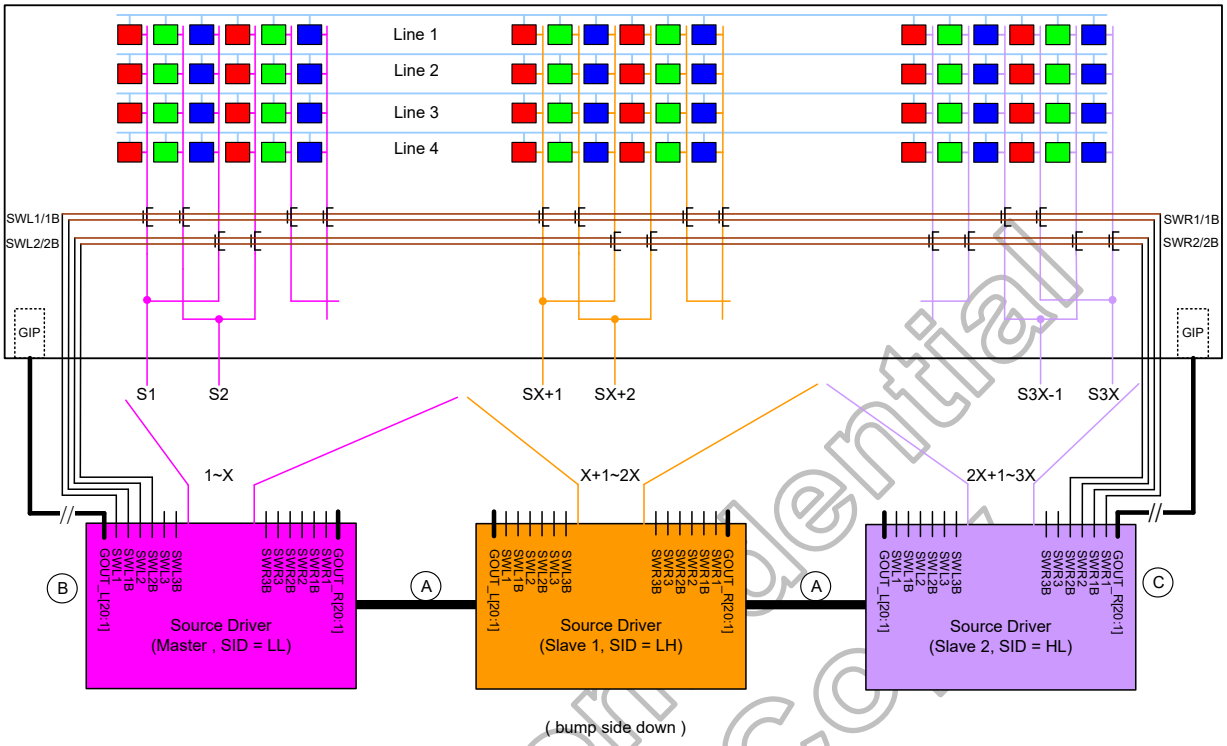


Figure 5.5: MUX2:4 application for Stripe panel (ZZS[1:0]=LL/HH)

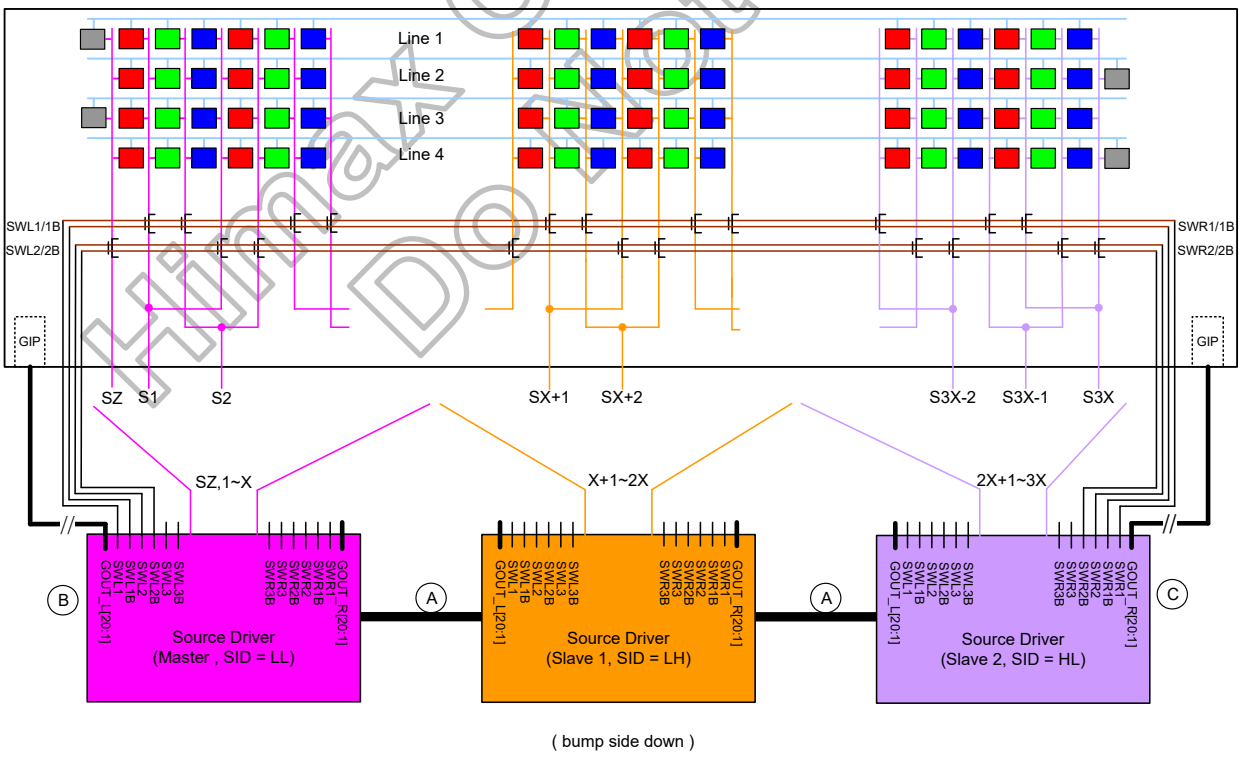


Figure 5.6: MUX2:4 application for Zig-Zag Type 1 panel (ZZS[1:0]=LH)

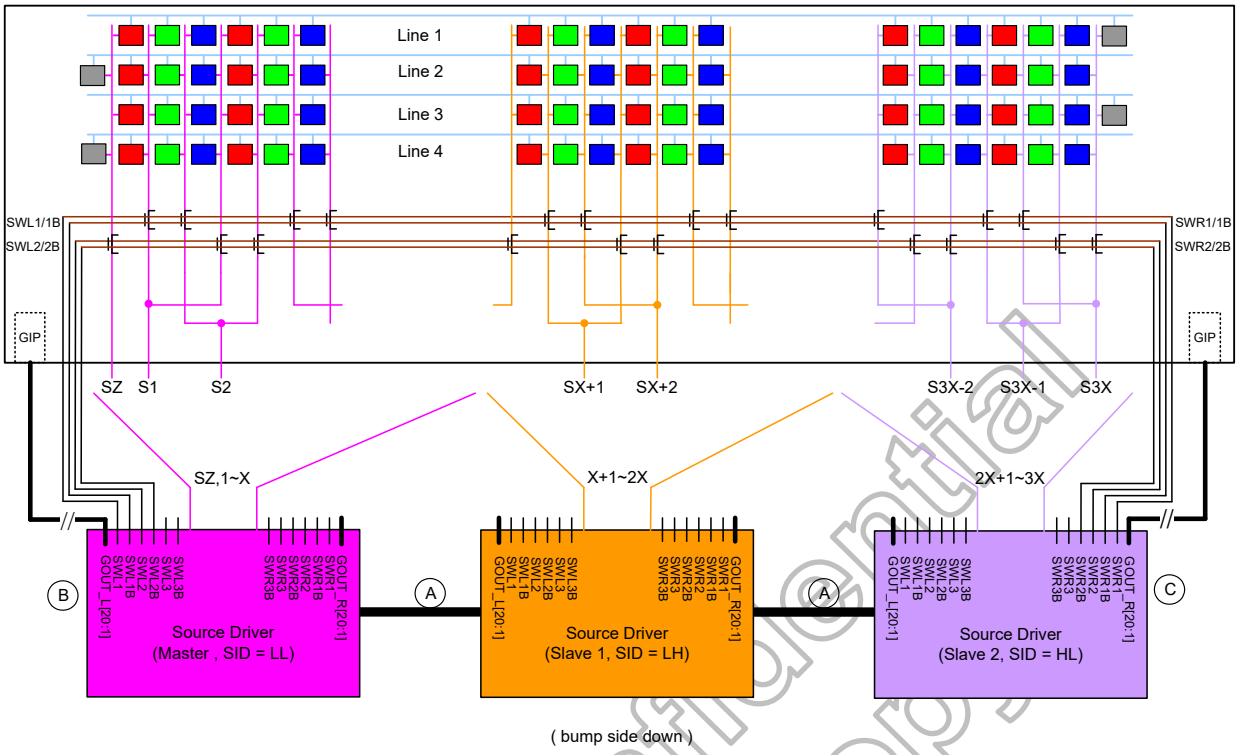


Figure 5.7: MUX2:4 application for Zig-Zag Type 2 panel (ZZS[1:0]=HL)

5.3.1.3. MUX2:6_Type 1 application

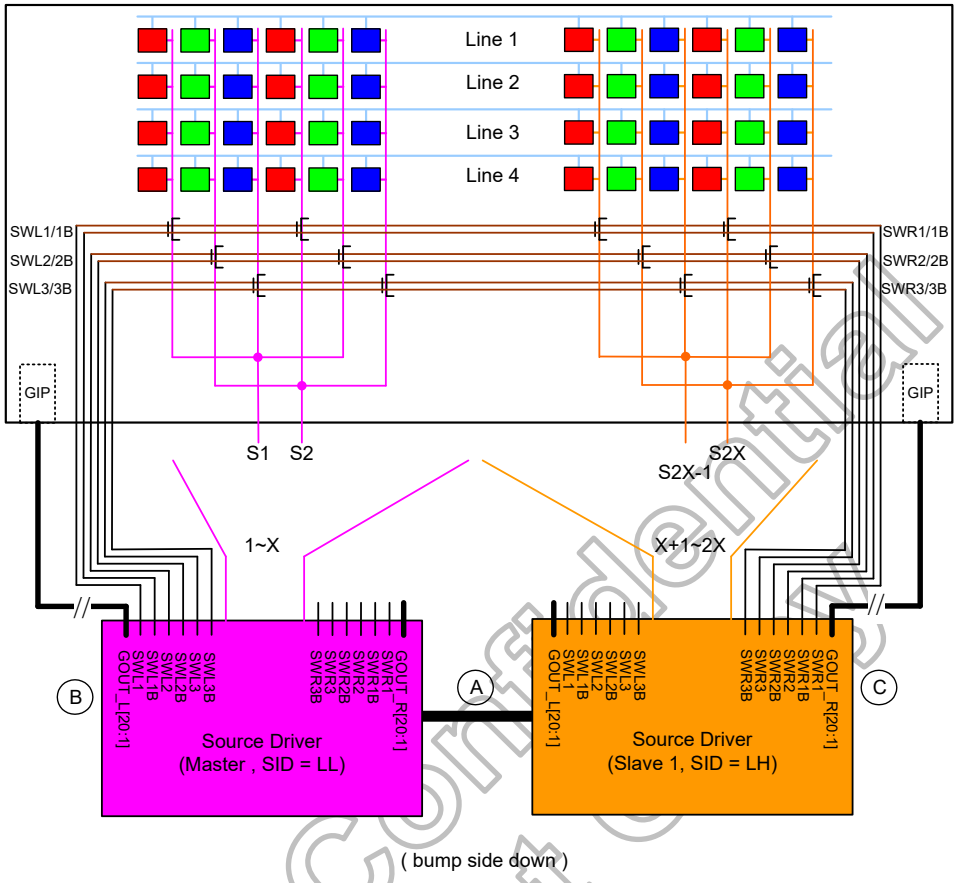


Figure 5.8: MUX2:6_Type 1 application for Stripe panel (ZZS[1:0]=LL/HH & PTS[2:0]=LLH)

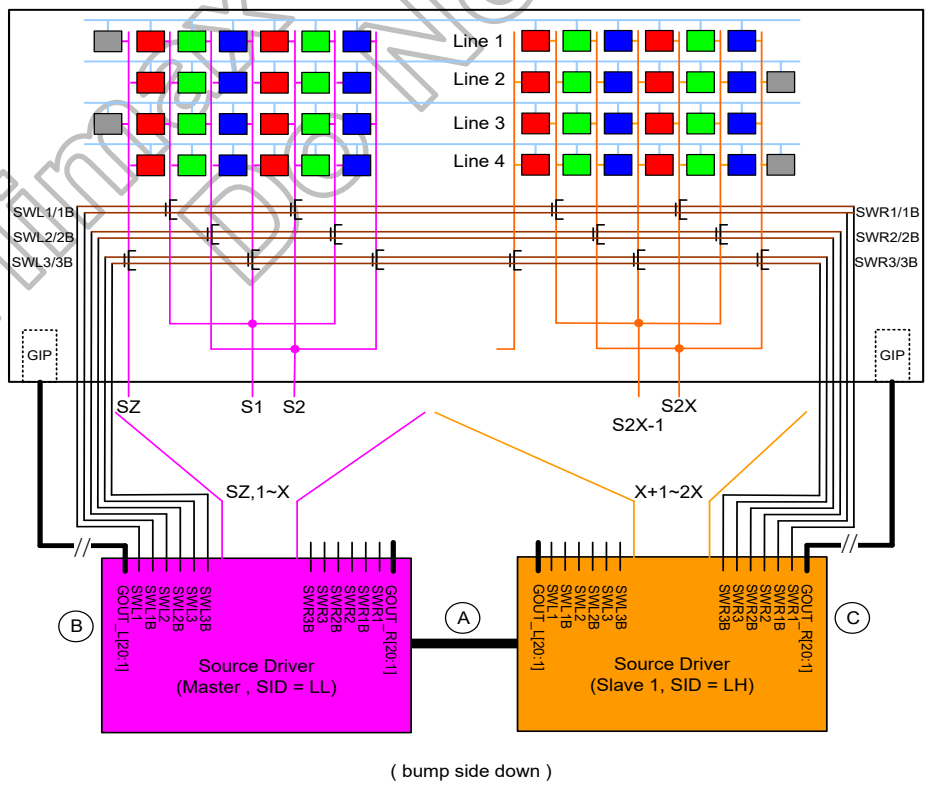


Figure 5.9: MUX2:6_Type 1 application for Zig-Zag Type 1 panel (ZZS[1:0]=LH & PTS[2:0]=LLH)

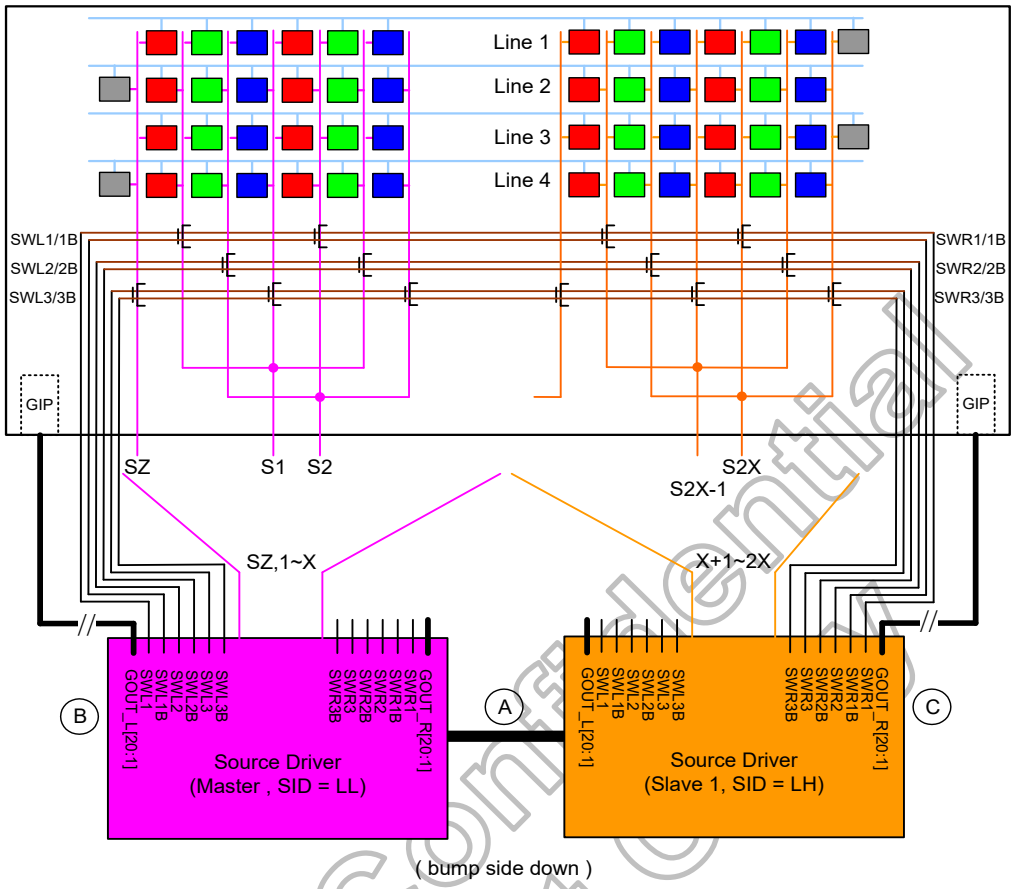


Figure 5.10: MUX2:6_Type 1 application for Zig-Zag Type 2 panel (ZZS[1:0]=HL & PTS[2:0]=LLH)

5.3.1.4. MUX2:6_Type 2 application

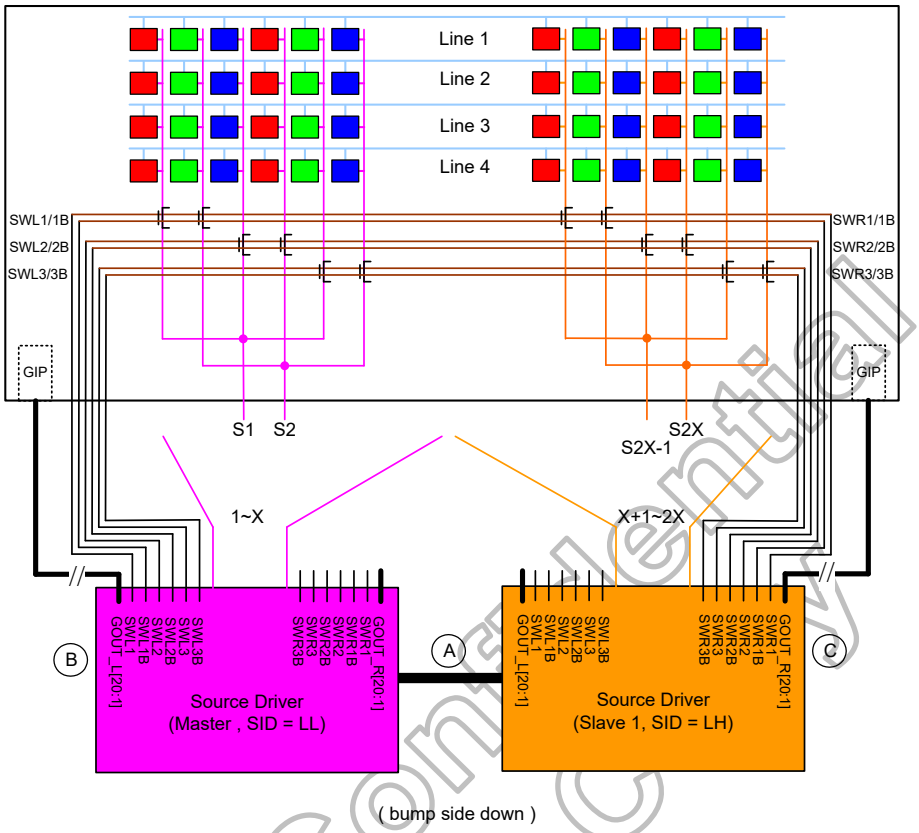


Figure 5.11: MUX2:6_Type 2 application for Stripe panel (ZZS[1:0]=LL/HH & PTS[2:0]=LHL)

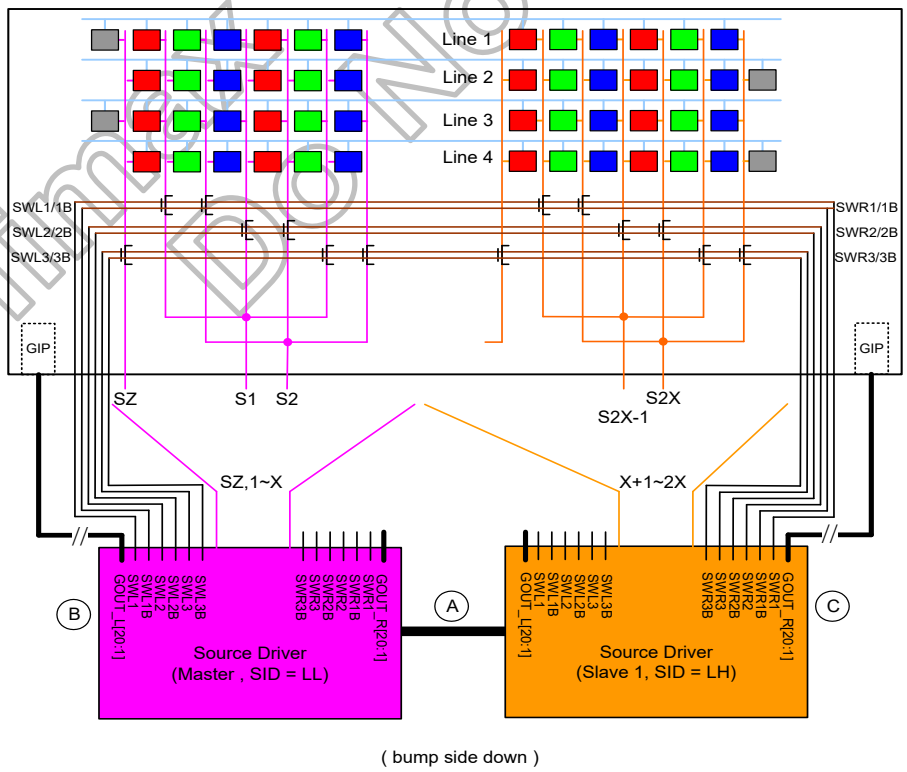


Figure 5.12: MUX2:6_Type 2 application for Zig-Zag Type 1 panel (ZZS[1:0]=LH & PTS[2:0]=LHL)

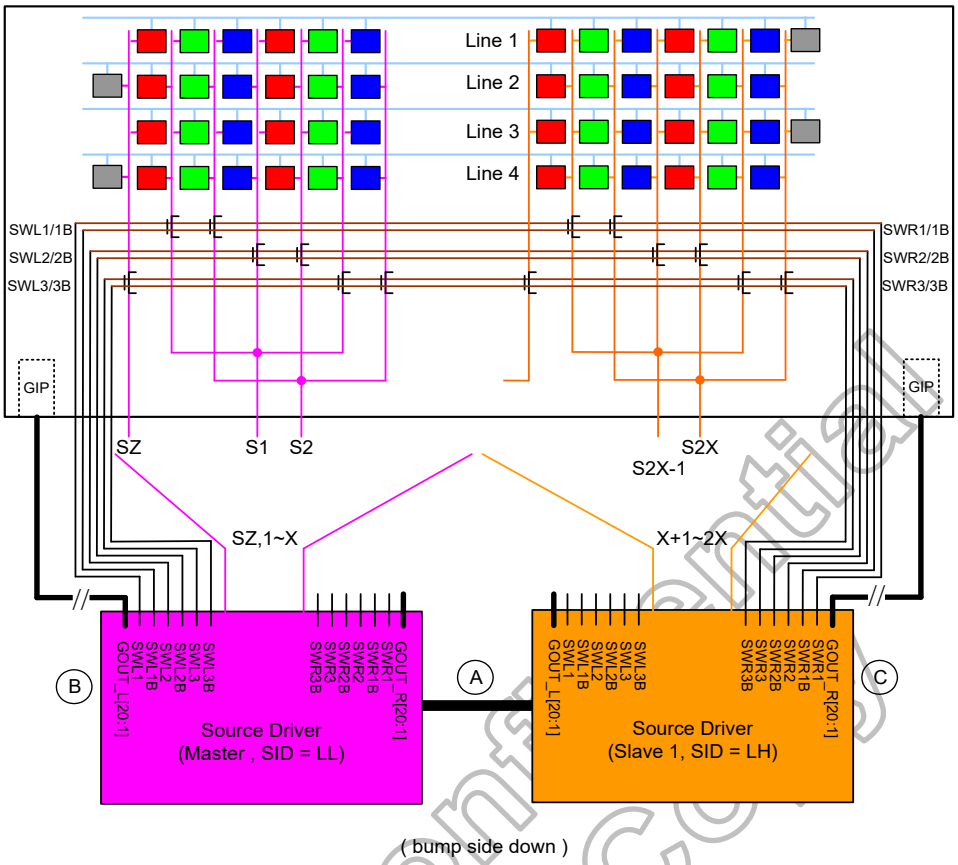


Figure 5.13: MUX2:6_Type 2 application for Zig-Zag Type 2 panel (ZZS[1:0]=HL & PTS[2:0]=LHL)

5.3.1.5. Single gate application

A. Set PTS[2:0]=LHH for single gate application and ZZS[1:0]=LL for stripe panel.

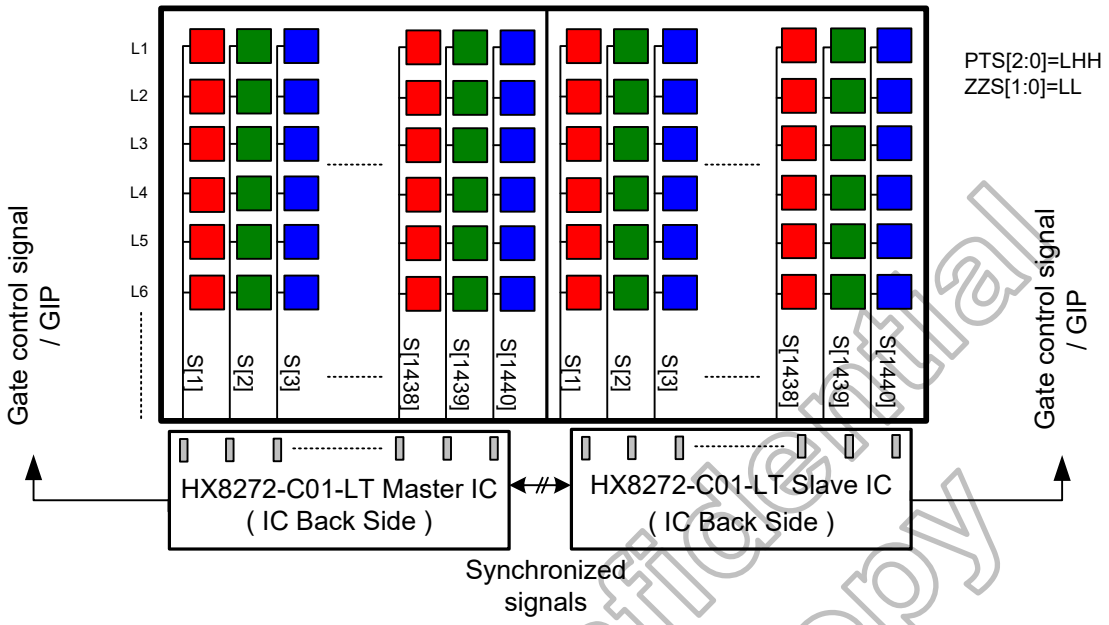


Figure 5.14: Single gate with Stripe panel application

B. Set PTS[2:0]=LHH for single gate application and ZZS[1:0]=LH for Zig-Zag Type 1 panel.

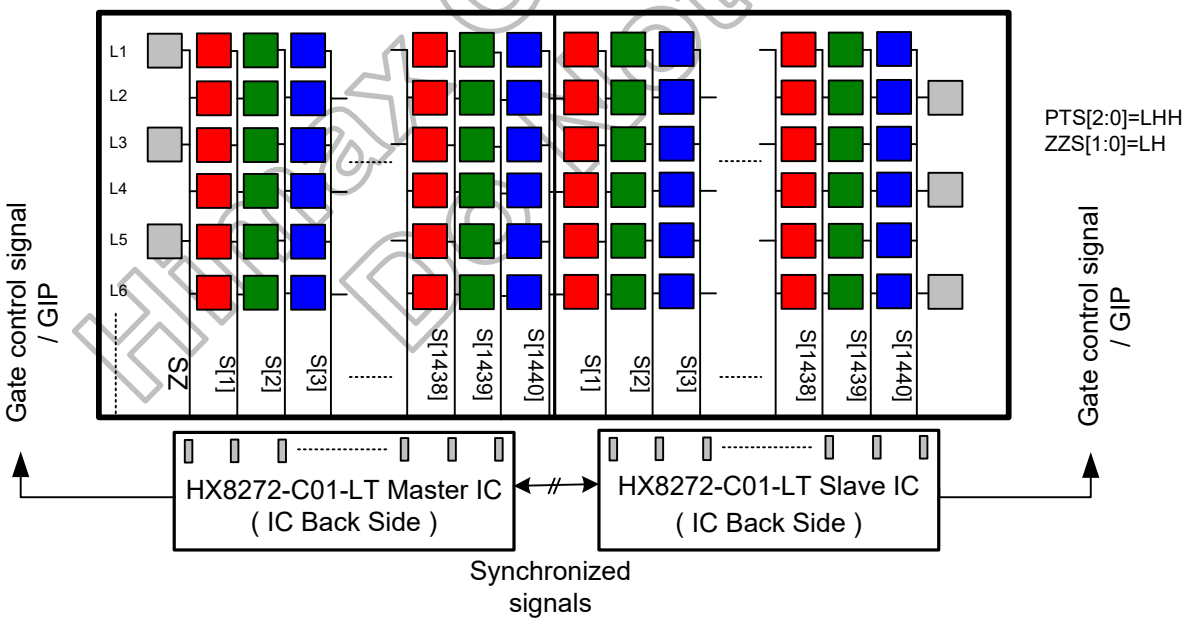


Figure 5.15: Single gate with Zig-Zag Type 1 panel application

C. Set PTS[2:0]=LHH for single gate application and ZZS[1:0]=HL for Zig-Zag Type 2 panel.

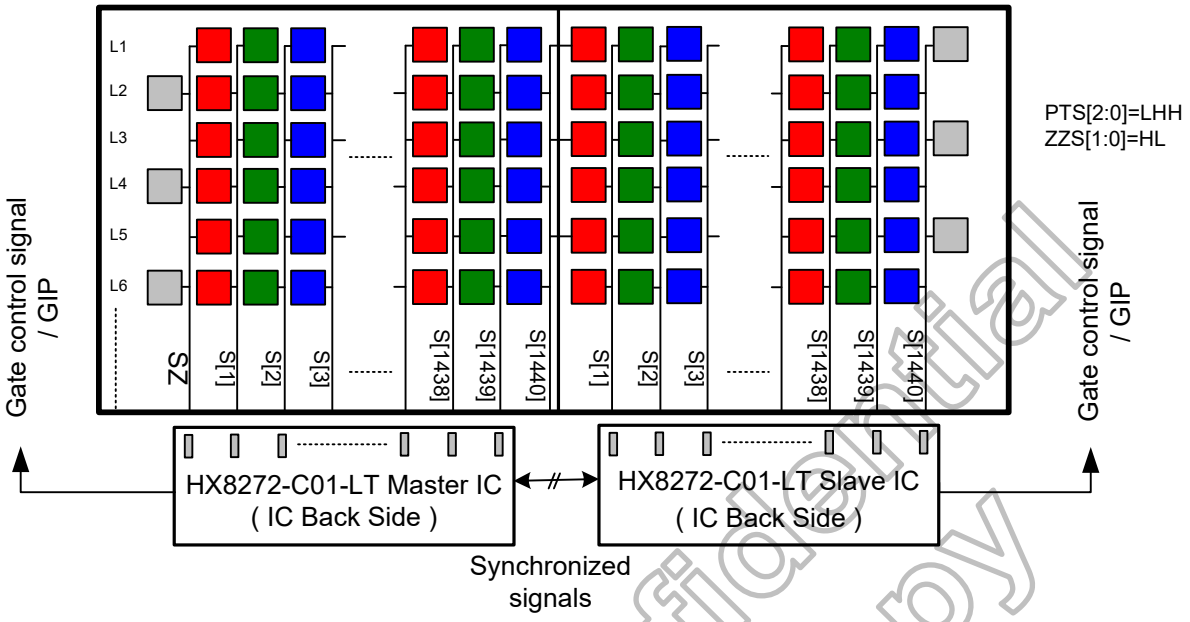


Figure 5.16: Single gate with Zig-Zag Type 2 panel application

5.3.1.6. Dual gate Type 1 application

A. Set PTS[2:0]=HLL for dual gate Type 1 application and ZZS[1:0]=LL for stripe panel.

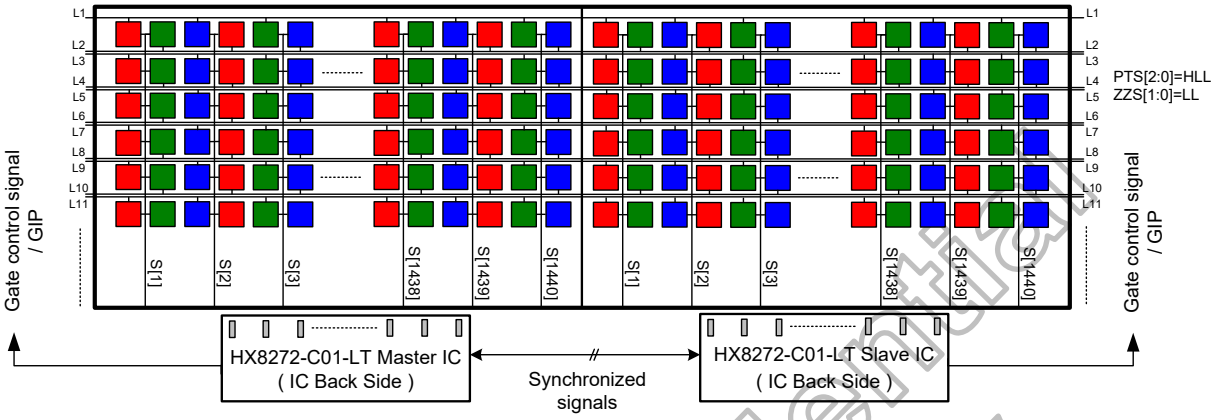


Figure 5.17: Dual gate Type 1 with stripe panel application

B. Set PTS[2:0]=HLL for dual gate Type 1 application and ZZS[1:0]=LH for Zig-Zag Type 1 panel.

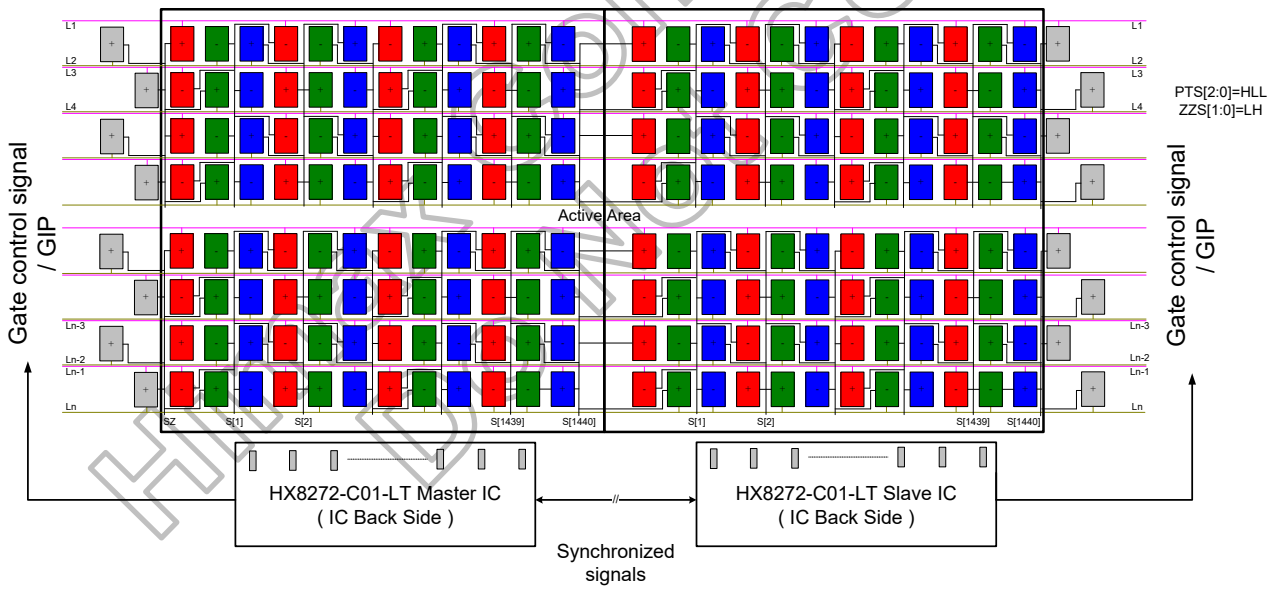


Figure 5.18: Dual gate Type 1 with Zig-Zag Type 1 panel application

C. Set PTS[2:0]=HLL for dual gate Type 1 application and ZZS[1:0]=HL for Zig-Zag Type 2 panel.

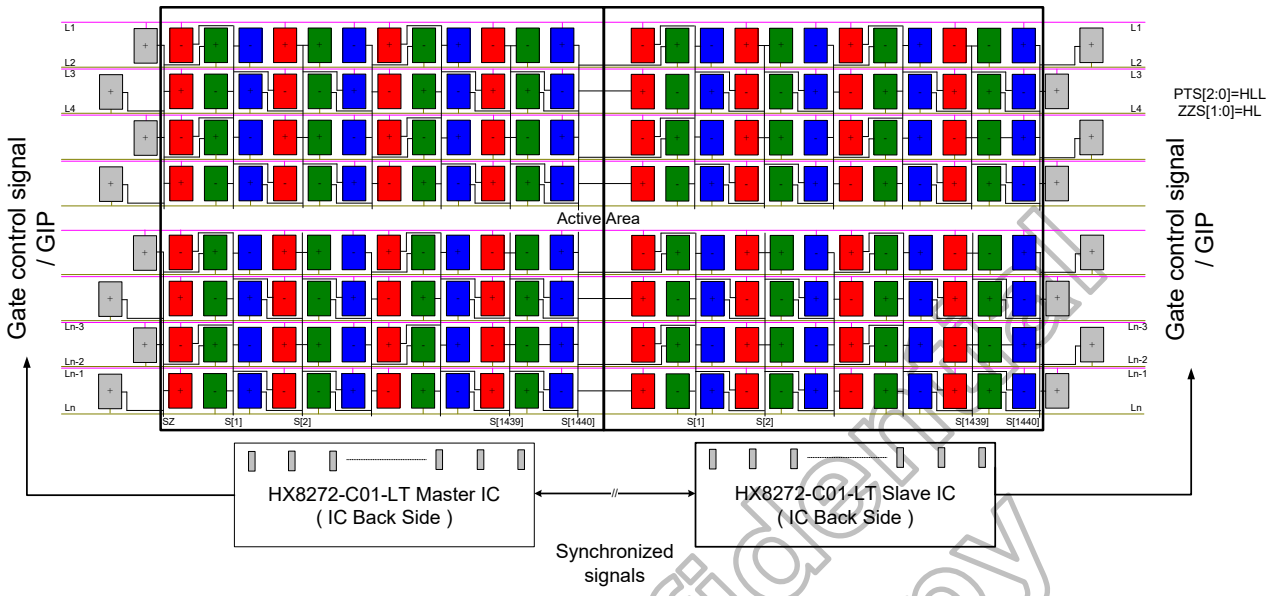


Figure 5.19: Dual gate Type 1 with Zig-Zag Type 2 panel application

5.3.1.7. Dual gate Type 2 application

A. Set PTS[2:0]=HHL for dual gate Type 2 application and ZZS[1:0]=LL for stripe panel.

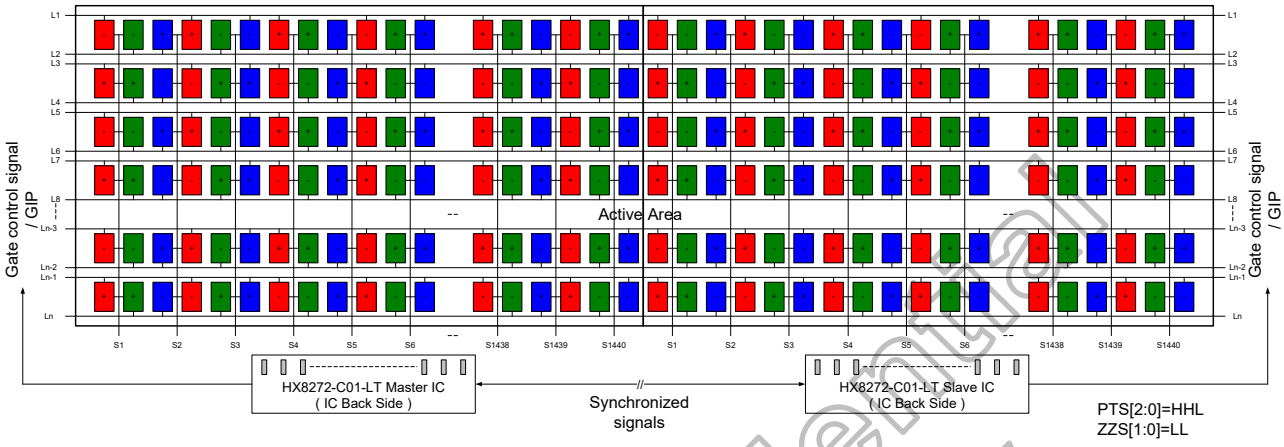


Figure 5.20: Dual gate Type 2 with stripe panel application

B. Set PTS[2:0]=HHL for dual gate Type 2 application and ZZS[1:0]=LH for Zig-Zag Type 1 panel. **(DUAL_ZZ_SEL=0)**

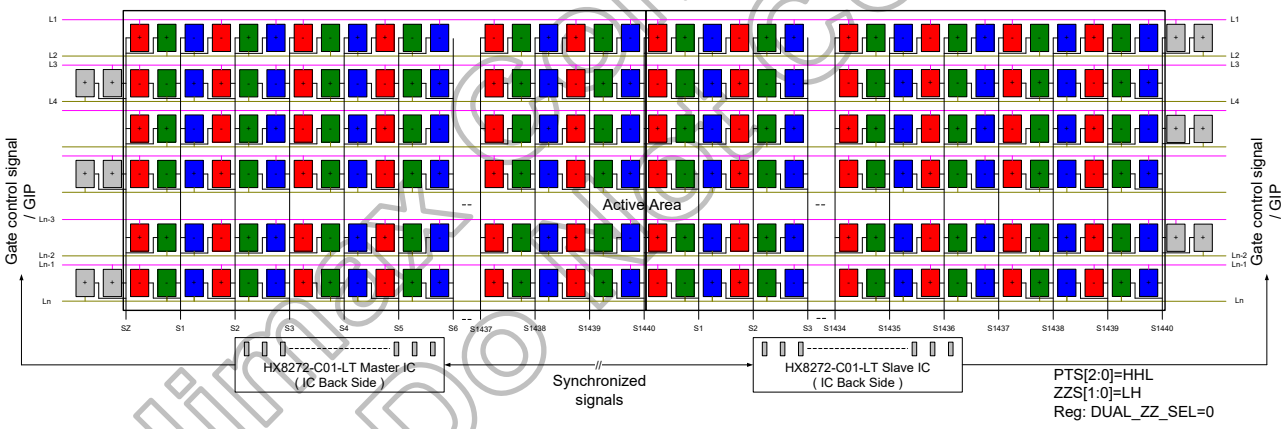


Figure 5.21: Dual gate Type 2 with Zig-Zag Type 1 panel application (DUAL_ZZ_SEL=0)

C. Set PTS[2:0]=HHL for dual gate Type 2 application and ZZS[1:0]=HL for Zig-Zag Type 2 panel. **(DUAL_ZZ_SEL=0)**

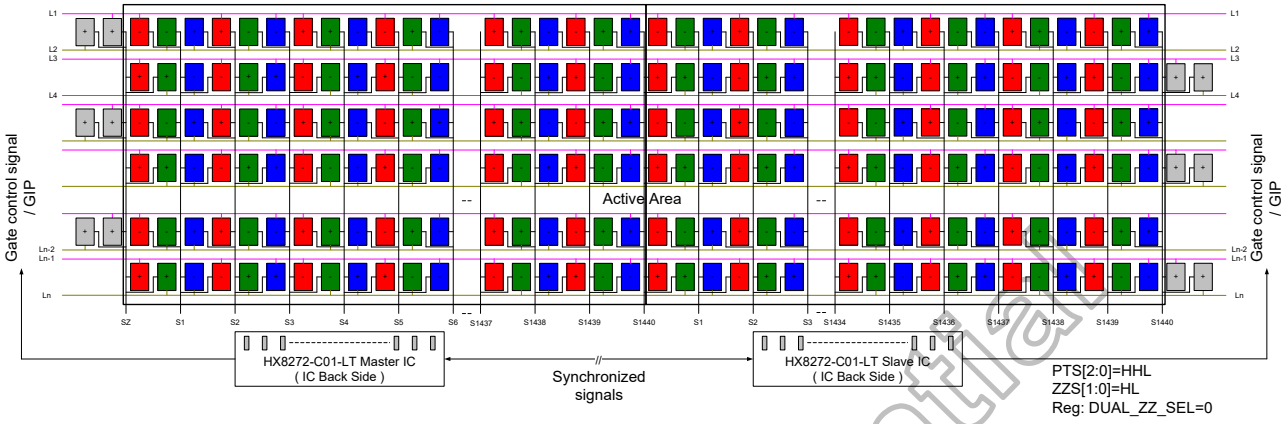


Figure 5.22: Dual gate Type 2 with Zig-Zag Type 2 panel application (DUAL_ZZ_SEL=0)

D. Set PTS[2:0]=HHL for dual gate Type 2 application and ZZS[1:0]=LH for Zig-Zag Type 1 panel. **(DUAL_ZZ_SEL=1)**

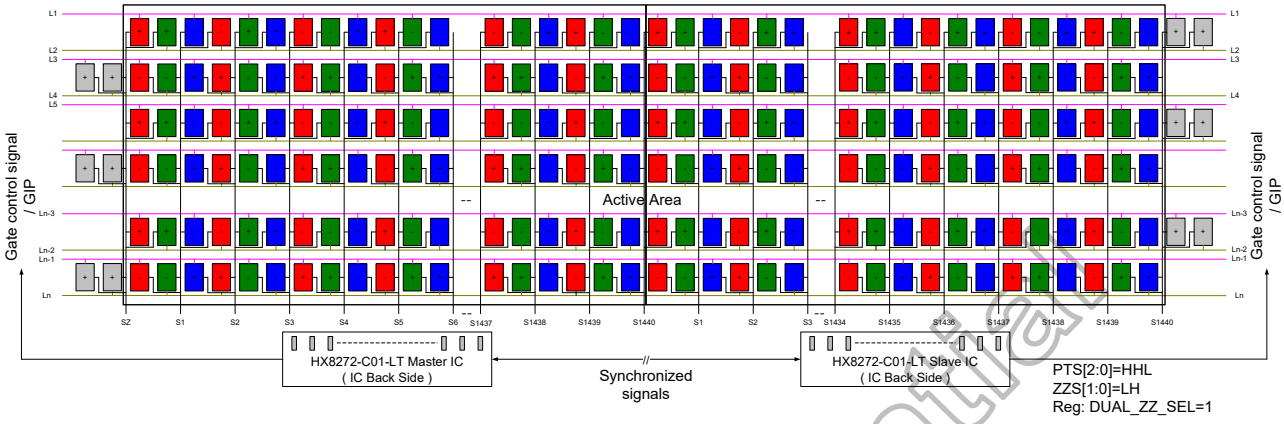


Figure 5.23: Dual gate Type 2 with Zig-Zag Type 1 panel application (DUAL_ZZ_SEL=1)

E. Set PTS[2:0]=HHL for dual gate Type 2 application and ZZS[1:0]=HL for Zig-Zag Type 2 panel. **(DUAL_ZZ_SEL=1)**

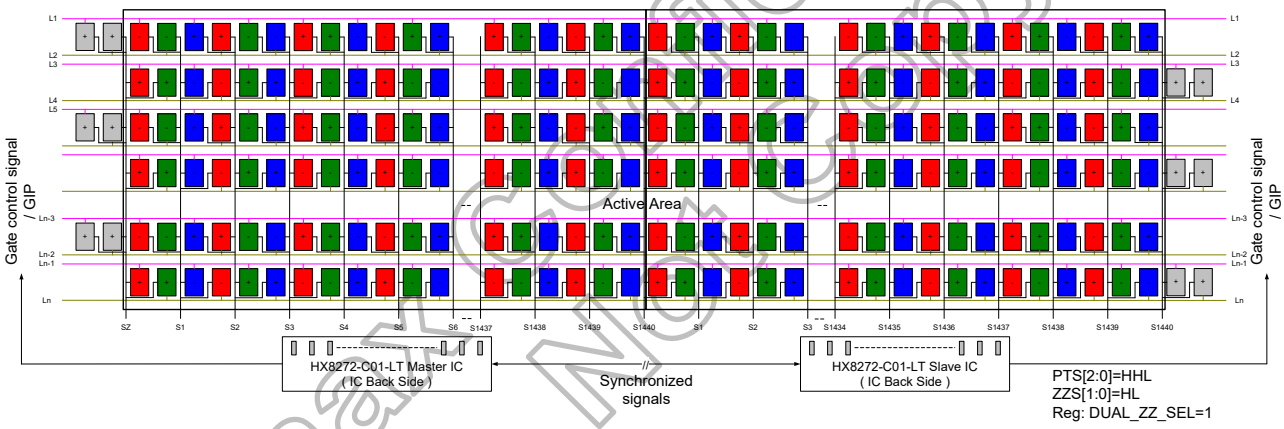


Figure 5.24: Dual gate Type 2 with Zig-Zag Type 2 panel application (DUAL_ZZ_SEL=1)

5.3.1.8. Dual gate Type 3 application

Dual gate Type 3 support Zig-Zag Type panel application only.

A. Set PTS[2:0]=HHH for dual gate Type 3 application and ZZS[1:0]=LH for Zig-Zag Type 1 panel.

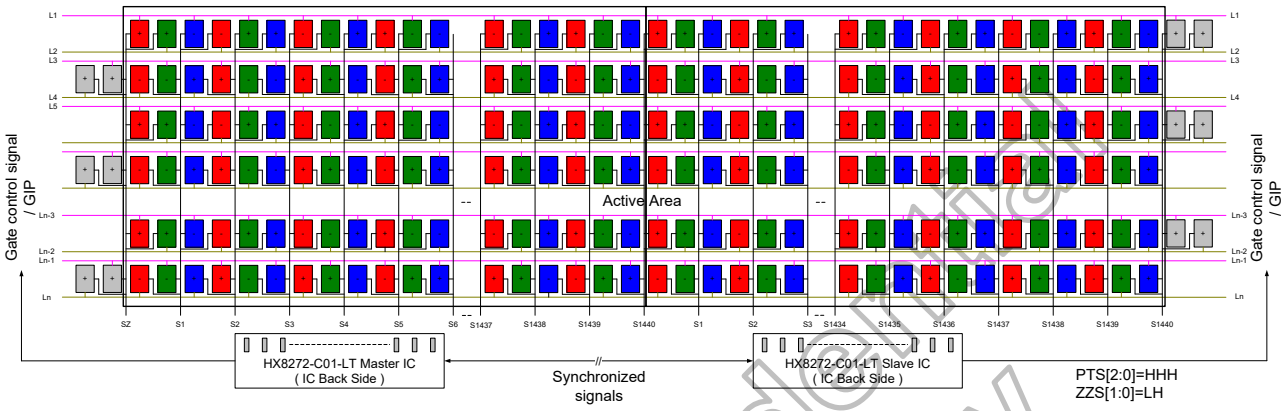


Figure 5.25: Dual gate Type 3 with Zig-Zag Type 1 panel application

B. Set PTS[2:0]=HHH for dual gate Type 3 application and ZZS[1:0]=HL for Zig-Zag Type 2 panel.

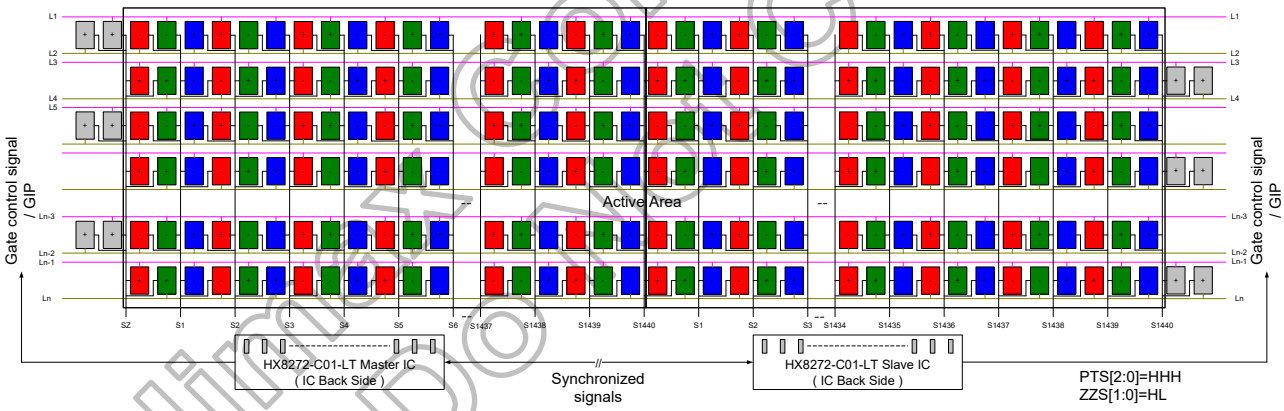


Figure 5.26: Dual gate Type 3 with Zig-Zag Type 2 panel application

5.3.1.9. Triple gate application

A. Set PTS[2:0]=HLH for triple gate application and ZZS[1:0]=LL for stripe panel.

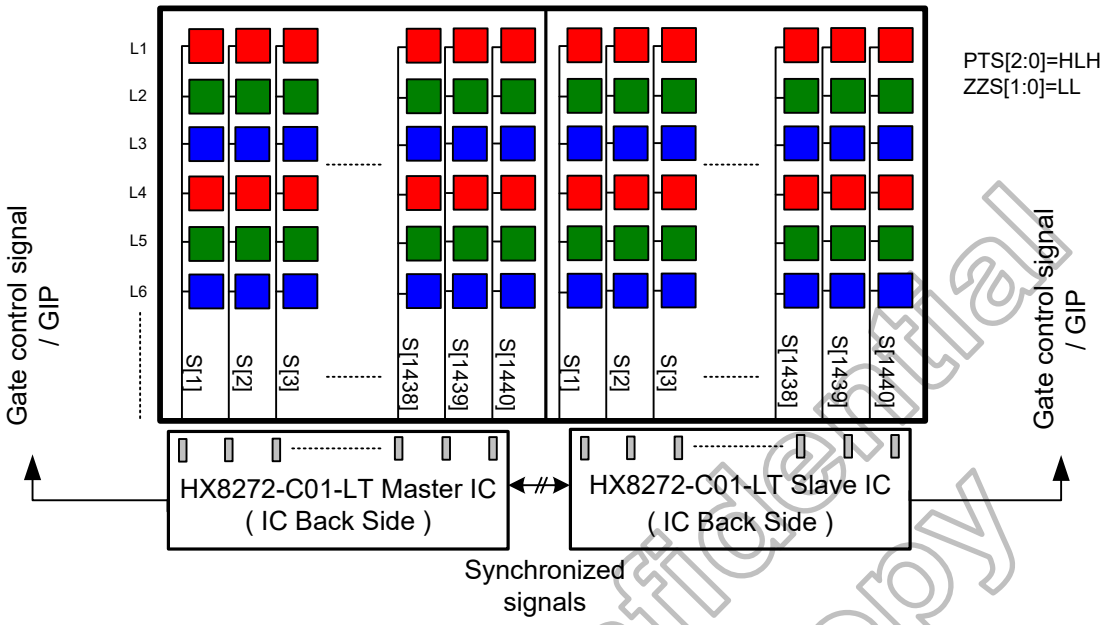


Figure 5.27: Triple gate with stripe panel application

B. Set PTS[2:0]=HLH for triple gate application and ZZS[1:0]=LH for Zig-Zag Type 1 panel.

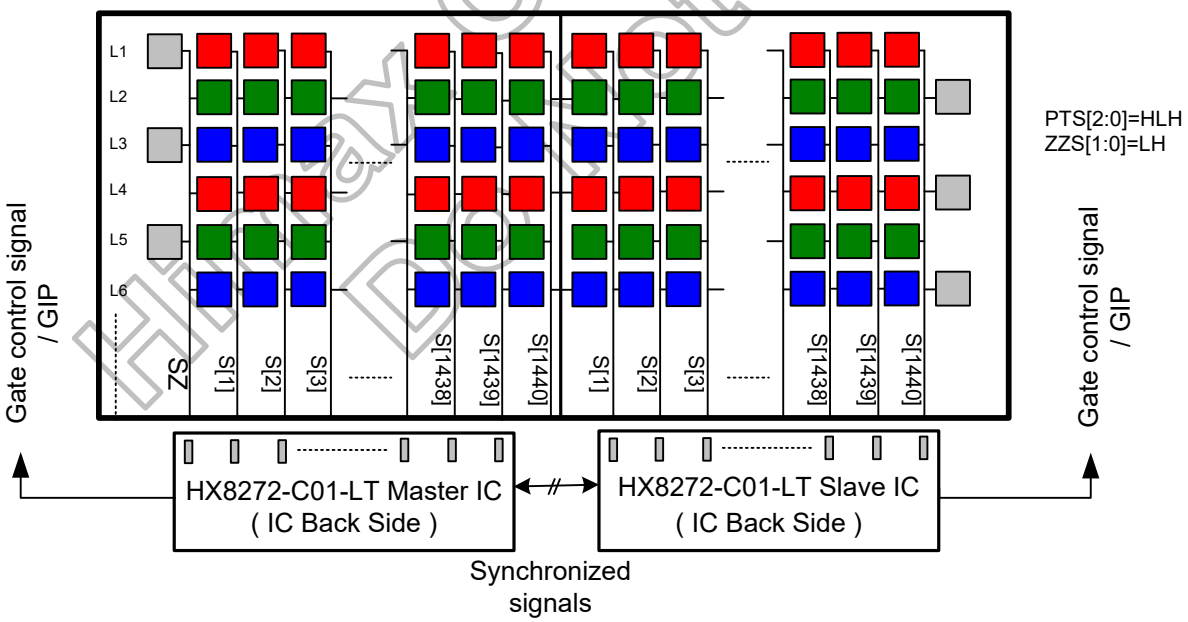


Figure 5.28: Triple gate with Zig-Zag Type 1 panel application

C. Set PTS[2:0]=HLH for triple gate application and ZZS[1:0]=HL for Zig-Zag Type 2 panel.

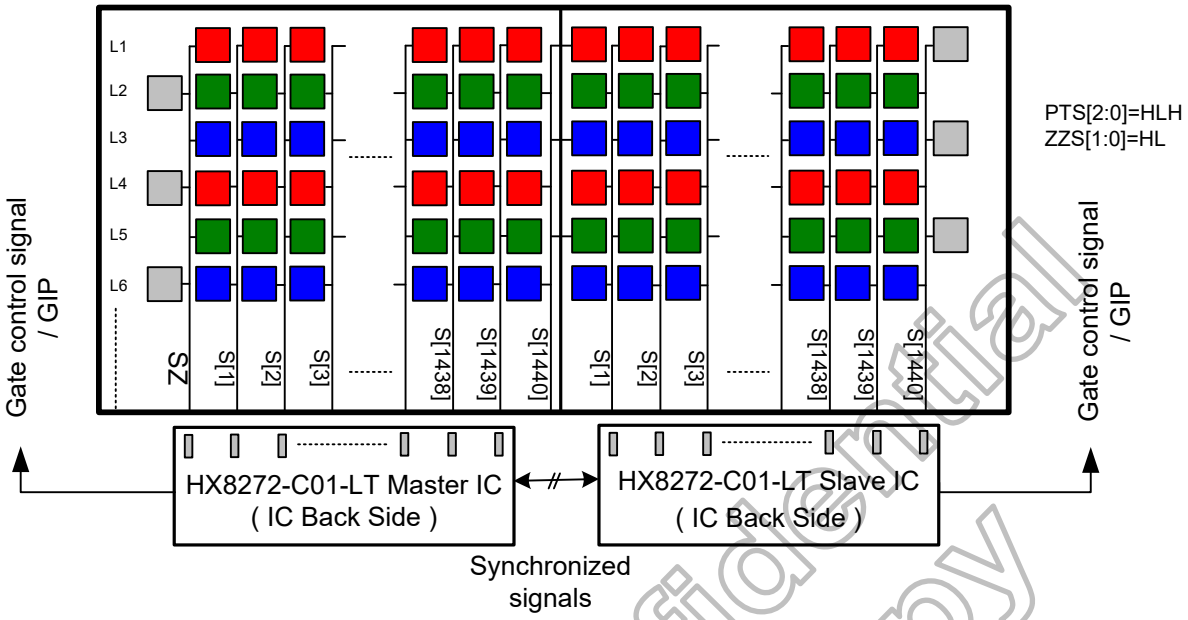


Figure 5.29: Triple gate with Zig-Zag Type 2 panel application

5.3.2. Cascade and gate driver control interface

A. Connections to the gate driver**(s)** depend on the type of the gate driver**(s)**. Refer to "Gate driver type definition".
B. Between each source drivers, it is must connect all of the side pins **(Case C)**.
C. Leave all of the side pins of the master chip floating if the gate driver**(s)** is at the right side **(Case D)**. Leave all of the side pins of the last slave chip floating if the gate driver**(s)** is at the left side **(Case E)**.

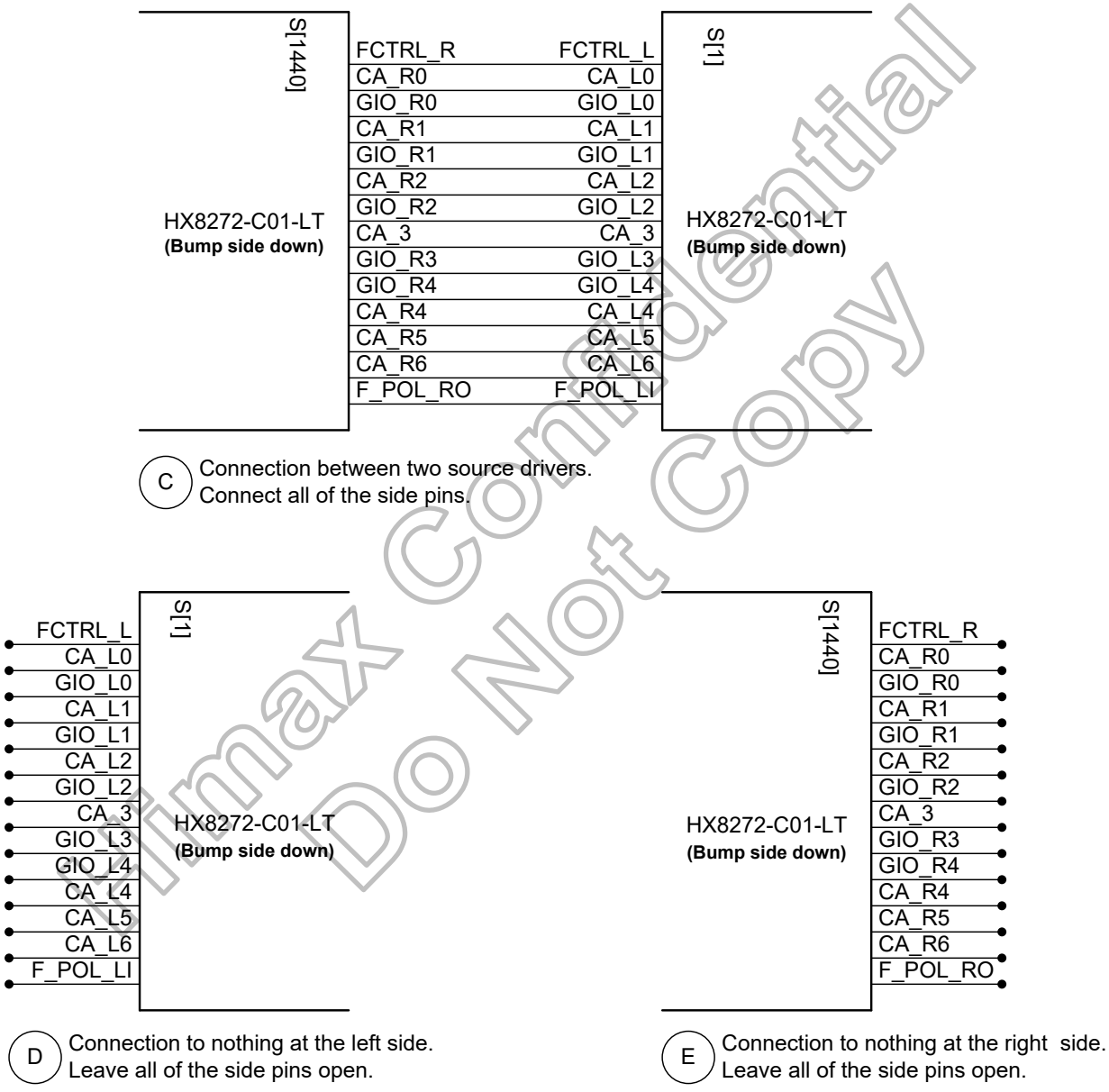


Figure 5.30: Cascade and gate driver control interface

5.3.3. Gate driver type definition

Two type sequences of gate driver control pins are supported.

A. Type 1

GSQ should be set to 0 when using this type of gate driver, such as HX8660-B-LT, HX8677-C-LT and HX8678-A-LT. Note that CA_L2 and CA_R2 pins are used as up/down control.

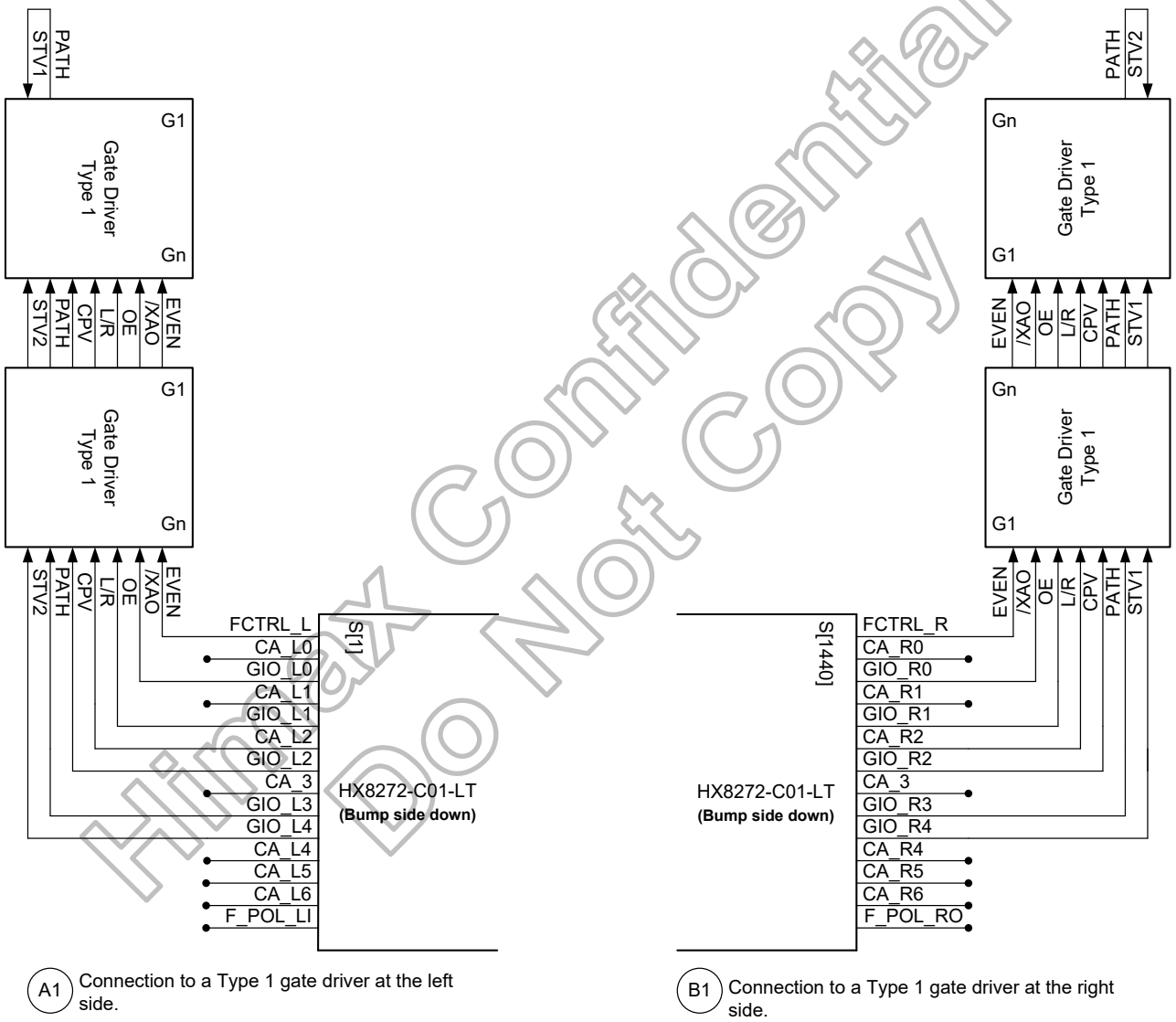


Figure 5.31: Gate control interface for Type 1 gate drivers

B. Type 2

GSQ should be set to 1 when using this type of gate driver such as HX8677-H. Note that CA_L0 and CA_R0 are used as up/down control.

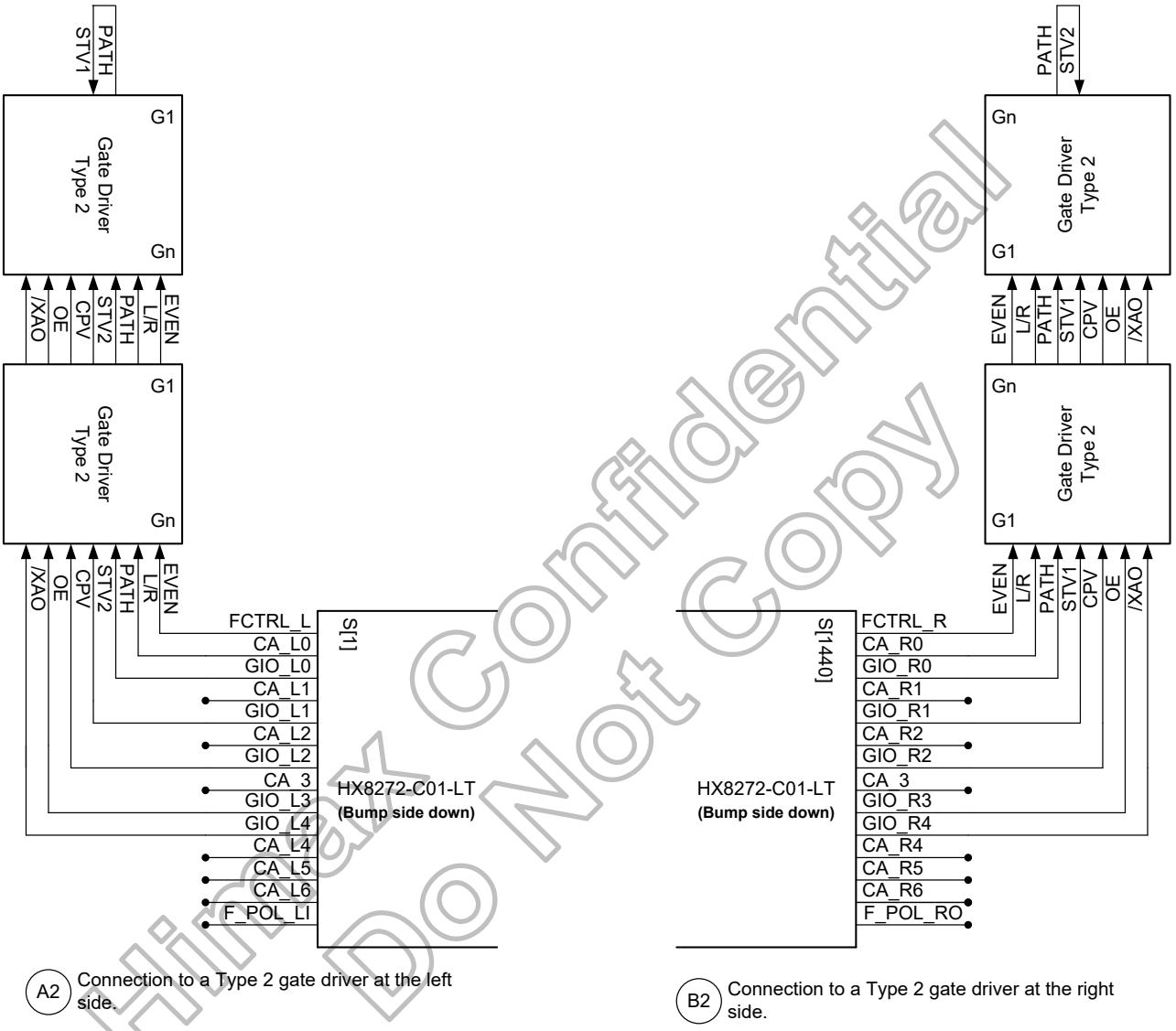


Figure 5.32: Gate control interface for Type 2 gate drivers

5.3.4. Gate driver signal definition

A. When only one source driver is used **(N=1)**, CA_L0/CA_L2/CA_R0/CA_R2 of the chip are used as UD.

	GSQ	GPOS [1:0]	TB	CA_L0 /UD	GIO_L 0	GIO_L 1	CA_L2 /UD	GIO_L 2	GIO_L 3	GIO_L 4	CA_R0 /UD	GIO_R 0	GIO_R 1	CA_R2 /UD	GIO_R 2	GIO_R 3	GIO_R 4
Master (single chip)	0	00	0	0	/XAO	OEV	0	CPV	Input	STV	1	/XAO	0	1	0	0	0
			1	1	/XAO	OEV	1	CPV	STV	Input	0	/XAO	0	0	0	0	0
		01	0	0	0	0	0	0	0	0	1	/XAO	OEV	1	CPV	Input	STV
			1	1	0	0	1	0	0	0	0	/XAO	OEV	0	CPV	STV	Input
		10	0	0	/XAO	OEV_B	0	CPV_B	Input	STV_B	1	/XAO	OEV_A	1	CPV_A	Input	STV_A
			1	1	/XAO	OEV_A	1	CPV_A	STV_A	Input	0	/XAO	OEV_B	0	CPV_B	STV_B	Input
		11	0	0	/XAO	OEV	0	CPV	Input	STV	1	/XAO	OEV	1	CPV	Input	STV
			1	1	/XAO	OEV	1	CPV	STV	Input	0	/XAO	OEV	0	CPV	STV	Input
	1	00	0	0	Input	STV	0	CPV	OEV	/XAO	1	0	0	1	0	0	/XAO
			1	1	STV	Input	1	CPV	OEV	/XAO	0	0	0	0	0	0	/XAO
		01	0	0	0	0	0	0	0	0	1	Input	STV	1	CPV	OEV	/XAO
			1	1	0	0	1	0	0	0	0	STV	Input	0	CPV	OEV	/XAO
		10	0	0	Input	STV_B	0	CPV_B	OEV_B	/XAO	1	Input	STV_A	1	CPV_A	OEV_A	/XAO
			1	1	STV_A	Input	1	CPV_A	OEV_A	/XAO	0	STV_B	Input	0	CPV_B	OEV_B	/XAO
		11	0	0	Input	STV	0	CPV	OEV	/XAO	1	Input	STV	1	CPV	OEV	/XAO
			1	1	STV	Input	1	CPV	OEV	/XAO	0	STV	Input	0	CPV	OEV	/XAO

B. When source drivers are cascaded **(N>1)**: CA_L0 and CA_L2 of the master chip **(SID=0)** are used as UD. CA_R0 and CA_R2 are used as cascade control.

	GSQ	GPOS [1:0]	TB	CA_L0 /UD	GIO_L 0	GIO_L 1	CA_L2 /UD	GIO_L 2	GIO_L 3	GIO_L 4	CA_R0 /UD	GIO_R 0	GIO_R 1	CA_R2 /UD	GIO_R 2	GIO_R 3	GIO_R 4
Master (cascaded)	0	00	0	0	/XAO	OEV	0	CPV	Input	STV	CA0	/XAO	0	CA2	0	0	0
			1	1	/XAO	OEV	1	CPV	STV	Input	CA0	/XAO	0	CA2	0	0	0
		01	0	0	0	0	0	0	0	0	CA0	/XAO	OEV	CA2	CPV	input	STV
			1	1	0	0	1	0	0	0	CA0	/XAO	OEV	CA2	CPV	STV	Input
		10	0	0	/XAO	OEV_B	0	CPV_B	Input	STV_B	CA0	/XAO	OEV_A	CA2	CPV_A	Input	STV_A
			1	1	/XAO	OEV_A	1	CPV_A	STV_A	Input	CA0	/XAO	OEV_B	CA2	CPV_B	STV_B	Input
		11	0	0	/XAO	OEV	0	CPV	Input	STV	CA0	/XAO	OEV	CA2	CPV	Input	STV
			1	1	/XAO	OEV	1	CPV	STV	Input	CA0	/XAO	OEV	CA2	CPV	STV	Input
	1	00	0	0	Input	STV	0	CPV	OEV	/XAO	CA0	0	0	CA2	0	0	0
			1	1	STV	Input	1	CPV	OEV	/XAO	CA0	0	0	CA2	0	0	0
		01	0	0	0	0	0	0	0	0	CA0	Input	STV	CA2	CPV	OEV	/XAO
			1	1	0	0	1	0	0	0	CA0	STV	Input	CA2	CPV	OEV	/XAO
		10	0	0	Input	STV_B	0	CPV_B	OEV_B	/XAO	CA0	Input	STV_A	CA2	CPV_A	OEV_A	/XAO
			1	1	STV_A	Input	1	CPV_A	OEV_A	/XAO	CA0	STV_B	Input	CA2	CPV_B	OEV_B	/XAO
		11	0	0	Input	STV	0	CPV	OEV	/XAO	CA0	Input	STV	CA2	CPV	OEV	/XAO
			1	1	STV	Input	1	CPV	OEV	/XAO	CA0	STV	Input	CA2	CPV	OEV	/XAO

For the slave chips except the last one (SID=1 to N-2)

	GSQ	GPOS [1:0]	TB	CA_L0 /UD	GIO_L 0	GIO_L 1	CA_L2 /UD	GIO_L 2	GIO_L 3	GIO_L 4	CA_R0 /UD	GIO_R 0	GIO_R 1	CA_R2 /UD	GIO_R 2	GIO_R 3	GIO_R 4
Slaves except the last (cascaded)	0	00	0	Input							CA0	GIO_L0	GIO_L1	CA2	GIO_L2	Input	GIO_L4
			1								CA0			CA2		GIO_L3	Input
		01	0								CA0			CA2		Input	GIO_L4
			1								CA0			CA2		GIO_L3	Input
		1X	0								CA0			CA2		Input	GIO_L4
			1								CA0			CA2		GIO_L3	Input
	1	00	0	Input							CA0	Input	GIO_L1	CA2	GIO_L2	GIO_L3	GIO_L4
			1								CA0	GIO_L0	Input	CA2			
		01	0								CA0	Input	GIO_L1	CA2			
			1								CA0	GIO_L0	Input	CA2			
		1X	0								CA0	Input	GIO_L1	CA2			
			1								CA0	GIO_L0	Input	CA2			

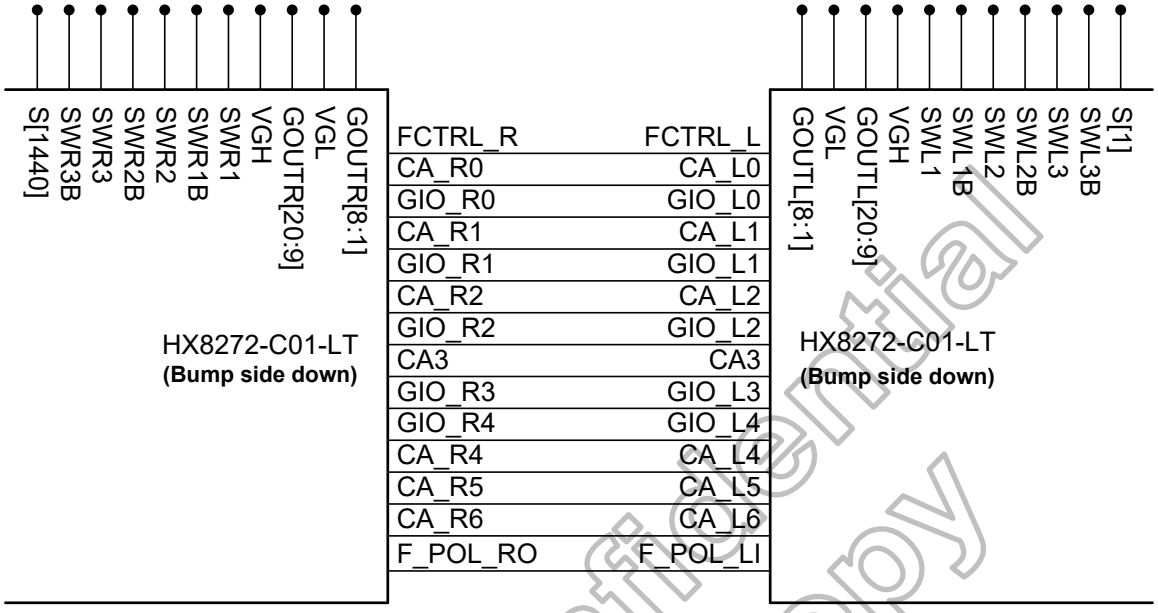
CA_R0 and CA_R2 of the last slave chip (SID=N-1) are used as UD

	GSQ	GPOS [1:0]	TB	CA_L0 /UD	GIO_L 0	GIO_L 1	CA_L2 /UD	GIO_L 2	GIO_L 3	GIO_L 4	CA_R0 /UD	GIO_R 0	GIO_R 1	CA_R2 /UD	GIO_R 2	GIO_R 3	GIO_R 4
The last slave (cascaded)	0	00	0	Input							1	GIO_L0	GIO_L1	1	GIO_L2	Input	GIO_L4
			1								0			0		GIO_L3	Input
		01	0								1			1		Input	GIO_L4
			1								0			0		GIO_L3	Input
		1X	0								1			1		Input	GIO_L4
			1								0			0		GIO_L3	Input
	1	00	0	Input							1	Input	GIO_L1	1	GIO_L2	GIO_L3	GIO_L4
			1								0	GIO_L0	Input	0			
		01	0								1	Input	GIO_L1	1			
			1								0	GIO_L0	Input	0			
		1X	0								1	Input	GIO_L1	1			
			1								0	GIO_L0	Input	0			

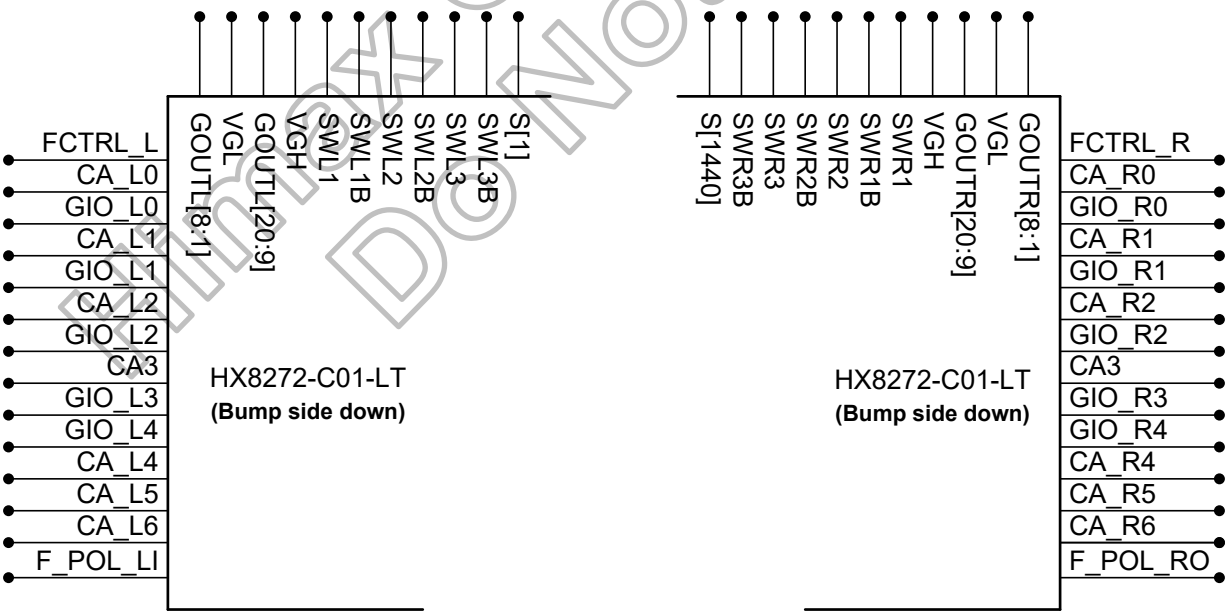
Table 5.3: Gate driver signal definition table

5.3.5. Cascade control interface

A. Between each source drivers, it must connect all of the side pins **(Case A)**.



A Connection between two source drivers.
Connect all of the side pins.



B Connection to nothing at the left side.
Leave all of the side pins open.

C Connection to nothing at the right side.
Leave all of the side pins open.

Figure 5.33: Cascade and GIP/SW control interface

5.3.6. GIP control interface

The HX8272-C01-LT has 20 output pins on each of right/left side for GIP circuit control use as show below. Each of these output pins can assign signal by setting register **(Page0Fh~Page14h)** in keeping with the GIP signal output.

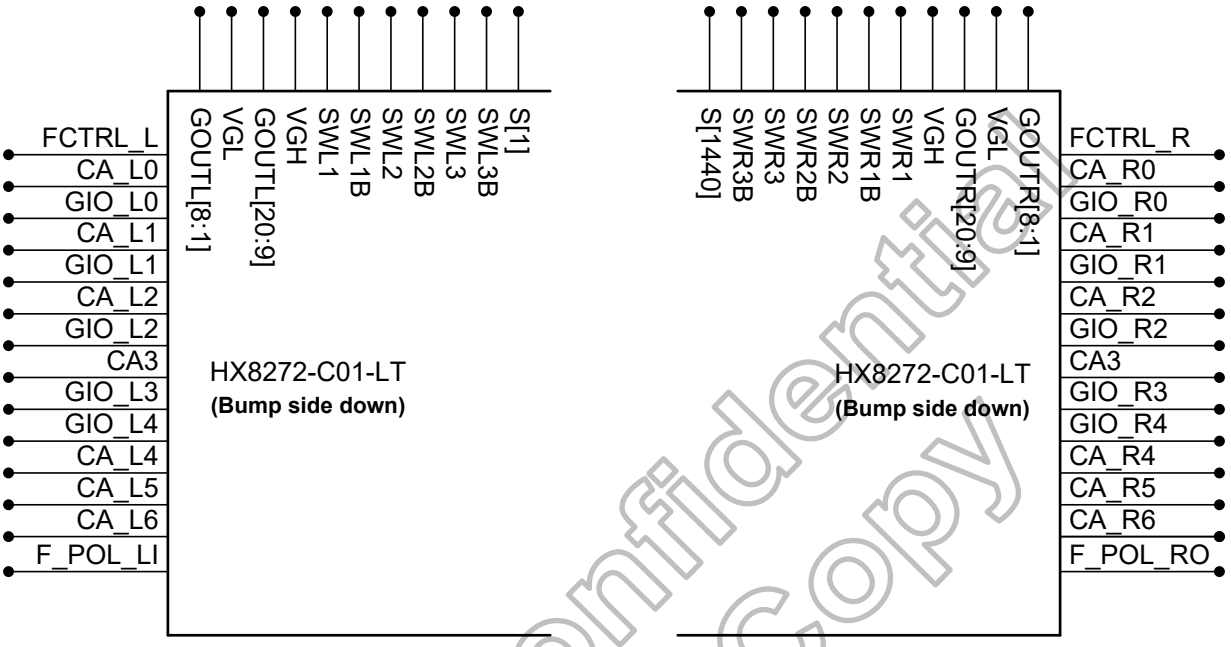


Figure 5.34: GIP control interface

5.3.7. Cascade design: Power application

A. The following voltages are provided by the master chip and should be connected to the slave chip:
VSP, VSN, VGH, VGL, VGMPHO, VGMPLO, VGMNHO, VGMNLO.
B. The following voltages are provided by the master chip and do not need to connect to slave chip:
VCOM.
C. The following voltages are provided by each chip with separate capacitors:
VSDP, VSDN, VCL, VDDD.
D. The following voltages are provided by the master chip with common capacitors:
VSP, VSN, VGMPHI, VGMPLI, VGMNHI, VGMNLI.
E. Note that for the master chip, do not connect gamma voltage inputs VGMPHI / VGMPLI / VGMNHI / VGMNLI to VGMPHO / VGMPLO / VGMNHO / VGMNLO on panel, but connect them through FPC or PCB traces. This helps to reduce difference between gamma voltages of each chip.
F. VCOM can be connected to the panel through VCOM_L and VCOM_R pins of each chip.

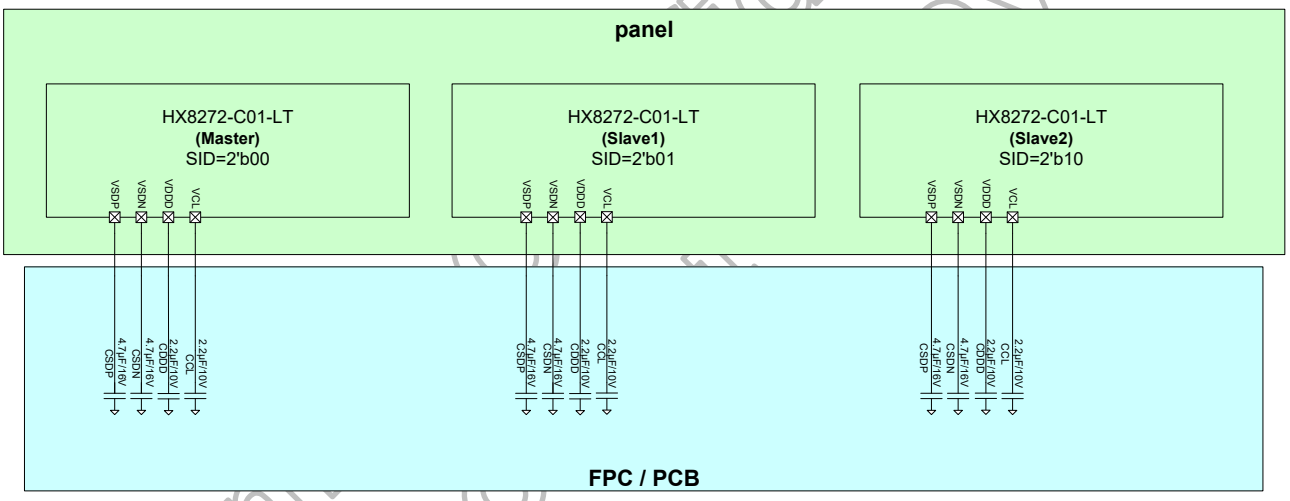


Figure 5.35: Cascade design for regulator outputs

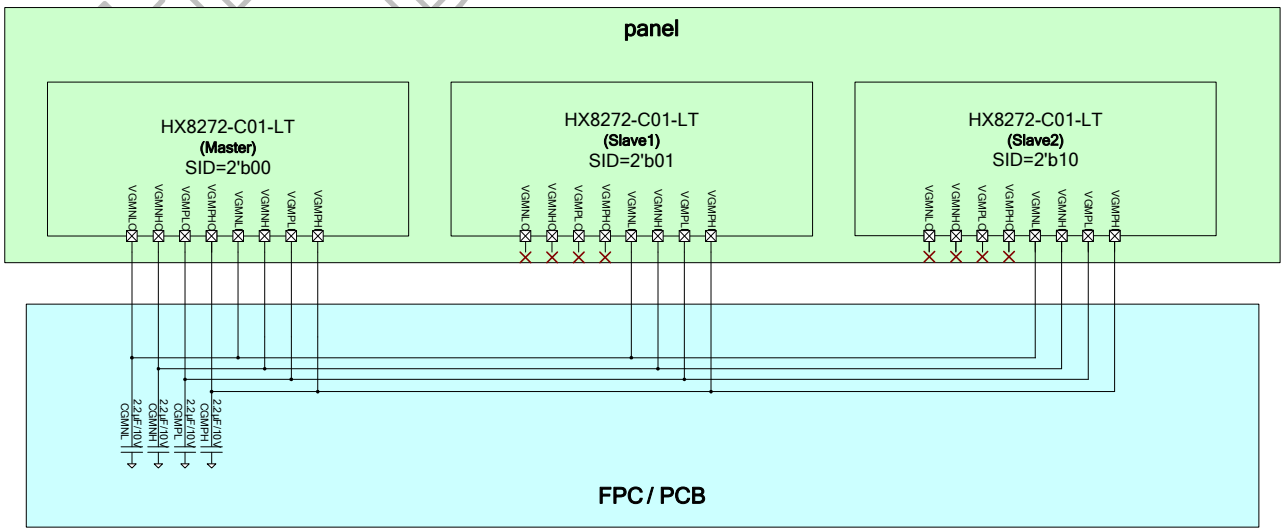


Figure 5.36: Cascade design for gamma reference voltages

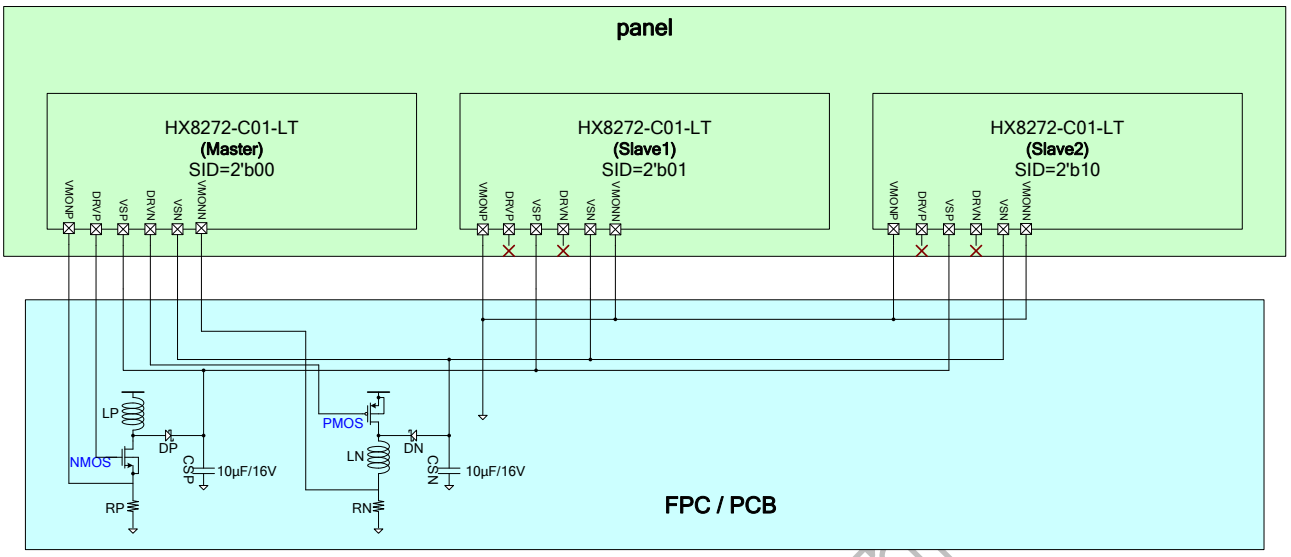


Figure 5.37: Cascade design for PFM

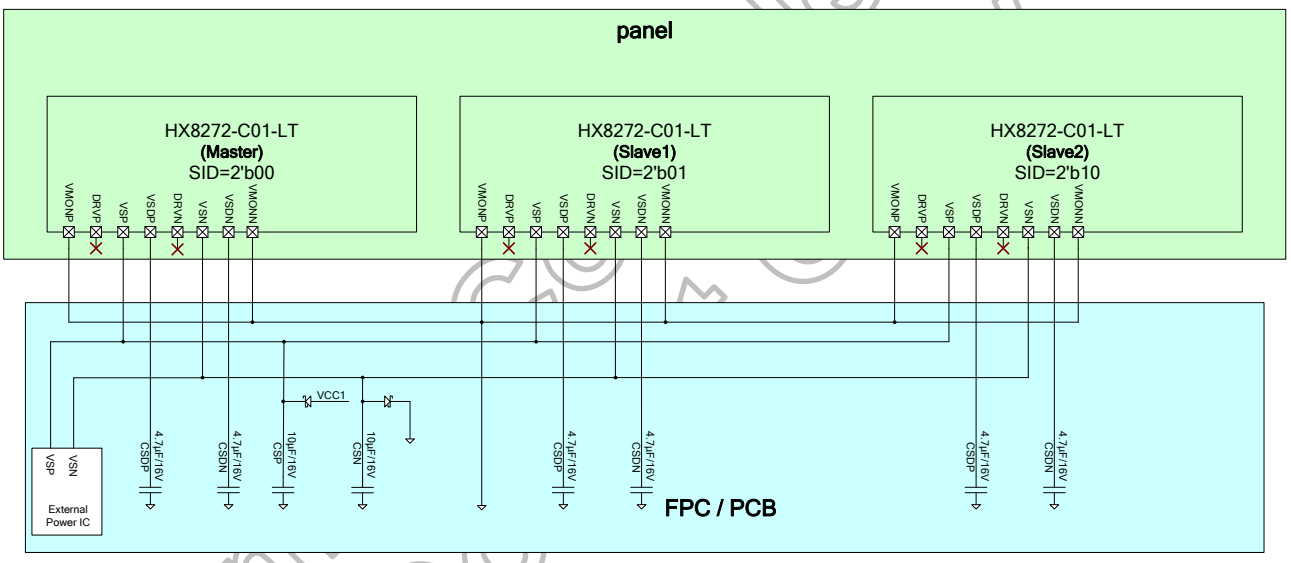


Figure 5.38: Cascade design with external power IC

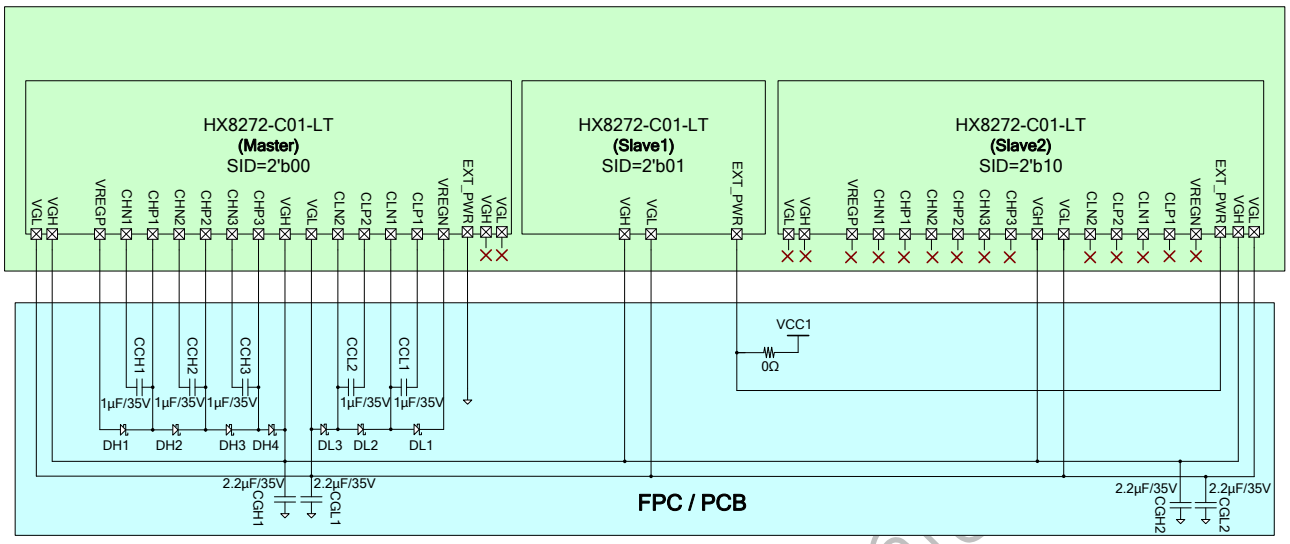


Figure 5.39: Cascade design for charge pumps

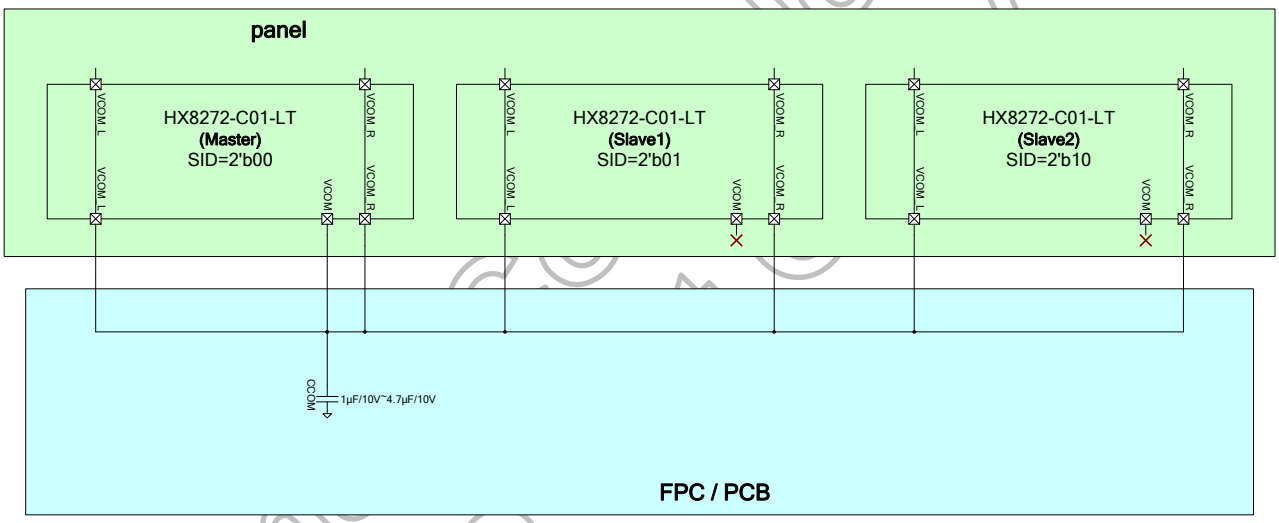


Figure 5.40: Cascade design for VCOM

5.3.8. Cascade design: RESETB application

A. Add external RC circuit to pin RESETB to start whole chip reset when power up.
B. If RESETB_SLP function not used, and pin RESETB_SLP should be connected to VCC1.

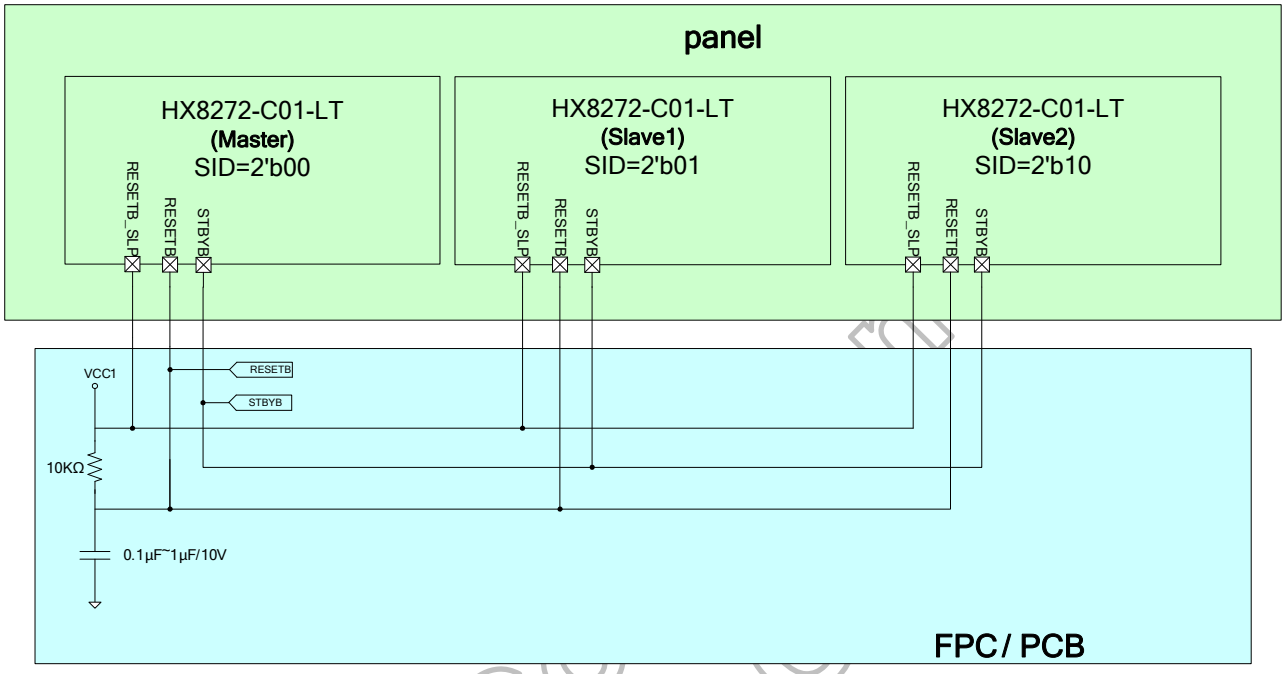


Figure 5.41: Cascade design for RESETB function

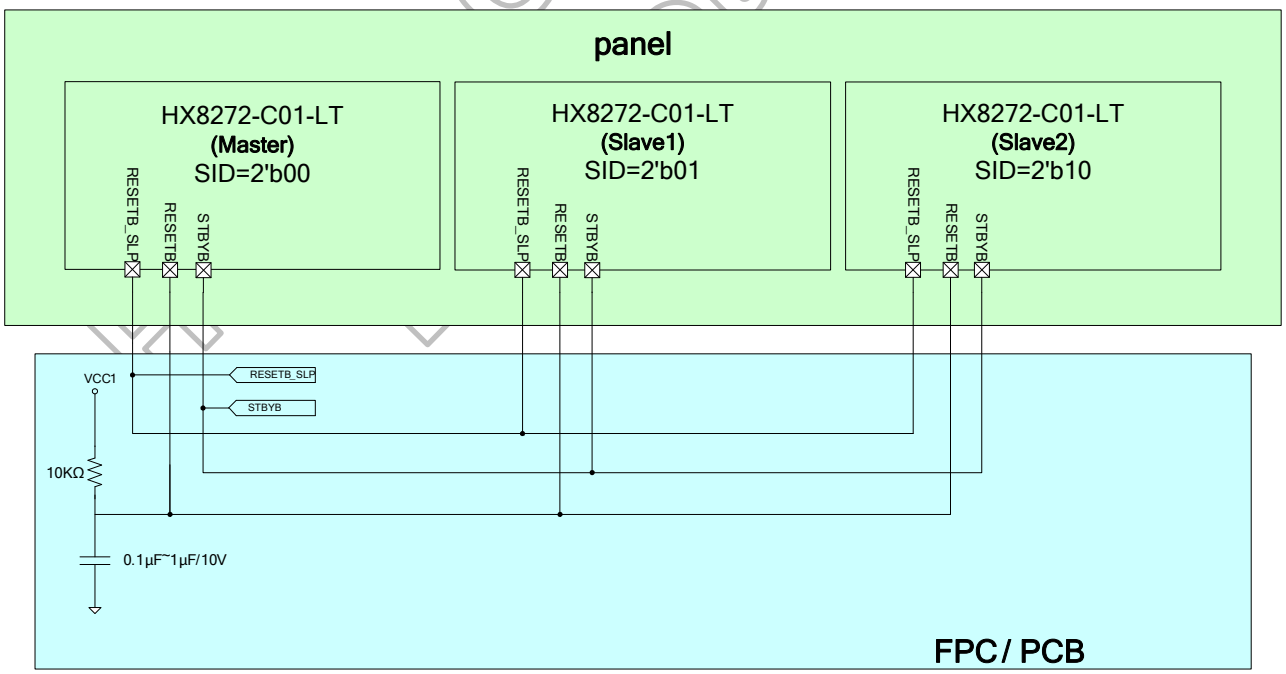


Figure 5.42: Cascade design for RESETB_SLP function

5.3.9. Cascade design: EEPROM application

A. Master and all slave IC set EEPEN=H to enable EEPROM reload setting.
B. HX8272-C01-LT supports 8K-bit EEPROM. HX8272-C01-LT recommends using Microchip 93LC76, 512 x 16-bit.
C. Connect EEPROM CS, CLK, DI, DO to HX8272-C01-LT ECS, ESCL, ESDAO, ESDAI.

(An external 10K_ pull-down protection resistor should be added to the CS pin, please refer to Microchip 93LC76 datasheet for details.)

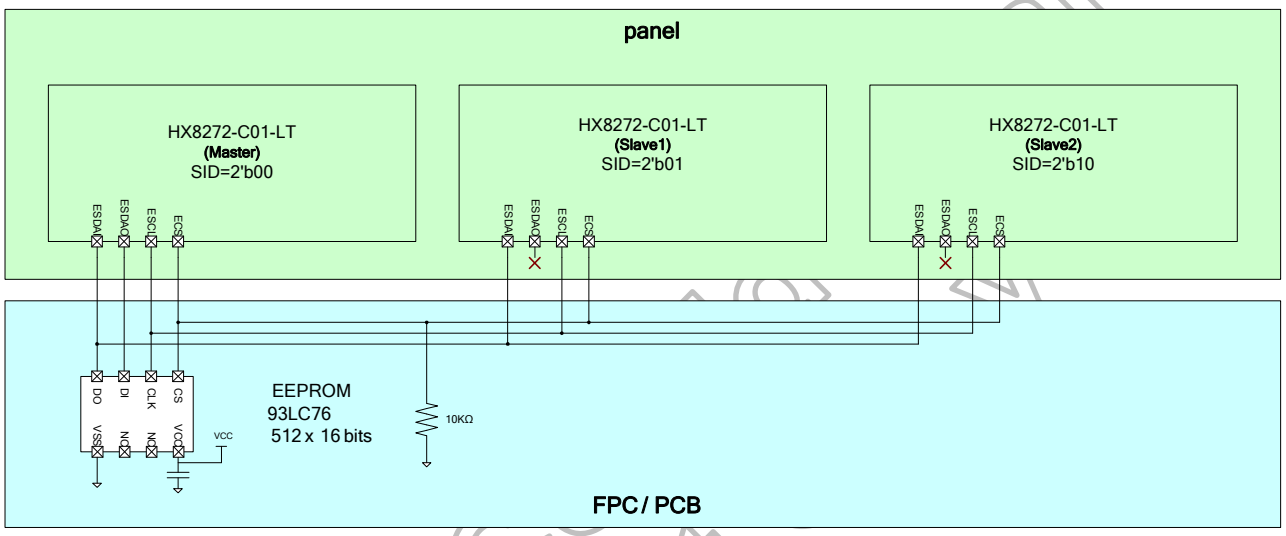


Figure 5.43: Cascade design for EEPROM application

6. Function Description

6.1. Data processing circuit

The input data from external display interface will be fed to the data processing circuit, which contains the functions of contrast **(Gain)** control; brightness **(Offset)** control, and gamma control. See the register descriptions for detail.

The contrast adjustment is done on RGB data with 3-set of 8-bit registers. The 8-bit register represents gain value in the range of 0.5 to 1.496. When output data of the gain multiplication exceeds 255, it will be clamped at 255. Default gain value is 1.0.

The brightness adjustment is done on RGB data with 3-set of 6-bit registers. The 6-bit register represents offset value in the range of -16 to +47. When output data of the offset shifting exceeds the range of 0 to 255, it will be clamped to 0 and 255. Default offset is 0.

The digital gamma correction is done by 23-segment piecewise linear interpolation. The 23 segments are defined with 24 register values for level 0, 1, 3, 7, 11, 15, 23, 31, 47, 63, 95, 127, 128, 160, 192, 208, 224, 232, 240, 244, 248, 252, 254 and 255. The gamma correction output is then fed to 8-bit DAC and OP to drive the source lines on the panel.

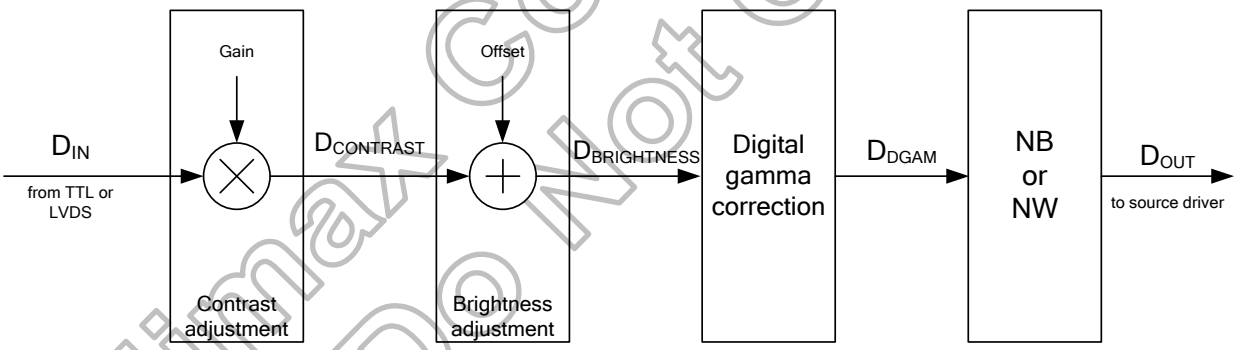


Figure 6.1: Data processing

6.1.1. Contrast adjustment

Contrast adjustment is done on RGB data separately by multiplying a gain ranging from 0.5 to 1.496. The gain for each color is set with 3-set of 8-bit registers **(RGC[7:0], GGC[7:0], BGC[7:0])**. If the resulting output data exceeds 255, it will be clamped to 255. Default gain value is 1.0.

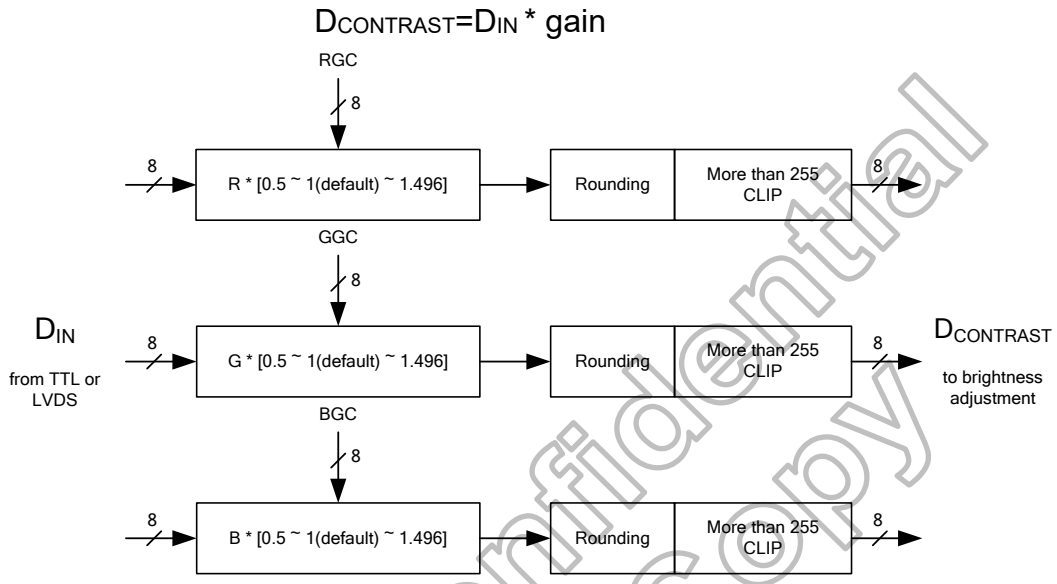


Figure 6.2: Contrast adjustment

6.1.2. Brightness adjustment

Brightness adjustment is done on RGB data separately by adding an offset ranging from -16 to +47. The offset of each color is set with 3-set of 6-bit registers **(ROB[5:0], GOB[5:0], BOB[5:0])**. If the resulting output data exceeds the range of 0 to 255, it will be clamped to 0 and 255. Default offset is 0.

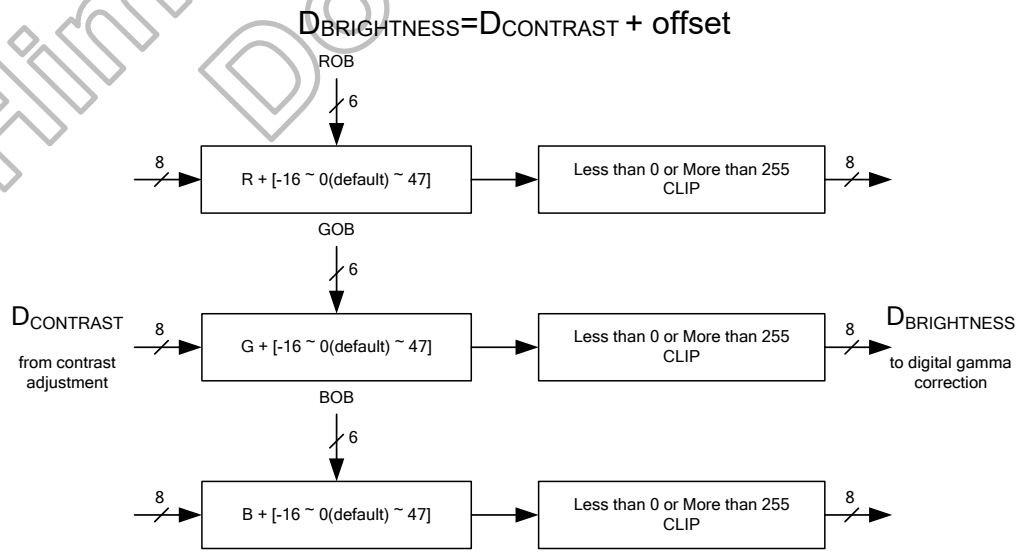


Figure 6.3: Brightness adjustment

6.1.3. Digital gamma correction

The digital gamma correction is done on RGB data separately with 23-segment piecewise linear interpolation. The 23 segments are defined with 24 register values Y_1~Y_{24} **(in register Page09h~Page0Bh)** for level X_1~X_{24}=0, 1, 3, 7, 11, 15, 23, 31, 47, 63, 95, 127, 128, 160, 192, 208, 224, 232, 240, 244, 248, 252, 254 and 255. Y on X between X_n and X_{n+1} is interpolated with the following equations.

$$Y= Y_n + (Y_{n+1} – Y_n) * (X-X_n) / (X_{n+1}-X_n)$$

The gamma correction output 10-bit data D_{DGAM} is then fed to 8-bit DAC and OP to drive the source lines on the panel with dithering.

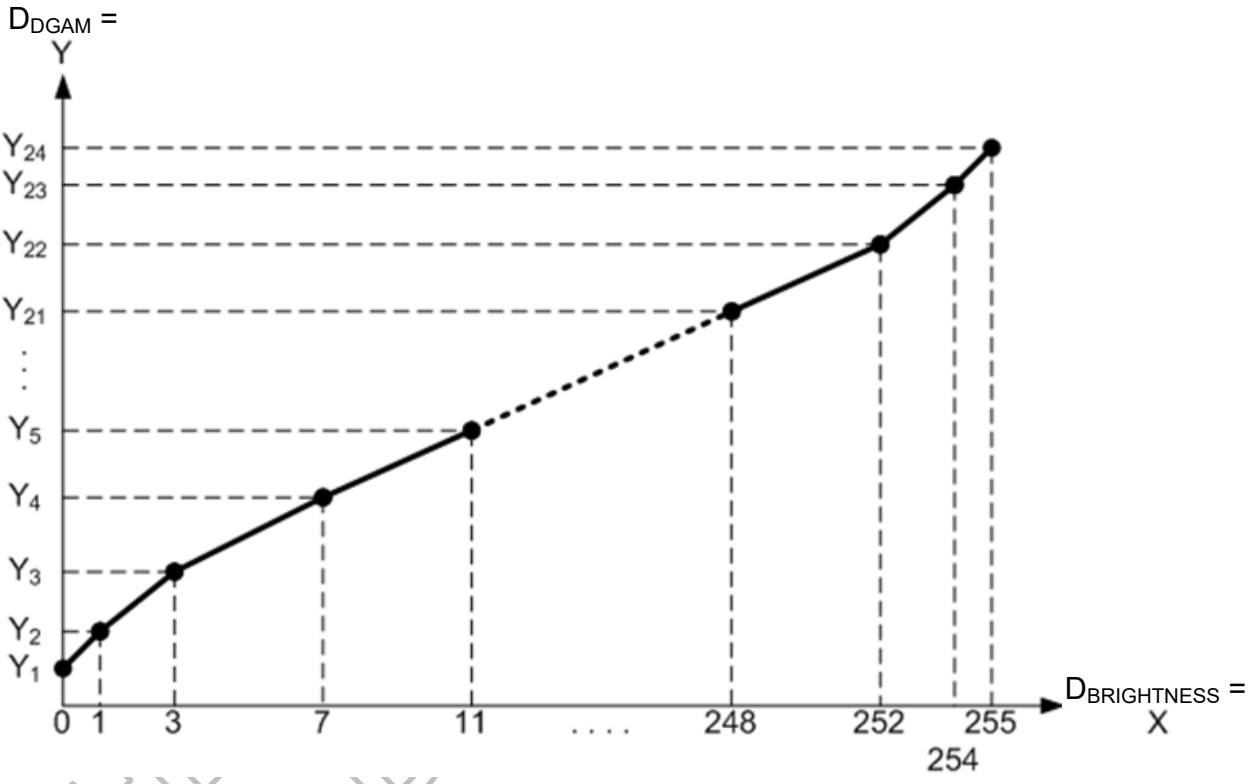


Figure 6.4: Digital gamma correction

6.2. NB/NW selection

The data after digital gamma processing D_{DGAM} will go to NB/NW block. It will transfer input data to corresponding correct NB or NW data.

6.3. LCD driver

The LCD driver circuit consists of a 1440-channel source driver **(S[1440:1])** and outputs a liquid crystal drive voltage **(Grayscale voltage)**, which corresponds to the display data. The source lines of the display could be cascaded to support maximum resolution 2560xRGBx960 with 3-chip at LTPS MUX2:4 panel structure.

6.4. Timing controller

The control circuit generates internal control signals from input VS, HS, or DE signals. The LCD timing generator generates internal control signals for the source and gate driver. The timing generator also generates signals to control the operation timings of display data latching circuit.

6.5. Display interface

The HX8272-C01-LT supports different display resolutions with single port LVDS, dual port LVDS and TTL interface.

6.5.1. LVDS interface

For 1-port LVDS 8-bit mode with VESA format, only the odd port **(with OLVxxx pins)** is used.

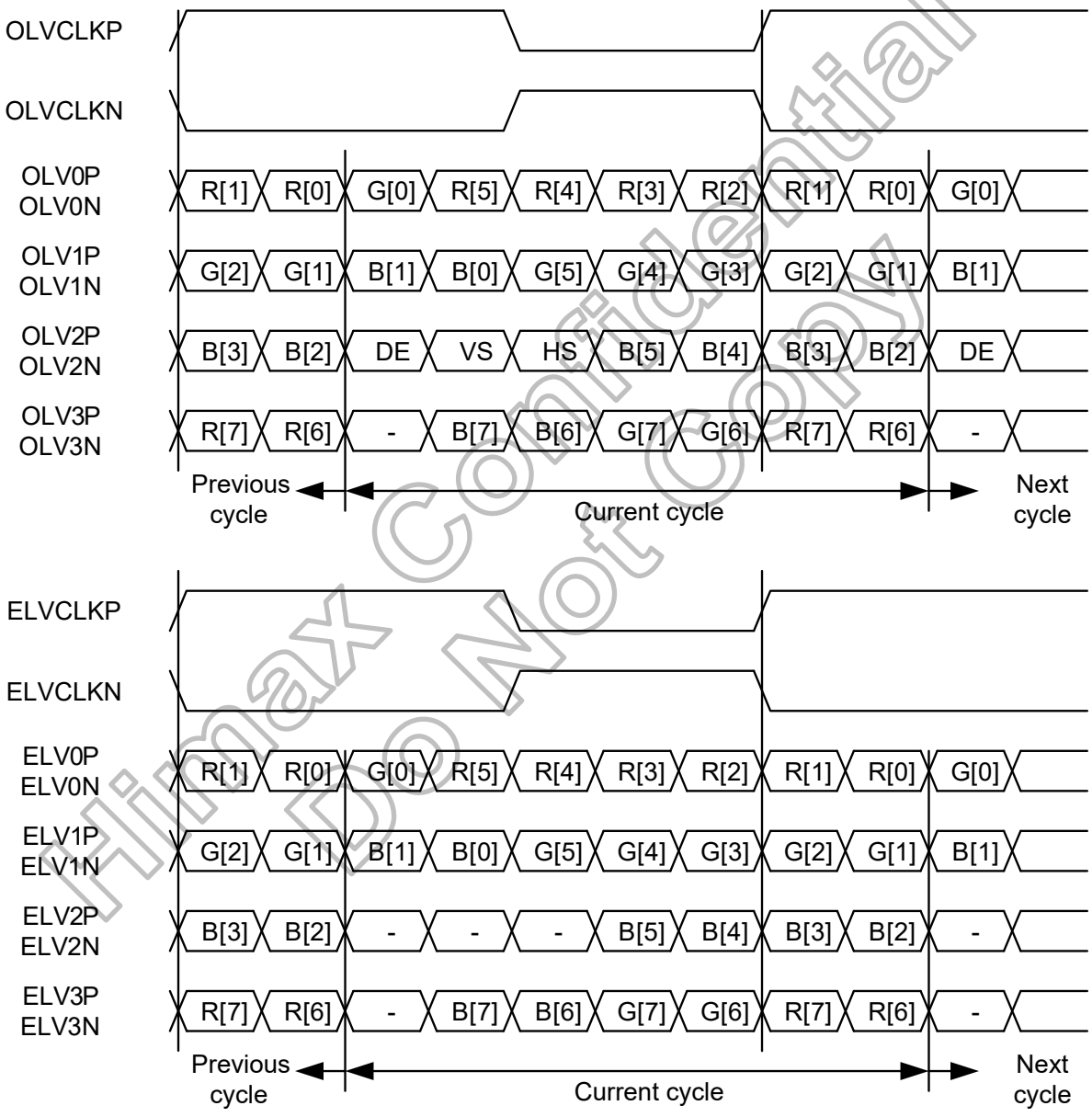


Figure 6.5: 2-port LVDS signals, VESA format, 8-bit mode

For 1-port LVDS 8-bit mode with JEIDA format, only the odd port **(with OLVxxx pins)** is used.

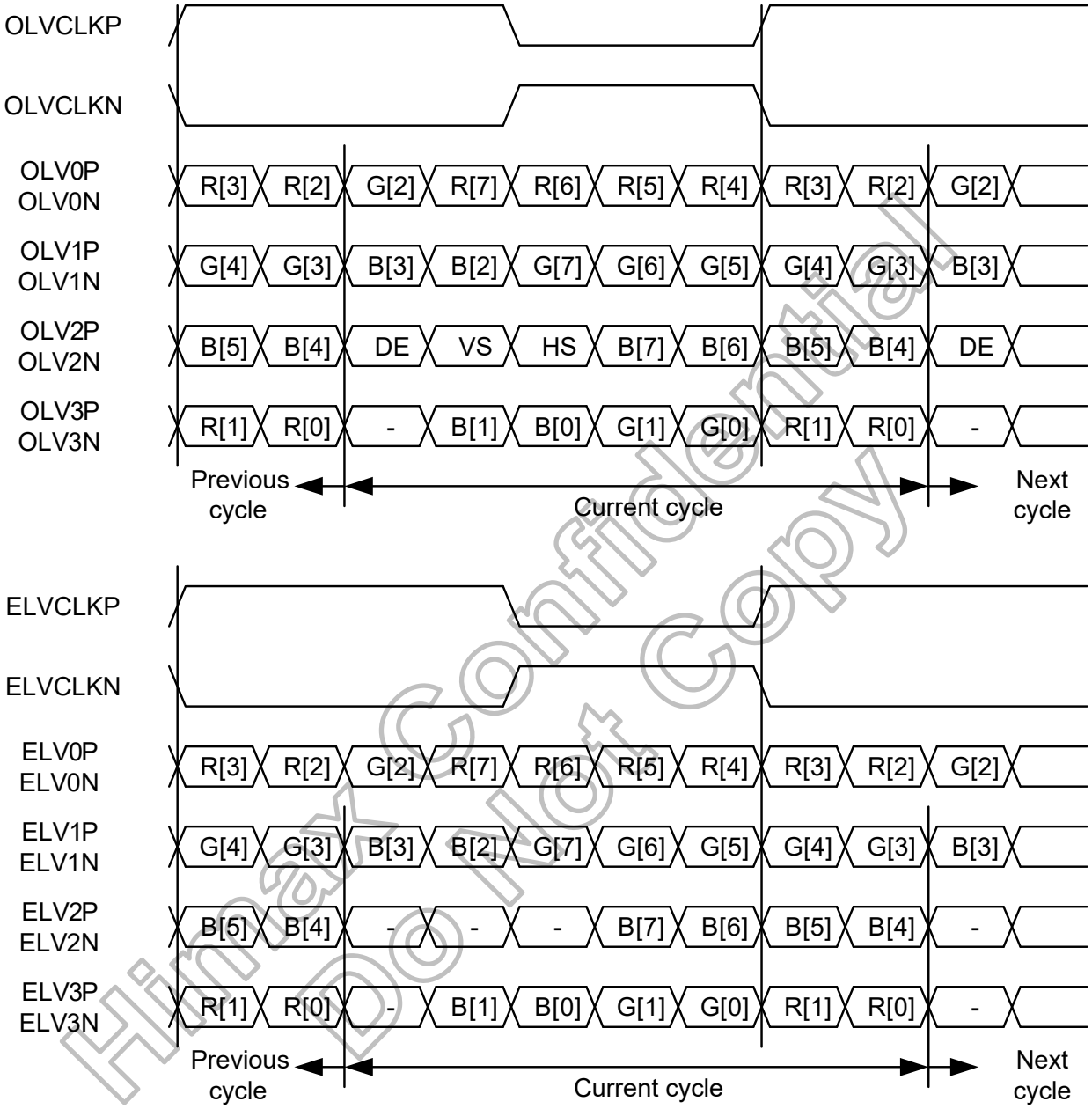


Figure 6.6: 2-port LVDS signals, JEIDA format, 8-bit mode

For 1-port LVDS 6-bit mode, only the odd port **(with OLVxxx pins)** is used.

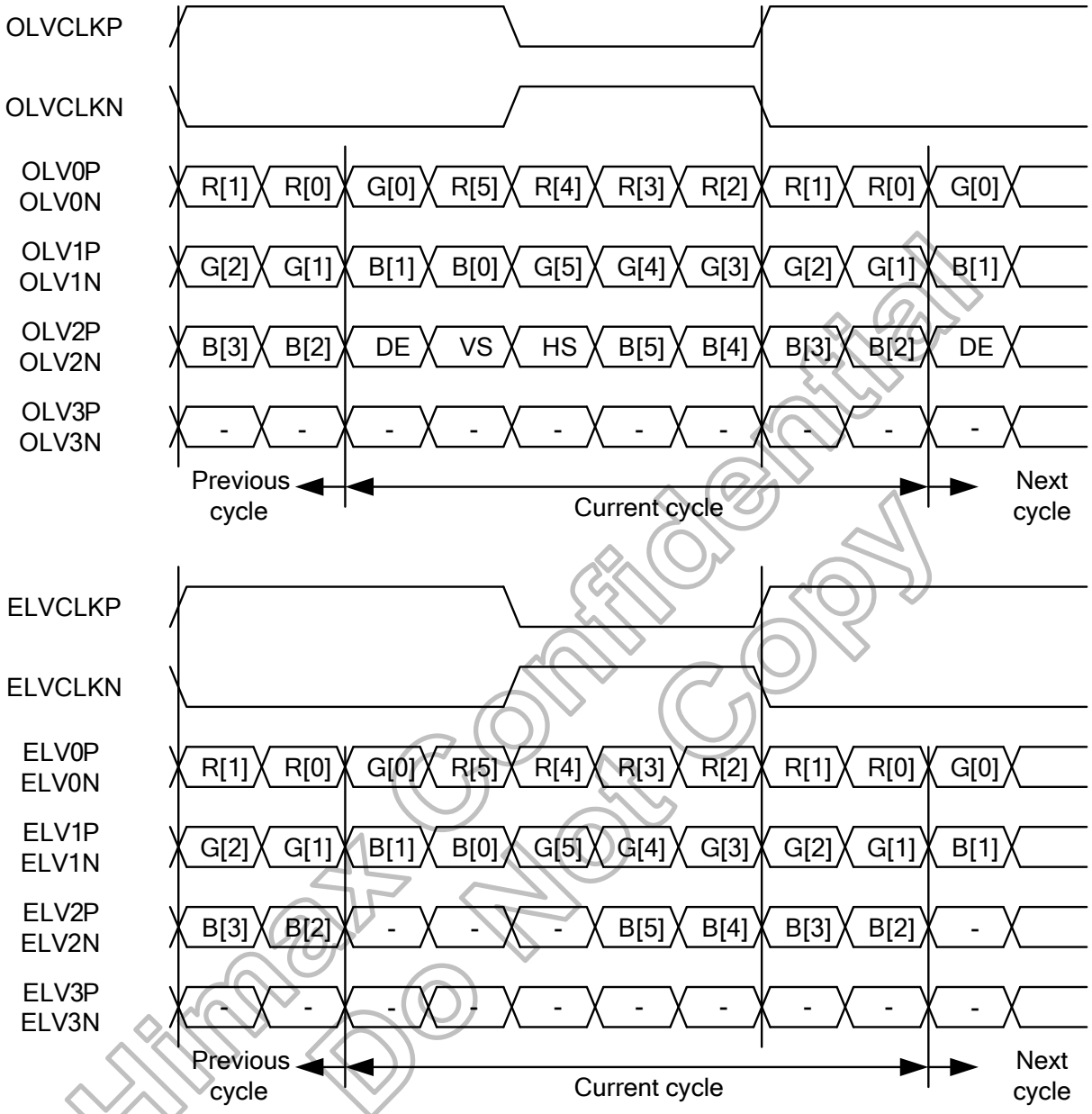


Figure 6.7: 2-port LVDS signals, 6-bit format

6.5.2. Parallel RGB with Sync mode at TTL interface

- Horizontal

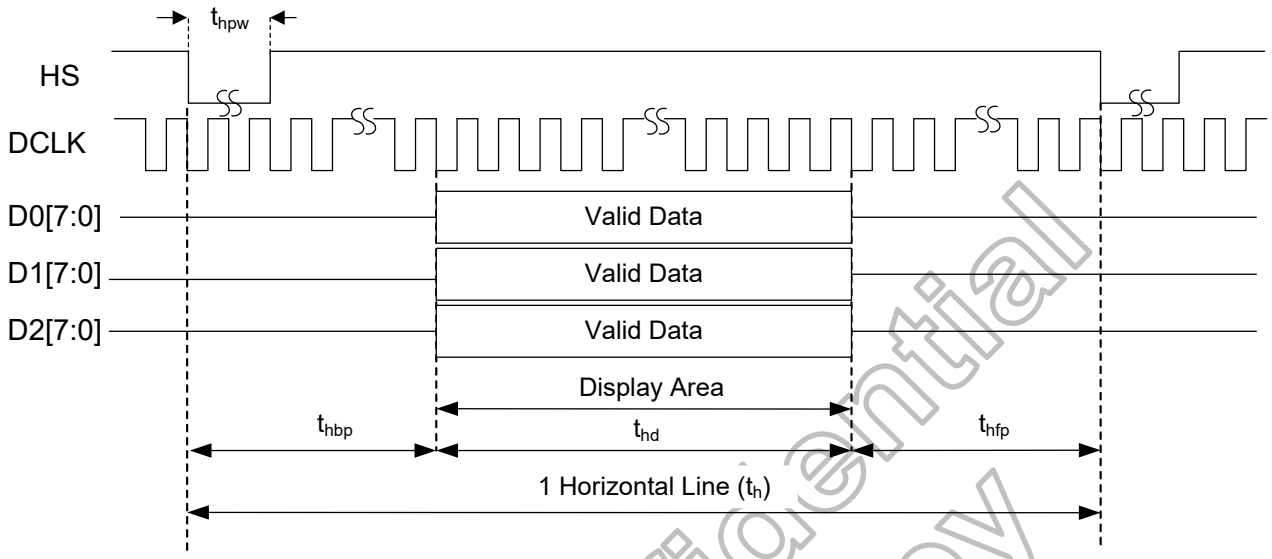


Figure 6.8: Horizontal input timing at Sync mode

- Vertical

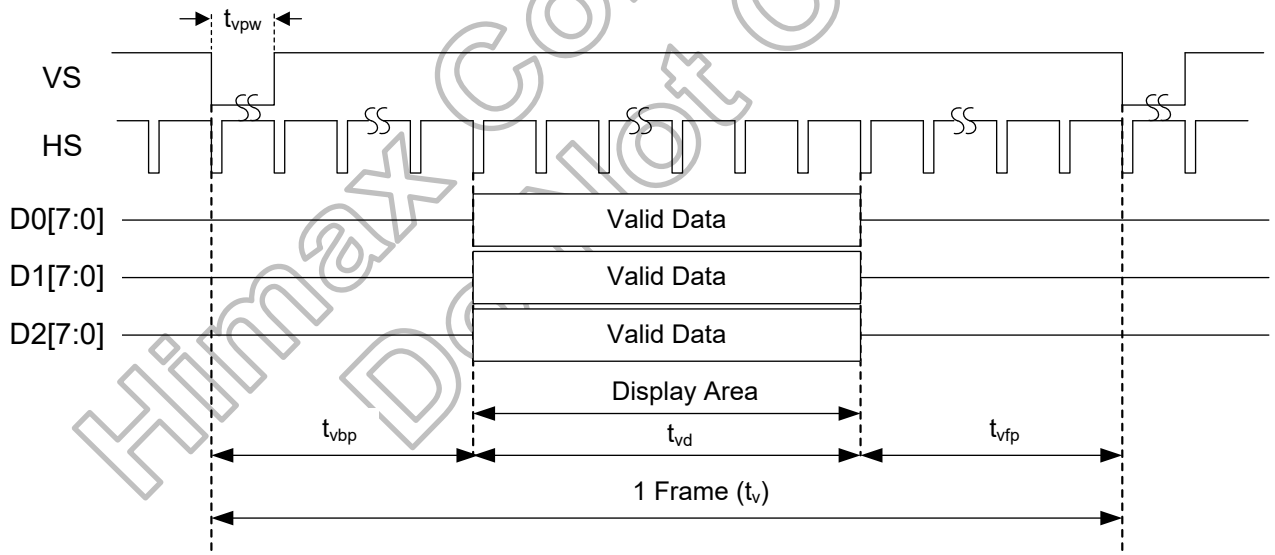


Figure 6.9: Vertical input timing at Sync mode

Parameter	Symbol	Panel Resolution									Unit
		2560xRGBx960 (Two Port)			2400xRGBx900 (Two Port)			1920xRGBx1080 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	81.12	-	-	71.74	-	-	69.35	-	MHz
Horizontal valid data	t_{hd}		1280			1200			960		DCLK
Hsync pulse width	t_{hpw}	6	12	254	6	12	254	6	12	254	DCLK
Hsync back porch	t_{hbp}(1)	5	16	255	5	16	255	5	16	255	DCLK
Hsync front porch	t_{hfp}	50	56	-	50	56	-	50	56	-	DCLK
1 horizontal line	t_h(2)	1335	1352	1920	1255	1272	1800	1015	1032	1440	DCLK
Vertical valid data	t_{vd}		960			900			1080		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}(3)	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v(2)(4)	968	1000	1440	908	940	1350	1088	1120	1620	H
Frame rate	FR(5)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1920xRGBx720 (One Port)			1920xRGBx400 (One Port)			1600xRGBx320 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	90.84	-	-	52.59	-	-	36.12	-	MHz
Horizontal valid data	t_{hd}		1920			1920			1600		DCLK
Hsync pulse Width	t_{hpw}	6	12	254	6	12	254	6	12	254	DCLK
Hsync back porch	t_{hbp}(1)	5	16	255	5	16	255	5	16	255	DCLK
Hsync front porch	t_{hfp}	50	56	-	50	56	-	50	56	-	DCLK
1 horizontal line	t_h(2)	1975	1992	2880	1975	1992	2880	1655	1672	2400	DCLK
Vertical valid data	t_{vd}		720			400			320		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}(3)	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v(2)(4)	728	760	1080	408	440	700	328	360	600	H
Frame rate	FR(5)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1560xRGBx700 (One Port)			1540xRGBx720 (One Port)			1440xRGBx540 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	72.46	-	-	73.51	-	-	52.62	-	MHz
Horizontal valid data	t_{hd}		1560			1540			1440		DCLK
Hsync pulse Width	t_{hpw}	6	12	254	6	12	254	6	12	254	DCLK
Hsync back porch	t_{hbp}(1)	5	16	255	5	16	255	5	16	255	DCLK
Hsync front porch	t_{hfp}	50	56	-	50	56	-	50	56	-	DCLK
1 horizontal line	t_h(2)	1615	1632	2340	1595	1612	2310	1495	1512	2160	DCLK
Vertical valid data	t_{vd}		700			720			540		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}(3)	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v(2)(4)	708	740	1050	728	760	1080	548	580	810	H
Frame rate	FR(5)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1280xRGBx720 (One Port)			1280xRGBx480 (One Port)			1280xRGBx400 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	61.65	-	-	42.18	-	-	35.69	-	MHz
Horizontal valid data	t_{hd}		1280			1280			1280		DCLK
Hsync pulse Width	t_{hpw}	6	12	254	6	12	254	6	12	254	DCLK
Hsync back porch	t_{hbp}(1)	5	16	255	5	16	255	5	16	255	DCLK
Hsync front porch	t_{hfp}	50	56	-	50	56	-	50	56	-	DCLK
1 horizontal line	t_h(2)	1335	1352	1920	1335	1352	1920	1335	1352	1920	DCLK
Vertical valid data	t_{vd}		720			480			400		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}(3)	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v(2)(4)	728	760	1080	488	520	750	408	440	700	H
Frame rate	FR(5)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		960xRGBx2560 (Two Port)			960xRGBx540 (One Port)			800xRGBx480 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	86.11	-	-	35.91	-	-	27.21	-	MHz
Horizontal valid data	t_{hd}		480			960			800		DCLK
Hsync pulse Width	t_{hpw}	6	12	150	6	12	254	6	12	254	DCLK
Hsync back porch	t_{hbp}(1)	5	16	151	5	16	255	5	16	255	DCLK
Hsync front porch	t_{hfp}	50	56	-	50	56	-	50	56	-	DCLK
1 horizontal line	t_h(2)	535	552	720	1015	1032	1440	855	872	1200	DCLK
Vertical valid data	t_{vd}		2560			540			480		H
Vsync pulse width	t_{vpw}	1	3	254	1	3	254	1	3	254	H
Vsync back porch	t_{vbp}(3)	2	24	255	2	24	255	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	6	16	-	6	16	-	H
1 vertical field	t_v(2)(4)	2568	2600	3840	548	580	810	488	520	750	H
Frame rate	FR(5)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution			Unit
		480xRGBx240 (One Port)			
		Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	9.27	-	MHz
Horizontal valid data	t_{hd}		480		DCLK
Hsync pulse Width	t_{hpw}	6	12	150	DCLK
Hsync back porch	t_{hbp}(1)	5	16	151	DCLK
Hsync front porch	t_{hfp}	50	56	-	DCLK
1 horizontal line	t_h(2)	535	552	720	DCLK
Vertical valid data	t_{vd}		240		H
Vsync pulse width	t_{vpw}	1	3	254	H
Vsync back porch	t_{vbp}(3)	2	24	255	H
Vsync front porch	t_{vfp}	6	16	-	H
1 vertical field	t_v(2)(4)	248	280	600	H
Frame rate	FR(5)	-	60	-	Hz

Note: (1) Horizontal back-porch could be adjusted at Sync mode by register Page00h R07h.
(2) $t_h=t_{hbp} + t_{hfp} + t_{hd}$ and $t_v=t_{vbp} + t_{vfp} + t_{vd}$.
(3) Vertical back-porch could be adjusted at Sync mode by register Page00h R06h.
(4) Minimum value of vertical blanking **($t_{vbp} + t_{vfp}$)** could support the GIP timing that must reference the GIP structure of panel.
(5) FR **(Frame rate)**=F_{DCLK} / t_h / t_v.

Table 6.1: Input timing table at Sync mode

6.5.3. Parallel RGB with DE only mode at TTL interface

It just needs DE signal only, when DE only mode enabled.

- Horizontal

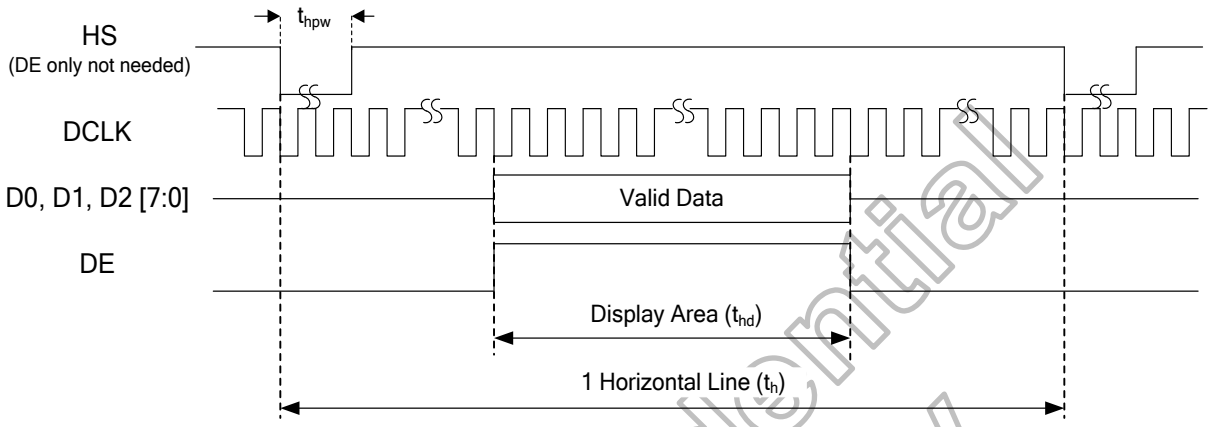


Figure 6.10: Horizontal input timing at DE only mode

- Vertical

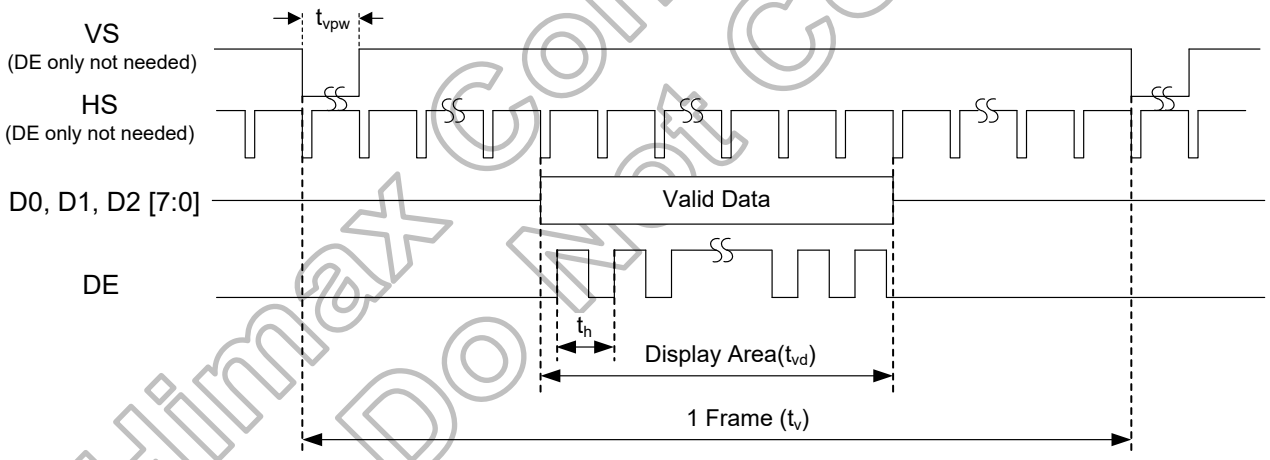
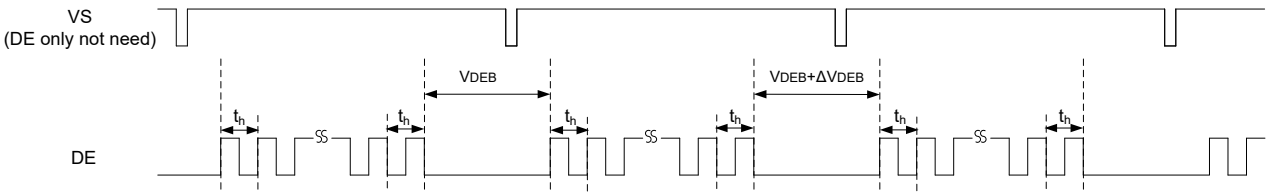


Figure 6.11: Vertical input timing at DE only mode

The restriction of input DE variation



Note: The variation of vertical blank (ΔV_{DEB}) must be less than 50 DCLK.

Figure 6.12: The restriction of input DE variation

Parameter	Symbol	Panel Resolution									Unit
		2560xRGBx960 (Two Port)			2400xRGBx900 (Two Port)			1920xRGBx1080 (Two Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	81.12	-	-	71.74	-	-	69.35	-	MHz
Horizontal valid data	t_{hd}		1280			1200			960		DCLK
1 horizontal line	t_h	1335	1352	1920	1256	1272	1800	1015	1032	1440	DCLK
Vertical valid data	t_{vd}		960			900			1080		H
1 vertical field	t_v(1)(2)	968	1000	1440	908	940	1350	1088	1120	1620	H
Frame rate	FR(3)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1920xRGBx720 (One Port)			1920xRGBx400 (One Port)			1600xRGBx320 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	90.84	-	-	52.59	-	-	36.12	-	MHz
Horizontal valid data	t_{hd}		1920			1920			1600		DCLK
1 horizontal line	t_h	1975	1992	2880	1975	1992	2880	1655	1672	2400	DCLK
Vertical valid data	t_{vd}		720			400			320		H
1 vertical field	t_v(1)(2)	728	760	1080	408	440	700	328	360	600	H
Frame rate	FR(3)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1560xRGBx700 (One Port)			1540xRGBx720 (One Port)			1440xRGBx540 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	72.46	-	-	73.51	-	-	52.62	-	MHz
Horizontal valid data	t_{hd}		1560			1540			1440		DCLK
1 horizontal line	t_h	1615	1632	2340	1595	1612	2310	1495	1512	2160	DCLK
Vertical valid data	t_{vd}		700			720			540		H
1 vertical field	t_v(1)(2)	708	740	1050	728	760	1080	548	580	810	H
Frame rate	FR(3)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		1280xRGBx720 (One Port)			1280xRGBx480 (One Port)			1280xRGBx400 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	61.65	-	-	42.18	-	-	35.69	-	MHz
Horizontal valid data	t_{hd}		1280			1280			1280		DCLK
1 horizontal line	t_h	1335	1352	1920	1335	1352	1920	1335	1352	1920	DCLK
Vertical valid data	t_{vd}		720			480			400		H
1 vertical field	t_v(1)(2)	728	760	1080	488	520	750	408	440	700	H
Frame rate	FR(3)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution									Unit
		960xRGBx2560 (Two Port)			960xRGBx540 (One Port)			800xRGBx480 (One Port)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	86.11	-	-	35.91	-	-	27.21	-	MHz
Horizontal valid data	t_{hd}		480			960			800		DCLK
1 horizontal line	t_h	535	552	720	1015	1032	1440	855	872	1200	DCLK
Vertical valid data	t_{vd}		2560			540			480		H
1 vertical field	t_v(1)(2)	2568	2600	3840	548	580	810	488	520	750	H
Frame rate	FR(3)	-	60	-	-	60	-	-	60	-	Hz

Parameter	Symbol	Panel Resolution 480xRGBx240 (One Port)			Unit
		Min.	Typ.	Max.	
DCLK frequency	F_{DCLK}	-	9.27	-	MHz
Horizontal valid data	t_{hd}		480		DCLK
1 horizontal line	t_h	535	552	720	DCLK
Vertical valid data	t_{vd}		240		H
1 vertical field	t_v(1)(2)	248	280	600	H
Frame rate	FR(3)	-	60	-	Hz

Note: (1) Minimum value of vertical blanking **(t_v- t_{vd})** must ≥ 10H when traditional gate driver pre-scan application.
(2) Minimum value of vertical blanking **(t_v- t_{vd})** could support the GIP timing that must reference the GIP structure of panel. **(Minimum value of vertical blanking (t_v- t_{vd}) must ≥ (9+n)H, "n" is the number of lines where the GIP timing leads the DE signal at vertical blanking)**.
(3) FR **(Frame rate)**=F_{DCLK} / t_h / t_v.

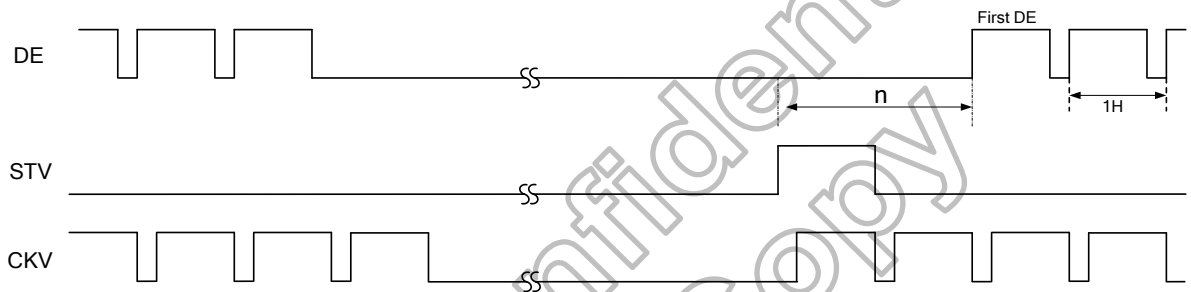


Table 6.2: Input timing table at DE only mode

6.6. Power on/off sequence

6.6.1. Power on sequence

A. If VSP and VSN are generated by PFM circuits:

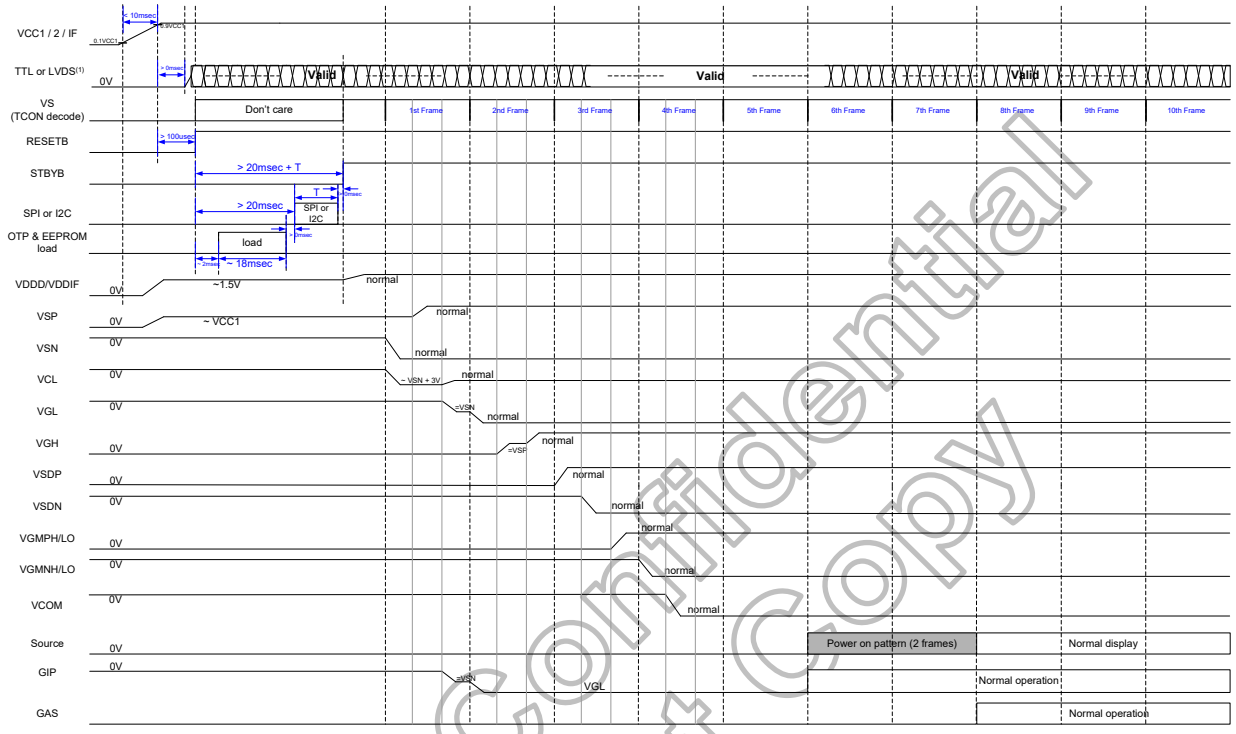


Figure 6.13: Power-on sequence with PFM

B. If VSP/VSN & VGH/VGL are generated by external power circuits:

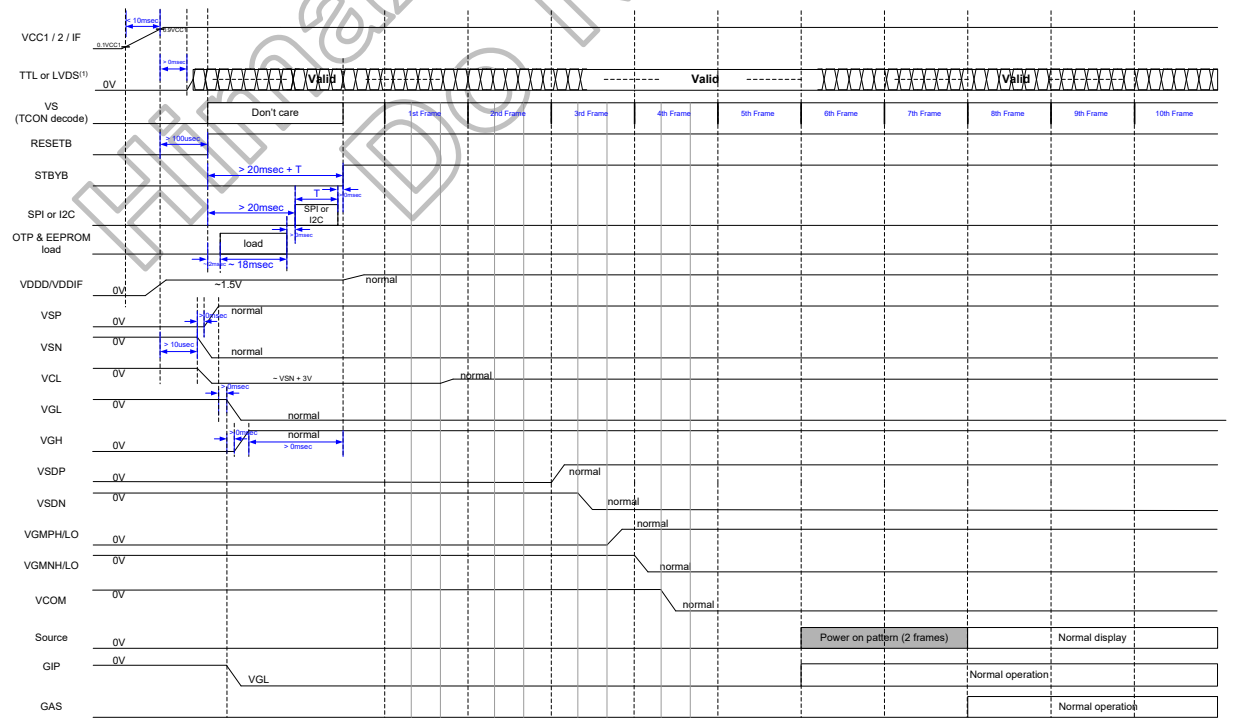


Figure 6.14: Power-on sequence with external power supply

6.6.2. Power off sequence

A. If VSP and VSN are generated by PFM circuits:

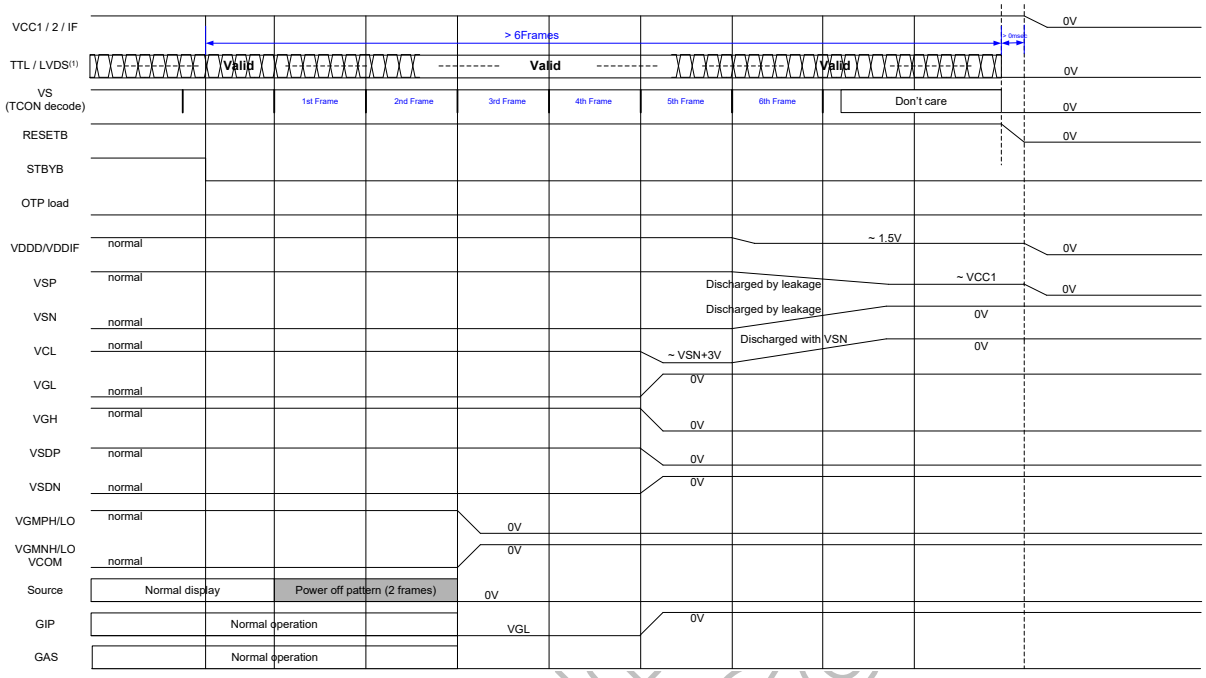


Figure 6.15: Power-off sequence with PFM

B. If VSP/VSN & VGH/VGL are generated by external power circuits:

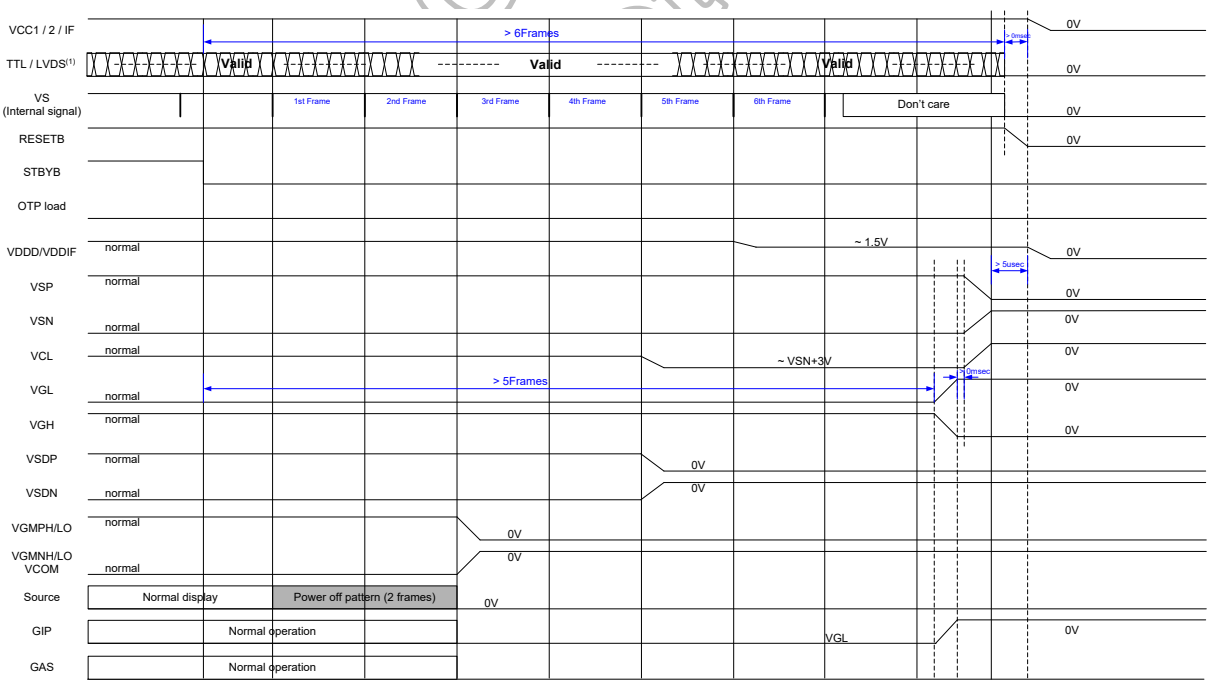


Figure 6.16: Power-off sequence with external power supply

Note: (1) The valid LVDS signals **(Clock pair and all data pairs in toggling state)** must be consistent with panel resolution and input timing specification.

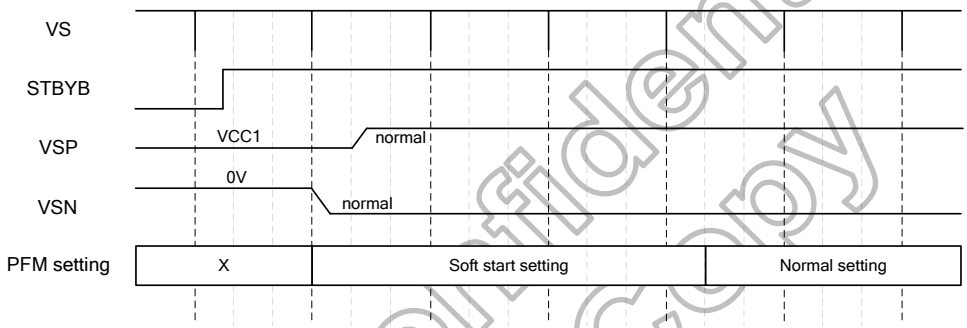
6.7. PFM setting parameter

In HX8272-C01-LT, PFM applies different settings to the power on sequence. Below table is the parameter setting for PFM soft start and normal mode.

	Soft Start	Normal
PFM parameter	VSPON_S[3:0](1) VSNON_S[3:0](2) VSPOFF_S[3:0](1) VSNOFF_S[3:0](2)	VSPON[3:0](3) VSNON[3:0](4) VSPOFF[3:0](3) VSNOFF[3:0](4)

Note: (1) VSPON_S[3:0] / VSPOFF_S[3:0] **(Page02h R0Ah)**
(2) VSNON_S[3:0] / VSNOFF_S[3:0] **(Page02h R0Bh)**
(3) VSPON[3:0] / VSPOFF[3:0] **(Page02h R08h)**
(4) VSNON[3:0] / VSNOFF[3:0] **(Page02h R09h)**

Table 6.3: PFM setting parameter



Note: (1) Soft start duration can be setting by register **(Page02h R10h[7:6]).**

Figure 6.17: PFM power on setting.

6.8. TP_SYNC1/TP_SYNC2 for touch panel synchronization

HX8272-C01-LT provides two output TP_SYNC1/TP_SYNC2 pins for touch panel synchronization. It can be adjusted by Page01h registers TP_SYNC1_SEL[2:0]/ TP_SYNC2_SEL[2:0], TP_WIDTH[7:0] & TP_DLY[7:0]. The related register let TP_SYNC1/TP_SYNC2 pin output is HS, VS, VDEN_INT, FAIL_DET, /XAO, or Source_SW.

VDEN_INT is an internal delayed version of VS, and its width is Vactive. Source_SW is OPA output enable time. TP_DLY[7:0] is TP_SYNC1/TP_SYNC2 timing adjustment, and it is effective only when TP_SYNC1_SEL[2:0]/TP_SYNC2_SEL[2:0]=3'b110.

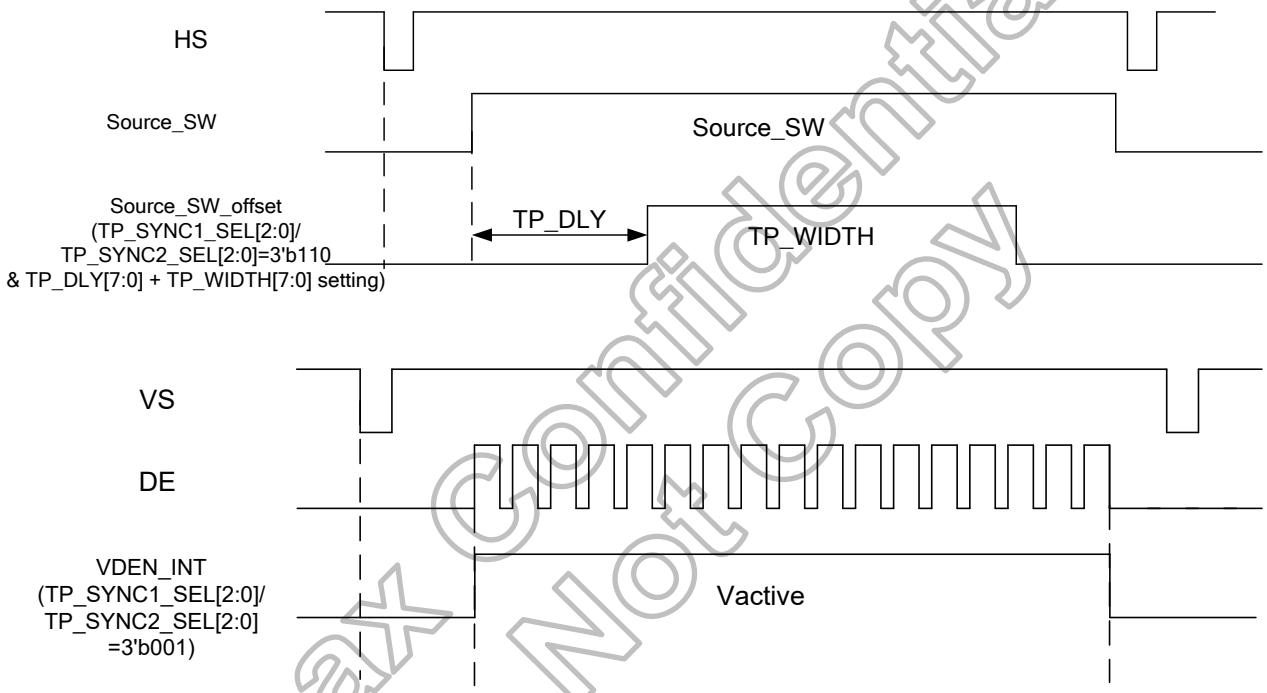


Figure 6.18: TP_SYNC timing adjustment

6.9. Built-In Self Test function

A BIST **(Built-In Self Test)** pattern generator is embedded in HX8272-C01-LT for aging mode. When BISTEN is set to 1 **(by input pin or register)**, HX8272-C01-LT will generate the following patterns. When the bit of register PTSEL[15:0] **(Page08h R07h[7:0]~R08h[7:0])** to be asserted, means that the corresponding patterns to be selected. The selected patterns will be displayed sequentially and periodically.

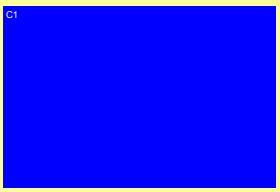
PTSEL[15:0](1)	Pattern name	Color	R	G	B
[0]	Full Black	C1	0	0	0
[1]	Full White	C1	255	255	255
[2]	Full Red	C1	255	0	0
[3]	Full Green	C1	0	255	0
[4]	Full Blue	C1	0	0	255
[5]	Color Bar	C1	0	0	0
		C2	0	0	255
		C3	255	0	0
		C4	255	0	255
		C5	0	255	0
		C6	0	255	255
		C7	255	255	0
		C8	255	255	255
[6]	Gray Scale 16	C1	0	0	0
		C2	17	17	17
		C3	34	34	34
		C4	51	51	51
		C5	68	68	68
		C6	85	85	85
		C7	102	102	102
		C8	119	119	119
		C9	136	136	136
		C10	153	153	153
		C11	170	170	170
		C12	187	187	187
		C13	204	204	204
		C14	221	221	221
		C15	238	238	238
		C16	255	255	255
[7]	Checkerboard **(32x32)**	C1	0	0	0
		C2	255	255	255
[8]	Cross talk	C1	128	128	128
		C2	0	0	0
[9]	VCOM trimming	C1	0	0	0
		C2	128	128	128
[10]	V Gray scale 256(2)	C1	0~255 increase by Int(Vactive/256) line		
[11]	RGBW	C1	0	0	255
		C2	255	0	0
		C3	255	255	255
		C4	0	255	0
[12]	BIST Gray level(3)	C1	128	128	128
[13]	White boarder	C1	255	255	255
		C2	0	0	0
[14]	Pixel on/off	-	255 / 0	255 / 0	255 / 0
[15]	Dot on/off	-	255 / 0	255 / 0	255 / 0

Note: (1) If GATEPASS[3:0] **(Page00h R11h[7:4])**=0101 or HSETPASS[3:0] **(Page00h R13h[7:4])**=0101 is enabled. The frame rate of the display can't guarantee 60Hz at BIST mode.
(2) V Gray scale 256 Pattern: 0~255 increase by one line when Vactive < 256 Line.
(3) BIST gray level depends on Register **Page00h R17h** setting value.

Table 6.4: BIST patterns

Pattern 0: Full Black

Pattern 4: Full Blue

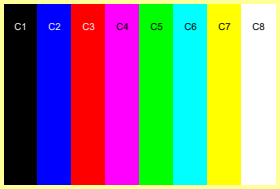


Pattern 8: Cross talk

Pattern 12: BIST Gray level

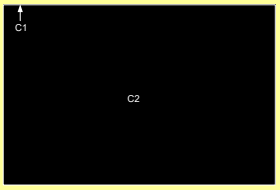
Pattern 1: Full White

Pattern 5: Color Bar

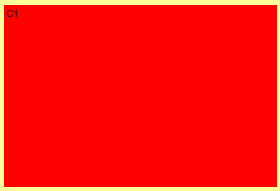


Pattern 9: VCOM trimming

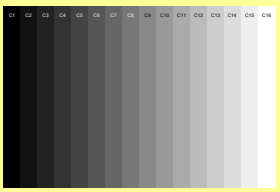
Pattern 13: White border



Pattern 2: Full Red

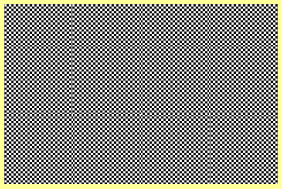


Pattern 6: Gray Scale 16

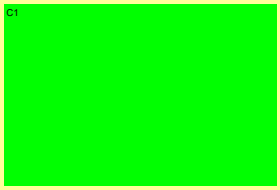


Pattern 10: V Gray scale 256

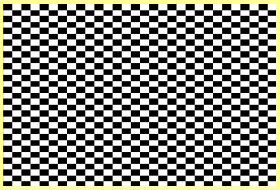
Pattern 14: Pixel on/off



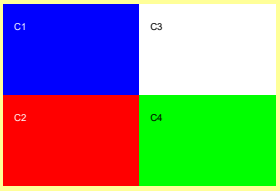
Pattern 3: Full Green



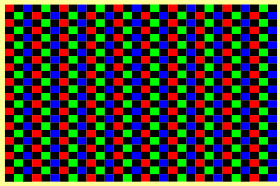
Pattern 7: Checker board



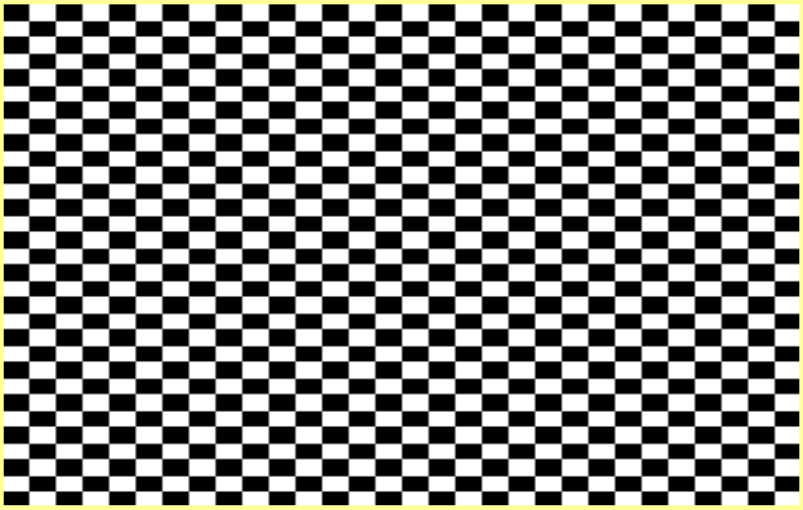
Pattern 11: RGBW pattern

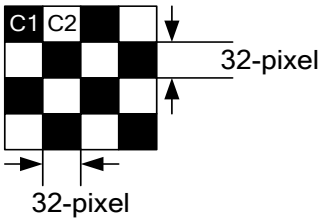


Pattern 15: Dot on/off



Pattern 7: Checkerboard





Note: (1) Pattern 7 Checkerboard pattern is combination of the 32-pixel x 32-pixel black and white block.
(2) Pattern 9 VCOM trimming pattern type is depended on the inversion method. In addition, Zig-Zag type panel only support column inversion VCOM trimming pattern

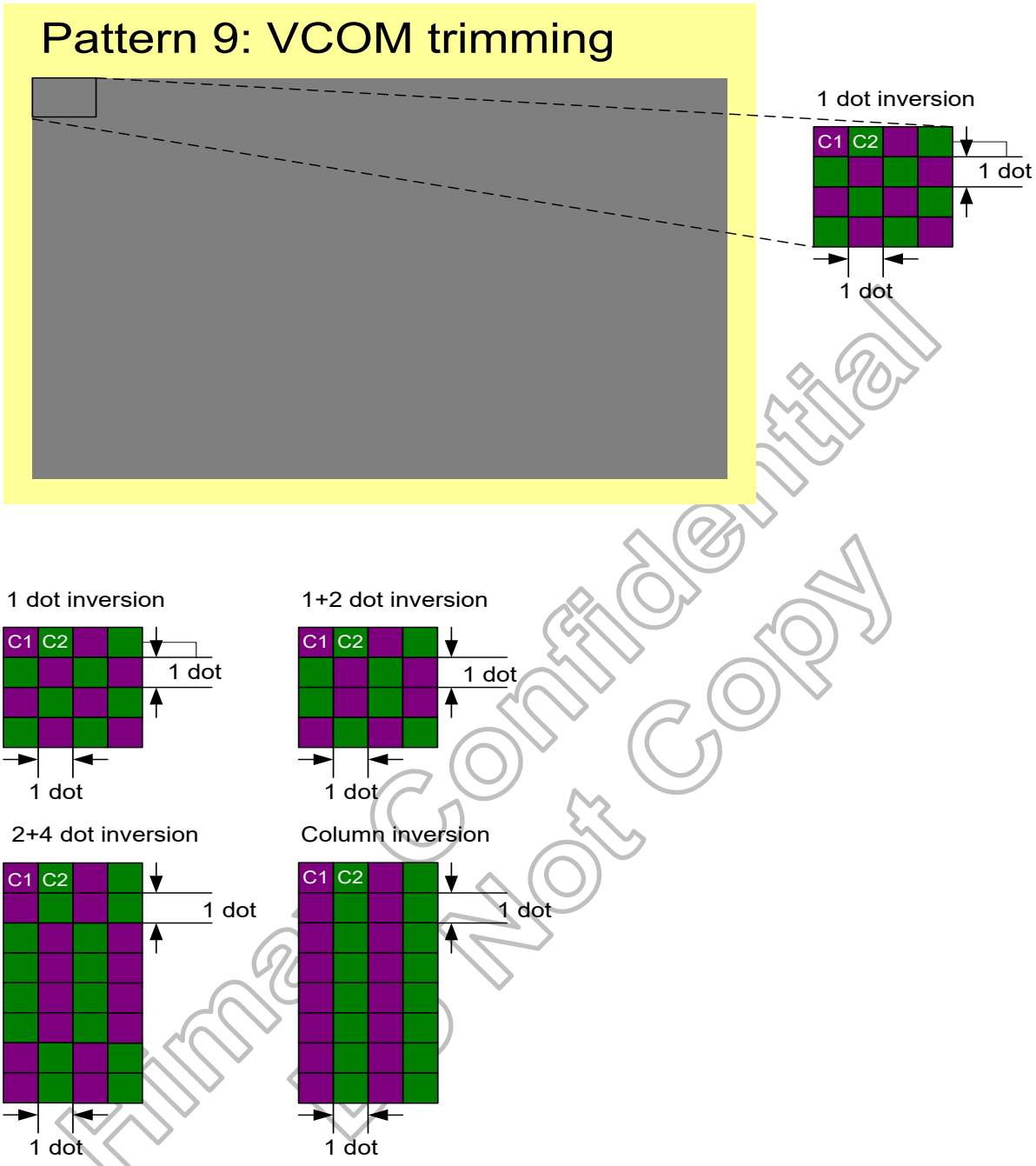


Figure 6.19: BIST patterns

6.10. Protection function

6.10.1. GAS function

When power is removed from an electronic device, the image still keeps on the LCD panel for a long time. GAS **(Gate all select)** function can speed up the process that image disappears.

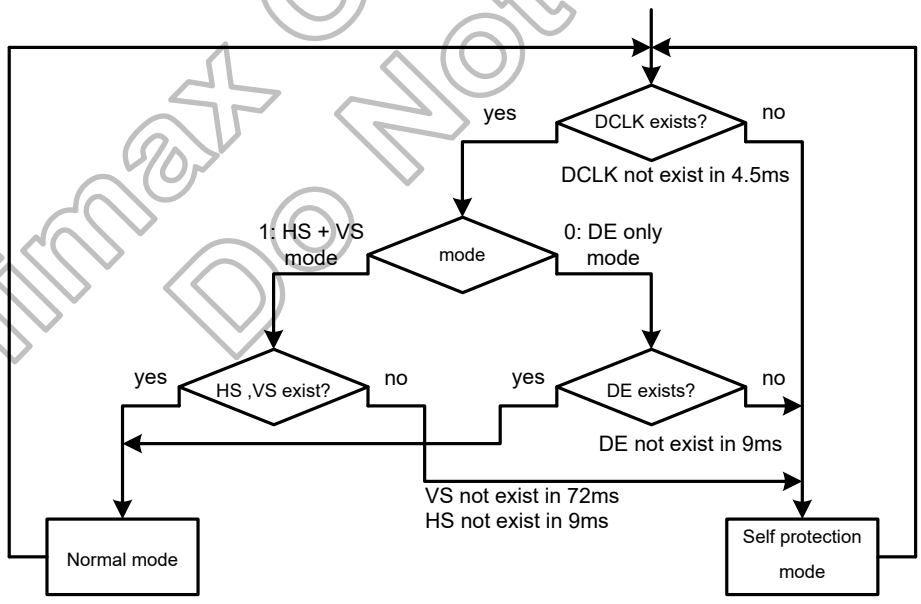
HX8272-C01-LT can detect abnormally low voltage and send GIP signal to the gate by the register setting to discharge residual potential in LCD panel and removes image.

Any one of the following cases with duration larger than 10μs will trigger GAS function.

A. VCC1 is lower than 2.5V
B. VSP is lower than 4V
C. VSN is higher than -4V

6.10.2. Self protection mode

HX8272-C01-LT keeps detecting input signals DE, HS, VS, and DCLK. If any of these signals is missing, HX8272-C01-LT will enter self protection mode. In the self protection mode, it would display black or white pattern which could be set by the register. The flow is shown as below figure.



Note: (1) This flow is done regardless of LVDS Lock / Unlock.

Figure 6.20: Self-protection detection

6.10.3. Over current protection

HX8272-C01-LT detects the PFM current by monitoring VMONP and VMONN. In any one of the following cases, the chip will entry over current protection.

A. DRVP is set to VSS to turn off the external NMOS immediately when VMONP is over its threshold voltage.
B. DRVN is set to VDD to turn off the external PMOS immediately when VMONN is over its threshold voltage.

VMONPS[1:0]: VSP over current detection voltage selection.

VMONPS[1:0]		Function	Note
0	0	0.100V	-
0	1	0.125V	-
1	0	0.150V	Default
1	1	0.175V	-

VMONNS[1:0]: VSN over current detection voltage selection.

VMONNS[1:0]		Function	Note
0	0	0.100V	-
0	1	0.125V	-
1	0	0.150V	Default
1	1	0.175V	-

6.11. FAIL detect function

HX8272-C01-LT can detect abnormally condition to set the FAIL_DET to low.

Any one of the following cases will trigger the fail detect function to set the FAIL_DET to low. Those follow cases can be enable or disable separate by the register Page02h R15h~R16h.

A. OTP values are different with register values after OTP programming.
B. Checksum of EEPROM is wrong after EEPROM reloading.
C. Input signals are detected fail to enter self protection mode.
D. STV signal is detected fail for tradition Gate driver only.
E. Internal source signal output fail.
F. Abnormal low voltages are detected to enter GAS function.
G. Input LVDS signals are unlock.
H. GIP feedback signal failure detection.

6.12. GATE_NUM_SEL function

GATE_NUM_SEL is a special feature for HX8272-C01-LT that can satisfy a variety of vertical resolutions. It can support DE, SYNC and BIST modes. Set GATEPASS[3:0] =1010 **(at Page00h R10h[7:4])** to enable the GATE_NUM_SEL, vertical resolution t_{vd} is controlled by GATENUM[11:0] **(at Page00h R10h[3:0] & R11h[7:0])**.

The vertical lines of front-end timing must same as GATENUM[11:0] when GATEPASS is enable.

6.13. OTP programming sequence

When programming OTP function, the initial value should be written by following steps.

The FAIL detection function will detect OTP trimming status.

SIDEN=L, OTP program sequence is executed to all chip. SIDEN=H, OTP program sequence that each chip needs to execute independently by SID[1:0] of command.

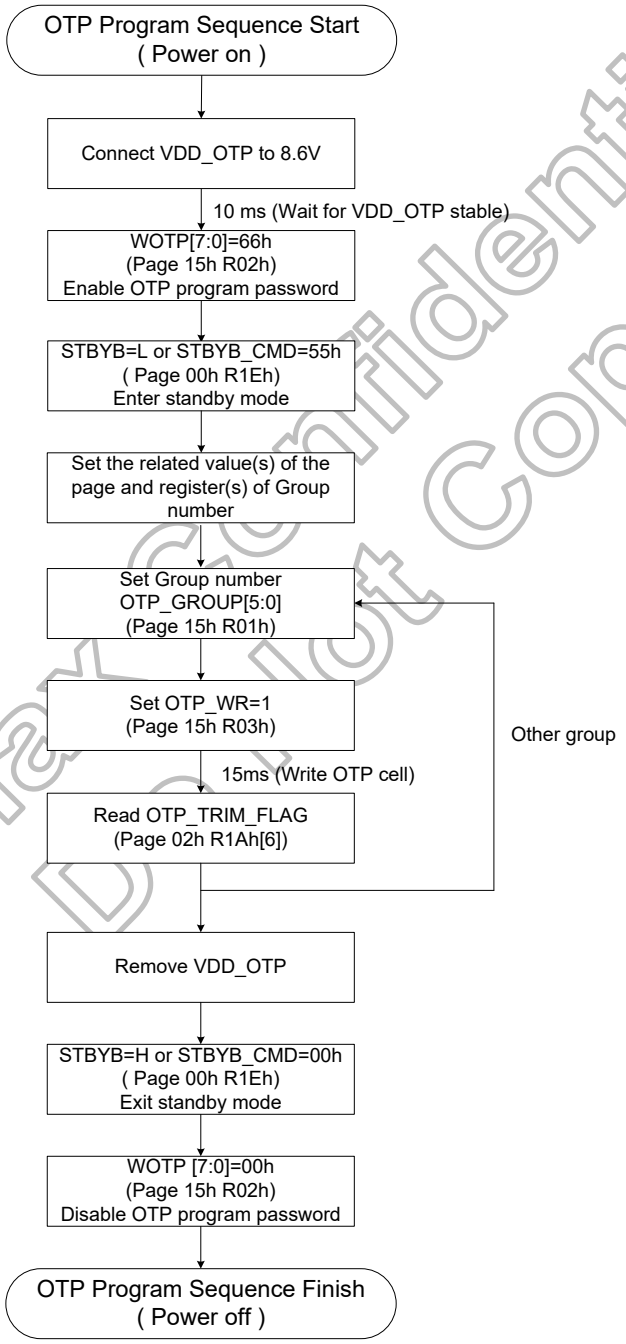


Figure 6.21: OTP program-group flow

6.14. OTP marginal read sequence

OTP marginal reload provides a critical read condition to filter out “weak programmed” bits. To cover all worse corners, it should be implemented after programming OTP.

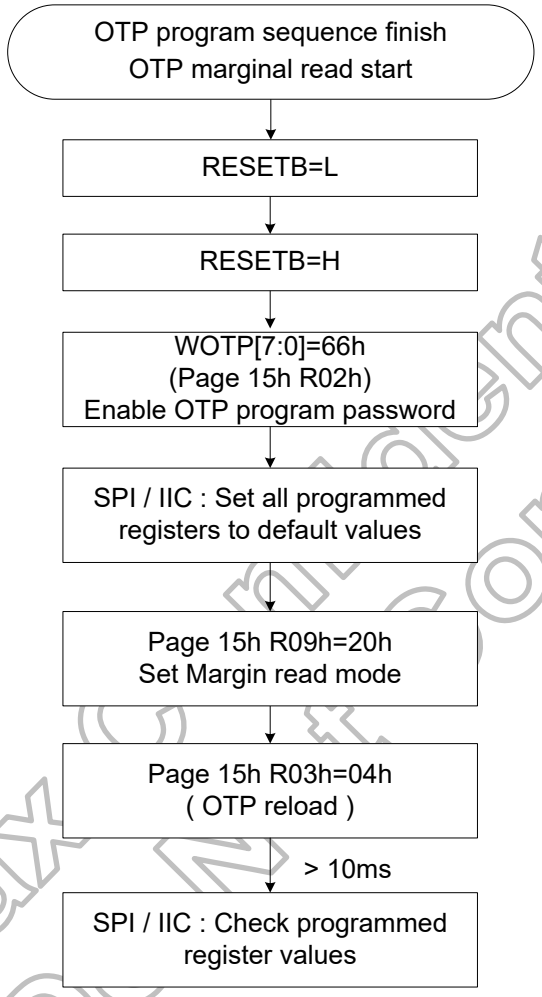


Figure 6.22: OTP marginal read flow

6.15. SPI interface

HX8272-C01-LT supports 3/4-wire SPI **(Serial peripheral interface)** to set internal registers. Setting one command needs 16 SCL clocks. The address and data are transferred from the MSB to LSB edge sequentially at SCL rising edge. Note that ATREN should be set to low when accessing SPI.

A. The first bit R/W selects read/write mode. Setting R/W to 0 selects write mode and setting R/W to 1 selects read mode.
B. If there are two chips or three chips cascaded, the second and third bits SID[1:0] select chip being active. Note that when SIDEN=L and R/W=1, only read from the master chip.
C. Short the SDAI and SDAO together for 3-wire SPI application.
D. A[4:0] specify the address of the register to be read or written.
E. D[7:0] is the 8-bit data of each register.

SIDEN	R/W	SID[1:0]	Function	Target
L	1	xx	Read	Master
	0	xx	Write	Master and slave
H	1	00	Read	Master
		01		Slave 1
		10		Slave 2
		11		Slave 3
	0	00	Write	Master
		01		Slave 1
		10		Slave 2
		11		Slave 3

Table 6.5: SPI timing parameter

6.15.1. SPI normal read/write mode

In normal write mode, the read/write control bit must be set to 0, and SDAI is address input and data input pin.

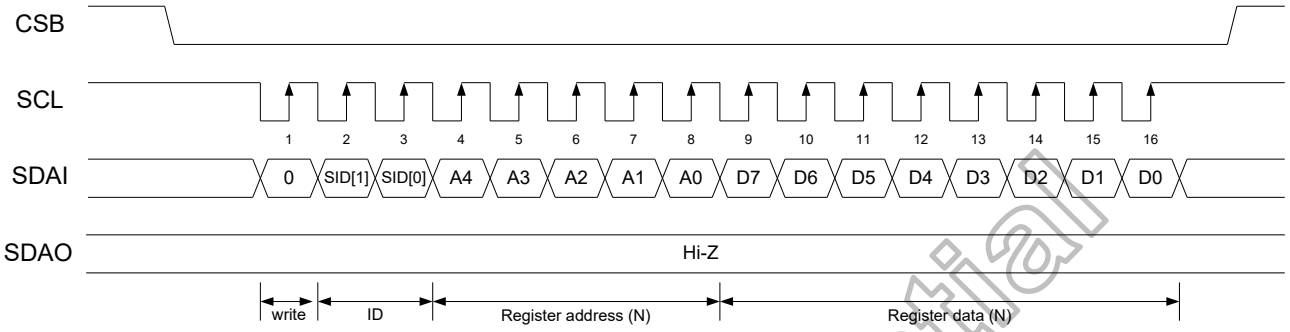


Figure 6.23: SPI signals, normal write mode

In normal read mode, the read/write control bit must be set to 1. The SDAI is address input pin and SDAO is data output pin.

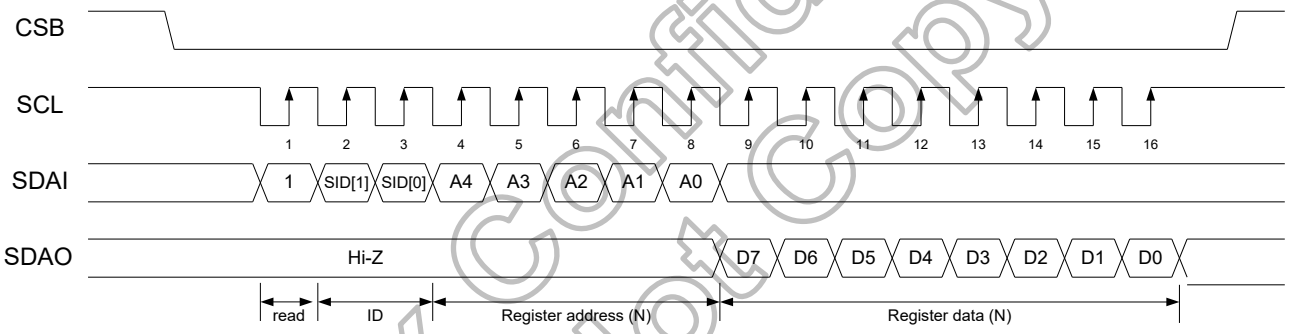


Figure 6.24: SPI signals, normal read mode

6.15.2. SPI burst read/write mode

HX8272-C01-LT supports burst mode for writing all registers one time. After choose Page want to write, only the start address is needed, and repeats one set of 8 SCL pulses to access the following registers sequentially.

In burst write mode, the read/write control bit must be set to 0, and SDAI is address input and data input pin.

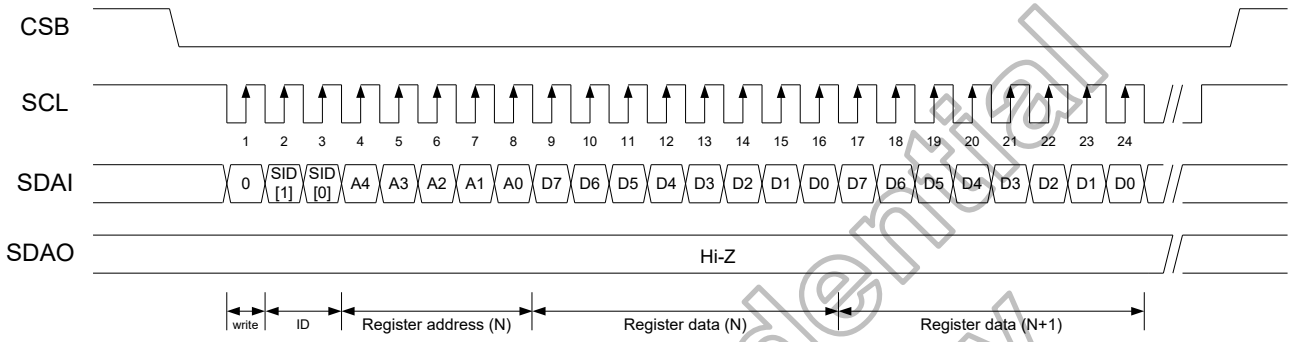


Figure 6.25: SPI signals, burst write mode

In burst read mode, the read/write control bit must be set to 1. The SDAI is address input pin and SDAO is data output pin.

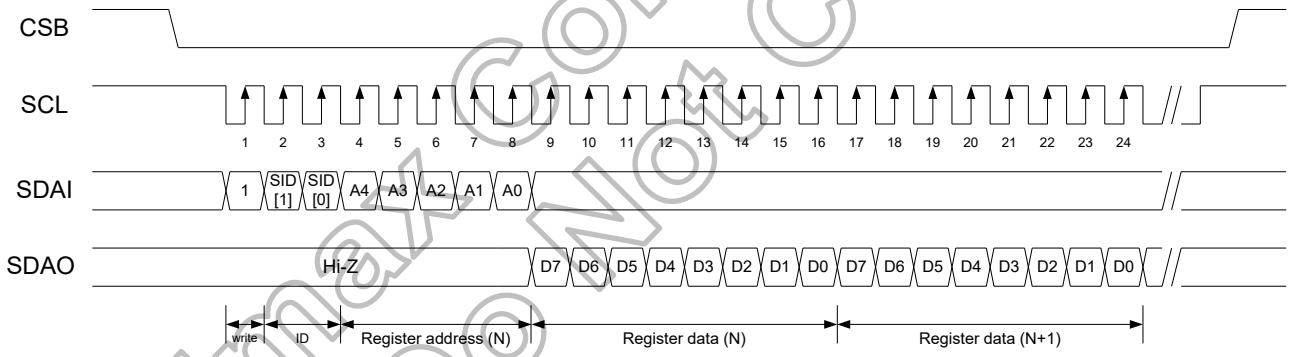


Figure 6.26: SPI signals, burst read mode

6.16. I2C interface

HX8272-C01-LT supports 2-wire serial interface **(I2C)** to set internal registers.
HX8272-C01-LT is a slave device, and the slave address is fixed 1010010.

A. If there are many chips cascaded, the second and third bits SID[1:0] select chip being active. Note that when SIDEN=L and R/W=1, only read from the master chip.
B. If there are many chips cascaded, when Master chip and Slave chips received the slave address from Host, the ACK will response from Master chip **(SID[1:0]=00)** only.

SIDEN	R/W	SID[1:0]	Function	Target
L	1	xx	Read	Master
	0	xx	Write	Master and slave
H	1	00	Read	Master
		01		Slave 1
		10		Slave 2
		11		Slave 3
	0	00	Write	Master
		01		Slave 1
		10		Slave 2
		11		Slave 3

Table 6.6: I2C timing parameter

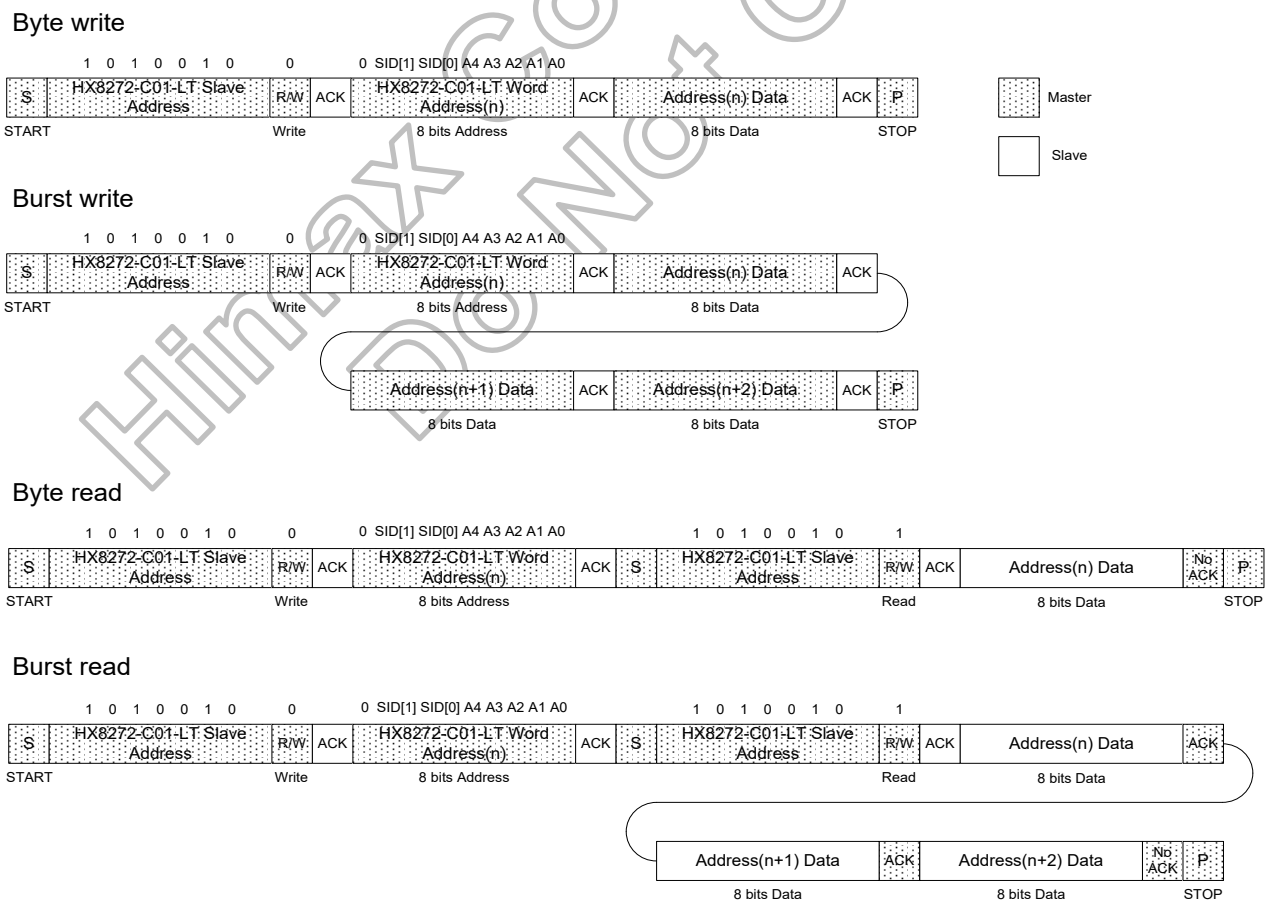


Figure 6.27: I2C R/W format

7. Gamma Correction Function

7.1. Gamma reference voltage

For positive polarity, two voltages VGMPHO/VGMPLO are generated as gamma reference. They are connected to VGMPHI/VGMPLI and used to generate all gamma reference voltages.

GSH0/2/4/8/14/23/31/47/79/111/143/175/207/223/231/240/246/251/253/255, and all grayscale voltages are GSH[0:255].

For negative polarity, the structure is exactly the same to positive gamma circuit.

Setting for positive gamma voltage

Gamma code	Register	Reference voltage
GSH0	T_VP0_[4:0]	VGMPL + (1/512)*(VP0_[4:0]*2)*(VGMPH – VGMPL)
GSH2	T_VP2_[5:0]	VGMPL + (1/512)*(VP2_[5:0]*2 + 2)*(VGMPH – VGMPL)
GSH4	T_VP4_[5:0]	VGMPL + (1/512)*(VP4_[5:0]*2 + 10)*(VGMPH – VGMPL)
GSH8	T_VP8_[5:0]	VGMPL + (1/512)*(VP8_[5:0]*2 + 28)*(VGMPH – VGMPL)
GSH14	T_VP14_[5:0]	VGMPL + (1/512)*(VP14_[5:0]*2 + 53)*(VGMPH – VGMPL)
GSH23	T_VP23_[5:0]	GSH14 + (1/250)*(VP23_[5:0] + 5)*(GSH240 – GSH14)
GSH31	T_VP31_[5:0]	GSH14 + (1/250)*(VP31_[5:0] + 13)*(GSH240 – GSH14)
GSH47	T_VP47_[5:0]	GSH14 + (1/250)*(VP47_[5:0] + 27)*(GSH240 – GSH14)
GSH79	T_VP79_[5:0]	GSH14 + (1/250)*(VP79_[5:0] + 47)*(GSH240 – GSH14)
GSH111	T_VP111_[5:0]	GSH14 + (1/250)*(VP111_[5:0] + 67)*(GSH240 – GSH14)
GSH143	T_VP143_[5:0]	GSH14 + (1/250)*(VP143_[5:0] + 87)*(GSH240 – GSH14)
GSH175	T_VP175_[5:0]	GSH14 + (1/250)*(VP175_[5:0] + 123)*(GSH240 – GSH14)
GSH207	T_VP207_[5:0]	GSH14 + (1/250)*(VP207_[5:0] + 163)*(GSH240 – GSH14)
GSH223	T_VP223_[5:0]	GSH14 + (1/250)*(VP223_[5:0] + 183)*(GSH240 – GSH14)
GSH231	T_VP231_[5:0]	GSH14 + (1/250)*(VP231_[5:0] + 186)*(GSH240 – GSH14)
GSH240	T_VP240_[5:0]	VGMPL + (1/512)*(VP240_[5:0]*2 + 334)*(VGMPH – VGMPL)
GSH246	T_VP246_[5:0]	VGMPL + (1/512)*(VP246_[5:0]*2 + 376)*(VGMPH – VGMPL)
GSH251	T_VP251_[5:0]	VGMPL + (1/512)*(VP251_[5:0]*2 + 380)*(VGMPH – VGMPL)
GSH253	T_VP253_[5:0]	VGMPL + (1/512)*(VP253_[5:0]*2 + 384)*(VGMPH – VGMPL)
GSH255	T_VP255_[4:0]	VGMPL + (1/512)*(VP255_[4:0]*2 + 450)*(VGMPH – VGMPL)

Setting for negative gamma voltage

Gamma code	Register	Reference voltage
GSL0	T_VN0_[4:0]	VGMNL + (1/512)*(VN0_[4:0]*2)*(VGMNH – VGMNL)
GSL2	T_VN2_[5:0]	VGMNL + (1/512)*(VN2_[5:0]*2 + 2)*(VGMNH – VGMNL)
GSL4	T_VN4_[5:0]	VGMNL + (1/512)*(VN4_[5:0]*2 + 10)*(VGMNH – VGMNL)
GSL8	T_VN8_[5:0]	VGMNL + (1/512)*(VN8_[5:0]*2 + 28)*(VGMNH – VGMNL)
GSL14	T_VN14_[5:0]	VGMNL + (1/512)*(VN14_[5:0]*2 + 53)*(VGMNH – VGMNL)
GSL23	T_VN23_[5:0]	GSL14 + (1/250)*(VN23_[5:0] + 5)*(GSL240 – GSL14)
GSL31	T_VN31_[5:0]	GSL14 + (1/250)*(VN31_[5:0] + 13)*(GSL240 – GSL14)
GSL47	T_VN47_[5:0]	GSL14 + (1/250)*(VN47_[5:0] + 27)*(GSL240 – GSL14)
GSL79	T_VN79_[5:0]	GSL14 + (1/250)*(VN79_[5:0] + 47)*(GSL240 – GSL14)
GSL111	T_VN111_[5:0]	GSL14 + (1/250)*(VN111_[5:0] + 67)*(GSL240 – GSL14)
GSL143	T_VN143_[5:0]	GSL14 + (1/250)*(VN143_[5:0] + 87)*(GSL240 – GSL14)
GSL175	T_VN175_[5:0]	GSL14 + (1/250)*(VN175_[5:0] + 123)*(GSL240 – GSL14)
GSL207	T_VN207_[5:0]	GSL14 + (1/250)*(VN207_[5:0] + 163)*(GSL240 – GSL14)
GSL223	T_VN223_[5:0]	GSL14 + (1/250)*(VN223_[5:0] + 183)*(GSL240 – GSL14)
GSL231	T_VN231_[5:0]	GSL14 + (1/250)*(VN231_[5:0] + 186)*(GSL240 – GSL14)
GSL240	T_VN240_[5:0]	VGMNL + (1/512)*(VN240_[5:0]*2 + 334)*(VGMNH – VGMNL)
GSL246	T_VN246_[5:0]	VGMNL + (1/512)*(VN246_[5:0]*2 + 376)*(VGMNH – VGMNL)
GSL251	T_VN251_[5:0]	VGMNL + (1/512)*(VN251_[5:0]*2 + 380)*(VGMNH – VGMNL)
GSL253	T_VN253_[5:0]	VGMNL + (1/512)*(VN253_[5:0]*2 + 384)*(VGMNH – VGMNL)
GSL255	T_VN255_[4:0]	VGMNL + (1/512)*(VN255_[4:0]*2 + 450)*(VGMNH – VGMNL)

7.1.1. Resistor ratio for gamma code

Resistor ratio in the resistor chain 3 of both positive and negative gamma circuits is described in the following table. The resistor RGMA[k] is between GSH[k] and GSH[k-1], or GSL[k] and GSL[k-1].

Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio
RGMA[255]	17R	RGMA[223]	4.3325R	RGMA[191]	2.8125R	RGMA[159]	2.1875R
RGMA[254]	16R	RGMA[222]	4.3325R	RGMA[190]	2.8125R	RGMA[158]	2.1875R
RGMA[253]	14.5R	RGMA[221]	4.3325R	RGMA[189]	2.8125R	RGMA[157]	2.1875R
RGMA[252]	13R	RGMA[220]	4.3325R	RGMA[188]	2.8125R	RGMA[156]	2.1875R
RGMA[251]	13R	RGMA[219]	4.0625R	RGMA[187]	2.75R	RGMA[155]	2.125R
RGMA[250]	12R	RGMA[218]	4.0625R	RGMA[186]	2.75R	RGMA[154]	2.125R
RGMA[249]	12R	RGMA[217]	4.0625R	RGMA[185]	2.75R	RGMA[153]	2.125R
RGMA[248]	11R	RGMA[216]	4.0625R	RGMA[184]	2.75R	RGMA[152]	2.125R
RGMA[247]	11R	RGMA[215]	3.8125R	RGMA[183]	2.625R	RGMA[151]	2.0625R
RGMA[246]	10R	RGMA[214]	3.8125R	RGMA[182]	2.625R	RGMA[150]	2.0625R
RGMA[245]	10R	RGMA[213]	3.8125R	RGMA[181]	2.625R	RGMA[149]	2.0625R
RGMA[244]	9R	RGMA[212]	3.8125R	RGMA[180]	2.625R	RGMA[148]	2.0625R
RGMA[243]	9R	RGMA[211]	3.5R	RGMA[179]	2.5R	RGMA[147]	2R
RGMA[242]	8R	RGMA[210]	3.5R	RGMA[178]	2.5R	RGMA[146]	2R
RGMA[241]	8R	RGMA[209]	3.5R	RGMA[177]	2.5R	RGMA[145]	2R
RGMA[240]	7R	RGMA[208]	3.5R	RGMA[176]	2.5R	RGMA[144]	2R
RGMA[239]	7R	RGMA[207]	3.5R	RGMA[175]	2.5R	RGMA[143]	2R
RGMA[238]	6.5R	RGMA[206]	3.5R	RGMA[174]	2.5R	RGMA[142]	2R
RGMA[237]	6R	RGMA[205]	3.5R	RGMA[173]	2.5R	RGMA[141]	2R
RGMA[236]	5.75R	RGMA[204]	3.5R	RGMA[172]	2.5R	RGMA[140]	2R
RGMA[235]	5.5R	RGMA[203]	3.3125R	RGMA[171]	2.375R	RGMA[139]	1.9375R
RGMA[234]	5.25R	RGMA[202]	3.3125R	RGMA[170]	2.375R	RGMA[138]	1.9375R
RGMA[233]	5R	RGMA[201]	3.3125R	RGMA[169]	2.375R	RGMA[137]	1.9375R
RGMA[232]	4.75R	RGMA[200]	3.3125R	RGMA[168]	2.375R	RGMA[136]	1.9375R
RGMA[231]	4.75R	RGMA[199]	3.0625R	RGMA[167]	2.3125R	RGMA[135]	1.9375R
RGMA[230]	4.75R	RGMA[198]	3.0625R	RGMA[166]	2.3125R	RGMA[134]	1.9375R
RGMA[229]	4.75R	RGMA[197]	3.0625R	RGMA[165]	2.3125R	RGMA[133]	1.9375R
RGMA[228]	4.5R	RGMA[196]	3.0625R	RGMA[164]	2.3125R	RGMA[132]	1.9375R
RGMA[227]	4.5R	RGMA[195]	2.9375R	RGMA[163]	2.25R	RGMA[131]	1.915R
RGMA[226]	4.5R	RGMA[194]	2.9375R	RGMA[162]	2.25R	RGMA[130]	1.915R
RGMA[225]	4.5R	RGMA[193]	2.9375R	RGMA[161]	2.25R	RGMA[129]	1.915R
RGMA[224]	4.66R	RGMA[192]	2.9375R	RGMA[160]	2.25R	RGMA[128]	1.915R

Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio	Gamma code	Resistor ratio
RGMA[127]	1.915R	RGMA[95]	1.875R	RGMA[63]	2.3125R	RGMA[31]	3.75R
RGMA[126]	1.915R	RGMA[94]	1.875R	RGMA[62]	2.3125R	RGMA[30]	4.2R
RGMA[125]	1.915R	RGMA[93]	1.875R	RGMA[61]	2.3125R	RGMA[29]	4.33R
RGMA[124]	1.915R	RGMA[92]	1.875R	RGMA[60]	2.3125R	RGMA[28]	4.5R
RGMA[123]	1.875R	RGMA[91]	1.875R	RGMA[59]	2.4375R	RGMA[27]	4.66R
RGMA[122]	1.875R	RGMA[90]	1.875R	RGMA[58]	2.4375R	RGMA[26]	4.75R
RGMA[121]	1.875R	RGMA[89]	1.875R	RGMA[57]	2.4375R	RGMA[25]	5R
RGMA[120]	1.875R	RGMA[88]	1.875R	RGMA[56]	2.4375R	RGMA[24]	5.1R
RGMA[119]	1.875R	RGMA[87]	1.875R	RGMA[55]	2.5625R	RGMA[23]	5.2R
RGMA[118]	1.875R	RGMA[86]	1.875R	RGMA[54]	2.5625R	RGMA[22]	5.5R
RGMA[117]	1.875R	RGMA[85]	1.875R	RGMA[53]	2.5625R	RGMA[21]	5.8R
RGMA[116]	1.875R	RGMA[84]	1.875R	RGMA[52]	2.5625R	RGMA[20]	6R
RGMA[115]	1.875R	RGMA[83]	1.875R	RGMA[51]	2.75R	RGMA[19]	6.2R
RGMA[114]	1.875R	RGMA[82]	1.875R	RGMA[50]	2.75R	RGMA[18]	6.33R
RGMA[113]	1.875R	RGMA[81]	1.875R	RGMA[49]	2.75R	RGMA[17]	6.5R
RGMA[112]	1.875R	RGMA[80]	1.875R	RGMA[48]	2.75R	RGMA[16]	6.75R
RGMA[111]	1.875R	RGMA[79]	2R	RGMA[47]	2.875R	RGMA[15]	7.125R
RGMA[110]	1.875R	RGMA[78]	2R	RGMA[46]	2.875R	RGMA[14]	8R
RGMA[109]	1.875R	RGMA[77]	2R	RGMA[45]	2.875R	RGMA[13]	8.25R
RGMA[108]	1.875R	RGMA[76]	2R	RGMA[44]	2.875R	RGMA[12]	8.75R
RGMA[107]	1.875R	RGMA[75]	2.0625R	RGMA[43]	3.0625R	RGMA[11]	9.5R
RGMA[106]	1.875R	RGMA[74]	2.0625R	RGMA[42]	3.0625R	RGMA[10]	10.25R
RGMA[105]	1.875R	RGMA[73]	2.0625R	RGMA[41]	3.0625R	RGMA[9]	10.5R
RGMA[104]	1.875R	RGMA[72]	2.0625R	RGMA[40]	3.0625R	RGMA[8]	12R
RGMA[103]	1.875R	RGMA[71]	2.125R	RGMA[39]	3.3125R	RGMA[7]	13R
RGMA[102]	1.875R	RGMA[70]	2.125R	RGMA[38]	3.3125R	RGMA[6]	14R
RGMA[101]	1.875R	RGMA[69]	2.125R	RGMA[37]	3.3125R	RGMA[5]	13R
RGMA[100]	1.875R	RGMA[68]	2.125R	RGMA[36]	3.3125R	RGMA[4]	11R
RGMA[99]	1.875R	RGMA[67]	2.20825R	RGMA[35]	3.5R	RGMA[3]	10R
RGMA[98]	1.875R	RGMA[66]	2.20825R	RGMA[34]	3.5R	RGMA[2]	9R
RGMA[97]	1.875R	RGMA[65]	2.20825R	RGMA[33]	3.5R	RGMA[1]	8R
RGMA[96]	1.875R	RGMA[64]	2.20825R	RGMA[32]	3.5R	-	-

8. Register Function

8.1. Register table

8.1.1. Register table: Page00h (Normal function)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	30h	R/W	[7]	DUAL_ZZ_SEL	Zig-Zag type sub-option.	Group 01h **(2)**
			[6:4]	PANEL_TYPE[2:0]	Panel type selection.	
			[3]	RESET_GAS_OPT	RESETB_SLP Sleep or GAS mode option.	
			[2:1]	ZIG-ZAG_TYPE[1:0]	Zig-Zag type selection.	
			[0]	GDSEL	Gate type selection.	
02h	F1h	R/W	[7:6]	TR[1:0]	Interface selection.	
			[5]	DINT	Input data 6-bit or 8-bit selection.	
			[4]	MODE	Sync or DE mode selection.	
			[3]	HSP	HS polarity.	
			[2]	VSP	VS polarity.	
			[1]	CLOCKP	Clock latch data edge for TTL mode.	
			[0]	NB	Normally white/black selection.	
03h	03h	R/W	[7]	RL	Horizontal scan direction.	
			[6]	TB	Vertical scan direction.	
			[5:4]	INV[1:0]	Inversion algorithm selection.	
			[3:0]	RS[3:0]	Resolution selection.	
04h	00h	R/W	[7]	RB_INV	R data and B data exchange.	
			[6]	DGAMEN	Digital Gamma function enable.	
			[5:4]	GPOS[1:0]	Tradition Gate driver location.	
			[3:2]	SD_GND_V[1:0]	Source output state in vertical blanking.	
			[1]	PON	White/Black pattern selection at power on sequence.	
			[0]	POFF	White/Black pattern selection at power off sequence.	
05h	CCh	R/W	[7]	GAS_VSPN_EN	GAS detect VSP/VSN enable.	
			[6]	SPFEN	Self-protection mode enables.	
			[5]	SPFSEL	White/Black pattern selection in self-protection mode.	
			[4]	BISTEN	BIST mode enable.	
			[3:2]	-	Reserved.	
			[1:0]	BIST_FNUM[1:0]	BIST pattern refresh frame setting.	
06h	18h	R/W	[7:0]	VSTS[7:0]	Vertical back porch adjustment.	Group 02h **(2)**
07h	10h	R/W	[7:0]	HSTS[7:0]	Horizontal back porch adjustment.	
08h	07h	R/W	[7:6]	ENDRVP[1:0]	Source driver capability selection.	
			[5:0]	OEW[5:0]	Timing for gate driver control.	
09h	06h	R/W	[7:6]	ENDRVN[1:0]	Source driver capability selection.	
			[5:0]	GEQW[5:0]	Timing for gate driver control.	
0Ah	86h	R/W	[7:6]	PCR[1:0]	Source SW divided selection.	
			[5:0]	EQ0W[5:0]	Time for pre-charging source output to ground.	
0Bh	B0h	R/W	[7]	-	Reserved.	
			[6:4]	BC[2:0]	Source driver bias current selection.	
			[3:2]	POCSD[1:0]	Source output offset cancelling selection.	
			[1:0]	POCGM[1:0]	Gamma offset cancelling selection.	

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
0Ch	80h	R/W	[7:0]	DMY_DATA[7:0]	Source dummy data select for Zig-Zag type panel.	Group 03h **(2)**
0Dh	08h	R/W	[7:4]	-	Reserved.	
			[3]	PWR_MASK_FAIL_EN	Power on mode selection.	
			[2]	GIP_PWR_OPT	GIP output voltage level option before power ready.	
			[1]	-	Reserved.	
			[0]	EQ0_MODE	EQ0 mode selection.	
0Eh	00h	R/W	[7:3]	-	Reserved.	
			[2]	CH_OPT	Channel output option.	
			[1:0]	-	Reserved.	
0Fh	40h	R/W	[7]	-	Reserved.	
			[6]	TS_RHL_OPT	AGAM register selected by temperature mode setting or OTP write flag.	
			[5:4]	GIP_MX_TAB_SEL[1:0]	GIP MUX setting table selection.	
			[3]	GATE_INTER_SEL	Gate interlace type selection.	
			[2:0]	-	Reserved.	
10h	68h	R/W	[7:0]	GATENUM[7:0]	Vertical resolution setting when manual selection is enabled. VRES=GATENUM[11:0] * 1	Group 04h **(2)**
11h	A1h	R/W	[7:4]	GATEPASS[3:0]	Password for manual vertical resolution selection.	
			[3:0]	GATENUM[11:8]	Vertical resolution setting when manual selection is enabled. VRES=GATENUM[11:0] * 1	
12h	00h	R/W	[7:0]	HSETNUM[7:0]	Horizontal resolution setting when manual selection is enabled. HRES=HSETNUM[10:0] * 4	
13h	A5h	R/W	[7:4]	HSETPASS[3:0]	Password for manual horizontal resolution Selection.	
			[3]	-	Reserved.	
			[2:0]	HSETNUM[10:8]	Horizontal resolution setting when manual selection is enabled. HRES=HSETNUM[10:0]* 4	
14h	40h	R/W	[7:5]	-	Reserved.	Group 05h **(2)**
			[4:0]	EQ1W[4:0]	Timing for source pre-charge setting to VCC1.	
15h	00h	R/W	[7:3]	BIST_VFP[4:0]	Adjust vertical front porch of BIST mode.	
			[2:0]	-	Reserved.	
16h	00h	R/W	[7:4]	POL_INV_FRM[3:0]	Polarity change sequence method selection.	
			[3]	POL_TOG_VBLK	POL keep toggle at vertical blanking.	
			[2]	-	Reserved.	
			[1:0]	PRE_SCAN[1:0]	Tradition Gate driver pre-scan mode selection.	
17h	80h	R/W	[7:0]	BIST_GRAY[7:0]	BIST mode gray scale pattern setting.	
18h	00h	R/W	[7:0]	BIST_H_OFF[7:0]	Add Htotal width for BIST mode, step is 1T.	
19h	0Fh	R/W	[7:6]	-	Reserved.	
			[5]	BIST_OSC_SEL	Oscillator frequency selection for BIST.	
			[4:0]	H_OSCLK_SEL[4:0]	Oscillator selection for BIST mode.	
1Ah	2Bh	R/W	[7]	-	Reserved.	
			[6]	DISPOFF_EN	Display off function enable.	
			[5:0]	-	Reserved.	
1Bh	00h	R/W	[7:0]	-	Reserved.	
1Ch	72h	R/W	[7:0]	CHIP_ID[7:0]	CHIP_ID.	
1Dh	00h	R/W	[7:0]	-	Reserved.	-
1Eh	00h	R/W	[7:0]	STBYB_CMD[7:0]	Standby mode command.	-

8.1.2. Register table: Page01h (Normal function)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01~03h	-	R/W	[7:0]	-	Reserved.	Group 07h **(2)**
04h	22h	R/W	[7:6]	-	Reserved.	
			[5:4]	VCLS[1:0]	VCL voltage selection, VCL=-2.25V-VCLS[1:0] x 0.25V.	
			[3:0]	-	Reserved.	
05h	84h	R/W	[7]	FAIL_DET_SEL	FAIL_DET output selection.	
			[6]	FAIL_DET_INV	FAIL_DET output inverse.	
			[5]	-	Reserved.	
			[4]	ASIL_NOSIG_SEL	ASIL detect function selection.	
			[3]	ASIL_INV	ASIL output signal inverse.	
			[2:0]	ASIL_WD[2:0]	ASIL output pulse width selection.	
06h	00h	R/W	[7:0]	BANK12_OFT[7:0]	Shift divided position between Bank1 and Bank2.	Group 08h **(2)**
07h	00h	R/W	[7:0]	BANK23_OFT[7:0]	Shift divided position between Bank2 and Bank3.	
08~09h	00h	R/W	[7:0]	-	Reserved.	
0Ah	08h	R/W	[7:0]	-	Reserved.	
0Bh	0Ah	R/W	[7:0]	-	Reserved.	
0Ch	08h	R/W	[7:0]	-	Reserved.	
0Dh	0Ah	R/W	[7:0]	-	Reserved.	
0Eh	08h	R/W	[7:0]	-	Reserved.	
0Fh	0Ah	R/W	[7:0]	-	Reserved.	
10h	00h	R/W	[7:4]	H_TOTAL_OFT[3:0]	H total number offset.	
			[3:0]	-	Reserved.	
11h	00h	R/W	[7:0]	-	Reserved.	
12h	80h	R/W	[7:0]	-	Reserved.	
13h	07h	R/W	[7:0]	-	Reserved.	Group 09h **(1)**
14h	06h	R/W	[7:0]	-	Reserved.	
15h	00h	R/W	[7:2]	-	Reserved.	
			[1:0]	ASIL_WD_OPT[1:0]	ASIL pulse width step option.	
16~1Eh	-	-	[7:0]	-	Reserved.	

8.1.3. Register table: Page02h (Power control function)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	3Ah	R/W	[7]	-	Reserved.	Group 0Ah **(2)**
			[6]	PFMFREN	PFM frequency randomizer enable.	
			[5]	VSPEN	VSP enable.	
			[4]	VSNEN	VSN enable.	
			[3:2]	DRVPD[1:0]	DRVP buffer size selection.	
			[1:0]	DRVND[1:0]	DRVN buffer size selection.	
02h	94h	R/W	[7]	GAS_VCC_EN	GAS detect VCC1 enable.	
			[6:5]	-	Reserved.	
			[4:0]	VSPS[4:0]	VSP voltage selection, VSP=5V+VSPS[4:0] x 0.1V.	
03h	54h	R/W	[7:5]	-	Reserved.	
			[4:0]	VSNS[4:0]	VSN voltage selection, VSN=-5V-VSNS[4:0] x 0.1V.	
04h	4Eh	R/W	[7:6]	VGHXS[1:0]	VGH boosting mode selection.	
			[5:0]	VGHS[5:0]	VGH voltage selection, VGH=5+VGHS[5:0] x 0.5V.	
05h	06h	R/W	[7:6]	-	Reserved.	
			[5]	VGLXS	VGL boosting mode selection.	
			[4:0]	VGLS[4:0]	VGL voltage selection, VGL=-5+VGLS[4:0] x (-0.5)V.	
06h	B4h	R/W	[7:6]	VMONPS[1:0]	PFM of VSP over current detection voltage selection.	
			[5]	VSDPEN	VSDP regulator enable.	
			[4:0]	VSDPS[4:0]	VSDP voltage selection, VSDP=4.8V+VSDPS[4:0] x 0.1V.	
07h	B4h	R/W	[7:6]	VMONNS[1:0]	PFM of VSN over current detection voltage selection.	
			[5]	VSDNEN	VSDN regulator enable.	
			[4:0]	VSDNS[4:0]	VSDN voltage selection, VSDN= -4.8V-VSDNS[4:0] x 0.1V.	
08h	55h	R/W	[7:4]	VSPON[3:0]	PFM turn on duty of DRVP **(tONP)** at normal operation.	
			[3:0]	VSPOFF[3:0]	PFM turn off duty of DRVP **(tOFFP)** at normal operation.	
09h	55h	R/W	[7:4]	VSNON[3:0]	PFM turn on duty of DRVN **(tONN)** at normal operation.	
			[3:0]	VSNOFF[3:0]	PFM turn off duty of DRVN **(tOFFN)** at normal operation.	
0Ah	2Fh	R/W	[7:4]	VSPON_S[3:0]	PFM turn on duty of DRVP **(tONP)** at soft start of power on sequence.	
			[3:0]	VSPOFF_S[3:0]	PFM turn off duty of DRVP **(tOFFP)** at soft start of power on sequence.	
0Bh	2Fh	R/W	[7:4]	VSNON_S[3:0]	PFM turn on duty of DRVN **(tONN)** at soft start of power on sequence.	
			[3:0]	VSNOFF_S[3:0]	PFM turn off duty of DRVN **(tOFFN)** at soft start of power on sequence.	
0Ch	40h	R/W	[7:0]	TP_DLY[7:0]	TPSYNC delay setting.	
0Dh	40h	R/W	[7:0]	TP_WIDTH[7:0]	TPSYNC pulse width setting.	
0Eh	FCh	R/W	[7:5]	TPSYNC1_SEL[2:0]	TPSYNC1 output selection.	
			[4:2]	TPSYNC2_SEL[2:0]	TPSYNC2 output selection.	
			[1]	TPSYNC_INV	TPSYNC output inverse.	
			[0]	TPSYNC_VBLK	TPSYNC output in vertical blanking.	

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
0Fh	48h	R/W	[7]	TP_WIDTH_ENB	TPSYNC output enable when SD driving.	
			[6]	PFM_DET_EN	PFM abnormal detect function enable.	
			[5]	-	Reserved.	
			[4]	PFM_NG_OPT	Polarity option of PFM abnormal flag output to TEST4 pin.	
			[3:2]	PFM_OSC_SEL[1:0]	PFM clock frequency selection.	
			[1:0]	PFM_DET_OPT[1:0]	PFM fail-detect time selection.	
10h	11h	R/W	[7]	-	Reserved.	
			[6]	PFM_SS_SEL	PFM soft start duration selection.	
			[5]	VCOM_OPT	VCOMS setting selection.	
			[4]	VCOMEN	VCOM regulator enable.	
			[3]	S_VCL_ENB	Slave chip VCL regulator enable.	
			[2]	M_VCL_ENB	Master chip VCL regulator enable.	
			[1:0]	VCOMD[1:0]	VCOM driving capability selection.	
11h	EFh	R/W	[7]	VGHL_LIMIT	Auto setting for (VGH + |VGL| ≤ 32).	
			[6]	VGHEN	VGH charge pump circuit enable.	
			[5]	VGLEN	VGL charge pump circuit enable.	
			[4]	FCPS	VGH and VGL charge pump frequency option.	
			[3:2]	-	Reserved.	
			[1:0]	FCP[1:0]	VGH and VGL charge pump frequency setting.	
12h	3Ah	R/W	[7]	T_OCPEN	PFM over current protection function enable.	
			[6]	-	Reserved.	
			[5]	T_VGMREGEN	VGMPHO/VGMPLO and VGMNHO/VGMNLO regulators enable.	
			[4:0]	T_VGMPHS[4:0]	VGMPHO voltage selection.	
13h	1Ah	R/W	[7:5]	-	Reserved.	
			[4:0]	T_VGMNHS[4:0]	VGMNHO voltage selection.	
14h	11h	R/W	[7:4]	T_VGMPLS[3:0]	VGMPLO voltage selection.	
			[3:0]	T_VGMNLS[3:0]	VGMNLO voltage selection.	
15h	7Ch	R/W	[7:2]	-	Reserved.	
			[1]	OTP_RL_FAIL_ENB	OTP reload fail signal output to Fail_Flag and FAIL_DET pin.	
			[0]	-	Reserved.	
16h	00h	R/W	[7]	PFM_NG_ENB	PFM abnormal signal output to Fail_Flag and FAIL_DET pin.	
			[6]	OTP_TRIM_FAIL_ENB	OTP program fail signal output to Fail_Flag and FAIL_DET pin.	
			[5]	EEPROM_FAIL_ENB	EEPROM reload fail signal output to Fail_Flag and FAIL_DET pin.	
			[4]	NOVIDEO_FAIL_ENB	Fail mode signal output to Fail_Flag and FAIL_DET pin.	
			[3]	GIP_DET_FAIL_ENB / GATE_FAIL_ENB	GIP detect signal fail signal output to Fail_Flag and FAIL_DET pin / Tradition gate signal fail signal output to Fail_Flag and FAIL_DET pin.	
			[2]	SOURCE_FAIL_ENB	Internal source circuit fail signal output to Fail_Flag and FAIL_DET pin.	
			[1]	POWER_FAIL_ENB	GAS function fail signal output to Fail_Flag and FAIL_DET pin.	
			[0]	LVDS_FAIL_ENB	LVDS lock fail signal output to Fail_Flag and FAIL_DET pin.	
17h	01h	R/W	[7:1]	-	Reserved.	Group 0Bh **(10)**
			[0]	VCOMS[8]	VCOM voltage selection.	
18h	5Ch	R/W	[7:0]	VCOMS[7:0]	VCOM voltage selection.	
19h	00h	R/W	[7:0]	VCOM_OFST[7:0]	VCOM voltage offset setting.	Group 0Ch **(2)**
1Ah	-	R	[7:0]	-	Reserved.	-
1Bh	-	R	[7:0]	-	Reserved.	-
1Ch	-	R	[7:0]	VCOM_FLAG[7:0]	Flag for OTP of VCOM_FLAG trimming times. **(Read only)**	-

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
1Dh	-	R	[7:2]	GAMMA_FLAG[5:0]	Flag for OTP of GAMMA **(Page03h, Page06h)** trimming times. **(Read only)**	-
			[1:0]	VCOM_FLAG[9:8]	Flag for OTP of VCOM_FLAG trimming times. **(Read only)**	
1Eh	-	R	[7:5]	-	Reserved.	-
			[4:0]	TS_VCOM_FLAG[4:0]	Flag for OTP of VCOM_HT / VCOM_LT trimming times. **(Read only)**	

8.1.4. Register table: Page03h (Positive analog gamma correction, PAGM)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	00h	R/W	[7:5]	-	Reserved.	Group 0Dh **(3)**
			[4:0]	T_VP0[4:0]	Positive gamma reference GSH0 selection.	
02h	04h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP2[5:0]	Positive gamma reference GSH2 selection.	
03h	08h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP4[5:0]	Positive gamma reference GSH4 selection.	
04h	18h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP8[5:0]	Positive gamma reference GSH8 selection.	
05h	23h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP14[5:0]	Positive gamma reference GSH14 selection.	
06h	12h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP23[5:0]	Positive gamma reference GSH23 selection.	
07h	11h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP31[5:0]	Positive gamma reference GSH31 selection.	
08h	17h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP47[5:0]	Positive gamma reference GSH47 selection.	
09h	20h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP79[5:0]	Positive gamma reference GSH79 selection.	
0Ah	23h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP111[5:0]	Positive gamma reference GSH111 selection.	
0Bh	26h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP143[5:0]	Positive gamma reference GSH143 selection.	
0Ch	2Bh	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP175[5:0]	Positive gamma reference GSH175 selection.	
0Dh	25h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP207[5:0]	Positive gamma reference GSH207 selection.	
0Eh	25h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP223[5:0]	Positive gamma reference GSH223 selection.	
0Fh	35h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP231[5:0]	Positive gamma reference GSH231 selection.	
10h	30h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP240[5:0]	Positive gamma reference GSH240 selection.	
11h	24h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP246[5:0]	Positive gamma reference GSH246 selection.	
12h	31h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP251[5:0]	Positive gamma reference GSH251 selection.	
13h	38h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VP253[5:0]	Positive gamma reference GSH253 selection.	
14h	1Eh	R/W	[7:5]	-	Reserved.	
			[4:0]	T_VP255[4:0]	Positive gamma reference GSH255 selection.	

8.1.5. Register table: Page06h (Negative analog gamma correction, NAGM)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	00h	R/W	[7:5]	-	Reserved.	Group 0Eh **(3)**
			[4:0]	T_VN0[4:0]	Negative gamma reference GSL0 selection.	
02h	04h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN2[5:0]	Negative gamma reference GSL2 selection.	
03h	08h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN4[5:0]	Negative gamma reference GSL4 selection.	
04h	18h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN8[5:0]	Negative gamma reference GSL8 selection.	
05h	23h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN14[5:0]	Negative gamma reference GSL14 selection.	
06h	12h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN23[5:0]	Negative gamma reference GSL23 selection.	
07h	11h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN31[5:0]	Negative gamma reference GSL31 selection.	
08h	17h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN47[5:0]	Negative gamma reference GSL47 selection.	
09h	20h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN79[5:0]	Negative gamma reference GSL79 selection.	
0Ah	23h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN111[5:0]	Negative gamma reference GSL111 selection.	
0Bh	26h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN143[5:0]	Negative gamma reference GSL143 selection.	
0Ch	2Bh	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN175[5:0]	Negative gamma reference GSL175 selection.	
0Dh	25h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN207[5:0]	Negative gamma reference GSL207 selection.	
0Eh	25h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN223[5:0]	Negative gamma reference GSL223 selection.	
0Fh	35h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN231[5:0]	Negative gamma reference GSL231 selection.	
10h	30h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN240[5:0]	Negative gamma reference GSL240 selection.	
11h	24h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN246[5:0]	Negative gamma reference GSL246 selection.	
12h	31h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN251[5:0]	Negative gamma reference GSL251 selection.	
13h	38h	R/W	[7:6]	-	Reserved.	
			[5:0]	T_VN253[5:0]	Negative gamma reference GSL253 selection.	
14h	1Eh	R/W	[7:5]	-	Reserved.	
			[4:0]	T_VN255[4:0]	Negative gamma reference GSL255 selection.	

8.1.6. Register table: Page08h (Normal function)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	10h	R/W	[7:6]	-	Reserved.	Group 0Fh **(2)**
			[5:0]	ROB[5:0]	Offset of Red data.	
02h	10h	R/W	[7:6]	-	Reserved.	
			[5:0]	GOB[5:0]	Offset of Green data.	
03h	10h	R/W	[7:6]	-	Reserved.	
			[5:0]	BOB[5:0]	Offset of Blue data.	
04h	80h	R/W	[7:0]	RGC[7:0]	Gain of Red data.	
05h	80h	R/W	[7:0]	GGC[7:0]	Gain of Green data.	
06h	80h	R/W	[7:0]	BGC[7:0]	Gain of Blue data.	
07h	FFh	R/W	[7:0]	PTSEL[15:8]	BIST pattern selection.	Group 10h **(2)**
08h	FFh	R/W	[7:0]	PTSEL[7:0]	BIST pattern selection.	
09h	00h	R/W	[7:0]	-	Reserved.	Group 11h **(2)**
0Ah	5Fh	R/W	[7:4]	-	Reserved.	
			[3:2]	GIP_DRVP[1:0]	GIP output driving ability setting.	
			[1:0]	GIP_DRVN[1:0]	GIP output driving ability setting.	
0Bh	80h	R/W	[7:0]	-	Reserved.	
0Ch	0Ah	R/W	[7:0]	-	Reserved.	
0Dh	00h	R/W	[7:0]	-	Reserved.	
0Eh	00h	R/W	[7:0]	-	Reserved.	
0Fh	0Ah	R/W	[7:0]	-	Reserved.	
10h	00h	R/W	[7:0]	-	Reserved.	

8.1.7. Register table: Page09h (Digital gamma correction of Red color)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	00h	R/W	[7:0]	DGMA1R[7:0]	Digital gamma reference Y1[7:0]: Red.	Group 12h **(1)**
02h	04h	R/W	[7:0]	DGMA2R[7:0]	Digital gamma reference Y2[7:0]: Red.	
03h	0Ch	R/W	[7:0]	DGMA3R[7:0]	Digital gamma reference Y3[7:0]: Red.	
04h	1Ch	R/W	[7:0]	DGMA4R[7:0]	Digital gamma reference Y4[7:0]: Red.	
05h	2Ch	R/W	[7:0]	DGMA5R[7:0]	Digital gamma reference Y5[7:0]: Red.	
06h	3Ch	R/W	[7:0]	DGMA6R[7:0]	Digital gamma reference Y6[7:0]: Red.	
07h	5Ch	R/W	[7:0]	DGMA7R[7:0]	Digital gamma reference Y7[7:0]: Red.	
08h	7Ch	R/W	[7:0]	DGMA8R[7:0]	Digital gamma reference Y8[7:0]: Red.	
09h	BCh	R/W	[7:0]	DGMA9R[7:0]	Digital gamma reference Y9[7:0]: Red.	
0Ah	FCh	R/W	[7:0]	DGMA10R[7:0]	Digital gamma reference Y10[7:0]: Red.	
0Bh	7Ch	R/W	[7:0]	DGMA11R[7:0]	Digital gamma reference Y11[7:0]: Red.	
0Ch	FCh	R/W	[7:0]	DGMA12R[7:0]	Digital gamma reference Y12[7:0]: Red.	
0Dh	00h	R/W	[7:0]	DGMA13R[7:0]	Digital gamma reference Y13[7:0]: Red.	
0Eh	80h	R/W	[7:0]	DGMA14R[7:0]	Digital gamma reference Y14[7:0]: Red.	
0Fh	00h	R/W	[7:0]	DGMA15R[7:0]	Digital gamma reference Y15[7:0]: Red.	
10h	40h	R/W	[7:0]	DGMA16R[7:0]	Digital gamma reference Y16[7:0]: Red.	
11h	80h	R/W	[7:0]	DGMA17R[7:0]	Digital gamma reference Y17[7:0]: Red.	
12h	A0h	R/W	[7:0]	DGMA18R[7:0]	Digital gamma reference Y18[7:0]: Red.	
13h	C0h	R/W	[7:0]	DGMA19R[7:0]	Digital gamma reference Y19[7:0]: Red.	
14h	D0h	R/W	[7:0]	DGMA20R[7:0]	Digital gamma reference Y20[7:0]: Red.	
15h	E0h	R/W	[7:0]	DGMA21R[7:0]	Digital gamma reference Y21[7:0]: Red.	
16h	F0h	R/W	[7:0]	DGMA22R[7:0]	Digital gamma reference Y22[7:0]: Red.	
17h	F8h	R/W	[7:0]	DGMA23R[7:0]	Digital gamma reference Y23[7:0]: Red.	
18h	FCh	R/W	[7:0]	DGMA24R[7:0]	Digital gamma reference Y24[7:0]: Red.	
19h	00h	R/W	[7:6]	DGMA1R[9:8]	Digital gamma reference Y1[9:8]: Red.	
			[5:4]	DGMA2R[9:8]	Digital gamma reference Y2[9:8]: Red.	
			[3:2]	DGMA3R[9:8]	Digital gamma reference Y3[9:8]: Red.	
			[1:0]	DGMA4R[9:8]	Digital gamma reference Y4[9:8]: Red.	
1Ah	00h	R/W	[7:6]	DGMA5R[9:8]	Digital gamma reference Y5[9:8]: Red.	
			[5:4]	DGMA6R[9:8]	Digital gamma reference Y6[9:8]: Red.	
			[3:2]	DGMA7R[9:8]	Digital gamma reference Y7[9:8]: Red.	
			[1:0]	DGMA8R[9:8]	Digital gamma reference Y8[9:8]: Red.	
1Bh	05h	R/W	[7:6]	DGMA9R[9:8]	Digital gamma reference Y9[9:8]: Red.	
			[5:4]	DGMA10R[9:8]	Digital gamma reference Y10[9:8]: Red.	
			[3:2]	DGMA11R[9:8]	Digital gamma reference Y11[9:8]: Red.	
			[1:0]	DGMA12R[9:8]	Digital gamma reference Y12[9:8]: Red.	
1Ch	AFh	R/W	[7:6]	DGMA13R[9:8]	Digital gamma reference Y13[9:8]: Red.	
			[5:4]	DGMA14R[9:8]	Digital gamma reference Y14[9:8]: Red.	
			[3:2]	DGMA15R[9:8]	Digital gamma reference Y15[9:8]: Red.	
			[1:0]	DGMA16R[9:8]	Digital gamma reference Y16[9:8]: Red.	
1Dh	FFh	R/W	[7:6]	DGMA17R[9:8]	Digital gamma reference Y17[9:8]: Red.	
			[5:4]	DGMA18R[9:8]	Digital gamma reference Y18[9:8]: Red.	
			[3:2]	DGMA19R[9:8]	Digital gamma reference Y19[9:8]: Red.	
			[1:0]	DGMA20R[9:8]	Digital gamma reference Y20[9:8]: Red.	
1Eh	FFh	R/W	[7:6]	DGMA21R[9:8]	Digital gamma reference Y21[9:8]: Red.	
			[5:4]	DGMA22R[9:8]	Digital gamma reference Y22[9:8]: Red.	
			[3:2]	DGMA23R[9:8]	Digital gamma reference Y23[9:8]: Red.	
			[1:0]	DGMA24R[9:8]	Digital gamma reference Y24[9:8]: Red.	

8.1.8. Register table: Page0Ah (Digital gamma correction of Green color)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	00h	R/W	[7:0]	DGMA1G[7:0]	Digital gamma reference Y1[7:0]: Green.	Group 13h **(1)**
02h	04h	R/W	[7:0]	DGMA2G[7:0]	Digital gamma reference Y2[7:0]: Green.	
03h	0Ch	R/W	[7:0]	DGMA3G[7:0]	Digital gamma reference Y3[7:0]: Green.	
04h	1Ch	R/W	[7:0]	DGMA4G[7:0]	Digital gamma reference Y4[7:0]: Green.	
05h	2Ch	R/W	[7:0]	DGMA5G[7:0]	Digital gamma reference Y5[7:0]: Green.	
06h	3Ch	R/W	[7:0]	DGMA6G[7:0]	Digital gamma reference Y6[7:0]: Green.	
07h	5Ch	R/W	[7:0]	DGMA7G[7:0]	Digital gamma reference Y7[7:0]: Green.	
08h	7Ch	R/W	[7:0]	DGMA8G[7:0]	Digital gamma reference Y8[7:0]: Green.	
09h	BCh	R/W	[7:0]	DGMA9G[7:0]	Digital gamma reference Y9[7:0]: Green.	
0Ah	FCh	R/W	[7:0]	DGMA10G[7:0]	Digital gamma reference Y10[7:0]: Green.	
0Bh	7Ch	R/W	[7:0]	DGMA11G[7:0]	Digital gamma reference Y11[7:0]: Green.	
0Ch	FCh	R/W	[7:0]	DGMA12G[7:0]	Digital gamma reference Y12[7:0]: Green.	
0Dh	00h	R/W	[7:0]	DGMA13G[7:0]	Digital gamma reference Y13[7:0]: Green	
0Eh	80h	R/W	[7:0]	DGMA14G[7:0]	Digital gamma reference Y14[7:0]: Green.	
0Fh	00h	R/W	[7:0]	DGMA15G[7:0]	Digital gamma reference Y15[7:0]: Green.	
10h	40h	R/W	[7:0]	DGMA16G[7:0]	Digital gamma reference Y16[7:0]: Green	
11h	80h	R/W	[7:0]	DGMA17G[7:0]	Digital gamma reference Y17[7:0]: Green.	
12h	A0h	R/W	[7:0]	DGMA18G[7:0]	Digital gamma reference Y18[7:0]: Green.	
13h	C0h	R/W	[7:0]	DGMA19G[7:0]	Digital gamma reference Y19[7:0]: Green.	
14h	D0h	R/W	[7:0]	DGMA20G[7:0]	Digital gamma reference Y20[7:0]: Green.	
15h	E0h	R/W	[7:0]	DGMA21G[7:0]	Digital gamma reference Y21[7:0]: Green.	
16h	F0h	R/W	[7:0]	DGMA22G[7:0]	Digital gamma reference Y22[7:0]: Green.	
17h	F8h	R/W	[7:0]	DGMA23G[7:0]	Digital gamma reference Y23[7:0]: Green.	
18h	FCh	R/W	[7:0]	DGMA24G[7:0]	Digital gamma reference Y24[7:0]: Green.	
19h	00h	R/W	[7:6]	DGMA1G[9:8]	Digital gamma reference Y1[9:8]: Green.	
			[5:4]	DGMA2G[9:8]	Digital gamma reference Y2[9:8]: Green.	
			[3:2]	DGMA3G[9:8]	Digital gamma reference Y3[9:8]: Green.	
			[1:0]	DGMA4G[9:8]	Digital gamma reference Y4[9:8]: Green.	
1Ah	00h	R/W	[7:6]	DGMA5G[9:8]	Digital gamma reference Y5[9:8]: Green.	
			[5:4]	DGMA6G[9:8]	Digital gamma reference Y6[9:8]: Green.	
			[3:2]	DGMA7G[9:8]	Digital gamma reference Y7[9:8]: Green.	
			[1:0]	DGMA8G[9:8]	Digital gamma reference Y8[9:8]: Green.	
1Bh	05h	R/W	[7:6]	DGMA9G[9:8]	Digital gamma reference Y9[9:8]: Green.	
			[5:4]	DGMA10G[9:8]	Digital gamma reference Y10[9:8]: Green.	
			[3:2]	DGMA11G[9:8]	Digital gamma reference Y11[9:8]: Green.	
			[1:0]	DGMA12G[9:8]	Digital gamma reference Y12[9:8]: Green.	
1Ch	AFh	R/W	[7:6]	DGMA13G[9:8]	Digital gamma reference Y13[9:8]: Green.	
			[5:4]	DGMA14G[9:8]	Digital gamma reference Y14[9:8]: Green.	
			[3:2]	DGMA15G[9:8]	Digital gamma reference Y15[9:8]: Green.	
			[1:0]	DGMA16G[9:8]	Digital gamma reference Y16[9:8]: Green.	
1Dh	FFh	R/W	[7:6]	DGMA17G[9:8]	Digital gamma reference Y17[9:8]: Green.	
			[5:4]	DGMA18G[9:8]	Digital gamma reference Y18[9:8]: Green.	
			[3:2]	DGMA19G[9:8]	Digital gamma reference Y19[9:8]: Green.	
			[1:0]	DGMA20G[9:8]	Digital gamma reference Y20[9:8]: Green.	
1Eh	FFh	R/W	[7:6]	DGMA21G[9:8]	Digital gamma reference Y21[9:8]: Green.	
			[5:4]	DGMA22G[9:8]	Digital gamma reference Y22[9:8]: Green.	
			[3:2]	DGMA23G[9:8]	Digital gamma reference Y23[9:8]: Green.	
			[1:0]	DGMA24G[9:8]	Digital gamma reference Y24[9:8]: Green.	

8.1.9. Register table: Page0Bh (Digital gamma correction of Blue color)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Bh	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	00h	R/W	[7:0]	DGMA1B[7:0]	Digital gamma reference Y1[7:0]: Blue.	Group 14h **(1)**
02h	04h	R/W	[7:0]	DGMA2B[7:0]	Digital gamma reference Y2[7:0]: Blue.	
03h	0Ch	R/W	[7:0]	DGMA3B[7:0]	Digital gamma reference Y3[7:0]: Blue.	
04h	1Ch	R/W	[7:0]	DGMA4B[7:0]	Digital gamma reference Y4[7:0]: Blue.	
05h	2Ch	R/W	[7:0]	DGMA5B[7:0]	Digital gamma reference Y5[7:0]: Blue.	
06h	3Ch	R/W	[7:0]	DGMA6B[7:0]	Digital gamma reference Y6[7:0]: Blue.	
07h	5Ch	R/W	[7:0]	DGMA7B[7:0]	Digital gamma reference Y7[7:0]: Blue.	
08h	7Ch	R/W	[7:0]	DGMA8B[7:0]	Digital gamma reference Y8[7:0]: Blue.	
09h	BCh	R/W	[7:0]	DGMA9B[7:0]	Digital gamma reference Y9[7:0]: Blue.	
0Ah	FCh	R/W	[7:0]	DGMA10B[7:0]	Digital gamma reference Y10[7:0]: Blue.	
0Bh	7Ch	R/W	[7:0]	DGMA11B[7:0]	Digital gamma reference Y11[7:0]: Blue.	
0Ch	FCh	R/W	[7:0]	DGMA12B[7:0]	Digital gamma reference Y12[7:0]: Blue.	
0Dh	00h	R/W	[7:0]	DGMA13B[7:0]	Digital gamma reference Y13[7:0]: Blue.	
0Eh	80h	R/W	[7:0]	DGMA14B[7:0]	Digital gamma reference Y14[7:0]: Blue.	
0Fh	00h	R/W	[7:0]	DGMA15B[7:0]	Digital gamma reference Y15[7:0]: Blue	
10h	40h	R/W	[7:0]	DGMA16B[7:0]	Digital gamma reference Y16[7:0]: Blue.	
11h	80h	R/W	[7:0]	DGMA17B[7:0]	Digital gamma reference Y17[7:0]: Blue.	
12h	A0h	R/W	[7:0]	DGMA18B[7:0]	Digital gamma reference Y18[7:0]: Blue.	
13h	C0h	R/W	[7:0]	DGMA19B[7:0]	Digital gamma reference Y19[7:0]: Blue.	
14h	D0h	R/W	[7:0]	DGMA20B[7:0]	Digital gamma reference Y20[7:0]: Blue.	
15h	E0h	R/W	[7:0]	DGMA21B[7:0]	Digital gamma reference Y21[7:0]: Blue.	
16h	F0h	R/W	[7:0]	DGMA22B[7:0]	Digital gamma reference Y22[7:0]: Blue.	
17h	F8h	R/W	[7:0]	DGMA23B[7:0]	Digital gamma reference Y23[7:0]: Blue.	
18h	FCh	R/W	[7:0]	DGMA24B[7:0]	Digital gamma reference Y24[7:0]: Blue.	
19h	00h	R/W	[7:6]	DGMA1B[9:8]	Digital gamma reference Y1[9:8]: Blue.	
			[5:4]	DGMA2B[9:8]	Digital gamma reference Y2[9:8]: Blue.	
			[3:2]	DGMA3B[9:8]	Digital gamma reference Y3[9:8]: Blue.	
			[1:0]	DGMA4B[9:8]	Digital gamma reference Y4[9:8]: Blue.	
1Ah	00h	R/W	[7:6]	DGMA5B[9:8]	Digital gamma reference Y5[9:8]: Blue.	
			[5:4]	DGMA6B[9:8]	Digital gamma reference Y6[9:8]: Blue.	
			[3:2]	DGMA7B[9:8]	Digital gamma reference Y7[9:8]: Blue.	
			[1:0]	DGMA8B[9:8]	Digital gamma reference Y8[9:8]: Blue.	
1Bh	05h	R/W	[7:6]	DGMA9B[9:8]	Digital gamma reference Y9[9:8]: Blue.	
			[5:4]	DGMA10B[9:8]	Digital gamma reference Y10[9:8]: Blue.	
			[3:2]	DGMA11B[9:8]	Digital gamma reference Y11[9:8]: Blue.	
			[1:0]	DGMA12B[9:8]	Digital gamma reference Y12[9:8]: Blue.	
1Ch	AFh	R/W	[7:6]	DGMA13B[9:8]	Digital gamma reference Y13[9:8]: Blue.	
			[5:4]	DGMA14B[9:8]	Digital gamma reference Y14[9:8]: Blue.	
			[3:2]	DGMA15B[9:8]	Digital gamma reference Y15[9:8]: Blue.	
			[1:0]	DGMA16B[9:8]	Digital gamma reference Y16[9:8]: Blue.	
1Dh	FFh	R/W	[7:6]	DGMA17B[9:8]	Digital gamma reference Y17[9:8]: Blue.	
			[5:4]	DGMA18B[9:8]	Digital gamma reference Y18[9:8]: Blue.	
			[3:2]	DGMA19B[9:8]	Digital gamma reference Y19[9:8]: Blue.	
			[1:0]	DGMA20B[9:8]	Digital gamma reference Y20[9:8]: Blue.	
1Eh	FFh	R/W	[7:6]	DGMA21B[9:8]	Digital gamma reference Y21[9:8]: Blue.	
			[5:4]	DGMA22B[9:8]	Digital gamma reference Y22[9:8]: Blue.	
			[3:2]	DGMA23B[9:8]	Digital gamma reference Y23[9:8]: Blue.	
			[1:0]	DGMA24B[9:8]	Digital gamma reference Y24[9:8]: Blue.	

8.1.10. Register table: Page0Ch (LVDS function)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	00h	R/W	[7]	-	Reserved.	Group 15h **(1)**
			[6]	DLL_BANK	LVDS input frequency range selection.	
			[5]	LVDS_AGING	LVDS power saving enable.	
			[4]	FMT	LVDS and TTL input data format selection.	
			[3]	LANE_SW	LVDS lane swapping selection.	
			[2]	LANE_PN	LVDS lane PN polarity swapping selection.	
			[1:0]	-	Reserved.	
02h	55h	R/W	[7:0]	-	Reserved.	
03h	63h	R/W	[7:0]	-	Reserved.	
04h	23h	R/W	[7:0]	-	Reserved.	
05h	FFh	R/W	[7:0]	-	Reserved.	
06h	AAh	R/W	[7:0]	-	Reserved.	
07h	AAh	R/W	[7:0]	-	Reserved.	
08h	AAh	R/W	[7:0]	-	Reserved.	
09h	AAh	R/W	[7:0]	-	Reserved.	
0Ah	AAh	R/W	[7:0]	-	Reserved.	
0Bh	AAh	R/W	[7:0]	-	Reserved.	
0Ch	AAh	R/W	[7:0]	-	Reserved.	
0Dh	AAh	R/W	[7:0]	-	Reserved.	
0Eh	AAh	R/W	[7:0]	-	Reserved.	
0Fh	AAh	R/W	[7:0]	-	Reserved.	
10h	00h	R/W	[7:0]	-	Reserved.	
11h	00h	R/W	[7:0]	-	Reserved.	
12h	00h	R/W	[7:0]	-	Reserved.	
13h	00h	R/W	[7:0]	-	Reserved.	-

8.1.11. Register table: Page0Eh (Temperature mode)

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	03h	R/W	[7:2]	-	Reserved.	Group 17h **(5)**
			[1]	VCOMS_HT[8]	VCOM voltage adjustment at high temperature mode.	
			[0]	VCOMS_LT[8]	VCOM voltage adjustment at low temperature mode.	
02h	5Ch	R/W	[7:0]	VCOMS_HT[7:0]	VCOM voltage adjustment at high temperature mode.	
03h	5Ch	R/W	[7:0]	VCOMS_LT[7:0]	VCOM voltage adjustment at low temperature mode.	
04h	0Eh	R/W	[7:6]	-	Reserved.	Group 18h **(2)**
			[5:0]	VGHS_HT[5:0]	VGH voltage adjustment at high temperature mode.	
05h	06h	R/W	[7:5]	-	Reserved.	
			[4:0]	VGLS_HT[4:0]	VGL voltage adjustment at high temperature mode.	
06h	0Eh	R/W	[7:6]	-	Reserved.	
			[5:0]	VGHS_LT[5:0]	VGH voltage adjustment at low temperature mode.	
07h	06h	R/W	[7:5]	-	Reserved.	
			[4:0]	VGLS_LT[4:0]	VGL voltage adjustment at low temperature mode.	
08h	5Ah	R/W	[7]	DIM_EN	Voltage dimming enable at temperature mode.	
			[6:5]	DIM_FRAME[1:0]	Voltage dimming frame period setting.	
			[4:0]	VGMPHS_HT[4:0]	VGMPH voltage adjustment at high temperature mode.	
09h	1Ah	R/W	[7]	DIM_OPT	AGAM dimming option.	
			[6:5]	-	Reserved.	
			[4:0]	VGMNHS_HT[4:0]	VGMNH voltage adjustment at high temperature mode.	
0Ah	11h	R/W	[7:4]	VGMPLS_HT[3:0]	VGMPL voltage adjustment at high temperature mode.	
			[3:0]	VGMNLS_HT[3:0]	VGMNL voltage adjustment at high temperature mode.	
0Bh	1Ah	R/W	[7]	TS_GOE_EN	GOE setting by temperature mode.	
			[6]	TS_AGAM_EN	AGAM setting by temperature mode.	
			[5]	-	Reserved.	
			[4:0]	VGMPHS_LT[4:0]	VGMPH voltage adjustment at low temperature mode.	
0Ch	1Ah	R/W	[7]	TS_VCOM_EN	VCOM setting by temperature mode.	
			[6]	TS_VGHL_EN	VGH/VGL setting by temperature mode.	
			[5]	-	Reserved.	
			[4:0]	VGMNHS_LT[4:0]	VGMNH voltage adjustment at low temperature mode.	
0Dh	11h	R/W	[7:4]	VGMPLS_LT[3:0]	VGMPL voltage adjustment at low temperature mode.	
			[3:0]	VGMNLS_LT[3:0]	VGMNL voltage adjustment at low temperature mode.	
0Eh	00h	R/W	[7:0]	-	Reserved.	Group 19h **(1)**
0Fh	04h	R/W	[7:0]	-	Reserved.	
10h	17h	R/W	[7:0]	-	Reserved.	
11h	41h	R/W	[7:0]	-	Reserved.	
12h	20h	R/W	[7:0]	-	Reserved.	

Address	Default	Read/ Write	D[7:0]	Name	Description	OTP Group (times)
13h	00h	R/W	[7:0]	-	Reserved.	
14h	FFh	R/W	[7:0]	-	Reserved.	Group 1Ah **(1)**
15h	FFh	R/W	[7:0]	-	Reserved.	
16h	FFh	R/W	[7:0]	-	Reserved.	
17h	00h	R/W	[7:0]	-	Reserved.	
18h	00h	R/W	[7:0]	-	Reserved.	
19h	00h	R/W	[7:0]	-	Reserved.	
1Ah	00h	R/W	[7:0]	-	Reserved.	
1Bh	00h	R/W	[7:0]	-	Reserved.	
1Ch	00h	R/W	[7:0]	-	Reserved.	Group 1Bh **(1)**
1Dh	00h	R/W	[7:0]	-	Reserved.	
1Eh	00h	R/W	[7:0]	-	Reserved.	

8.1.12. Register table: Page0Fh~Page14h (GIP function)

The register table of GIP function will set for the customer's request.
(At OTP group 1Ch~21h and can be programmed 2 times.)

8.1.13. Register table: Page15h (OTP function)

Address	Default	Read/ Write	D[7:0]	Name	Description	Remark
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01h	00h	R/W	[7:6]	-	Reserved.	-
			[5:0]	OTP_GROUP[5:0]	OTP group select.	-
02h	99h	R/W	[7:0]	WOTP[7:0]	OTP program command enable.	-
03h	00h	R/W	[7:4]	-	Reserved.	-
			[3]	OTP_WR_ALL	OTP write all group function enable.	-
			[2]	OTP_RELOAD	OTP reload function enable.	-
			[1]	OTP_RD	OTP read function enable.	-
			[0]	OTP_WR	OTP write function enable.	-
04h	00h	R/W	[7:2]	-	Reserved.	-
			[1:0]	OTP_INDEX[9:8]	OTP address for read.	-
05h	00h	R/W	[7:0]	OTP_INDEX[7:0]	OTP address for read.	-
06h	00h	R	[7:0]	PDOB	OTP read out data.	**(Read only)**
07h	00h	R/W	[7:0]	-	Reserved.	-
08h	5Ah	R/W	[7:0]	-	Reserved.	-
09h	00h	R/W	[7:0]	-	Reserved.	-
0Ah	5Ah	R/W	[7:0]	EEP_PWD[7:0]	EEPROM software reload enable.	-
0Bh	00h	R	[7]	EEP_CKSUM_FAIL	EEPROM check-sum flag.	**(Read only)**
			[6:1]	-	Reserved.	-
			[0]	EEP_RL_CMD	EEPROM software reload.	-
0Ch	00h	R/W	[7:5]	-	Reserved.	-
			[4]	EESEL	EEPROM controlled by System or Driver IC.	-
			[3:0]	-	Reserved.	-
0Dh	00h	R	[7:0]	IC_VERSION[7:0]	IC version.	**(Read only)**
0Eh	00h	R/W	[7:0]	DISPOFF_CMD[7:0]	Display off command.	-
0Fh	00h	R	[7:0]	EEP_CKSUM_TCON [7:0]	EEPROM checksum value calculated by TCON.	**(Read only)**
10h	00h	R	[7:0]	EEP_CKSUM_DESIRE [7:0]	EEPROM checksum value read from EEPROM.	**(Read only)**
11~1Eh	-	-	[7:0]	-	Reserved.	-

8.1.14. Register table: Page16h (Fail Flag)

Address	Default	Read/ Write	D[7:0]	Name	Description	Remark
00h	1Ah	R/W	[7:0]	PAGE[7:0]	Register Page selection.	-
01~06h	00h	R/W	[7:0]	-	Reserved.	-
07~14h	00h	R	[7:0]		Reserved.	
15h	00h	R	[7]	-	Reserved.	-
			[6]	-	Reserved.	-
			[5]	-	Reserved.	-
			[4:2]	-	Reserved	
			[1]	OTP_RL_FAIL_FLAG	OTP reload fail flag.	**(Read only)**
			[0]	-	Reserved.	-
16h	00h	R	[7]	PFM_NG_FAIL_FLAG	PFM abnormal fail flag.	**(Read only)**
			[6]	OTPTRIM_FAIL_FLAG	OTP program fail flag.	**(Read only)**
			[5]	EEPROM_FAIL_FLAG	EEPROM reload fail flag.	**(Read only)**
			[4]	NOVIDEO_FAIL_FLAG	Fail mode fail flag.	**(Read only)**
			[3]	GIP_DET_FAIL_FLAG/ Gate_FAIL_FLAG	GIP detect fail flag/ Traditional gate signal fail flag.	**(Read only)**
			[2]	SOURCE_FAIL_FLAG	Internal source circuit fail flag.	**(Read only)**
			[1]	POWER_FAIL_FLAG	GAS function fail flag.	**(Read only)**
			[0]	LVDS_FAIL_FLAG	LVDS lock fail flag.	**(Read only)**
17h	00h	R	[7:0]	-	Reserved.	-
18h	00h	R	[7:0]	-	Reserved.	-
19h	00h	R	[7:0]	-	Reserved.	-
1Ah	00h	R	[7:0]	-	Reserved.	-
1Bh	00h	R	[7:0]	-	Reserved.	-
1Ch	00h	R	[7:5]	-	Reserved.	-
			[4:0]	-	Reserved.	-
1Dh	00h	R	[7:0]	-	Reserved.	-

8.2. Register description

8.2.1. Page00h for Normal function

Page00h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page00h R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	01h	1/0	DUAL_ZZ_SEL	PANEL_TYPE[2:0]			RESET_GAS_OPT	ZIG-ZAG_TYPE [1:0]		GDSEL
			0	0	1	1	0	0	0	0

DUAL_ZZ_SEL: Option of Dual gate Type 2 with Zig-Zag type panel structure.

DUAL_ZZ_SEL	Function	Note
0	Option 0 of Dual gate Type 2 with Zig-Zag type panel structure.	Default
1	Option 1 of Dual gate Type 2 with Zig-Zag type panel structure.	-

PANEL_TYPE[2:0]: Panel type selection.

PANEL_TYPE[2:0]			Function	Note
0	0	0	LTPS MUX2:4	-
0	0	1	LTPS MUX2:6 Type 1	-
0	1	0	LTPS MUX2:6 Type 2	-
0	1	1	LTPS MUX1:1 / Single gate	Default
1	0	0	Dual gate Type 1	-
1	0	1	Triple gate	-
1	1	0	Dual gate Type 2	-
1	1	1	Dual gate Type 3(1)	-

Note: (1) Dual gate Type 3 only support Zig-Zag type panel.

RESET_GAS_OPT: Sleep or GAS mode option for RESETB_SLP function.

RESET_GAS_OPT	Function	Note
0	Enter Sleep mode at RESETB_SLP falling edge.	Default
1	Enter GAS mode at RESETB_SLP falling edge.	-

ZIG-ZAG_TYPE[1:0]: Zig-Zag type selection.

ZIG-ZAG_TYPE[1:0]		Function	Note
0	0	Stripe panel	Default
0	1	Zig-Zag Type 1	-
1	0	Zig-Zag Type 2	-
1	1	Stripe panel	-

GDSEL: Gate type selection.

GDSEL	Function	Note
0	GIP	Default
1	Tradition Gate driver	-

Page00h R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	02h	1/0	TR[1:0]		DINT	MODE	HSP	VSP	CLOCKP	NB
			1	1	1	1	0	0	0	1

TR[1:0]: Interface selection.

TR[1:0]	Function	Note
00	TTL	-
01	TTL	-
10	1-port LVDS	-
11	2-port LVDS	Default

DINT: Input data 6-bit or 8-bit selection.

DINT	Function	Note
0	6-bit	-
1	8-bit	Default

MODE: Sync or DE(1) mode selection.

MODE	Function	Note
0	DE only mode	-
1	Sync **(HS+VS)** mode	Default

Note: (1) Refer to "The restriction of input DE variation"

HSP: HS polarity.

HSP	Function	Note
0	Low pulse	Default
1	High pulse	-

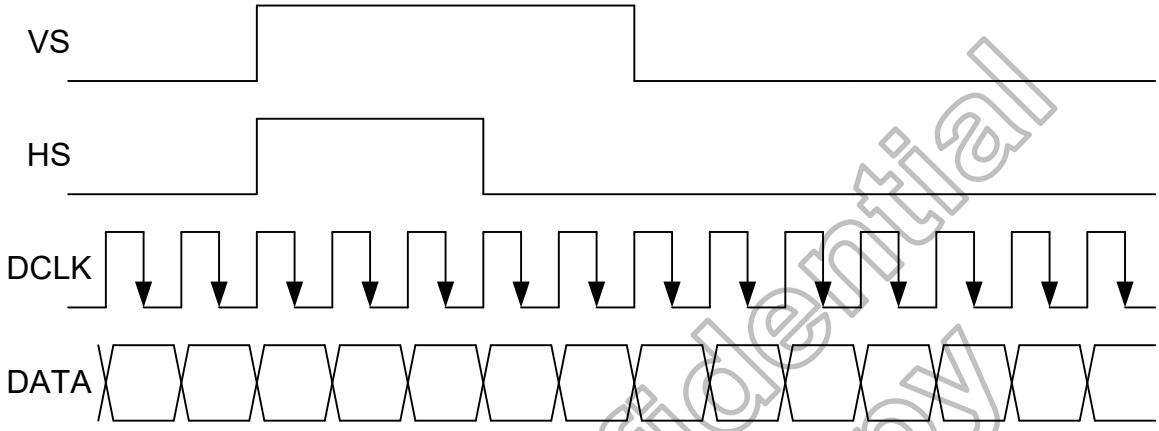
VSP: VS polarity.

VSP	Function	Note
0	Low pulse	Default
1	High pulse	-

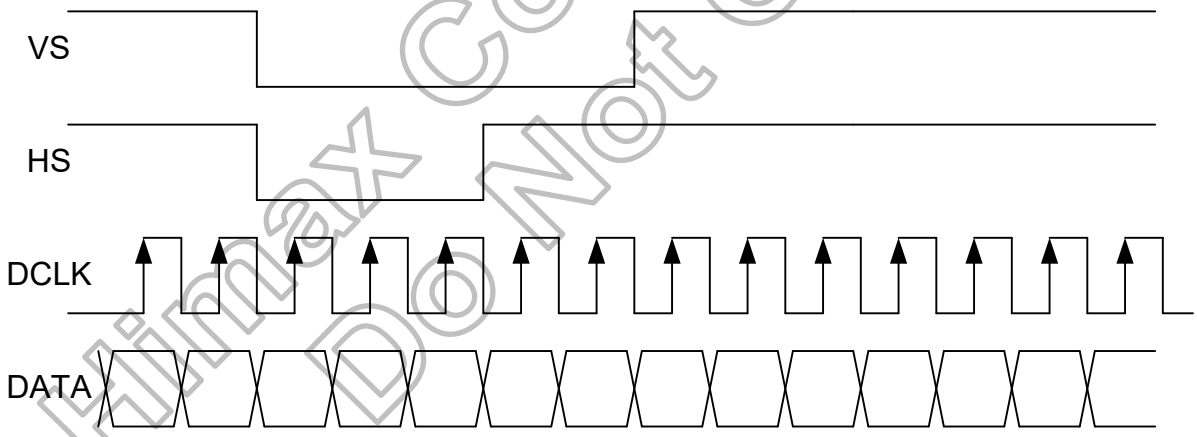
CLOCKP: Clock latch data edge for TTL mode.

CLOCKP	Function	Note
0	Rising edge	Default
1	Falling edge	-

Example1: CLOCKP=1, VSP=1, HSP=1



Example2: CLOCKP=0, VSP=0, HSP=0 (default setting)



NB: Normally white/black selection.

NB	Function	Note
0	Normally white	-
1	Normally black	Default

Page00h R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	03h	1/0	RL	TB	INV[1:0]		RS[3:0]			
			0	0	0	0	0	0	1	1

RL: Horizontal scan direction.
The horizontal scan direction=RL hardware pin "XOR" with RL register setting when FCS=L.

RL Hardware pin	RL Page00h R03h[7]	Function	Note
L	0	Reverse **(S[1440]→S[1])**	-
L	1	Forward **(S[1]→S[1440])**	-
H	0	Forward **(S[1]→S[1440])**	Default
H	1	Reverse **(S[1440]→S[1])**	-

TB: Vertical scan direction.
The vertical scan direction=TB hardware pin "XOR" with TB register setting when FCS=L.

TB Hardware pin	TB Page00h R03h[6]	Function	Note
L	0	Reverse **(Bottom→Top)**	-
L	1	Forward **(Top→Bottom)**	-
H	0	Forward **(Top→Bottom)**	Default
H	1	Reverse **(Bottom→Top)**	-

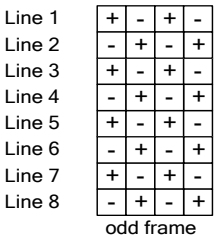
INV[1:0]: Inversion algorithm selection.

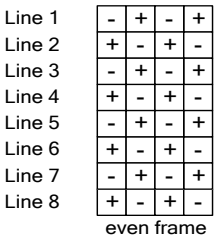
A. When R01h[6:4]=PANEL_TYPE[2:0]=3'b011 for Single gate

(Zig-Zag type only support column inversion)

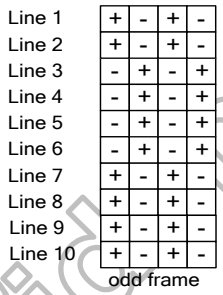
INV[1:0]		Function	Note
0	0	Dot inversion **(Vertical)**	Default
0	1	1+2 Line inversion **(Vertical)**	-
1	0	2+4 Line inversion **(Vertical)**	-
1	1	Column inversion **(Vertical)**	-

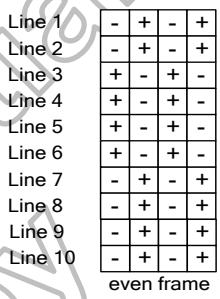
Dot inversion



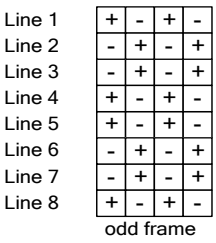


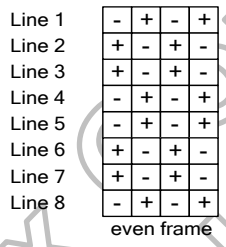
2+4 line inversion



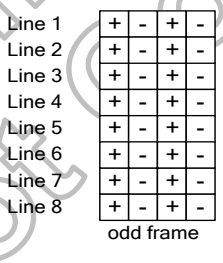


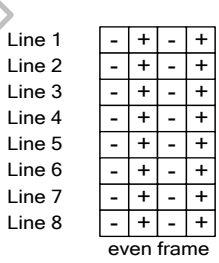
1+2 Line inversion





Column inversion



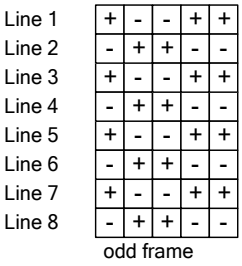


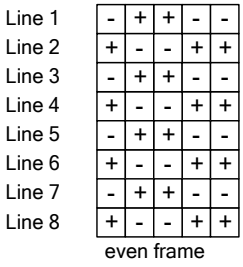
B. When R01h[6:4]=PANEL_TYPE[2:0]=3'b100/3'b110/3'b111 for Dual gate

(Zig-Zag type only support column inversion)

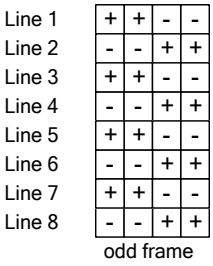
INV[1:0]		Function	Note
0	0	1+2 dot inversion **(Vertical)**	Default
0	1	Reserved	-
1	0	1+2 dot inversion **(Vertical)**	-
1	1	2-dot inversion **(Vertical)**	-

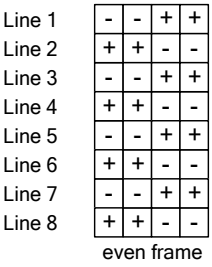
1+2 dot inversion





2 dot inversion





C. When R01h[6:4]=PANEL_TYPE[2:0]=3'b101 for Triple gate

(Zig-Zag type only support column inversion)

INV[1:0]		Function	Note
0	0	Dot inversion **(Vertical)**	Default
0	1	3 dot inversion **(Vertical)**	-
1	0	3+6 dot inversion **(Vertical)**	-
1	1	Column inversion **(Vertical)**	-

Dot inversion

Dot 1 (R)	+	-	+	-	
Dot 2 (G)	-	+	-	+	
Dot 3 (B)	+	-	+	-	
Dot 4 (R)	-	+	-	+	
Dot 5 (G)	+	-	+	-	
Dot 6 (B)	-	+	-	+	
Dot 7 (R)	+	-	+	-	
Dot 8 (G)	-	+	-	+	

odd frame

Dot 1 (R)	-	+	-	+	
Dot 2 (G)	+	-	+	-	
Dot 3 (B)	-	+	-	+	
Dot 4 (R)	+	-	+	-	
Dot 5 (G)	-	+	-	+	
Dot 6 (B)	+	-	+	-	
Dot 7 (R)	-	+	-	+	
Dot 8 (G)	+	-	+	-	

even frame

3 dot inversion

Dot 1 (R)	+	-	+	-	
Dot 2 (G)	+	-	+	-	
Dot 3 (B)	+	-	+	-	
Dot 4 (R)	-	+	-	+	
Dot 5 (G)	-	+	-	+	
Dot 6 (B)	-	+	-	+	
Dot 7 (R)	+	-	+	-	
Dot 8 (G)	+	-	+	-	
Dot 9 (B)	+	-	+	-	

odd frame

Dot 1 (R)	-	+	-	+	
Dot 2 (G)	-	+	-	+	
Dot 3 (B)	-	+	-	+	
Dot 4 (R)	+	-	+	-	
Dot 5 (G)	+	-	+	-	
Dot 6 (B)	+	-	+	-	
Dot 7 (R)	-	+	-	+	
Dot 8 (G)	-	+	-	+	
Dot 9 (B)	-	+	-	+	

even frame

3+6 dot inversion

Dot 1 (R)	+	-	+	-	
Dot 2 (G)	+	-	+	-	
Dot 3 (B)	+	-	+	-	
Dot 4 (R)	-	+	-	+	
Dot 5 (G)	-	+	-	+	
Dot 6 (B)	-	+	-	+	
Dot 7 (R)	-	+	-	+	
Dot 8 (G)	-	+	-	+	
Dot 9 (B)	-	+	-	+	
Dot 10 (R)	+	-	+	-	
Dot 11 (G)	+	-	+	-	
Dot 12 (B)	+	-	+	-	
Dot 13 (R)	+	-	+	-	
Dot 14 (G)	+	-	+	-	
Dot 15 (B)	+	-	+	-	

odd frame

Dot 1 (R)	-	+	-	+	
Dot 2 (G)	-	+	-	+	
Dot 3 (B)	-	+	-	+	
Dot 4 (R)	+	-	+	-	
Dot 5 (G)	+	-	+	-	
Dot 6 (B)	+	-	+	-	
Dot 7 (R)	+	-	+	-	
Dot 8 (G)	+	-	+	-	
Dot 9 (B)	+	-	+	-	
Dot 10 (R)	-	+	-	+	
Dot 11 (G)	-	+	-	+	
Dot 12 (B)	-	+	-	+	
Dot 13 (R)	-	+	-	+	
Dot 14 (G)	-	+	-	+	
Dot 15 (B)	-	+	-	+	

even frame

Column inversion

Dot 1 (R)	+	-	+	-	
Dot 2 (G)	+	-	+	-	
Dot 3 (B)	+	-	+	-	
Dot 4 (R)	+	-	+	-	
Dot 5 (G)	+	-	+	-	
Dot 6 (B)	+	-	+	-	
Dot 7 (R)	+	-	+	-	
Dot 8 (G)	+	-	+	-	

odd frame

Dot 1 (R)	-	+	-	+	
Dot 2 (G)	-	+	-	+	
Dot 3 (B)	-	+	-	+	
Dot 4 (R)	-	+	-	+	
Dot 5 (G)	-	+	-	+	
Dot 6 (B)	-	+	-	+	
Dot 7 (R)	-	+	-	+	
Dot 8 (G)	-	+	-	+	

even frame

RS[3:0]: Resolution selection.

RS[3:0]				Function	Note
0	0	0	0	2560RGB X 960	-
0	0	0	1	2400RGB X 900	-
0	0	1	0	1920RGB X 1080	-
0	0	1	1	1920RGB X 720	Default
0	1	0	0	1920RGB X 400	-
0	1	0	1	1600RGB X 320	-
0	1	1	0	1560RGB X 700	-
0	1	1	1	1540RGB X 720	-
1	0	0	0	1440RGB X 540	-
1	0	0	1	1280RGB X 720	-
1	0	1	0	1280RGB X 480	-
1	0	1	1	1280RGB X 400	-
1	1	0	0	960RGB X 2560	-
1	1	0	1	960RGB X 540	-
1	1	1	0	800RGB X 480	-
1	1	1	1	480RGB X 240	-

Page00h R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	04h	1/0	RB_INV	DGAMEN	GPOS[1:0]		SD_GND_V[1:0]		PON	POFF
			0	0	0	0	0	0	0	0

RB_INV: R data and B data exchange.

RB_INV	Function	Note
0	R data and B data no exchange	Default
1	R data and B data exchange	-

DGAMEN: Digital gamma function enable.

DGAMEN	Function	Note
0	Disable	Default
1	Enable	-

GPOS[1:0]: Tradition Gate driver location.

GPOS[1:0]	Function	Note
00	Left side	Default
01	Right side	-
10	Interlaced driving at dual side	-
11	Progressive driving the same line at dual side **(multi-driving)**	-

SD_GND_V[1:0]: Source output state in vertical blanking.

SD_GND_V[1:0]	Function	Note
00	Source output keep the last data at V blanking	Default
01	Source output pulled to ground at V blanking	-
10	Source output keep Hi-Z at V blanking	-
11	Source output keep Hi-Z at V blanking	-

PON: White/Black pattern selection at power on sequence.

PON	Function	Note
0	Black pattern	Default
1	White pattern	-

POFF: White/Black pattern selection at power off sequence.

NB	POFF	Function	Note
1	0	Black pattern	Default
1	1	White pattern	-
0	0	White pattern	-
0	1	Black pattern	-

Page00h R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	05h	1/0	GAS_VSPN_EN	SPFEN	SPFSEL	BISTEN	-	-	BIST_FNUM[1:0]	
			1	1	0	0	-	-	0	0

GAS_VSPN_EN: GAS detect VSP/VSN enable.

GAS_VSPN_EN	Function	Note
0	Disable	-
1	Enable	Default

SPFEN: Self-protection mode enable.

SPFEN	Function	Note
0	Disable	-
1	Enable	Default

SPFSEL: White/Black pattern selection at self protection mode.

SPFSEL	Function	Note
0	Black pattern	Default
1	White pattern	-

BISTEN: BIST mode enable.
The BIST mode enable=BISTEN hardware pin "XOR" with BISTEN register setting when FCS=L.

BISTEN Hardware pin	BISTEN Page00h R05h[4]	Function	Note
L	0	Disable	Default
L	1	Enable	-
H	0	Enable	-
H	1	Disable	-

BIST_FNUM[1:0]: BIST pattern refresh frame setting.

BIST_FNUM[1:0]	Function	Note
00	120 Frame	Default
01	240 Frame	-
10	360 Frame	-
11	480 Frame	-

Page00h R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	06h	1/0	VSTS[7:0]							
			0	0	0	1	1	0	0	0

VSTS[7:0]: Vertical back porch adjustment.

VSTS[7:0]								Function	Note
0	0	0	0	0	0	0	0	3H(1)	-
0	0	0	0	0	0	0	1	3H(1)	-
0	0	0	0	0	0	1	0	3H(1)	-
0	0	0	0	0	0	1	1	3H(1)	-
0	0	0	0	0	1	0	0	4H(1)	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	0	0	24H(1)	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255H(1)	-

Note: (1) H is the horizontal line unit.

Page00h R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	07h	1/0	HSTS[7:0]							
			0	0	0	1	0	0	0	0

HSTS[7:0]: Horizontal back porch adjustment.

HSTS[7:0]								Function	Note
0	0	0	0	0	0	0	0	$5T_{DCLK}$(1)	-
:	:	:	:	:	:	:	:	$5T_{DCLK}$(1)	-
0	0	0	0	0	1	0	1	$5T_{DCLK}$(1)	-
0	0	0	0	0	1	1	0	$6T_{DCLK}$(1)	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	0	0	0	0	$16T_{DCLK}$(1)	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	$255T_{DCLK}$(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

Page00h R08h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	08h	1/0	ENDRVP[1:0]		OEW[5:0]					
			0	0	0	0	0	1	1	1

ENDRVP[1:0]: Channel OP(+) driving ability control signal.

ENDRVP[1:0]	Function	Note
00	100%	Default
01	150%	-
10	200%	-
11	250%	-

OEW[5:0]: Timing for gate driver control. tOEV is the high pulse width of OEV which is the time that all gate channels are off between two lines.
tOEV=OEW[5:0] * $8T_{DCLK}$(1), and it should be smaller than 0.5*t_h **(which is period of one line, in microsecond)**.
Note that tOEV should be larger than (SSC_{MR} x 120% x t_h) when SSC is applied. For example, SSC_{MR}=±3% and period of one line is 10μs, tOEV should be larger than (10μs x 3% x 120%)=0.36μs.

OEW[5:0]						Function	Note
0	0	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	-
0	0	0	0	1	0	Reserved	-
0	0	0	0	1	1	$24T_{DCLK}$(1)	-
:	:	:	:	:	:	:	-
0	0	0	1	1	1	$56T_{DCLK}$(1)	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	$504T_{DCLK}$(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

Page00h R09h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	09h	1/0	ENDRVN[1:0]		GEQW[5:0]					
			0	0	0	0	0	1	1	0

ENDRVN[1:0]: Channel OP(-) driving ability control signal.

ENDRVN[1:0]	Function	Note
00	100%	Default
01	150%	-
10	200%	-
11	250%	-

GEQW[5:0]: Timing for gate driver control. tGEQ is the time from the falling edge of CPV to the rising edge of OEV.
tGEQ=GEQW[5:0] * $4T_{DCLK}$(1).

GEQW[5:0]						Function	Note
0	0	0	0	0	0	$0T_{DCLK}$(1)	-
:	:	:	:	:	:	:	-
0	0	0	1	1	0	$24T_{DCLK}$(1)	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	$252T_{DCLK}$(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

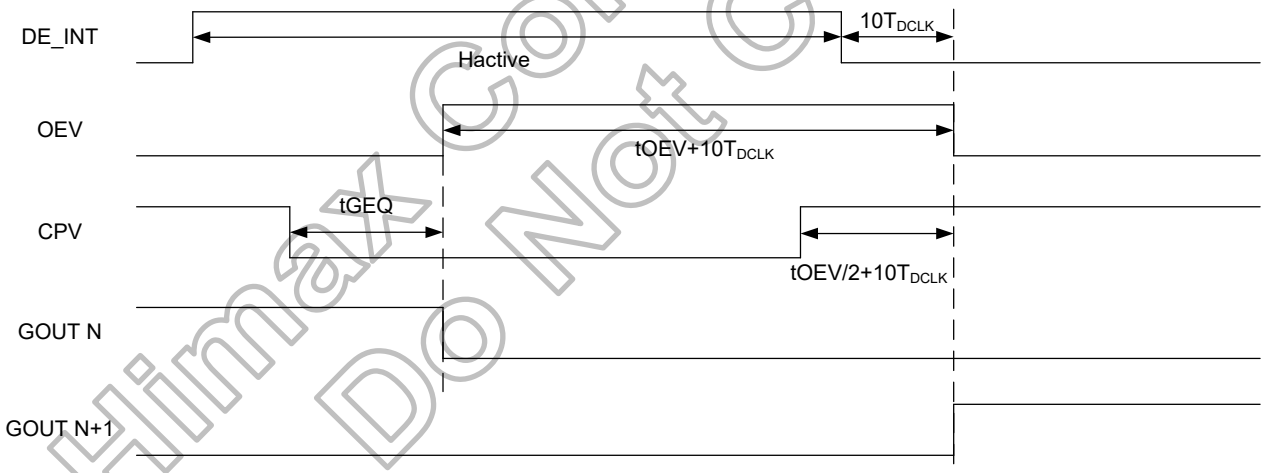


Figure 8.1: Gate control signals output

Page00h R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Ah	1/0	PCR[1:0]		EQ0W[5:0]					
			1	0	0	0	0	1	1	0

PCR[1:0]: Source SW divided selection.

PCR[1:0]		Function	Note
0	0	tSW1=2T_{DCLK}(1), tSW2=2T_{DCLK}(1), tSW3=2T_{DCLK}(1), tSW4=2T_{DCLK}(1)	-
0	1	tSW1=2T_{DCLK}(1), tSW2=4T_{DCLK}(1), tSW3=6T_{DCLK}(1), tSW4=8T_{DCLK}(1)	-
1	0	tSW1=2T_{DCLK}(1), tSW2=6T_{DCLK}(1), tSW3=10T_{DCLK}(1), tSW4=14T_{DCLK}(1)	Default
1	1	tSW1=2T_{DCLK}(1), tSW2=8T_{DCLK}(1), tSW3=14T_{DCLK}(1), tSW4=20T_{DCLK}(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

EQ0W[5:0]: Timing for source driver control. Source outputs are pulled to ground between each line if polarity changes and tEQ is the time pulling output to ground. tEQ0=EQ0W[5:0] *4T_{DCLK}(1). It is suggested to set tEQ0 to 10%~20% of one line.

EQ0W[5:0](2)(3)(4)						Function	Note
0	0	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	-
0	0	0	0	1	0	Reserved	-
0	0	0	0	1	1	12T_{DCLK}(1)	-
:	:	:	:	:	:	:	-
0	0	0	1	1	0	24T_{DCLK}(1)	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	252T_{DCLK}(1)	-

Note: (1) T_{DCLK} is the DCLK unit.
(2) tEQ0+tEQ1 < Htotal - SD output time for single gate.
(3) tEQ0+tEQ1 < Htotal/2 - SD output time for dual gate.
(4) tEQ0+tEQ1 < Htotal/3 - SD output time for triple gate.

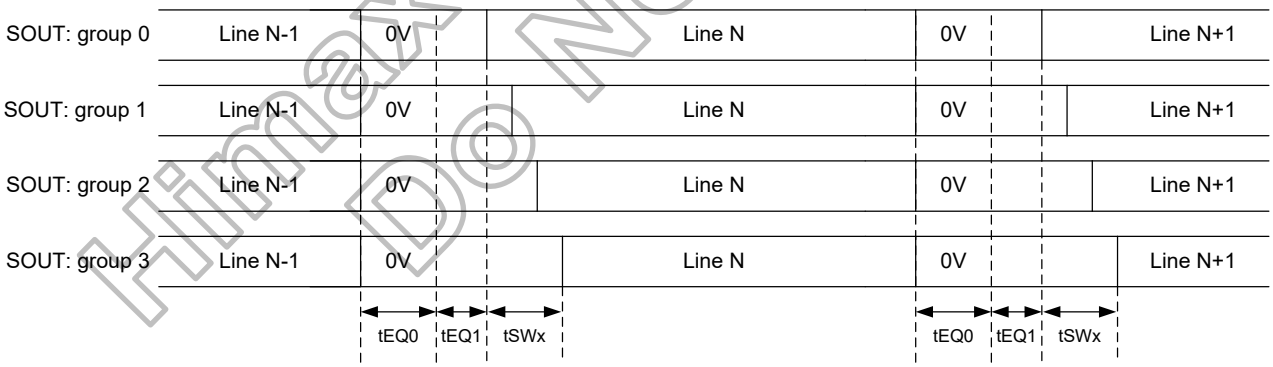


Figure 8.2: Source output timing

Page00h R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Bh	1/0	-	BC[2:0]			POCSD[1:0]		POCGM[1:0]	
			-	0	1	1	0	0	0	0

BC[2:0]: Source driver bias current selection.

BC[2:0]			Function	Note
0	0	0	40%	-
0	0	1	60%	-
0	1	0	80%	-
0	1	1	100%	Default
1	0	0	120%	-
1	0	1	140%	-
1	1	0	160%	-
1	1	1	180%	-

POCSD[1:0]: Source output offset cancelling selection.

POCSD[1:0]		Function	Note
0	0	Type 1	Default
0	1	Type 2	-
1	0	Type 3	-
1	1	Type 4	-

POCGM[1:0]: Gamma offset cancelling selection.

POCGM[1:0]		Function	Note
0	0	Type 1	Default
0	1	Type 2	-
1	0	Type 3	-
1	1	Type 4	-

Page00h R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Ch	1/0	DMY_DATA[7:0]							
			1	0	0	0	0	0	0	0

DMY_DATA[7:0]: Source dummy data select for Zig-Zag type panel.

DMY_DATA[7:0]								Function	Note
0	0	0	0	0	0	0	0	0	-
:	:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	0	128	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	255	-

Page00h R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Dh	1/0	-	-	-	-	PWR_MASK_FAIL_EN	GIP_PWR_OPT	-	EQ0_MODE
			-	-	-	-	1	0	-	0

PWR_MASK_FAIL_EN: Power on mode selection.
If IC enter self protection mode during the power on sequence, it doesn't matter the input signal and finish the power on sequence in self protection mode.

PWR_MASK_FAIL_EN	Function	Note
0	Disable	-
1	Enable	Default

GIP_PWR_OPT: GIP output voltage level option before power ready.

GIP_PWR_OPT	Function	Note
0	VGL	Default
1	GND	-

EQ0_MODE: EQ0 mode selection.

EQ0_MODE	Function	Note
0	EQ0 enable by POL toggle	Default
1	EQ0 always enable	-

Page00h R0Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Eh	1/0	-	-	-	-	-	CH_OPT	-	-
			-	-	-	-	-	0	-	-

CH_OPT: Channel output option.

CH_OPT	Function	Note
0	1440 channels	Default
1	720 channels	-

Page00h R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	0Fh	1/0	-	TS_RHL_OPT	GIP_MX_TABLE_SEL[1:0]		GATE_INTER_SEL	INTL_INV	-	-
			-	1	0	0	0	0	-	-

TS_RHL_OPT: AGAM register value load from OTP by write flag or temperature mode.
If TS_RHL_OPT=1 is selected by write flag, the OTP of AGAM can be written 3 times.
If TS_RHL_OPT=0 is selected by temperature mode, the OTP of AGAM must be written 3 times. And writing the first time is for high temperature (**[TS_H:TS_L=HL]**), the second time is for low temperature (**[TS_H:TS_L=LH]**), the third time is for room temperature (**[TS_H:TS_L=LL]**).

TS_RHL_OPT	Function	Note
0	By temperature mode	-
1	By write flag	Default

GIP_MX_TABLE_SEL[1:0]: GIP MUX setting table selection.

GIP_MX_TABLE_SEL[1:0]		Function	Note
0	0	GIP use Table1 (**Page11h~Page12h**)	Default
0	1	GIP use Table2 (**Page13h~Page14h**)	-
1	0	GIP use Table1 when TB=1 or GIP use Table2 when TB=0	-
1	1	Reserved	-

GATE_INTER_SEL: Gate interlace type selection.

GATE_INTER_SEL	Function	Note
0	L1→L2→R3→R4→L5→L6→R7→R8→....	Default
1	L1→R2→L3→R4→L5→R6→L7→R8→...	-

INTL_INV: NB hardware input pin inverse selection.

NB(1) Hardware pin	INTL_INV Page00h R0Fh[2]	Function	Note
L	0	Enable	-
H		Disable	Default
L	1	Disable	-
H		Enable	-

Note: (1) NB pin control polarity change sequence method Enable/Disable.

Page00h R10h~R11h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	10h	1/0	GATENUM[7:0]							
			0	1	1	0	1	0	0	0
	11h		GATEPASS[3:0]				GATENUM[11:8]			
			1	0	1	0	0	0	0	1

GATEPASS[3:0]: Password to enable manual vertical resolution selection.

GATEPASS[3:0]				Function	Note
0	1	0	1	Enable	-
1	0	1	0	Disable	Default
Else				Disable	-

GATENUM[11:0]: Manual vertical resolution selection. It is effective only if GATEPASS[3:0] is set to 0101. When manual vertical resolution selection is enabled, vertical resolution Vactive is set to GATENUM[11:0], where GATENUM[11:0]=80~4000 **(Vactive=80~4000)**.

GATENUM[11:0] (1)												Function	Note
0	0	0	0	0	0	0	0	0	0	0	0		-
:	:	:	:	:	:	:	:	:	:	:	:	Reserved	-
0	0	0	0	0	1	0	0	1	1	1	1		-
0	0	0	0	0	1	0	1	0	0	0	0	Vactive=80	-
0	0	0	0	0	1	0	1	0	0	0	1	Vactive=81	-
:	:	:	:	:	:	:	:	:	:	:	:	:	-
0	0	0	1	0	1	1	0	1	0	0	0	Vactive=360	Default
:	:	:	:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	0	1	0	0	0	0	0	Vactive=4000	-
1	1	1	1	1	0	1	0	0	0	0	1		-
:	:	:	:	:	:	:	:	:	:	:	:	Reserved	-
1	1	1	1	1	1	1	1	1	1	1	1		-

Note: (1) The Vtotal must less than 4094 Line.

Page00h R12h~R13h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	12h	1/0	HSETNUM[7:0]							
			0	0	0	0	0	0	0	0
	13h		HSETPASS[3:0]				-	HSETNUM[10:8]		
			1	0	1	0	-	0	0	1

HSETPASS[3:0]: HSET_NUM_SEL function enables.

HSETPASS[3:0]				Function	Note
0	1	0	1	Enable	-
1	0	1	0	Disable	Default
Else				Disable	-

HSETNUM[10:0]: Manual horizontal resolution selection. It is effective only if HSETPASS[3:0] is set to 0101. When manual horizontal resolution selection is enabled, horizontal resolution Hactive is set to HSETNUM[10:0] X 4. The Hactive setting range is HSETNUM[10:0] =160~1920.

HSETNUM[10:0]											Function	Note
0	0	0	0	0	0	0	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	:	:	:	:		-
0	0	0	0	0	1	0	0	1	1	1		-
0	0	0	0	0	1	0	1	0	0	0	Hactive=160	-
0	0	0	0	0	1	0	1	0	0	1	Hactive=164	-
:	:	:	:	:	:	:	:	:	:	:	:	-
0	0	1	0	0	0	0	0	0	0	0	Hactive=1024	Default
:	:	:	:	:	:	:	:	:	:	:	:	-
0	0	1	1	1	1	0	0	0	0	0	Hactive=1920	-
0	0	1	1	1	1	0	0	0	0	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	:		-
1	1	1	1	1	1	1	1	1	1	1		-

Page00h R14h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	14h	1/0	-	-	-	EQ1W[4:0]				
			-	-	-	0	0	0	0	0

EQ1W[4:0]: Timing for source pre-charge setting to VCC1.
tEQ1=EQ1W[4:0] *4T_{DCLK}(1).

EQ1W[4:0](2)(3)(4)					Function	Note
0	0	0	0	0	0T_{DCLK}(1)	Default
0	0	0	0	1	4T_{DCLK}(1)	-
0	0	0	1	0	8T_{DCLK}(1)	-
0	0	0	1	1	12T_{DCLK}(1)	-
:	:	:	:	:	:	-
1	1	1	1	1	124T_{DCLK}(1)	-

Note: (1) T_{DCLK} is the DCLK unit.
(2) tEQ0+tEQ1 < Htotal - SD output time for single gate.
(3) tEQ0+tEQ1 < Htotal/2 - SD output time for dual gate.
(4) tEQ0+tEQ1 < Htotal/3 - SD output time for triple gate.

Page00h R15h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	15h	1/0	BIST_VFP[4:0]					-	-	-
			0	0	0	0	0	-	-	-

BIST_VFP[4:0]: Adjust vertical front porch of BIST mode.
VFPB=(BIST_VFP * 2 + 16)

BIST_VFP[4:0]					Function	Note
0	0	0	0	0	16H(1)	Default
:	:	:	:	:	:	-
0	0	0	1	1	22H(1)	-
:	:	:	:	:	:	-
1	1	1	1	1	78H(1)	-

Note: (1) H is the horizontal line unit.

Page00h R16h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	16h	1/0	POL_INV_FRM[3:0]				POL_TOG_VBLK	-	PRE_SCAN[1:0]	
			0	0	0	0	0	-	0	0

POL_INV_FRM[3:0]: Polarity change sequence method selection.
When the polarity changes sequence inversion occurred, the VCOM has offset voltage continue one frame.

POL_INV_FRM[3:0]				Function	Note
0	0	0	0	Polarity doesn't inverse by frame	Default
0	0	0	1	Polarity change by 2 Frame	-
0	0	1	0	Polarity change by 4 Frame	-
0	0	1	1	Polarity change by 8 Frame	-
:	:	:	:	:	-
1	0	1	0	Polarity change by 1024 Frame	-
1	0	1	1	Polarity change by 2048 Frame	-

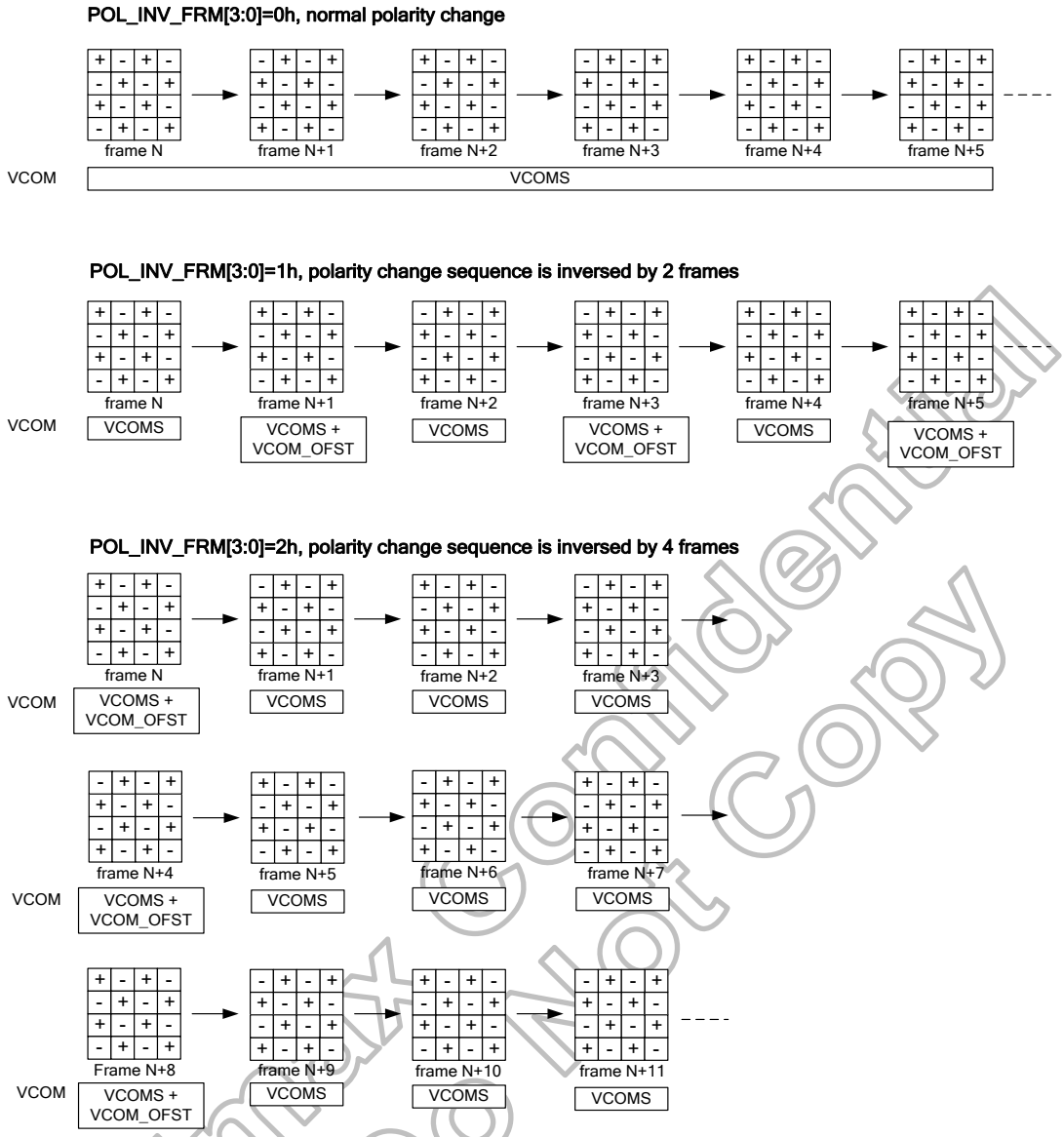


Figure 8.3: Polarity change sequence inversion

POL_TOG_VBLK: POL keep toggle at vertical blanking.

POL_TOG_VBLK	Function	Note
0	Disable	Default
1	Enable	-

PRE_SCAN[1:0]: Tradition Gate driver pre-scan mode select.

PRE_SCAN[1:0](1)(2)		Function	Note
0	0	Normal gate **(Disable pre-scan)**	Default
0	1	Gate Pre-scan md1	-
1	0	Gate Pre-scan md2	-
1	1	Gate Pre-scan md2	-

Note: (1) Pre-scan function does not support interlace mode. **(GPOS[1:0]=10)**
(2) Refer to Figure 6.12: The restriction of input DE variation.

Page00h R17h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	17h	1/0	BIST_GRAY[7:0]							
			1	0	0	0	0	0	0	0

BIST_GRAY[7:0]: BIST mode gray scale pattern setting.

Page00h R18h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	18h	1/0	BIST_H_OFFSET[7:0]							
			0	0	0	0	0	0	0	0

BIST_H_OFFSET[7:0]: Add Htotal width for BIST mode, step is 1T(1).
Note: (1) T is the internal oscillator clock unit.

Page00h R19h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	19h	1/0	-	-	BIST_OSC_SEL	H_OSCLK_SEL[4:0]				
			-	-	0	0	1	1	1	1

BIST_OSC_SEL: Oscillator frequency selection for BIST.

BIST_OSC_SEL	Function	Note
0	Setting by HRES*VRES*60	Default
1	Setting by H_OSCLK_SEL	-

H_OSCLK_SEL[4:0]: Oscillator selection for BIST mode.

H_OSCLK_SEL[4:0]					Function	Note
0	0	0	0	0	85.000MHz	-
0	0	0	0	1	80.000MHz	-
0	0	0	1	0	75.000MHz	-
0	0	0	1	1	70.000MHz	-
0	0	1	0	0	65.000MHz	-
0	0	1	0	1	57.000MHz	-
0	0	1	1	0	50.000MHz	-
0	0	1	1	1	42.000MHz	-
0	1	0	0	0	42.500MHz	-
0	1	0	0	1	40.000MHz	-
0	1	0	1	0	37.500MHz	-
0	1	0	1	1	35.000MHz	-
0	1	1	0	0	32.500MHz	-
0	1	1	0	1	28.500MHz	-
0	1	1	1	0	25.000MHz	-
0	1	1	1	1	21.000MHz	Default
1	0	0	0	0	21.250MHz	-
1	0	0	0	1	20.000MHz	-
1	0	0	1	0	18.750MHz	-
1	0	0	1	1	17.500MHz	-
1	0	1	0	0	16.250MHz	-
1	0	1	0	1	14.250MHz	-
1	0	1	1	0	12.500MHz	-
1	0	1	1	1	10.500MHz	-
1	1	0	0	0	10.625MHz	-
1	1	0	0	1	10.000MHz	-
1	1	0	1	0	9.375MHz	-
1	1	0	1	1	8.750MHz	-
1	1	1	0	0	8.125MHz	-
1	1	1	0	1	7.125MHz	-
1	1	1	1	0	6.250MHz	-
1	1	1	1	1	5.250MHz	-

Page00h R1Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	1Ah	1/0	-	DISPOFF_EN	-	-	-	-	-	-
			-	0	-	-	-	-	-	-

DISPOFF_EN: Display off function.

DISPOFF_EN	Function	Note
0	Disable	Default
1	Enable	-

Page00h R1Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	1Ch	1/0	CHIP_ID[7:0]							
			0	1	1	1	0	0	1	0

CHIP_ID[7:0]: CHIP_ID for product identification.
The default value of HX8272-C01-LT is 0x72.

Page00h R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	1Eh	1/0	STBYB_CMD[7:0]							
			0	0	0	0	0	0	0	0

STBYB_CMD[7:0]: Standby mode enable.

STBYB_CMD[7:0]								Function	Note
0	0	0	0	0	0	0	0	Normal mode	Default
0	1	0	1	0	1	0	1	Standby mode	-
Else								Normal mode	-

STBYB Hardware pin	STBYB_CMD[7:0] Page00h R1Eh[7:0]	Function	Note
H	Not 55h	Normal mode	-
H	55h	Standby mode	-
L	-	Standby mode	-
L	-	Standby mode	-

8.2.2. Page01h for Normal function

Page01h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page01h R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	04h	1/0	-	-	VCLS[1:0]		-	-	-	-
			-	-	1	0	-	-	-	-

VCLS[1:0]: VCL voltage selection, VCL=-2.25-VCLS[1:0] x 0.25V.

VCLS[1:0]		Function	Note
0	0	-2.25V	-
0	1	-2.50V	-
1	0	-2.75V	Default
1	1	-3.00V	-

Page01h R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	05h	1/0	FAIL_DET_SEL	FAIL_DET_INV	-	ASIL_NOSIG_SEL	ASIL_INV	ASIL_WD[2:0]		
			1	0	-	0	0	1	0	0

FAIL_DET_SEL: FAIL_DET output signal selection.

FAIL_DET_SEL	Function	Note
0	Fail flag output to FAIL_DET	-
1	ASIL signal output to FAIL_DET	Default

FAIL_DET_INV: FAIL_DET output signal inverse.

FAIL_DET_INV	Function	Note
0	Normal	Default
1	Inverse	-

ASIL_NOSIG_SEL: No signal define for ASIL.

ASIL_NOSIG_SEL	Function	Note
0	Only no clock, ASIL output 40Hz pulse.	Default
1	No clock / DE **(DEmode)** / HS/VS **(SYNC mode)**, ASIL output 40Hz pulse.	-

ASIL_INV: ASIL output inverse enable.

ASIL_INV	Function	Note
0	Disable	Default
1	Enable	-

ASIL_WD[2:0]: ASIL signal pulse width selection.
When ASIL output 60 Hz signal **(Same as frame rate)**, ASIL pulse width **(WD)** is controlled by ASIL_WD[2:0] & ASIL_WD_OPT[1:0] **(Page01h_R15h[1:0])**.

When ASIL_WD_OPT[1:0]=2'b00 or 2'b01, ASIL pulse width step (WS) is 1H(1).

ASIL_WD[2:0]			Function	Note
0	0	0	WD=2H(1) **(2WS)**	-
0	0	1	WD=2H(1) **(2WS)**	-
0	1	0	WD=4H(1) **(4WS)**	-
0	1	1	WD=6H(1)~7H(1) **(6WS~6WS+1)**	-
1	0	0	WD=8H(1)~9H(1) **(8WS~8WS+1)**	Default
1	0	1	WD=10H(1)~11H(1) **(10WS~10WS+1)**	-
1	1	0	WD=12H(1)~13H(1) **(12WS~12WS+1)**	-
1	1	1	WD=14H(1)~15H(1) **(14WS~14WS+1)**	-

Note: (1) H is the horizontal line unit.

When ASIL_WD_OPT[1:0]=2'b10, ASIL pulse width step (WS) is 32H(1).

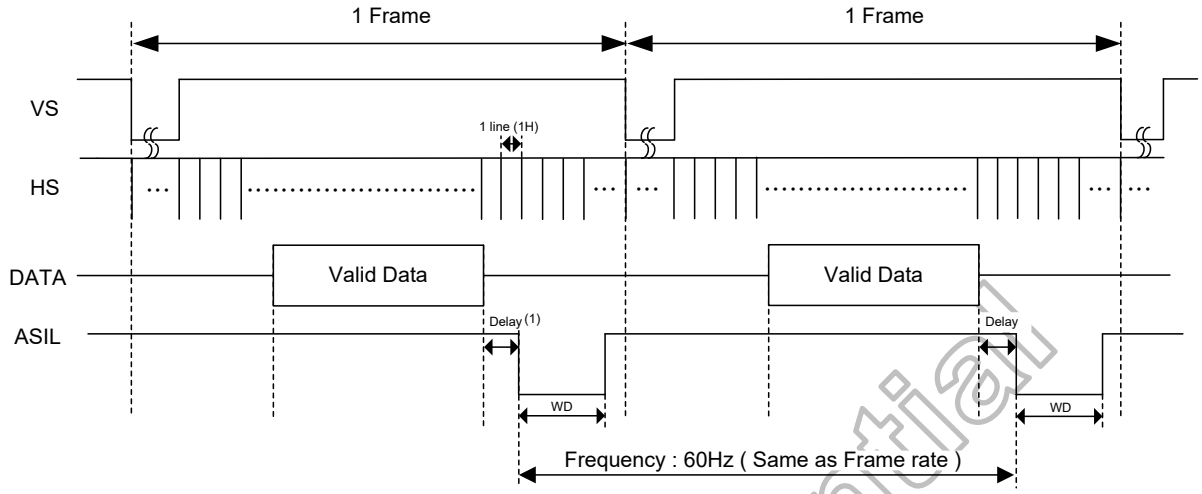
ASIL_WD[2:0]			Function	Note
0	0	0	WD=64H(1)~95H(1) **(2WS~3WS-1)**	-
0	0	1	WD=64H(1)~95H(1) **(2WS~3WS-1)**	-
0	1	0	WD=128H(1)~159H(1) **(4WS~5WS-1)**	-
0	1	1	WD=192H(1)~223H(1) **(6WS~7WS-1)**	-
1	0	0	WD=256H(1)~287H(1) **(8WS~9WS-1)**	Default
1	0	1	WD=320H(1)~351H(1) **(10WS~11WS-1)**	-
1	1	0	WD=384H(1)~415H(1) **(12WS~13WS-1)**	-
1	1	1	WD=448H(1)~479H(1) **(14WS~15WS-1)**	-

Note: (1) H is the horizontal line unit.

When ASIL_WD_OPT[1:0]=2'b11, ASIL pulse width step (WS) is 64H(1).

ASIL_WD[2:0]			Function	Note
0	0	0	WD=128H(1)~191H(1) **(2WS~3WS-1)**	-
0	0	1	WD=128H(1)~191H(1) **(2WS~3WS-1)**	-
0	1	0	WD=256H(1)~319H(1) **(4WS~5WS-1)**	-
0	1	1	WD=384H(1)~445H(1) **(6WS~7WS-1)**	-
1	0	0	WD=512H(1)~575H(1) **(8WS~9WS-1)**	Default
1	0	1	WD=640H(1)~703H(1) **(10WS~11WS-1)**	-
1	1	0	WD=768H(1)~831H(1) **(12WS~13WS-1)**	-
1	1	1	WD=896H(1)~959H(1) **(14WS~15WS-1)**	-

Note: (1) H is the horizontal line unit.



Note: (1) If Vactive & Vtotal are not a multiple of ASIL pulse width step **(WS)**, the range of Delay is (WS+1)~(3WS -1).

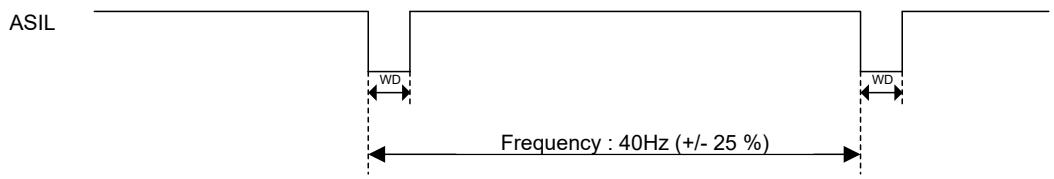
When ASIL output 40Hz signal **(±25%)**, ASIL pulse width **(WD)** is controlled by ASIL_WD[2:0] & ASIL_WD_OPT[1:0] **(Page01h R15h[1:0])**.

If ASIL_WD_OPT[1:0]=2'b00 or 2'b01, ASIL pulse width step (WS) is 100µs.

ASIL_WD[2:0]			Function	Note
0	0	0	WD=100µs **(100µs x 1)**	-
0	0	1	WD=100µs **(100µs x 1)**	-
0	1	0	WD=200µs **(100µs x 2)**	-
0	1	1	WD=300µs **(100µs x 3)**	-
1	0	0	WD=400µs **(100µs x 4)**	Default
1	0	1	WD=500µs **(100µs x 5)**	-
1	1	0	WD=600µs **(100µs x 6)**	-
1	1	1	WD=700µs **(100µs x 7)**	-

If ASIL_WD_OPT[1:0]=2'b10 or 2'b11, ASIL pulse width step (WS) is 3ms.

ASIL_WD[2:0]			Function	Note
0	0	0	WD=6ms **(3ms x 2)**	-
0	0	1	WD=6ms **(3ms x 2)**	-
0	1	0	WD=6ms **(3ms x 2)**	-
0	1	1	WD=9ms **(3ms x 3)**	-
1	0	0	WD=12ms **(3ms x 4)**	Default
1	0	1	WD=15ms **(3ms x 5)**	-
1	1	0	WD=18ms **(3ms x 6)**	-
1	1	1	WD=18ms **(3ms x 6)**	-



Page01h R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	06h	1/0	BANK12_OFT[7:0]							
			0	0	0	0	0	0	0	0

BANK12_OFT[7:0]: Shift divided position between Bank1 and Bank2.

BANK12_OFT[7:0]								Function	Note
0	0	0	0	0	0	0	0	$0T_{DCLK}$(1)	Default
0	0	0	0	0	0	0	1	Right shift $1T_{DCLK}$(1)	-
0	0	0	0	0	0	1	0	Right shift $2T_{DCLK}$(1)	-
:	:	:	:	:	:	:	:	:	-
0	1	1	1	1	1	1	1	Right shift $63T_{DCLK}$(1)	-
1	0	0	0	0	0	0	0	$0T_{DCLK}$(1)	-
1	0	0	0	0	0	0	1	Left shift $1T_{DCLK}$(1)	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	Left shift $63T_{DCLK}$(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

Page01h R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	07h	1/0	BANK23_OFT[7:0]							
			0	0	0	0	0	0	0	0

BANK23_OFT[7:0]: Shift divided position between Bank2 and Bank3.

BANK23_OFT[7:0]								Function	Note
0	0	0	0	0	0	0	0	$0T_{DCLK}$(1)	Default
0	0	0	0	0	0	0	1	Right shift $1T_{DCLK}$(1)	-
0	0	0	0	0	0	1	0	Right shift $2T_{DCLK}$(1)	-
:	:	:	:	:	:	:	:	:	-
0	1	1	1	1	1	1	1	Right shift $63T_{DCLK}$(1)	-
1	0	0	0	0	0	0	0	$0T_{DCLK}$(1)	-
1	0	0	0	0	0	0	1	Left shift $1T_{DCLK}$(1)	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	Left shift $63T_{DCLK}$(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

Page01h R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	10h	1/0	H_TOTAL_OFT[3:0]				-	-	-	-
			0	0	0	0	-	-	-	-

H_TOTAL_OFT[3:0]: H total number offset.

H_TOTAL_OFT[3:0]				Function	Note
0	0	0	0	$0T_{DCLK}$(1)	Default
0	0	0	1	$1T_{DCLK}$(1)	-
:	:	:	:	:	-
1	1	1	1	$255T_{DCLK}$(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

Page01h R15h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	15h	1/0	-						ASIL_WD_OPT [1:0]	
			0	0	0	0	0	0	0	0

ASIL_WD_OPT[1:0]: ASIL pulse width step **(WS)** option.

When ASIL output 60Hz signal (Same as frame rate), ASIL pulse width step is 1H(1) or 32H(1) or 64H(1).

ASIL_WD_OPT[1:0]		Function	Note
0	0	1H(1)	Default
0	1	1H(1)	-
1	0	32H(1)	-
1	1	64H(1)	-

Note: (1) H is the horizontal line unit.

When ASIL output 40Hz signal (±25%), ASIL pulse width step is 100μs or 3ms.

ASIL_WD_OPT[1:0]		Function	Note
0	0	100μs	Default
0	1	100μs	-
1	0	3ms	-
1	1	3ms	-

8.2.3. Page02h for Power control function

Page02h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page02h R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	01h	1/0	-	PFMFREN	VSPEN	VSNEN	DRVPD[1:0]		DRVND[1:0]	
			-	0	1	1	1	0	1	0

PFMFREN: PFM frequency randomizer enable.

PFMFREN	Function	Note
0	Disable	Default
1	Enable	-

VSPEN: VSP enable.

VSPEN	Function	Note
0	Disable	-
1	Enable	Default

VSNEN: VSN enable.

VSNEN	Function	Note
0	Disable	-
1	Enable	Default

DRVPD[1:0]: DRVP buffer size selection.

DRVPD[1:0]		Function	Note
0	0	25%	-
0	1	50%	-
1	0	100%	Default
1	1	150%	-

DRVND[1:0]: DRVN buffer size selection.

DRVND[1:0]		Function	Note
0	0	25%	-
0	1	50%	-
1	0	100%	Default
1	1	150%	-

Page02h R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	02h	1/0	GAS_VCC_EN	-	-	VSPS[4:0]				
			1	-	-	1	0	1	0	0

GAS_VCC_EN: GAS detect VCC1 enable.

GAS_VCC_EN	Function	Note
0	Disable	-
1	Enable	Default

VSPS[4:0]: VSP voltage selection, VSP=5V+VSPS[4:0] x 0.1V.

VSPS[4:0]					Function	Note
0	0	0	0	0	5.0V	-
0	0	0	0	1	5.1V	-
:	:	:	:	:	:	-
0	1	1	0	1	6.3V	-
:	:	:	:	:	:	-
1	0	0	1	1	6.9V	-
1	0	1	0	0	7.0V	Default
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page02h R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	03h	1/0	-	-	-	VSNS[4:0]				
			-	-	-	1	0	1	0	0

VSNS[4:0]: VSN voltage selection, VSN=-5V-VSNS[4:0] x 0.1V.

VSNS[4:0]					Function	Note
0	0	0	0	0	-5.0V	-
0	0	0	0	1	-5.1V	-
:	:	:	:	:	:	-
0	1	1	0	1	-6.3V	-
:	:	:	:	:	:	-
1	0	0	1	1	-6.9V	-
1	0	1	0	0	-7.0V	Default
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page02h R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	04h	1/0	VGHXS[1:0]		VGHS[5:0]					
			0	1	0	0	1	1	1	0

VGHXS[1:0]: VGH boosting mode selection.

VGHXS[1:0]		Function	Note
0	0	2X	-
0	1	3X	Default
1	0	4X	-
1	1	4X	-

VGHS[5:0]: VGH voltage selection, VGH=5+VGHS[5:0] x 0.5V.

VGHS[5:0](1)(2)						Function	Note
0	0	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	-
0	0	0	0	1	1	Reserved	-
0	0	0	1	0	0	7.0V	-
:	:	:	:	:	:	:	-
0	0	1	1	1	0	12.0V	Default
:	:	:	:	:	:	:	-
1	0	0	1	0	1	23.5V	-
1	0	0	1	1	0	24.0V	-
:	:	:	:	:	:	24.0V	-
1	1	1	1	1	1	24.0V	-

Note: (1) VGH + |VGL| ≤ 32V.
(2) VGH > VSP.

Page02h R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	05h	1/0	-	-	VGLXS	VGLS[4:0]				
			-	-	0	0	0	1	1	0

VGLXS: VGL boosting mode selection.

VGLXS	Function	Note
0	2X	Default
1	3X	-

VGLS[4:0]: VGL voltage selection, VGL=-5-VGLS[4:0] x 0.5V.

VGLS[4:0](1)(2)					Function	Note
0	0	0	0	0	Reserved	-
:	:	:	:	:	:	-
0	0	0	1	1	Reserved	-
0	0	1	0	0	-7.0V	-
0	0	1	0	1	-7.5V	-
0	0	1	1	0	-8.0V	Default.
:	:	:	:	:	:	-
1	0	1	1	0	-16.0V	-
:	:	:	:	:	-16.0V	-
1	1	1	1	1	-16.0V	-

Note: (1) VGH + |VGL| ≤ 32V.
(2) |VGL| > |VSN|.

Page02h R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	06h	1/0	VMONPS[1:0]		VSDPEN	VSDPS[4:0]				
			1	0	1	1	0	1	0	0

VMONPS[1:0]: PFM of VSP over current detection voltage selection.

VMONPS[1:0]		Function	Note
0	0	0.100V	-
0	1	0.125V	-
1	0	0.150V	Default
1	1	0.175V	-

VSDPEN: VSDP regulator enable.

VSDPEN	Function	Note
0	Disable	-
1	Enable	Default

VSDPS[4:0]: VSDP voltage selection, VSDP=4.8V+VSDPS[4:0] x 0.1V.

VSDPS[4:0]					Function	Note
0	0	0	0	0	4.8V	-
0	0	0	0	1	4.9V	-
:	:	:	:	:	:	-
0	1	1	0	0	6.0V	-
:	:	:	:	:	:	-
1	0	0	1	1	6.7V	-
1	0	1	0	0	6.8V	Default
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page02h R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	07h	1/0	VMONNS[1:0]		VSDNEN	VSDNS[4:0]				
			1	0	1	1	0	1	0	0

VMONNS[1:0]: PFM of VSN over current detection voltage selection.

VMONNS[1:0]		Function	Note
0	0	0.100V	-
0	1	0.125V	-
1	0	0.150V	Default
1	1	0.175V	-

VSDNEN: VSDN regulator enable.

VSDNEN	Function	Note
0	Disable	-
1	Enable	Default

VSDNS[4:0]: VSDN voltage selection, VSDN=-4.8V-VSDNS[4:0] x 0.1V.

VSDNS[4:0]					Function	Note
0	0	0	0	0	-4.8V	-
0	0	0	0	1	-4.9V	-
:	:	:	:	:	:	-
0	1	1	0	0	-6.0V	-
:	:	:	:	:	:	-
1	0	0	1	1	-6.7V	-
1	0	1	0	0	-6.8V	Default
1	0	1	0	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page02h R08h~R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	08h	1/0	VSPON[3:0]				VSPOFF[3:0]			
			0	1	0	1	0	1	0	1
	09h		VSNON[3:0]				VSNOFF[3:0]			
			0	1	0	1	0	1	0	1
	0Ah		VSPON_S[3:0]				VSPOFF_S[3:0]			
			0	0	1	0	1	1	1	1
	0Bh		VSNON_S[3:0]				VSNOFF_S[3:0]			
			0	0	1	0	1	1	1	1

VSPON[3:0]/VSNON[3:0]: PFM turn on duty of DRVP **(tONP)**/DRVN **(tONN)** at normal operation.

VSPON[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSNON[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSPON_S[3:0]/VSNON_S[3:0]: PFM turn on duty of DRVP **(tONP)**/DRVN **(tONN)** at soft start of power on sequence.

VSPON_S[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	0	1	0	tPFM * 4	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSNON_S[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	0	1	0	tPFM * 4	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSPOFF[3:0]/VSNOFF[3:0]: PFM turn off duty of DRVP **(tOFFP)**/DRVN **(tOFFP)** at normal operation. Also note that low state will be larger than setting if VSP/VSN already reaches **(higher than)** the target.

VSPOFF[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSNOFF[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
0	1	0	1	tPFM * 7	Default
:	:	:	:	:	-
1	1	1	1	tPFM * 17	-

VSPOFF_S[3:0]/VSNOFF_S[3:0]: PFM turn off duty of DRVP **(tOFFP)** /DRVN **(tOFFP)** at soft start of power on sequence. Also note that low state will be larger than setting if VSP/VSN already reaches **(higher than)** the target.

VSPOFF_S[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
1	1	1	0	tPFM * 16	-
1	1	1	1	tPFM * 17	Default

VSNOFF_S[3:0]				Function	Note
0	0	0	0	tPFM * 2	-
:	:	:	:	:	-
1	1	1	0	tPFM * 16	-
1	1	1	1	tPFM * 17	Default

Page02h R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	0Ch	1/0	TP_DLY[7:0]							
			0	1	0	0	0	0	0	0

TP_DLY[7:0]: TP_SYNC rising edge offset setting when TP_SYNC_SEL[2:0]=3'b110. Range=(1~255) * $4T_{DCLK}$(1).

TP_DLY[7:0]								Function	Note
0	0	0	0	0	0	0	0	$4T_{DCLK}$(1)	-
0	0	0	0	0	0	0	1	$4T_{DCLK}$(1)	-
0	0	0	0	0	0	1	0	$8T_{DCLK}$(1)	-
:	:	:	:	:	:	:	:	:	-
0	1	0	0	0	0	0	0	$256T_{DCLK}$(1)	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	$1020T_{DCLK}$(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

Page02h R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	0Dh	1/0	TP_WIDTH[7:0]							
			0	1	0	0	0	0	0	0

TP_WIDTH[7:0]: TP_SYNC width setting when TP_SYNC_SEL[2:0]=3'b110.
Range=(1~255) * $4T_{DCLK}$(1).

TP_WIDTH[7:0]								Function	Note
0	0	0	0	0	0	0	0	$4T_{DCLK}$(1)	-
0	0	0	0	0	0	0	1	$4T_{DCLK}$(1)	-
0	0	0	0	0	0	1	0	$8T_{DCLK}$(1)	-
:	:	:	:	:	:	:	:	:	-
0	1	0	0	0	0	0	0	$256T_{DCLK}$(1)	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	$1020T_{DCLK}$(1)	-

Note: (1) T_{DCLK} is the DCLK unit.

Page02h R0Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	0Eh	1/0	TP_SYNC1_SEL[2:0]			TP_SYNC2_SEL[2:0]			TP_SYNC_INV	TP_SYNC_VBLK
			1	1	1	1	1	1	0	0

TP_SYNC1_SEL[2:0]/TP_SYNC2_SEL[2:0]: TP_SYNC1/TP_SYNC2 output signal selection.

TP_SYNC1_SEL[2:0] TP_SYNC2_SEL[2:0]			Function	Note
0	0	0	Output HS signal.	-
0	0	1	Output Source output period by frame. **(Internal VDEN)**	-
0	1	0	Output VS signal.	-
0	1	1	Output ASIL.	-
1	0	0	Output FAIL_DET signal.	-
1	0	1	Output /XAO signal.	-
1	1	0	TP_SYNC register setting. **(TP_SYNC trigger by TP_DLY[7:0] and TP_WIDTH_ENB setting)**	-
1	1	1	output GND.	Default

TP_SYNC_INV: TP_SYNC output inverse function.

TP_SYNC_INV	Function	Note
0	Disable	Default
1	Enable	-

TP_SYNC_VBLK: TP_SYNC output toggle at vertical blanking.

TP_SYNC_VBLK	Function	Note
0	Disable	Default
1	Enable	-

Page02h R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	0Fh	1/0	TP_WIDTH_ENB	PFM_DET_EN	-	PFM_NG_OPT	PFM_OSC_SEL [1:0]		PFM_DET_OPT	
			0	1	-	0	1	0	0	0

TP_WIDTH_ENB: TP_SYNC width selection when TP_SYNC1_SEL[2:0]/TP_SYNC2_SEL[2:0]=3'b110.

TP_WIDTH_ENB	Function	Note
0	TP_SYNC width by TP_WIDTH[7:0] **(Page02h R0Dh)**	Default
1	TP_SYNC falling follow Source_SW rising edge.	-

PFM_DET_EN: PFM abnormal detect function enable.

PFM_DET_EN	Function	Note
0	Disable	-
1	Enable	Default

PFM_NG_OPT: Polarity option of PFM abnormal flag output to TEST4 pin.

PFM_NG_OPT	Function	Note
0	TEST4 output low when PFM abnormal	Default
1	TEST4 output high when PFM abnormal	-

PFM_OSC_SEL[1:0]: PFM clock frequency selection.

PFM_OSC_SEL[1:0]		Function	Note
0	0	5.0MHz	-
0	1	2.5MHz	-
1	0	10.0MHz	Default
1	1	10.0MHz	-

PFM_DET_OPT[1:0]: PFM fail-detect time selection.
PFM abnormal boost state over the N ms, then PFM_NG trigger and DRVP/DRVN stop.

PFM_DET_OPT[1:0]		Function	Note
0	0	N=60ms	Default
0	1	N=120ms	-
1	0	N=240ms	-
1	1	N=480ms	-

Page02h R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	10h	1/0	-	PFM_SS_SEL	VCOM_OTP	VCOMEN	S_VCL_ENB	M_VCL_ENB	VCOMD[1:0]	
			-	0	0	1	0	0	0	1

PFM_SS_SEL: PFM soft start duration selection.

PFM_SS_SEL	Function	Note
0	From 1st VS to 4th and 1/3 VS	Default
1	From 1st VS to 3rd VS	-

VCOM_OTP: VCOMS setting selection.

VCOM_OTP	Function	Note
0	If EEPEN=1, VCOMS from EEPROM	Default
1	VCOMS from OTP, doesn't matter EEPEN setting	-

VCOMEN: VCOM regulator enable.

VCOMEN	Function	Note
0	Disable	-
1	Enable	Default

S_VCL_ENB: Slave chip VCL regulator enable.

S_VCL_ENB	Function	Note
0	Enable	Default
1	Disable	-

M_VCL_ENB: Master chip VCL regulator enable.

M_VCL_ENB	Function	Note
0	Enable	Default
1	Disable	-

VCOMD[1:0]: VCOM driving capability selection.

VCOMD[1:0]		Function	Note
0	0	50%	-
0	1	100%	Default
1	0	150%	-
1	1	200%	-

Page02h R11h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	11h	1/0	VGHL_LIMIT	VGHEN	VGLEN	FCPS	-	-	FCP[1:0]	
			1	1	1	0	-	-	1	1

VGHL_LIMIT: Auto setting for (VGH + |VGL| ≤ 32).

VGHL_LIMIT	Function	Note
0	Disable	-
1	VGH + |VGL| ≤ 32	Default

VGHEN: VGH charge pump circuit enable.

EXT_PWR Hardware pin	VGHEN Page02h R11h[6]	Function	Note
L	0	Disable	-
L	1	Enable	Default
H	0	Disable	-
H	1	Disable	-

VGLEN: VGL charge pump circuit enable.

EXT_PWR Hardware pin	VGLEN Page02h R11h[5]	Function	Note
L	0	Disable	-
L	1	Enable	Default
H	0	Disable	-
H	1	Disable	-

FCPS: VGH and VGL charge pump frequency option.

FCPS	Function	Note
0	CPCLK setting by HS	Default
1	CPCLK setting by fixed oscillator	-

FCP[1:0]: VGH and VGL charge pump frequency setting.

When FCPS=0, CPCLK setting by HS.

FCPS	FCP[1:0]		Function	Note
0	0	0	1CPCLK / 2HS	-
0	0	1	1CPCLK / HS	-
0	1	0	2CPCLK / HS	-
0	1	1	4CPCLK / HS	Default

When FCPS=1, CPCLK setting by fixed oscillator.

FCPS	FCP[1:0]		Function	Note
1	0	0	312KHz	-
1	0	1	312KHz	-
1	1	0	500KHz	-
1	1	1	625KHz	Default

Page02h R12h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	12h	1/0	T_OCPEN	-	T_VGMREGEN	T_VGMPHS[4:0]				
			0	-	1	1	1	0	1	0

T_OCPEN: PFM over current protection function enable.

T_OCPEN	Function	Note
0	Disable	Default
1	Enable	-

T_VGMREGEN: VGMPHO/VGMPLO and VGMNHO/VGMNLO regulators enable.

T_VGMREGEN	Function	Note
0	Disable	-
1	Enable	Default

T_VGMPHS[4:0]: VGMPHO voltage selection, VGMPHO=4+T_VGMPHS[4:0] x 0.1V.

T_VGMPHS[4:0]					Function	Note
0	0	0	0	0	4.0V	-
0	0	0	0	1	4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	5.8V	-
:	:	:	:	:	:	-
1	1	0	0	1	6.5V	-
1	1	0	1	0	6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page02h R13h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	13h	1/0	-	-	-	T_VGMNHS[4:0]				
			-	-	-	1	1	0	1	0

T_VGMNHS[4:0]: VGMNHO voltage selection, VGMNHO=-4 -T_VGMNHS[4:0] x 0.1V.

T_VGMNHS[4:0]					Function	Note
0	0	0	0	0	-4.0V	-
0	0	0	0	1	-4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	-5.8V	-
:	:	:	:	:	:	-
1	1	0	0	1	-6.5V	-
1	1	0	1	0	-6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page02h R14h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	14h	1/0	T_VGMPLS[3:0]				T_VGMNLS[3:0]			
			0	0	0	1	0	0	0	1

T_VGMPLS[3:0]: VGMPLO voltage selection, VGMPLO=0.1+T_VGMPLS[3:0] x 0.1V.

T_VGMPLS[3:0]				Function	Note
0	0	0	0	Reserved	-
0	0	0	1	0.2V	Default
:	:	:	:	:	-
1	0	0	1	1.0V	-
:	:	:	:	:	-
1	1	1	0	1.5V	-
1	1	1	1	1.6V	-

T_VGMNLS[3:0]: VGMNLO voltage selection, VGMNLO=-0.1-T_VGMNLS[3:0] x 0.1V.

T_VGMNLS[3:0]				Function	Note
0	0	0	0	Reserved	-
0	0	0	1	-0.2V	Default
:	:	:	:	:	-
1	0	0	1	-1.0V	-
:	:	:	:	:	-
1	1	1	0	-1.5V	-
1	1	1	1	-1.6V	-

Page02h R15h~R16h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	15h	1/0	-	-	-	-	-	-	OTP_RL_FAIL_ENB	-
			-	-	-	-	-	-	0	-
	16h		PFM_NG_ENB	OTP_TRIM_FAIL_ENB	EEPROM_FAIL_ENB	NO_VIDEO_FAIL_ENB	GIP_DET_FAIL_ENB/GATE_FAIL_ENB(1)	SOURCE_FAIL_ENB	POWER_FAIL_ENB	LVDS_FAIL_ENB
			0	0	0	0	0	0	0	0

Note: (1) According to the GDSEL.

OTP_RL_FAIL_ENB: OTP reload fail signal output to Fail_Flag and FAIL_DET pin.

OTP_RL_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

PFM_NG_ENB: PFM abnormal signal output to Fail_Flag and FAIL_DET pin.

PFM_NG_ENB	Function	Note
0	Enable	Default
1	Disable	-

OTP_TRIM_FAIL_ENB: OTP program fail signal output to Fail_Flag and FAIL_DET pin.

OTP_TRIM_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

EEPROM_FAIL_ENB: EEPROM reload fail signal output to Fail_Flag and FAIL_DET pin.

EEPROM_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

NO_VIDEO_FAIL_ENB: Self-protection mode fail signal output to Fail_Flag and FAIL_DET pin.

NO_VIDEO_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

GIP_DET_FAIL_ENB: GIP detect fail signal output to Fail_Flag and FAIL_DET pin.

GIP_DET _FAIL_ENB(1)	Function	Note
0	Enable	Default
1	Disable	-

Note: (1) GIP_DET_FAIL_ENB must be disabled when GIP detection is not used.

GATE_FAIL_ENB: Tradition gate fail signal output to Fail_Flag and FAIL_DET pin.

GATE_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

SOURCE_FAIL_ENB: Internal source circuit fail signal output to Fail_Flag and FAIL_DET pin.

SOURCE_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

POWER_FAIL_ENB: GAS function fail signal output to Fail_Flag and FAIL_DET pin.

POWER_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

LVDS_FAIL_ENB: LVDS lock fail signal output to Fail_Flag and FAIL_DET pin.

LVDS_FAIL_ENB	Function	Note
0	Enable	Default
1	Disable	-

Page02h R17h~R18h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	17h	1/0	-	-	-	-	-	-	-	VCOMS [8]
			-	-	-	-	-	-	-	1
02h	18h	1/0	VCOMS[7:0]							
			0	1	0	1	1	1	0	0

VCOMS[8:0]: VCOM voltage selection.
VCOM=VCOMS[8:0] x (-0.005)V

VCOMS[8:0]									Function	Note
0	0	0	0	0	0	0	0	0	0.000V	-
0	0	0	0	0	0	0	0	1	-0.005V	-
:	:	:	:	:	:	:	:	:	:	-
1	0	1	0	1	1	1	0	0	-1.740V	Default
:	:	:	:	:	:	:	:	:	:	-
1	1	1	0	0	0	0	1	0	-2.250V	-
1	1	1	0	0	0	0	1	1	-2.255V	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	0	1	0	0	-2.500V	-
1	1	1	1	1	0	1	0	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1	Reserved	-

Page02h R19h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	19h	1/0	VCOM_OFST[7:0]							
			0	0	0	0	0	0	0	0

VCOM_OFST[7:0]: VCOM voltage offset setting.
When the polarity changes sequence inversion occurred, the VCOM has offset voltage continue one frame. The function is enabled when POL_INV_FRM≠0h **(Page00h R16h[7:4])**.
VCOM=(VCOMS[8:0] + VCOM_OFST[6:0]) x (-0.005)V when VCOM_OFST[7]=0.
VCOM=(VCOMS[8:0] - VCOM_OFST[6:0]) x (-0.005)V when VCOM_OFST[7]=1.

VCOM_OFST[7:0]								Function	Note
0	0	0	0	0	0	0	0	VCOM offset + 0	Default
0	0	0	0	0	0	0	1	VCOM offset + 1	-
:	:	:	:	:	:	:	:	:	-
:	:	:	:	:	:	:	:	:	-
0	1	1	1	1	1	1	1	VCOM offset + 127	-
1	0	0	0	0	0	0	0	VCOM offset - 0	-
:	:	:	:	:	:	:	:	:	-
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	0	VCOM offset - 126	-
1	1	1	1	1	1	1	1	VCOM offset - 127	-

Page02h R1Ch~R1Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	1Ch	1	VCOM_FLAG[7:0]							
			0	0	0	0	0	0	0	0
02h	1Dh	1	GAMMA_FLAG[5:0]						VCOM_FLAG[9:8]	
			0	0	0	0	0	0	0	0

VCOM_FLAG[9:0]: Flag for OTP of VCOM trimming times. **(Read only)**

VCOM_FLAG[9:0]										Function	Note
0	0	0	0	0	0	0	0	0	0	No trimming	Default
0	0	0	0	0	0	0	0	0	1	Trimming one time	-
0	0	0	0	0	0	0	0	1	0	Trimming two times	-
:	:	:	:	:	:	:	:	:	:	:	-
0	0	0	0	0	1	0	0	0	0	Trimming five times	-
:	:	:	:	:	:	:	:	:	:	:	-
0	1	0	0	0	0	0	0	0	0	Trimming nine times	-
1	0	0	0	0	0	0	0	0	0	Trimming ten times	-

GAMMA_FLAG[5:0]: Flag for OTP of positive/negative analog GAMMA **(Page03h, Page06h)** trimming. **(Read only)**

GAMMA_FLAG[2:0]			Function	Note
0	0	0	No trimming	Default
1	0	0	PAGM trimming one-time	-
1	1	0	PAGM trimming two-times	-
1	1	1	PAGM trimming three-times	-

GAMMA_FLAG[5:3]			Function	Note
0	0	0	No trimming	Default
1	0	0	NAGM trimming one-time	-
1	1	0	NAGM trimming two-times	-
1	1	1	NAGM trimming three-times	-

Page02h R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	1Eh	1	-	-	-	TS_VCOM_FLAG[4:0]				
			-	-	-	0	0	0	0	0

TS_VCOM_FLAG[4:0]: Flag for OTP of VCOM_HT / VCOM_LT trimming times. **(Read only)**

TS_VCOM_FLAG[4:0]					Function	Note
0	0	0	0	0	No trimming	Default
0	0	0	0	1	Trimming one time	-
0	0	0	1	0	Trimming two times	-
0	0	1	0	0	Trimming three times	-
0	1	0	0	0	Trimming four times	-
1	0	0	0	0	Trimming five times	-

8.2.4. Page03h for Positive analog gamma correction, PAGM

Page03h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
03h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page03h R01h~R14h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
03h	01h	1/0	-	-	-	T_VP0[4:0]				
			-	-	-	0	0	0	0	0
	02h		-	-	T_VP2[5:0]					
			-	-	0	0	0	1	0	0
	03h		-	-	T_VP4[5:0]					
			-	-	0	0	1	0	0	0
	04h		-	-	T_VP8[5:0]					
			-	-	0	1	1	0	0	0
	05h		-	-	T_VP14[5:0]					
			-	-	1	0	0	0	1	1
	06h		-	-	T_VP23[5:0]					
			-	-	0	1	0	0	1	0
	07h		-	-	T_VP31[5:0]					
			-	-	0	1	0	0	0	1
	08h		-	-	T_VP47[5:0]					
			-	-	0	1	0	1	1	1
	09h		-	-	T_VP79[5:0]					
			-	-	1	0	0	0	0	0
	0Ah		-	-	T_VP111[5:0]					
			-	-	1	0	0	0	1	1
	0Bh		-	-	T_VP143[5:0]					
			-	-	1	0	0	1	1	0
	0Ch		-	-	T_VP175[5:0]					
			-	-	1	0	1	0	1	1
	0Dh		-	-	T_VP207[5:0]					
			-	-	1	0	0	1	0	1
	0Eh		-	-	T_VP223[5:0]					
			-	-	1	0	0	1	0	1
	0Fh		-	-	T_VP231[5:0]					
			-	-	1	1	0	1	0	1
	10h		-	-	T_VP240[5:0]					
			-	-	1	1	0	0	0	0
	11h		-	-	T_VP246[5:0]					
			-	-	1	0	0	1	0	0
	12h		-	-	T_VP251[5:0]					
			-	-	1	1	0	0	0	1
	13h		-	-	T_VP253[5:0]					
			-	-	1	1	1	0	0	0
	14h		-	-	-	T_VP255[4:0]				
			-	-	-	1	1	1	1	0

Reg name	Setting value								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
T_VP0[4:0]	-	-	-	0	0	0	0	0	Positive gamma reference “GSH0” selection.
	-	-	-	:	:	:	:	:	
	-	-	-	1	1	1	1	1	
T_VP2[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH2” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP4[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH4” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP8[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH8” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP14[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH14” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP235:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH23” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP31[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH31” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP47[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH47” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP79[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH79” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP111[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH111” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP143[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH143” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP175[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH175” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP207[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH207” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP223[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH223” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP231[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH231” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP240[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH240” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP246[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH246” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP251[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH251” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	

Reg name	Setting value								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
T_VP253[5:0]	-	-	0	0	0	0	0	0	Positive gamma reference “GSH253” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP255[4:0]	-	-	-	0	0	0	0	0	Positive gamma reference “GSH255” selection.
	-	-	-	:	:	:	:	:	
	-	-	-	1	1	1	1	1	

8.2.5. Page06h for Negative analog gamma correction, NAGM

Page06h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
06h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page06h R01h~R14h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
06h	01h	1/0	-	-	-	T_VN0[4:0]				
			-	-	-	0	0	0	0	0
	02h		-	-	T_VN2[5:0]					
			-	-	0	0	0	1	0	0
	03h		-	-	T_VN4[5:0]					
			-	-	0	0	1	0	0	0
	04h		-	-	T_VN8[5:0]					
			-	-	0	1	1	0	0	0
	05h		-	-	T_VN14[5:0]					
			-	-	1	0	0	0	1	1
	06h		-	-	T_VN23[5:0]					
			-	-	0	1	0	0	1	0
	07h		-	-	T_VN31[5:0]					
			-	-	0	1	0	0	0	1
	08h		-	-	T_VN47[5:0]					
			-	-	0	1	0	1	1	1
	09h		-	-	T_VN79[5:0]					
			-	-	1	0	0	0	0	0
	0Ah		-	-	T_VN111[5:0]					
			-	-	1	0	0	0	1	1
	0Bh		-	-	T_VN143[5:0]					
			-	-	1	0	0	1	1	0
	0Ch		-	-	T_VN175[5:0]					
			-	-	1	0	1	0	1	1
	0Dh		-	-	T_VN207[5:0]					
			-	-	1	0	0	1	0	1
	0Eh		-	-	T_VN223[5:0]					
			-	-	1	0	0	1	0	1
	0Fh		-	-	T_VN231[5:0]					
			-	-	1	1	0	1	0	1
	10h		-	-	T_VN240[5:0]					
			-	-	1	1	0	0	0	0
	11h		-	-	T_VN246[5:0]					
			-	-	1	0	0	1	0	0
	12h		-	-	T_VN251[5:0]					
			-	-	1	1	0	0	0	1
	13h		-	-	T_VN253[5:0]					
			-	-	1	1	1	0	0	0
	14h		-	-	-	T_VN255[4:0]				
			-	-	-	1	1	1	1	0

Reg name	Setting value								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
T_VN0[4:0]	-	-	-	0	0	0	0	0	Negative gamma reference “GSL0” selection.
	-	-	-	:	:	:	:	:	
	-	-	-	1	1	1	1	1	
T_VN2[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL2” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN4[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL4” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN8[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL8” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN14[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL14” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN23[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL23” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN31[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL31” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN47[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL47” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN79[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL79” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP111[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL111” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN143[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL143” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN175[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL175” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN207[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL207” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VP223[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL223” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN231[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL231” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN240[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL240” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN246[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL246” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN251[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL251” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	

Reg name	Setting value								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
T_VN253[5:0]	-	-	0	0	0	0	0	0	Negative gamma reference “GSL253” selection.
	-	-	:	:	:	:	:	:	
	-	-	1	1	1	1	1	1	
T_VN255[4:0]	-	-	-	0	0	0	0	0	Negative gamma reference “GSL255” selection.
	-	-	-	:	:	:	:	:	
	-	-	-	1	1	1	1	1	

8.2.6. Page08h for Normal function

Page08h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
08h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page08h R01h~R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
08h	01h	1/0	-	-	ROB[5:0]					
			-	-	0	1	0	0	0	0
	02h		-	-	GOB[5:0]					
			-	-	0	1	0	0	0	0
	03h		-	-	BOB[5:0]					
			-	-	0	1	0	0	0	0

ROB[5:0]/GOB[5:0]/BOB[5:0]: Offset **(brightness)** setting for red/green/blue color.
D brightness=D contrast + Offset
Offset=-16+ROB/GOB/BOB[5:0].

ROB[5:0] GOB[5:0] BOB[5:0]						Function	Note
0	0	0	0	0	0	-16	-
0	0	0	0	0	1	-15	-
:	:	:	:	:	:	:	-
0	1	0	0	0	0	0	Default
:	:	:	:	:	:	:	-
1	1	1	1	1	1	47	-

Page08h R04h~R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
08h	04h	1/0	RGC[7:0]							
			1	0	0	0	0	0	0	0
	05h		GGC[7:0]							
			1	0	0	0	0	0	0	0
	06h		BGC[7:0]							
			1	0	0	0	0	0	0	0

RGC[7:0]/GGC[7:0]/BGC[7:0]: Gain **(Contrast)** setting for red/green/blue color.
D contrast=D in * Gain
Gain=0.5+RGC/GGC/BGC[7:0]/256.

RGC[7:0] GGC[7:0] BGC[7:0]								Function	Note
0	0	0	0	0	0	0	0	128/256=0.500	-
0	0	0	0	0	0	0	1	129/256=0.504	-
:	:	:	:	:	:	:	:	:	-
1	0	0	0	0	0	0	0	256/256=1.000	Default
:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	383/256=1.496	-

Page08h R07h~R08h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
08h	07h	1/0	PTSEL[15:8]							
			1	1	1	1	1	1	1	1
	08h		PTSEL[7:0]							
			1	1	1	1	1	1	1	1

PTSEL[15:0]: BIST pattern selection.

PTSEL[15:0]															Function	Note
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Dot on/off pattern selected	-
-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	Pixel on/off pattern selected	-
-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	White border pattern selected	-
-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	BIST Gray level pattern selected	-
-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	RGBW pattern selected	-
-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	V Gray scale 256 pattern selected	-
-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	VCOM trimming pattern selected	-
-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	Cross talk pattern selected	-
-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	Checkerboard pattern selected	-
-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	Gray scale 16 pattern selected	-
-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	Color Bar pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	Full Blue pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	Full Green pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	Full Red pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	Full White pattern selected	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Full Black pattern selected	-

Page08h R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
08h	0Ah	1/0	-	-	-	-	GIP_DRVP[1:0]		GIP_DRVN[1:0]	
			-	-	-	-	1	1	1	1

GIP_DRVP[1:0]/DRVN[1:0]: GIP output driving ability.

GIP_DRVP[1:0]	GIP_DRVN[1:0]	Function	Note
0	0	67%	-
0	1	100%	-
1	0	167%	-
1	1	200%	Default

8.2.7. Page09h for Digital gamma correction of Red color

Page09h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page09h R01h~R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	01h	1/0	DGMA1R[7:0]							
			0	0	0	0	0	0	0	0
	02h		DGMA2R[7:0]							
			0	0	0	0	0	1	0	0
	03h		DGMA3R[7:0]							
			0	0	0	0	1	1	0	0
	04h		DGMA4R[7:0]							
			0	0	0	1	1	1	0	0
	05h		DGMA5R[7:0]							
			0	0	1	0	1	1	0	0
	06h		DGMA6R[7:0]							
			0	0	1	1	1	1	0	0
	07h		DGMA7R[7:0]							
			0	1	0	1	1	1	0	0
	08h		DGMA8R[7:0]							
			0	1	1	1	1	1	0	0
	09h		DGMA9R[7:0]							
			1	0	1	1	1	1	0	0
	0Ah		DGMA10R[7:0]							
			1	1	1	1	1	1	0	0
	0Bh		DGMA11R[7:0]							
			0	1	1	1	1	1	0	0
	0Ch		DGMA12R[7:0]							
			1	1	1	1	1	1	0	0
	0Dh		DGMA13R[7:0]							
			0	0	0	0	0	0	0	0
	0Eh		DGMA14R[7:0]							
			1	0	0	0	0	0	0	0
	0Fh		DGMA15R[7:0]							
			0	0	0	0	0	0	0	0
	10h		DGMA16R[7:0]							
			0	1	0	0	0	0	0	0
	11h		DGMA17R[7:0]							
			1	0	0	0	0	0	0	0

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	12h		DGMA18R[7:0]							
			1	0	1	0	0	0	0	0
	13h		DGMA19R[7:0]							
			1	1	0	0	0	0	0	0
	14h		DGMA20R[7:0]							
			1	1	0	1	0	0	0	0
	15h		DGMA21R[7:0]							
			1	1	1	0	0	0	0	0
	16h		DGMA22R[7:0]							
			1	1	1	1	0	0	0	0
	17h		DGMA23R[7:0]							
			1	1	1	1	1	0	0	0
	18h		DGMA24R[7:0]							
			1	1	1	1	1	1	0	0
	19h		DGMA1R[9:8]		DGMA2R[9:8]		DGMA3R[9:8]		DGMA4R[9:8]	
			0	0	0	0	0	0	0	0
	1Ah		DGMA5R[9:8]		DGMA6R[9:8]		DGMA7R[9:8]		DGMA8R[9:8]	
			0	0	0	0	0	0	0	0
	1Bh		DGMA9R[9:8]		DGMA10R[9:8]		DGMA11R[9:8]		DGMA12R[9:8]	
			0	0	0	0	0	1	0	1
	1Ch		DGMA13R[9:8]		DGMA14R[9:8]		DGMA15R[9:8]		DGMA16R[9:8]	
			1	0	1	0	1	1	1	1
	1Dh		DGMA17R[9:8]		DGMA18R[9:8]		DGMA19R[9:8]		DGMA20R[9:8]	
			1	1	1	1	1	1	1	1
	1Eh		DGMA21R[9:8]		DGMA22R[9:8]		DGMA23R[9:8]		DGMA24R[9:8]	
			1	1	1	1	1	1	1	1

Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
DGMA1R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference ”Y1[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA2R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y2[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA3R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y3[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA4R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y4[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA5R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y5[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA6R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y6[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA7R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y7[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA8R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y8[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA9R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y9[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA10R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y10[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA11R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y11[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA12R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y12[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA13R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y13[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA14R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y14[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA15R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y15[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA16R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y16[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA17R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y17[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA18R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y18[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
DGMA19R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y19[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA20R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y20[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA21R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y21[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA22R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y22[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA23R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y23[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA24R[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y24[9:0]” for Red color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

8.2.8. Page0Ah for Digital gamma correction of Green color

Page0Ah R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page0Ah R01h~R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	01h	1/0	DGMA1G[7:0]							
			0	0	0	0	0	0	0	0
	02h		DGMA2G[7:0]							
			0	0	0	0	0	1	0	0
	03h		DGMA3G[7:0]							
			0	0	0	0	1	1	0	0
	04h		DGMA4G[7:0]							
			0	0	0	1	1	1	0	0
	05h		DGMA5G[7:0]							
			0	0	1	0	1	1	0	0
	06h		DGMA6G[7:0]							
			0	0	1	1	1	1	0	0
	07h		DGMA7G[7:0]							
			0	1	0	1	1	1	0	0
	08h		DGMA8G[7:0]							
			0	1	1	1	1	1	0	0
	09h		DGMA9G[7:0]							
			1	0	1	1	1	1	0	0
	0Ah		DGMA10G[7:0]							
			1	1	1	1	1	1	0	0
	0Bh		DGMA11G[7:0]							
			0	1	1	1	1	1	0	0
	0Ch		DGMA12G[7:0]							
			1	1	1	1	1	1	0	0
	0Dh		DGMA13G[7:0]							
			0	0	0	0	0	0	0	0
	0Eh		DGMA14G[7:0]							
			1	0	0	0	0	0	0	0
	0Fh		DGMA15G[7:0]							
			0	0	0	0	0	0	0	0
	10h		DGMA16G[7:0]							
			0	1	0	0	0	0	0	0
	11h		DGMA17G[7:0]							
			1	0	0	0	0	0	0	0

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ah	12h		DGMA18G[7:0]							
			1	0	0	0	0	0	0	0
	13h		DGMA19G[7:0]							
			1	1	0	0	0	0	0	0
	14h		DGMA20G[7:0]							
			1	1	0	1	0	0	0	0
	15h		DGMA21G[7:0]							
			1	1	1	0	0	0	0	0
	16h		DGMA22G[7:0]							
			1	1	1	1	0	0	0	0
	17h		DGMA23G[7:0]							
			1	1	1	1	1	0	0	0
	18h		DGMA24G[7:0]							
			1	1	1	1	1	1	0	0
	19h		DGMA1G[9:8]		DGMA2G[9:8]		DGMA3G[9:8]		DGMA4G[9:8]	
			0	0	0	0	0	0	0	0
	1Ah		DGMA5G[9:8]		DGMA6G[9:8]		DGMA7G[9:8]		DGMA8G[9:8]	
			0	0	0	0	0	0	0	0
	1Bh		DGMA9G[9:8]		DGMA10G[9:8]		DGMA11G[9:8]		DGMA12G[9:8]	
			0	0	0	0	0	1	0	1
	1Ch		DGMA13G[9:8]		DGMA14G[9:8]		DGMA15G[9:8]		DGMA16G[9:8]	
			1	0	1	0	1	1	1	1
	1Dh		DGMA17G[9:8]		DGMA18G[9:8]		DGMA19G[9:8]		DGMA20G[9:8]	
			1	1	1	1	1	1	1	1
	1Eh		DGMA21G[9:8]		DGMA22G[9:8]		DGMA23G[9:8]		DGMA24G[9:8]	
			1	1	1	1	1	1	1	1

Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
DGMA1G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference ”Y1[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA2G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y2[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA3G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y3[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA4G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y4[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA5G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y5[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA6G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y6[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA7G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y7[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA8G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y8[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA9G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y9[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA10G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y10[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA11G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y11[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA12G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y12[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA13G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y13[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA14G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y14[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA15G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y15[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA16G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y16[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA17G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y17[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA18G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y18[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
DGMA19G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y19[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA20G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y20[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA21G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y21[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA22G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y22[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA23G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y23[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA24G[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y24[9:0]” for Green color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

8.2.9. Page0Bh for Digital gamma correction of Blue color

Page0Bh R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page0Bh R01h~R1Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	01h	1/0	DGMA1B[7:0]							
			0	0	0	0	0	0	0	0
	02h		DGMA2B[7:0]							
			0	0	0	0	0	1	0	0
	03h		DGMA3B[7:0]							
			0	0	0	0	1	1	0	0
	04h		DGMA4B[7:0]							
			0	0	0	1	1	1	0	0
	05h		DGMA5B[7:0]							
			0	0	1	0	1	1	0	0
	06h		DGMA6B[7:0]							
			0	0	1	1	1	1	0	0
	07h		DGMA7B[7:0]							
			0	1	0	1	1	1	0	0
	08h		DGMA8B[7:0]							
			0	1	1	1	1	1	0	0
	09h		DGMA9B[7:0]							
			1	0	1	1	1	1	0	0
	0Ah		DGMA10B[7:0]							
			1	1	1	1	1	1	0	0
	0Bh		DGMA11B[7:0]							
			0	1	1	1	1	1	0	0
	0Ch		DGMA12B[7:0]							
			1	1	1	1	1	1	0	0
	0Dh		DGMA13B[7:0]							
			0	0	0	0	0	0	0	0
	0Eh		DGMA14B[7:0]							
			1	0	0	0	0	0	0	0
	0Fh		DGMA15B[7:0]							
			0	0	0	0	0	0	0	0
	10h		DGMA16B[7:0]							
			0	1	0	0	0	0	0	0
	11h		DGMA17B[7:0]							
			1	0	0	0	0	0	0	0

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Bh	12h		DGMA18B[7:0]							
			1	0	1	0	0	0	0	0
	13h		DGMA19B[7:0]							
			1	1	0	0	0	0	0	0
	14h		DGMA20B[7:0]							
			1	1	0	1	0	0	0	0
	15h		DGMA21B[7:0]							
			1	1	1	0	0	0	0	0
	16h		DGMA22B[7:0]							
			1	1	1	1	0	0	0	0
	17h		DGMA23B[7:0]							
			1	1	1	1	1	0	0	0
	18h		DGMA24B[7:0]							
			1	1	1	1	1	1	0	0
	19h		DGMA1B[9:8]		DGMA2B[9:8]		DGMA3B[9:8]		DGMA4B[9:8]	
			0	0	0	0	0	0	0	0
	1Ah		DGMA5B[9:8]		DGMA6B[9:8]		DGMA7B[9:8]		DGMA8B[9:8]	
			0	0	0	0	0	0	0	0
	1Bh		DGMA9B[9:8]		DGMA10B[9:8]		DGMA11B[9:8]		DGMA12B[9:8]	
			0	0	0	0	0	1	0	1
	1Ch		DGMA13B[9:8]		DGMA14B[9:8]		DGMA15B[9:8]		DGMA16B[9:8]	
			1	0	1	0	1	1	1	1
	1Dh		DGMA17B[9:8]		DGMA18B[9:8]		DGMA19B[9:8]		DGMA20B[9:8]	
			1	1	1	1	1	1	1	1
	1Eh		DGMA21B[9:8]		DGMA22B[9:8]		DGMA23B[9:8]		DGMA24B[9:8]	
			1	1	1	1	1	1	1	1

Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
DGMA1B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference ”Y1[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA2B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y2[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA3B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y3[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA4B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y4[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA5B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y5[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA6B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y6[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA7B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y7[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA8B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y8[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA9B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y9[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA10B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y10[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA11B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y11[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA12B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y12[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA13B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y13[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA14B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y14[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA15B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y15[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA16B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y16[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA17B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y17[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA18B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y18[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

Reg name	Setting value										Description
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
DGMA19B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y19[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA20B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y20[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA21B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y21[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA22B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y22[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA23B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y23[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	
DGMA24B[9:0]	0	0	0	0	0	0	0	0	0	0	Digital gamma reference “Y24[9:0]” for Blue color.
	:	:	:	:	:	:	:	:	:	:	
	1	1	1	1	1	1	1	1	1	1	

8.2.10. Page0Ch for LVDS function

Page0Ch R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page0Ch R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Ch	01h	1/0	-	DLL_BANK	LVDS_AGING	FMT	LANE_SW	LANE_PN	-	-
			-	0	0	0	0	0	-	-

DLL_BANK: LVDS input frequency range selection.

DLL_BANK	Function	Note
0	≥ 30MHz	Default
1	< 30MHz	-

LVDS_AGING: LVDS power saving enable.
When enabled, data lanes are turned off in BIST and self protection mode.

LVDS_AGING	Function	Note
0	Disabled	Default
1	Enabled	-

FMT: LVDS and TTL input data format selection.

Interface	TR[1]	FMT	Function	Note
TTL	0	0	[D07:D00] map DR[7:0]; [D17:D10] map DG[7:0]; [D27:D20] map DB[7:0]	-
		1	[D07:D00] map DR[0:7]; [D17:D10] map DG[0:7]; [D27:D20] map DB[0:7]	-
LVDS	1	0	NS **(JEIDA)** format	Default
		1	Thine **(VESA)** format	-

LANE_SW: LVDS Lane swap selection.

LVDS_SW	Function	Note
0	Not swap	Default
1	Swap	-

LVDS_PN: LVDS lane PN polarity swapping selection.

LVDS_PN	Function	Note
0	Not swap	Default
1	Swap	-

8.2.11. Page0Eh for Temperature mode

Page0Eh R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page0Eh R01h~R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	01h	1/0	-	-	-	-	-	-	VCOMS_HT[8]	VCOMS_LT[8]
			-	-	-	-	-	-	1	1
0Eh	02h	1/0	VCOMS_HT[7:0]							
			0	1	0	1	1	1	0	0
0Eh	03h	1/0	VCOMS_LT[7:0]							
			0	1	0	1	1	1	0	0

VCOMS_HT[8:0]: VCOM voltage adjustment at high temperature mode.
VCOM=VCOMS_HT[8:0] x (-0.005)V

VCOMS_HT[8:0]									Function	Note
0	0	0	0	0	0	0	0	0	0.000V	-
0	0	0	0	0	0	0	0	1	-0.005V	-
:	:	:	:	:	:	:	:	:	:	-
1	0	1	0	1	1	1	0	0	-1.740V	Default
:	:	:	:	:	:	:	:	:	:	-
1	1	1	0	0	0	0	1	0	-2.250V	-
1	1	1	0	0	0	0	1	1	-2.255V	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	0	1	0	0	-2.500V	-
1	1	1	1	1	0	1	0	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1	Reserved	-

VCOMS_LT[8:0]: VCOM voltage adjustment at low temperature mode.
VCOM=VCOMS_LT[8:0] x (-0.005)V

VCOMS_LT[8:0]									Function	Note
0	0	0	0	0	0	0	0	0	0.000V	-
0	0	0	0	0	0	0	0	1	-0.005V	-
:	:	:	:	:	:	:	:	:	:	-
1	0	1	0	1	1	1	0	0	-1.740V	Default
:	:	:	:	:	:	:	:	:	:	-
1	1	1	0	0	0	0	1	0	-2.250V	-
1	1	1	0	0	0	0	1	1	-2.255V	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	0	1	0	0	-2.500V	-
1	1	1	1	1	0	1	0	1	Reserved	-
:	:	:	:	:	:	:	:	:	:	-
1	1	1	1	1	1	1	1	1	Reserved	-

Page0Eh R04h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	04h	1/0	-	-	VGHS_HT[5:0]					
			-	-	0	0	1	1	1	0

VGHS_HT[5:0]: VGH voltage adjustment at high temperature mode.
VGH=5.0+VGHS_HT[5:0] x 0.5V

VGHS_HT[5:0](1)						Function	Note
0	0	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	-
0	0	0	0	1	1	Reserved	-
0	0	0	1	0	0	7.0V	-
:	:	:	:	:	:	:	-
0	0	1	1	1	0	12.0V	Default
:	:	:	:	:	:	:	-
1	0	0	1	0	1	23.5V	-
1	0	0	1	1	0	24.0V	-
:	:	:	:	:	:	24.0V	-
1	1	1	1	1	1	24.0V	-

Note: (1) VGH + |VGL| ≤ 32V.

Page0Eh R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	05h	1/0	-	-	-	VGLS_HT[4:0]				
			-	-	-	0	0	1	1	0

VGLS_HT[4:0]: VGL voltage adjustment at high temperature mode.
VGL=-5.0+VGLS_HT[4:0] x (-0.5)V

VGLS_HT[4:0](1)					Function	Note
0	0	0	0	0	Reserved	-
:	:	:	:	:	:	-
0	0	0	1	1	Reserved	-
0	0	1	0	0	-7.0V	-
0	0	1	0	1	-7.5V	-
0	0	1	1	0	-8.0V	Default
:	:	:	:	:	:	-
1	0	1	1	0	-16.0V	-
:	:	:	:	:	-16.0V	-
1	1	1	1	1	-16.0V	-

Note: (1) VGH + |VGL| ≤ 32V.

Page0Eh R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	06h	1/0	-	-	VGHS_LT[5:0]					
			-	-	0	0	1	1	1	0

VGHS_LT[5:0]: VGH voltage adjustment at low temperature mode.
VGH=5.0+VGHS_LT[5:0] x 0.5V

VGHS_LT[5:0](1)						Function	Note
0	0	0	0	0	0	Reserved	-
:	:	:	:	:	:	:	-
0	0	0	0	1	1	Reserved	-
0	0	0	1	0	0	7.0V	-
:	:	:	:	:	:	:	-
0	0	1	1	1	0	12.0V	Default
:	:	:	:	:	:	:	-
1	0	0	1	0	1	23.5V	-
1	0	0	1	1	0	24.0V	-
:	:	:	:	:	:	24.0V	-
1	1	1	1	1	1	24.0V	-

Note: (1) VGH + |VGL| ≤ 32V.

Page0Eh R07h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	07h	1/0	-	-	-	VGLS_LT[4:0]				
			-	-	-	0	0	1	1	0

VGLS_LT[4:0]: VGL voltage adjustment at low temperature mode.
VGL=-5.0+VGLS_LT[4:0] x (-0.5)V

VGLS_LT[4:0](1)					Function	Note
0	0	0	0	0	Reserved	-
:	:	:	:	:	:	-
0	0	0	1	1	Reserved	-
0	0	1	0	0	-7.0V	-
0	0	1	0	1	-7.5V	-
0	0	1	1	0	-8.0V	Default
:	:	:	:	:	:	-
1	0	1	1	0	-16.0V	-
:	:	:	:	:	-16.0V	-
1	1	1	1	1	-16.0V	-

Note: (1) VGH + |VGL| ≤ 32V.

Page0Eh R08h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	08h	1/0	DIM_EN	DIM_FRAME[1:0]		VGMPHS_HT[4:0]				
			0	1	0	1	1	0	1	0

DIM_EN: Voltage dimming enable at temperature mode.

DIM_EN	Function	Note
0	Disable	Default
1	Enable	-

DIM_FRAME[1:0]: Dimming frame period setting.

DIM_FRAME[1:0]		Function	Note
0	0	8 Frame	-
0	1	16 Frame	-
1	0	32 Frame	Default
1	1	64 Frame	-

VGMPHS_HT[4:0]: VGMPH voltage adjustment at high temperature mode.
VGMPH=4.0+VGMPHS_HT[4:0] x 0.1V

VGMPHS_HT[4:0]					Function	Note
0	0	0	0	0	4.0V	Min.
0	0	0	0	1	4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	5.8V	-
:	:	:	:	:	:	-
1	1	0	0	0	6.4V	-
1	1	0	0	1	6.5V	-
1	1	0	1	0	6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page0Eh R09h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	09h	1/0	DIM_OPT	-	-	VGMNHS_HT[4:0]				
			0	-	-	1	1	0	1	0

DIM_OPT: Analog gamma **(AGAM)** voltage dimming option.

DIM_OPT	Function	Note
0	AGAM dimming with VGMPH/PL/NH/NL & VCOM	Default
1	AGAM dimming after VGMPH/PL/NH/NL & VCOM done	-

VGMNHS_HT[4:0]: VGMNH voltage adjustment at high temperature mode.
VGMNH=-4.0 + VGMNHS_HT[4:0] x (-0.1)V

VGMNHS_HT[4:0]					Function	Note
0	0	0	0	0	-4.0V	Min.
0	0	0	0	1	-4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	-5.8V	-
:	:	:	:	:	:	-
1	1	0	0	0	-6.4V	-
1	1	0	0	1	-6.5V	-
1	1	0	1	0	-6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page0Eh R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	0Ah	1/0	VGMPLS_HT[3:0]				VGMNLS_HT[3:0]			
			0	0	0	1	0	0	0	1

VGMPLS_HT[3:0]: VGMPL voltage adjustment at high temperature mode.
VGMPL=0.2 + VGMPLS_HT[3:0] x 0.1V

VGMPLS_HT[3:0]				Function	Note
0	0	0	0	0.2V	-
0	0	0	1	0.3V	Default
:	:	:	:	:	-
1	1	1	1	1.7V	-

VGMNLS_HT[3:0]: VGMNL voltage adjustment at high temperature mode.
VGMNL=-0.2 + VGMNLS_HT[3:0] x (-0.1)V

VGMNLS_HT[3:0]				Function	Note
0	0	0	0	-0.2V	-
0	0	0	1	-0.3V	Default
:	:	:	:	:	-
1	1	1	1	-1.7V	-

Page0Eh R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	0Bh	1/0	TS_GOE_EN	TS_GAMMA_EN	-	VGMPHS_LT[4:0]				
			0	0	-	1	1	0	1	0

TS_GOE_EN: Temperature mode disable and GOE setting by RT register.

TS_GOE_EN	Function	Note
0	GOE timing setting by RT register	Default
1	GOE timing setting selection by [TS_H:TS_L]	-

TS_GAMMA_EN: Gamma voltage setting for temperature.

TS_GAMMA_EN	Function	Note
0	Disable	Default
1	Enable	-

VGMPHS_LT[4:0]: VGMPH voltage adjustment at low temperature mode.
VGMPH=4.0 + VGMPHS_LT[4:0] x 0.1V

VGMPHS_LT[4:0]					Function	Note
0	0	0	0	0	4.0V	Min.
0	0	0	0	1	4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	5.8V	-
:	:	:	:	:	:	-
1	1	0	0	0	6.4V	-
1	1	0	0	1	6.5V	-
1	1	0	1	0	6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page0Eh R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	0Ch	1/0	TS_VCOM_EN	TS_VGHL_EN	-	VGMNHS_LT[4:0]				
			0	0	-	1	1	0	1	0

TS_VCOM_EN: VCOM voltage setting for temperature.

TS_VCOM_EN	Function	Note
0	Disable	Default
1	Enable	-

TS_VGHL_EN: VGH and VGL voltage setting for temperature.

TS_VGHL_EN	Function	Note
0	Disable	Default
1	Enable	-

VGMNHS_LT[4:0]: VGMNH voltage adjustment at low temperature mode.
VGMNH=-4.0 + VGMNHS_LT[4:0] x (-0.1)V

VGMNHS_LT[4:0]					Function	Note
0	0	0	0	0	-4.0V	Min.
0	0	0	0	1	-4.1V	-
:	:	:	:	:	:	-
1	0	0	1	0	-5.8V	-
:	:	:	:	:	:	-
1	1	0	0	0	-6.4V	-
1	1	0	0	1	-6.5V	-
1	1	0	1	0	-6.6V	Default
1	1	0	1	1	Reserved	-
:	:	:	:	:	:	-
1	1	1	1	1	Reserved	-

Page0Eh R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
0Eh	0Dh	1/0	VGMPLS_LT[3:0]				VGMNLS_LT[3:0]			
			0	0	0	1	0	0	0	1

VGMPLS_LT[3:0]: VGMPL voltage adjustment at low temperature mode.
VGMPL=0.2 + VGMPLS_LT[3:0] x 0.1V

VGMPLS_LT[3:0]				Function	Note
0	0	0	0	0.2V	-
0	0	0	1	0.3V	Default
:	:	:	:	:	-
1	1	1	1	1.7V	-

VGMNLS_LT[3:0]: VGMNL voltage adjustment at low temperature mode.
VGMNL=-0.2 + VGMNLS_LT[3:0] x (-0.1)V

VGMNLS_LT[3:0]				Function	Note
0	0	0	0	-0.2V	-
0	0	0	1	-0.3V	Default
:	:	:	:	:	-
1	1	1	1	-1.7V	-

8.2.12. Page15h for OTP function

Page15h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page15h R01h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	01h	1/0	-	-	OTP_GROUP[5:0]					
			-	-	0	0	0	0	0	0

OTP_GROUP[5:0]: OTP group select.

OTP_GROUP[5:0] (HEX.)	Reg. mapping	OTP times	Note
00 0000 **(00h)**	-	-	-
00 0001 **(01h)**	Page00h R01h~R05h	2	Operation setting
00 0010 **(02h)**	Page00h R06h~R0Bh	2	TCON setting
00 0011 **(03h)**	Page00h R0Ch~R0Fh	2	TCON setting
00 0100 **(04h)**	Page00h R10h~R13h	2	TCON setting
00 0101 **(05h)**	Page00h R14h~R1Ch	2	TCON setting
00 0110 **(06h)**	-	-	Reserved
00 0111 **(07h)**	Page01h R01h~R05h	2	TCON setting
00 1000 **(08h)**	Page01h R06h~R12h	2	TCON setting
00 1001 **(09h)**	-	-	Reserved
00 1010 **(0Ah)**	Page02h R01h~R16h	2	Power setting
00 1011 **(0Bh)**	Page02h R17h~R18h	10	VCOM setting
00 1100 **(0Ch)**	Page02h R19h	2	VCOM setting
00 1101 **(0Dh)**	Page03h R01h~R14h	3	Positive analog gamma
00 1110 **(0Eh)**	Page06h R01h~R14h	3	Negative analog gamma
00 1111 **(0Fh)**	Page08h R01h~R06h	2	TCON setting
01 0000 **(10h)**	Page08h R07h~R08h	2	TCON setting
01 0001 **(11h)**	Page08h R09h~R10h	2	TCON setting
01 0010 **(12h)**	Page09h R01h~R1Eh	1	Digital gamma R
01 0011 **(13h)**	Page0Ah R01h~R1Eh	1	Digital gamma G
01 0100 **(14h)**	Page0Bh R01h~R1Eh	1	Digital gamma B
01 0101 **(15h)**	Page0Ch R01h~R13h	1	LVDS setting
01 0110 **(16h)**	-	-	Reserved
01 0111 **(17h)**	Page0Eh R01h~R03h	5	Temperature high/low voltage setting
01 1000 **(18h)**	Page0Eh R04h~R0Dh	2	Temperature high/low voltage setting
01 1001 **(19h)**	-	1	Reserved
01 1010 **(1Ah)**	-	1	Reserved
01 1011 **(1Bh)**	-	1	Reserved
01 1100 **(1Ch)**	Page0Fh R01h~R1Eh	2	GIP function setting
01 1101 **(1Dh)**	Page10h R01h~R1Eh	2	GIP function setting
01 1110 **(1Eh)**	Page11h R01h~R1Ah	2	GIP output setting
01 1111 **(1Fh)**	Page12h R01h~R1Ah	2	GIP output setting

OTP_GROUP[5:0] (HEX.)	Reg. mapping	OTP times	Note
10 0000 **(20h)**	Page13h R01h~R14h	2	GIP output setting
10 0001 **(21h)**	Page14h R01h~R14h	2	GIP output setting

Page15h R02h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	02h	1/0	WOTP[7:0]							
			1	0	0	1	1	0	0	1

WOTP[7:0]: OTP program command enable.

WOTP[7:0]								Function	Note
0	1	1	0	0	1	1	0	Enable	-
1	0	0	1	1	0	0	1	Disable	Default
Else								Disable	-

Page15h R03h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	03h	1/0	-	-	-	-	OTP_WR_ALL	OTP_RELOAD	OTP_RD	OTP_WR
			-	-	-	-	0	0	0	0

OTP_WR_ALL: OTP write all group function enable. **(Automatically cleared)**

OTP_WR_ALL	Function	Note
0	Disable	Default
1	Enable	-

OTP_RELOAD: OTP reload function enable. **(Automatically cleared)**

OTP_RELOAD	Function	Note
0	Disable	Default
1	Enable	-

OTP_RD: OTP read function enable. **(Automatically cleared)**

OTP_RD	Function	Note
0	Disable	Default
1	Enable	-

OTP_WR: OTP write function enable. **(Automatically cleared)**

OTP_WR	Function	Note
0	Disable	Default
1	Enable	-

Page15h R04h~R05h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	04h	1/0	-	-	-	-	-	-	OTP_INDEX[9:8]	
			-	-	-	-	-	-	0	0
	05h		OTP_INDEX[7:0]							
			0	0	0	0	0	0	0	0

OTP_INDEX[9:0]: OTP address for read.

Page15h R06h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	06h	1	PDOB[7:0]							
			0	0	0	0	0	0	0	0

PDOB[7:0]: OTP read out data. **(Read only)**

Page15h R0Ah:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	0Ah	1/0	EEP_PWD[7:0]							
			0	1	0	1	1	0	1	0

EEP_PWD[7:0]: EEPROM software reload password.

EEP_PWD[7:0]								Function	Note
0	1	0	1	1	0	1	0	Disable	Default
1	0	1	0	0	1	0	1	Enable	-
Else								Disable	-

Page15h R0Bh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	0Bh	1/0	EEP_CKSUM_FAIL	-	-	-	-	-	-	EEP_RL_CMD
			0	-	-	-	-	-	-	0

EEP_CKSUM_FAIL: EEPROM Check-sum flag. **(Read only)**

EEP_CKSUM_FAIL	Function	Note
0	Check-sum pass	Default
1	Check-sum fail	-

EEP_RL_CMD: EEPROM software reload. **(Automatically cleared)**

EEP_RL_CMD	Function	Note
0	-	Default
1	Reload	-

Page15h R0Ch:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	0Ch	1/0	-	-	-	EESEL	-	-	-	-
			-	-	-	0	-	-	-	-

EESEL: EEPROM controlled by System or Driver IC.

EESEL	Function	Note
0	EEPROM controlled by Driver IC	Default
1	EEPROM controlled by System	-

Page15h R0Dh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	0Dh	1	IC_VERSION[7:0]							
			0	0	0	0	0	0	0	0

IC_VERSION[7:0]: IC version. **(Read only)**

Page15h R0Eh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	0Eh	1/0	DISPOFF_CMD[7:0]							
			0	0	0	0	0	0	0	0

DISPOFF_CMD[7:0]: Display off command enable.

DISPOFF_CMD[7:0](1)								Function	Note
0	0	0	0	0	0	0	0	Display on	Default
0	1	0	1	0	1	0	1	Display off	-
Else								Display on	-

Note: (1) Only set DISPOFF_CMD[7:0]=0x55 and DISPOFF_EN **(Page00h R1Ah[6])**=1 to enter display off mode.

Page15h R0Fh:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	0Fh	1	EEP_CKSUM_TCON[7:0]							
			0	0	0	0	0	0	0	0

EEP_CKSUM_TCON[7:0]: EEPROM checksum value calculated by TCON. **(Read only)**

Page15h R10h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
15h	10h	1	EEP_CKSUM_DESIRE[7:0]							
			0	0	0	0	0	0	0	0

EEP_CKSUM_DESIRE[7:0]: EEPROM checksum value read from EEPROM. **(Read only)**

8.2.13. Page16h for Fail Flag

Page16h R00h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
16h	00h	1/0	PAGE[7:0]							
			0	0	0	1	1	0	1	0

PAGE[7:0]: Register Page selection. Register R00h is defined as PAGE[7:0] for all pages.

PAGE[7:0]								Function	Note
0	0	0	0	0	0	0	0	Page00h	-
0	0	0	0	0	0	0	1	Page01h	-
0	0	0	0	0	0	1	0	Page02h	-
:	:	:	:	:	:	:	:	:	-
0	0	0	1	1	0	1	0	Page1Ah	Default

Page16h R15h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
16h	15h	1	FAIL_FLAG2[7:0]							
			0	0	0	0	0	0	0	0

FAIL_FLAG2[7:0]: Fail detection flag2. **(Read only)**

FAIL_FLAG2[7:0]								Function	Note
-	-	-	-	-	-	-	1	Reserved	-
-	-	-	-	-	-	1	-	Fail flag for OTP reload	-
-	-	-	-	-	1	-	-	Reserved	-
-	-	-	-	1	-	-	-	Reserved	-
-	-	-	1	-	-	-	-	Reserved	-
-	-	1	-	-	-	-	-	Reserved	-
-	1	-	-	-	-	-	-	Reserved	-
1	-	-	-	-	-	-	-	Reserved	-

Page16h R16h:

Page	Address	R/W	Content and default value							
			D7	D6	D5	D4	D3	D2	D1	D0
16h	16h	1	FAIL_FLAG1[7:0]							
			0	0	0	0	0	0	0	0

FAIL_FLAG1[7:0]: Fail detection flag1. **(Read only)**

FAIL_FLAG1[7:0]								Function	Note
-	-	-	-	-	-	-	1	Fail flag for LVDS lock	-
-	-	-	-	-	-	1	-	Fail flag for GAS function	-
-	-	-	-	-	1	-	-	Fail flag for Internal source circuit	-
-	-	-	-	1	-	-	-	Fail flag for GIP detect or tradition gate signal	-
-	-	-	1	-	-	-	-	Fail flag for Self-protection mode	-
-	-	1	-	-	-	-	-	Fail flag for EEPROM reload	-
-	1	-	-	-	-	-	-	Fail flag for OTP trimming	-
1	-	-	-	-	-	-	-	Fail flag for PFM abnormal	-

8.3. EEPROM mapping table

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
0	PASS1[7:0]=0X72							
1	DUAL_ZZ_SEL	PANEL_TYPE[2:0]			RESET_GAS_OPT	ZIG-ZAG_TYPE[1:0]		GDSEL
2	TR[1:0]		DINT	MODE	HSP	VSP	CLOCKP	NB
3	RL	TB	INV[1:0]		RS[3:0]			
4	RB_INV	DGAMEN	GPOS[1:0]		SD_GND_V[1:0]		PON	POFF
5	GAS_VSPN_EN	SPFEN	SPFSEL	BISTEN	-		BIST_FNUM[1:0]	
6	VSTS[7:0]							
7	HSTS[7:0]							
8	ENDRVP[1:0]		OEW[5:0]					
9	ENDRVN[1:0]		GEQW[5:0]					
10	PCR[1:0]		EQ0W[5:0]					
11	-	BC[2:0]			POCSD[1:0]		POCGM[1:0]	
12	DMY_DATA[7:0]							
13	-				PWR_MASK_FAIL_EN	GIP_PWR_OPT	-	EQ0_MODE
14	-					CH_OPT	-	
15	-	TS_RHL_OPT	GIP_MX_TAB_SEL[1:0]		GATE_INTER SEL	INTL_INV	-	
16	GATENUM[7:0]							
17	GATEPASS[3:0]				GATENUM[11:8]			
18	HSETPASS[7:0]							
19	HSETPASS[3:0]				-	HSETNUM[10:8]		
20	-			EQ1W[4:0]				
21	BIST_VFP[4:0]					RESERVED		
22	POL_INV_FRM[3:0]				POL_TOG_VBLK	-	PRE-SCAN[1:0]	
23	BIST_GRAY[7:0]							
24	BIST_H_OFFSET[7:0]							
25	-		BIST_OSC_SEL	H_OSCLK_SEL[4:0]				
26	-	DISPOFF_EN	-	-	-	-	-	-
27	-							
28	CHIP_ID[7:0]							
29	RESERVED							
30	RESERVED							
31	RESERVED							
32	-	-	VCLS[1:0]		-		-	-
33	FAIL_DET_SEL	FAIL_DET_INV	-	ASIL_NOSIG SEL	ASIL_INV	ASIL_WD[2:0]		
34	BANK12_OFT[7:0]							
35	BANK23_OFT[7:0]							
36	RESERVED							
37	RESERVED							
38	-	-						
39	-	-						
40	-	-						
41	-	-						
42	-	-						
43	-	-						
44	H_TOTAL_OFT[3:0]				-			
45	RESERVED							
46	RESERVED							
47	RESERVED							
48	RESERVED							
49	-						ASIL_WD_OPT[1:0]	
50	RESERVED							
51	RESERVED							

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
52	RESERVED							
53	RESERVED							
54	RESERVED							
55	RESERVED							
56	RESERVED							
57	RESERVED							
58	RESERVED							
59	-	PFMFREN	VSPEN	VSNEN	DRVPD[1:0]		DRVND[1:0]	
60	GAS_VCC_EN	-	-	VSPS[4:0]				
61	-	-	-	VSNS[4:0]				
62	VGHXS[1:0]		VGHS[5:0]					
63	-		VGLXS	VGLS[4:0]				
64	VMONPS[1:0]		VSDPEN	VSDPS[4:0]				
65	VMONNS[1:0]		VSDNEN	VSDNS[4:0]				
66	VSPON[3:0]				VSPOFF[3:0]			
67	VSNON[3:0]				VSNOFF[3:0]			
68	VSPON_S[3:0]				VSPOFF_S[3:0]			
69	VSNON_S[3:0]				VSNOFF_S[3:0]			
70	TP_DLY[7:0]							
71	TP_WIDTH[7:0]							
72	TPSYNC1_SEL[2:0]			TPSYNC2_SEL[2:0]			TPSYNC_INV	TPSYNC_VBLK
73	TP_WIDTH_ENB	PFM_DET_EN	-	PFM_NG_OPT	PFM_OSC_SEL[1:0]		PFM_DET_OPT[1:0]	
74	-	PFM_SS_SEL	VCOM_OTP	VCOMEN	S_VCL_ENB	M_VCL_ENB	VCOMD[1:0]	
75	VGHL_LIMIT	VGHEN	VGLEN	FCPS	-		FCP[1:0]	
76	T_OCPEN	FAIL_FLAG_GP_SEL	T_VGMREGEN	T_VGMPHS[4:0]				
77	-			T_VGMNHS[4:0]				
78	T_VGMPLS[3:0]				T_VGMNLS[3:0]			
79	-		-	-	-		OTP_RL_FAIL_ENB	-
80	-	OTP_TRIM_FAIL_ENB	EEPROM_FAIL_ENB	NVIDEO_FAIL_ENB	GIP_DETECT_FAIL/GATE_FAIL_ENB	SOURCE_FAIL_ENB	POWER_FAIL_ENB	LVDS_FAIL_ENB
81	-	-	-	-	-	-	-	VCOMS[8]
82	VCOMS[7:0]							
83	VCOM_OFST[7:0]							
84	-	-	-	T_VP1_0[4:0]				
85	-	-	T_VP1_2[5:0]					
86	-	-	T_VP1_4[5:0]					
87	-	-	T_VP1_8[5:0]					
88	-	-	T_VP1_14[5:0]					
89	-	-	T_VP1_23[5:0]					
90	-	-	T_VP1_31[5:0]					
91	-	-	T_VP1_47[5:0]					
92	-	-	T_VP1_79[5:0]					
93	-	-	T_VP1_111[5:0]					
94	-	-	T_VP1_143[5:0]					
95	-	-	T_VP1_175[5:0]					
96	-	-	T_VP1_207[5:0]					
97	-	-	T_VP1_223[5:0]					
98	-	-	T_VP1_231[5:0]					
99	-	-	T_VP1_240[5:0]					
100	-	-	T_VP1_246[5:0]					
101	-	-	T_VP1_251[5:0]					
102	-	-	T_VP1_253[5:0]					
103	-	-	T_VP1_255[5:0]					
104	-	-	-	T_VP2_0[4:0]				
105	-	-	T_VP2_2[5:0]					
106	-	-	T_VP2_4[5:0]					

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
107	-	-	T_VP2_8[5:0]					
108	-	-	T_VP2_14[5:0]					
109	-	-	T_VP2_23[5:0]					
110	-	-	T_VP2_31[5:0]					
111	-	-	T_VP2_47[5:0]					
112	-	-	T_VP2_79[5:0]					
113	-	-	T_VP2_111[5:0]					
114	-	-	T_VP2_143[5:0]					
115	-	-	T_VP2_175[5:0]					
116	-	-	T_VP2_207[5:0]					
117	-	-	T_VP2_223[5:0]					
118	-	-	T_VP2_231[5:0]					
119	-	-	T_VP2_240[5:0]					
120	-	-	T_VP2_246[5:0]					
121	-	-	T_VP2_251[5:0]					
122	-	-	T_VP2_253[5:0]					
123	-	-	T_VP2_255[5:0]					
124	-	-	-	T_VP3_0[4:0]				
125	-	-	T_VP3_2[5:0]					
126	-	-	T_VP3_4[5:0]					
127	-	-	T_VP3_8[5:0]					
128	-	-	T_VP3_14[5:0]					
129	-	-	T_VP3_23[5:0]					
130	-	-	T_VP3_31[5:0]					
131	-	-	T_VP3_47[5:0]					
132	-	-	T_VP3_79[5:0]					
133	-	-	T_VP3_111[5:0]					
134	-	-	T_VP3_143[5:0]					
135	-	-	T_VP3_175[5:0]					
136	-	-	T_VP3_207[5:0]					
137	-	-	T_VP3_223[5:0]					
138	-	-	T_VP3_231[5:0]					
139	-	-	T_VP3_240[5:0]					
140	-	-	T_VP3_246[5:0]					
141	-	-	T_VP3_251[5:0]					
142	-	-	T_VP3_253[5:0]					
143	-	-	T_VP3_255[5:0]					
144	-	-	-	T_VN1_0[4:0]				
145	-	-	T_VN1_2[5:0]					
146	-	-	T_VN1_4[5:0]					
147	-	-	T_VN1_8[5:0]					
148	-	-	T_VN1_14[5:0]					
149	-	-	T_VN1_23[5:0]					
150	-	-	T_VN1_31[5:0]					
151	-	-	T_VN1_47[5:0]					
152	-	-	T_VN1_79[5:0]					
153	-	-	T_VN1_111[5:0]					
154	-	-	T_VN1_143[5:0]					
155	-	-	T_VN1_175[5:0]					
156	-	-	T_VN1_207[5:0]					
157	-	-	T_VN1_223[5:0]					
158	-	-	T_VN1_231[5:0]					
159	-	-	T_VN1_240[5:0]					
160	-	-	T_VN1_246[5:0]					
161	-	-	T_VN1_251[5:0]					
162	-	-	T_VN1_253[5:0]					
163	-	-	T_VN1_255[5:0]					
164	-	-	-	T_VN2_0[4:0]				
165	-	-	T_VN2_2[5:0]					
166	-	-	T_VN2_4[5:0]					
167	-	-	T_VN2_8[5:0]					
168	-	-	T_VN2_14[5:0]					
169	-	-	T_VN2_23[5:0]					

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
170	-	-	T_VN2_31[5:0]					
171	-	-	T_VN2_47[5:0]					
172	-	-	T_VN2_79[5:0]					
173	-	-	T_VN2_111[5:0]					
174	-	-	T_VN2_143[5:0]					
175	-	-	T_VN2_175[5:0]					
176	-	-	T_VN2_207[5:0]					
177	-	-	T_VN2_223[5:0]					
178	-	-	T_VN2_231[5:0]					
179	-	-	T_VN2_240[5:0]					
180	-	-	T_VN2_246[5:0]					
181	-	-	T_VN2_251[5:0]					
182	-	-	T_VN2_253[5:0]					
183	-	-	T_VN2_255[5:0]					
184	-	-	-	T_VN3_0[4:0]				
185	-	-	T_VN3_2[5:0]					
186	-	-	T_VN3_4[5:0]					
187	-	-	T_VN3_8[5:0]					
188	-	-	T_VN3_14[5:0]					
189	-	-	T_VN3_23[5:0]					
190	-	-	T_VN3_31[5:0]					
191	-	-	T_VN3_47[5:0]					
192	-	-	T_VN3_79[5:0]					
193	-	-	T_VN3_111[5:0]					
194	-	-	T_VN3_143[5:0]					
195	-	-	T_VN3_175[5:0]					
196	-	-	T_VN3_207[5:0]					
197	-	-	T_VN3_223[5:0]					
198	-	-	T_VN3_231[5:0]					
199	-	-	T_VN3_240[5:0]					
200	-	-	T_VN3_246[5:0]					
201	-	-	T_VN3_251[5:0]					
202	-	-	T_VN3_253[5:0]					
203	-	-	T_VN3_255[5:0]					
204	-	-	ROB[5:0]					
205	-	-	GOB[5:0]					
206	-	-	BOB[5:0]					
207	RGC[7:0]							
208	GGC[7:0]							
209	BGC[7:0]							
210	BIST_PTSEL[15:8]							
211	BIST_PTSEL[7:0]							
212	-	-	-	-	-			
213	-		-		GIP_DRVP[1:0]		GIP_DRVN[1:0]	
214	-	-						
215	-							
216	-							
217	-							
218	-							
219	-							
220	DGMA1R[7:0]							
221	DGMA2R[7:0]							
222	DGMA3R[7:0]							
223	DGMA4R[7:0]							
224	DGMA5R[7:0]							
225	DGMA6R[7:0]							
226	DGMA7R[7:0]							
227	DGMA8R[7:0]							
228	DGMA9R[7:0]							
229	DGMA10R[7:0]							
230	DGMA11R[7:0]							
231	DGMA12R[7:0]							
232	DGMA13R[7:0]							

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
233	DGMA14R[7:0]							
234	DGMA15R[7:0]							
235	DGMA16R[7:0]							
236	DGMA17R[7:0]							
237	DGMA18R[7:0]							
238	DGMA19R[7:0]							
239	DGMA20R[7:0]							
240	DGMA21R[7:0]							
241	DGMA22R[7:0]							
242	DGMA23R[7:0]							
243	DGMA24R[7:0]							
244	DGMA1R[9:8]		DGMA2R[9:8]		DGMA3R[9:8]		DGMA4R[9:8]	
245	DGMA5R[9:8]		DGMA6R[9:8]		DGMA7R[9:8]		DGMA8R[9:8]	
246	DGMA9R[9:8]		DGMA10R[9:8]		DGMA11R[9:8]		DGMA12R[9:8]	
247	DGMA13R[9:8]		DGMA14R[9:8]		DGMA15R[9:8]		DGMA16R[9:8]	
248	DGMA17R[9:8]		DGMA18R[9:8]		DGMA19R[9:8]		DGMA20R[9:8]	
249	DGMA21R[9:8]		DGMA22R[9:8]		DGMA23R[9:8]		DGMA24R[9:8]	
250	DGMA1G[7:0]							
251	DGMA2G[7:0]							
252	DGMA3G[7:0]							
253	DGMA4G[7:0]							
254	DGMA5G[7:0]							
255	DGMA6G[7:0]							
256	DGMA7G[7:0]							
257	DGMA8G[7:0]							
258	DGMA9G[7:0]							
259	DGMA10G[7:0]							
260	DGMA11G[7:0]							
261	DGMA12G[7:0]							
262	DGMA13G[7:0]							
263	DGMA14G[7:0]							
264	DGMA15G[7:0]							
265	DGMA16G[7:0]							
266	DGMA17G[7:0]							
267	DGMA18G[7:0]							
268	DGMA19G[7:0]							
269	DGMA20G[7:0]							
270	DGMA21G[7:0]							
271	DGMA22G[7:0]							
272	DGMA23G[7:0]							
273	DGMA24G[7:0]							
274	DGMA1G[9:8]		DGMA2G[9:8]		DGMA3G[9:8]		DGMA4G[9:8]	
275	DGMA5G[9:8]		DGMA6G[9:8]		DGMA7G[9:8]		DGMA8G[9:8]	
276	DGMA9G[9:8]		DGMA10G[9:8]		DGMA11G[9:8]		DGMA12G[9:8]	
277	DGMA13G[9:8]		DGMA14G[9:8]		DGMA15G[9:8]		DGMA16G[9:8]	
278	DGMA17G[9:8]		DGMA18G[9:8]		DGMA19G[9:8]		DGMA20G[9:8]	
279	DGMA21G[9:8]		DGMA22G[9:8]		DGMA23G[9:8]		DGMA24G[9:8]	
280	DGMA1B[7:0]							
281	DGMA2B[7:0]							
282	DGMA3B[7:0]							
283	DGMA4B[7:0]							
284	DGMA5B[7:0]							
285	DGMA6B[7:0]							
286	DGMA7B[7:0]							
287	DGMA8B[7:0]							
288	DGMA9B[7:0]							
289	DGMA10B[7:0]							
290	DGMA11B[7:0]							
291	DGMA12B[7:0]							
292	DGMA13B[7:0]							
293	DGMA14B[7:0]							
294	DGMA15B[7:0]							
295	DGMA16B[7:0]							

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
296	DGMA17B[7:0]							
297	DGMA18B[7:0]							
298	DGMA19B[7:0]							
299	DGMA20B[7:0]							
300	DGMA21B[7:0]							
301	DGMA22B[7:0]							
302	DGMA23B[7:0]							
303	DGMA24B[7:0]							
304	DGMA1B[9:8]		DGMA2B[9:8]		DGMA3B[9:8]		DGMA4B[9:8]	
305	DGMA5B[9:8]		DGMA6B[9:8]		DGMA7B[9:8]		DGMA8B[9:8]	
306	DGMA9B[9:8]		DGMA10B[9:8]		DGMA11B[9:8]		DGMA12B[9:8]	
307	DGMA13B[9:8]		DGMA14B[9:8]		DGMA15B[9:8]		DGMA16B[9:8]	
308	DGMA17B[9:8]		DGMA18B[9:8]		DGMA19B[9:8]		DGMA20B[9:8]	
309	DGMA21B[9:8]		DGMA22B[9:8]		DGMA23B[9:8]		DGMA24B[9:8]	
310	-	DLL_BANK	LVDS_AGING	FMT	LANE_SW	LANE_PN	-	
311	RESERVED							
312	RESERVED							
313	RESERVED							
314	RESERVED							
315	RESERVED							
316	RESERVED							
317	RESERVED							
318	RESERVED							
319	RESERVED							
320	RESERVED							
321	RESERVED							
322	RESERVED							
323	RESERVED							
324	RESERVED							
325	RESERVED							
326	RESERVED							
327	RESERVED							
328	RESERVED							
329	RESERVED							
330	RESERVED							
331	RESERVED							
332	RESERVED							
333	RESERVED							
334	RESERVED							
335	RESERVED							
336	RESERVED							
337	RESERVED							
338	RESERVED							
339	RESERVED							
340	RESERVED							
341	RESERVED							
342	RESERVED							
343	RESERVED							
344	RESERVED							
345	-						VCOMS_HT[8]	VCOMS_LT[8]
346	VCOMS_HT[7:0]							
347	VCOMS_LT[7:0]							
348	-	-	VGHS_HT[5:0]					
349	-	-	-	VGLS_HT[4:0]				
350	-	-	VGHS_LT[5:0]					
351	-	-		VGLS_LT[4:0]				
352	DIM_EN	DIM_FRAME[1:0]		VGMPHS_HT[4:0]				
353	DIM_OPT	-		VGMNHS_HT[4:0]				
354	VGMPLS_HT[3:0]				VGMNLS_HT[3:0]			
355	TS_GOE_EN	TS_AGAM_EN	-	VGMPHS_LT[4:0]				

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
356	TS_VCOM_EN	TS_VGHL_EN	-	VGMNHS_LT[4:0]				
357	VGMPLS_LT[3:0]				VGMNLS_LT[3:0]			
358	RESERVED							
359	RESERVED							
360	RESERVED							
361	RESERVED							
362	RESERVED							
363	RESERVED							
364	RESERVED							
365	RESERVED							
366	RESERVED							
367	RESERVED							
368	RESERVED							
369	RESERVED							
370	RESERVED							
371	RESERVED							
372	RESERVED							
373	RESERVED							
374	RESERVED							
375 ~ 434	GIP function setting							
435	-	-	GOUTL_1_SEL[5:0]					
436	-	-	GOUTL_2_SEL[5:0]					
437	-	-	GOUTL_3_SEL[5:0]					
438	-	-	GOUTL_4_SEL[5:0]					
439	-	-	GOUTL_5_SEL[5:0]					
440	-	-	GOUTL_6_SEL[5:0]					
441	-	-	GOUTL_7_SEL[5:0]					
442	-	-	GOUTL_8_SEL[5:0]					
443	-	-	GOUTL_9_SEL[5:0]					
444	-	-	GOUTL_10_SEL[5:0]					
445	-	-	GOUTL_11_SEL[5:0]					
446	-	-	GOUTL_12_SEL[5:0]					
447	-	-	GOUTL_13_SEL[5:0]					
448	-	-	GOUTL_14_SEL[5:0]					
449	-	-	GOUTL_15_SEL[5:0]					
450	-	-	GOUTL_16_SEL[5:0]					
451	-	-	GOUTL_17_SEL[5:0]					
452	-	-	GOUTL_18_SEL[5:0]					
453	-	-	GOUTL_19_SEL[5:0]					
454	-	-	GOUTL_20_SEL[5:0]					
455	-	-	RESERVED					
456	-	-	RESERVED					
457	-	-	RESERVED					
458	-	-	RESERVED					
459	-	-	RESERVED					
460	-	-	RESERVED					
461	-	-	GOUTR_1_SEL[5:0]					
462	-	-	GOUTR_2_SEL[5:0]					
463	-	-	GOUTR_3_SEL[5:0]					
464	-	-	GOUTR_4_SEL[5:0]					
465	-	-	GOUTR_5_SEL[5:0]					
466	-	-	GOUTR_6_SEL[5:0]					
467	-	-	GOUTR_7_SEL[5:0]					
468	-	-	GOUTR_8_SEL[5:0]					
469	-	-	GOUTR_9_SEL[5:0]					
470	-	-	GOUTR_10_SEL[5:0]					
471	-	-	GOUTR_11_SEL[5:0]					
472	-	-	GOUTR_12_SEL[5:0]					
473	-	-	GOUTR_13_SEL[5:0]					

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
474	-	-	GOUTR_14_SEL[5:0]					
475	-	-	GOUTR_15_SEL[5:0]					
476	-	-	GOUTR_16_SEL[5:0]					
477	-	-	GOUTR_17_SEL[5:0]					
478	-	-	GOUTR_18_SEL[5:0]					
479	-	-	GOUTR_19_SEL[5:0]					
480	-	-	RESERVED					
481	-	-	RESERVED					
482	-	-	RESERVED					
483	-	-	RESERVED					
484	-	-	RESERVED					
485	-	-	RESERVED					
486	-	-	RESERVED					
487	-	-	GOUTL_1_SEL2[5:0]					
488	-	-	GOUTL_2_SEL2[5:0]					
489	-	-	GOUTL_3_SEL2[5:0]					
490	-	-	GOUTL_4_SEL2[5:0]					
491	-	-	GOUTL_5_SEL2[5:0]					
492	-	-	GOUTL_6_SEL2[5:0]					
493	-	-	GOUTL_7_SEL2[5:0]					
494	-	-	GOUTL_8_SEL2[5:0]					
495	-	-	GOUTL_9_SEL2[5:0]					
496	-	-	GOUTL_10_SEL2[5:0]					
497	-	-	GOUTL_11_SEL2[5:0]					
498	-	-	GOUTL_12_SEL2[5:0]					
499	-	-	GOUTL_13_SEL2[5:0]					
500	-	-	GOUTL_14_SEL2[5:0]					
501	-	-	GOUTL_15_SEL2[5:0]					
502	-	-	GOUTL_16_SEL2[5:0]					
503	-	-	GOUTL_17_SEL2[5:0]					
504	-	-	GOUTL_18_SEL2[5:0]					
505	-	-	GOUTL_19_SEL2[5:0]					
506	-	-	GOUTL_20_SEL2[5:0]					
507	-	-	GOUTR_1_SEL2[5:0]					
508	-	-	GOUTR_2_SEL2[5:0]					
509	-	-	GOUTR_3_SEL2[5:0]					
510	-	-	GOUTR_4_SEL2[5:0]					
511	-	-	GOUTR_5_SEL2[5:0]					
512	-	-	GOUTR_6_SEL2[5:0]					
513	-	-	GOUTR_7_SEL2[5:0]					
514	-	-	GOUTR_8_SEL2[5:0]					
515	-	-	GOUTR_9_SEL2[5:0]					
516	-	-	GOUTR_10_SEL2[5:0]					
517	-	-	GOUTR_11_SEL2[5:0]					
518	-	-	GOUTR_12_SEL2[5:0]					
519	-	-	GOUTR_13_SEL2[5:0]					
520	-	-	GOUTR_14_SEL2[5:0]					
521	-	-	GOUTR_15_SEL2[5:0]					
522	-	-	GOUTR_16_SEL2[5:0]					
523	-	-	GOUTR_17_SEL2[5:0]					
524	-	-	GOUTR_18_SEL2[5:0]					
525	-	-	GOUTR_19_SEL2[5:0]					
526	-	-	GOUTR_20_SEL2[5:0]					
527	USER_ID1[7:0]							
528	USER_ID2[7:0]							
529	USER_ID3[7:0]							
530	USER_ID4[7:0]							
531	USER_ID5[7:0]							
532	USER_ID6[7:0]							
533	USER_ID7[7:0]							
534	USER_ID8[7:0]							
535	USER_ID9[7:0]							
536	USER_ID10[7:0]							

EEP Index	D7	D6	D5	D4	D3	D2	D1	D0
537	RESERVED							
:								
560								
561	EXPECTED CHECKSUM[7:0]							

EEPROM address	EEPROM Data (EEP Index)	
	High Byte	Low Byte
0	0	1
1	2	3
2	4	5
3	6	7
:	:	:
n	EEPROM index=2n	EEPROM index=2n+1
280	560	561

9. DC Characteristics

9.1. Absolute maximum ratings(1)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Main power supply	VCC1/VCC1P	-0.3	-	4.0	V
Power supply for internal reference	VCC2	-0.3	-	4.0	V
I/O power supply	VCCIF	-0.3	-	4.0	V
Power supply for source driver	VSP	-0.3	-	7.7	V
Power supply for source driver	VSN	-7.7	-	0.3	V
Programming voltage **(Under 5sec)**	VDD_OTP	-0.3	-	8.7	V
Storage temperature	T_{ST}	-55	-	+125	°C
Operating temperature	T_A	-40	-	+105	°C
Junction temperature	T_{JC}	-	-	+125	°C
Digital I/O input signals: Input interface pins Input control pins, group1 Input control pins, group2 Serial interface pins Cascade and gate driver control pins Please refer to Ch. 4.1. Pin description	V_{IO}	-0.3	-	VCC1 + 0.3	V

Note: (1) Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2. Recommended operating conditions and electrical characteristics

9.2.1. Digital circuit: Normal mode

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40°C to +105°C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Operating frequency, TTL mode	F_{TTL}	-	2	-	60	MHz
Operating frequency, LVDS mode	F_{LVDS}	1-port	15	-	110	MHz
		2-port	15	-	105	MHz
Supply voltage	VCC1 VCC1P VCC2 VCCIF	-	3.0	3.3	3.6	V
Internal digital operating voltage	VDDD	-	1.4	1.5	1.6	V
OTP programming voltage	VDD_OTP	Current loading @10mA	8.5	8.6	8.7	V
Low level input voltage	V_{IL}	-	VSS1-0.3	-	0.3xVCC1	V
High level input voltage	V_{IH}	-	0.7xVCC1	-	VCC1+0.3	V
High level output voltage	V_{OH}	-	VCC1-0.4	-	-	V
Low level output voltage	V_{OL}	-	GND	-	GND+0.4	V
Pull low/high resistor	R_I	For I/O circuit	150	350	550	KΩ

9.2.2. Digital circuit: LVDS mode

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40°C to +105°C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Differential input high Threshold voltage	V_{TH}	V_{CM}=1.2V	+0.10	-	-	V
Differential input low threshold voltage	V_{TL}	V_{CM}=1.2V	-	-	-0.10	V
Differential input common Mode voltage	V_{CM}	-	0.45	1.2	1.7-|V_{ID}|/2	V
Differential input voltage	|V_{ID}|	-	0.1	-	0.6	V
Differential input leakage Current	I_{LVLEAK}	-	-10	-	+10	μA

Table 9.1: LVDS mode DC electrical characteristics

Single-ended:
LVCLKP,
LVCLKN,
LVD[3:0]P,
LVD[3:0]N

Differential:
LVCLKP-LVCLKN,
LVD[3:0]P-LVD[3:0]N

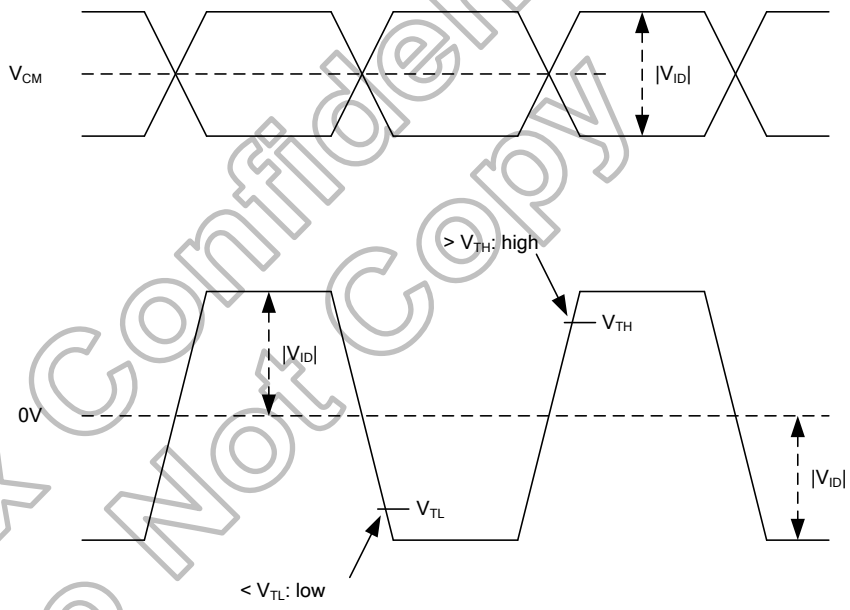


Figure 9.1: LVDS mode DC electrical characteristics

9.2.3. Analog circuit: Normal mode

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40°C to +105°C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Analog positive supply voltage	VSP	VSP is generated by PFM, VSPS[4:0]=14h,with proper settings and components.	6.7	7	7.3	V
Analog negative supply voltage	VSN	VSN is generated by PFM, VSNS[4:0]=14h,with proper settings and components.	-7.3	-7	-6.7	V
Source driver positive supply voltage	VSDP	VSP ≥ 7V, VSDPS[4:0]=14h, loading current=0	6.65	6.8	6.95	V
Source driver negative supply voltage	VSDN	VSN ≤ -7V, VSDNS[4:0]=14h, loading current=0	-6.95	-6.8	-6.65	V
Internal regulator output for negative level shifter	VCL	-	-2.88	-2.75	-2.62	V
Output for positive gamma reference high voltage	VGMPHO	VSDP ≥ 6.8V, VGMPHS[4:0]=0x1Ah	6.48	6.6	6.72	V
Output for positive gamma reference low voltage	VGMPLO	VGMPLS[3:0]=0x01h	0.12	0.2	0.28	V
Output for negative gamma reference high voltage	VGMNHO	VSDN ≤ -6.8V, VGMNHS[4:0]=0x1Ah	-6.72	-6.6	-6.48	V
Output for negative gamma reference low voltage	VGMNLO	VGMNLS[3:0]=0x01h	-0.28	-0.2	-0.12	V
VCOM voltage	VCOM	VCOMS[8:0]=0x15Ch	-1.79	-1.74	-1.69	V
Source output voltage, positive polarity	V_{SDOP}	-	0.2	-	VSDP-0.2	V
Source output voltage, negative polarity	V_{SDON}	-	VSDN+0.2	-	-0.2	V
Output for GIP/gate driver positive power supply	VGH	VGH is generated by charge pump, VGHS[5:0]=0x0Eh, loading current=0mA	11.0	12.0	13.0	V
Output for GIP/gate driver negative power supply	VGL	VGL is generated by charge pump, VGLS[4:0]=0x06h, loading current=0mA	-9.0	-8.0	-7.0	V

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Source output voltage deviation	V_{OD}	V_{SDOP}=0.5V to VSDP-0.5V, V_{SDON}=VSDN+0.5V to -0.5V	-	-	10	mV
		V_{SDOP}=0.2V to 0.5V or V_{SDOP}=VSDP-0.5V to VSDP-0.2V, V_{SDON}=VSDN+0.2V to VSDN+0.5V or V_{SDON}=-0.5V to -0.2V	-	-	15	mV
Standby current **(VCC1 + VCC2)**	I_{STBvcc}	"STBYB=L" and all inputs are default.	-	-	300	μA
Standby current **(VSN or VSP)**	I_{STB}	"STBYB=L", VSP or VSN external input	-	-	100	μA

9.2.4. LVDS mode AC electrical characteristics

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40°C to +105°C)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency **(1-port/2-port)**	F_{LVCYC}	15	-	110/105	MHz
Clock period **(1-port/2-port)**	T_{LVCYC}	9.09/9.52	-	-	ns
1 data bit time	UI	-	1/7 T_{LVCYC}	-	ns
Clock high time	T_{LVHW}	-	4	-	UI
Clock low time	T_{LVLW}	-	3	-	UI
Position 1	T_{POS1}	-0.2	0	0.2	UI
Position 0	T_{POS0}	0.8	1	1.2	UI
Position 6	T_{POS6}	1.8	2	2.2	UI
Position 5	T_{POS5}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 3	T_{POS3}	4.8	5	5.2	UI
Position 2	T_{POS2}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.6	-	-	UI
Input eye border	T_{EX}	-	-	0.2	UI
LVDS wake up time	T_{ENLVDS}	-	-	150	µs
LVDS clock to clock skew	T_{SKEW_EO}	-1	-	1	UI

Table 9.2: LVDS mode AC electrical characteristics

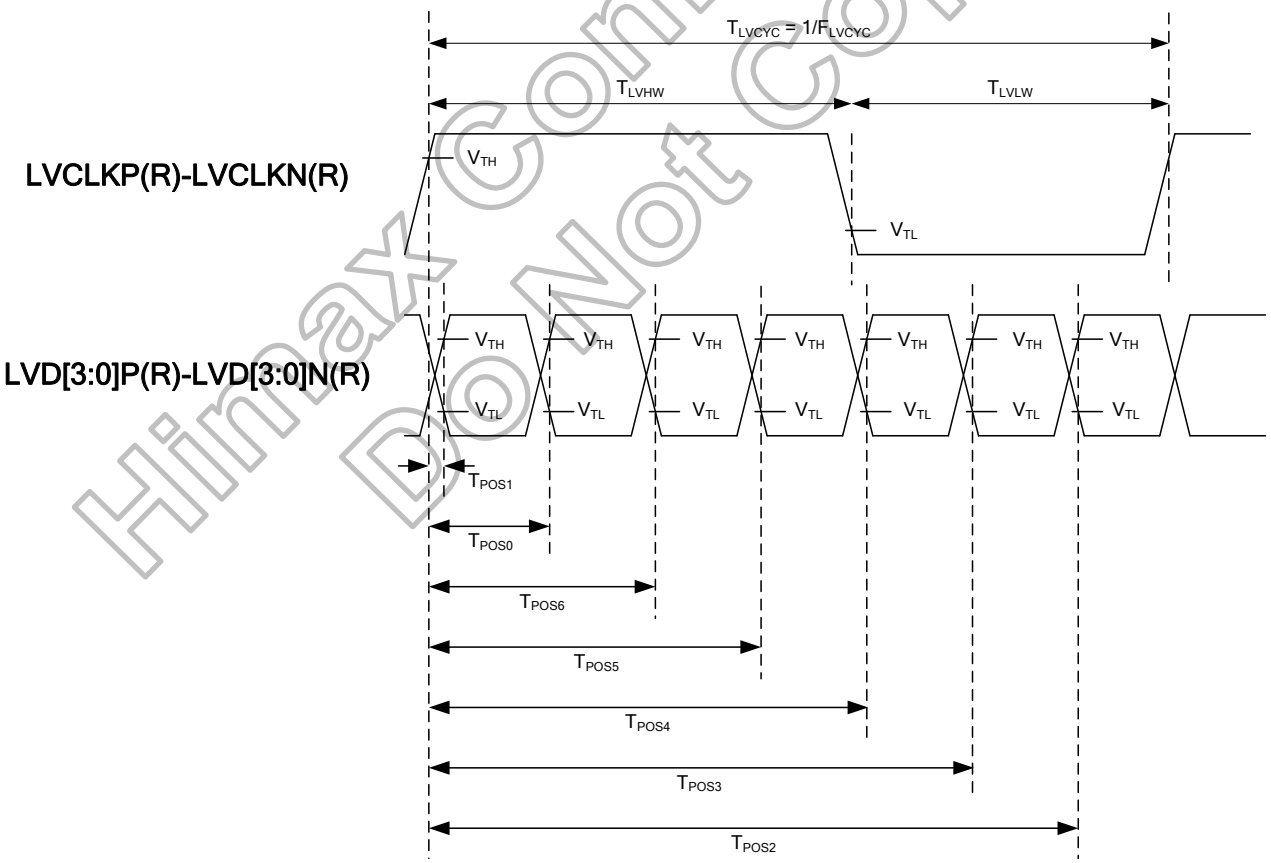
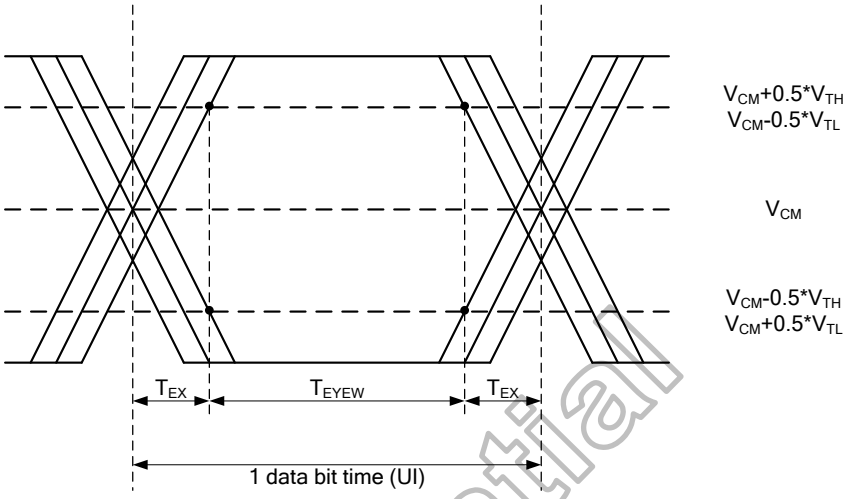


Figure 9.2: LVDS input timing

Single-ended:
LVD[3:0]P,
LVD[3:0]N



Differential:
LVD[3:0]P-LVD[3:0]N

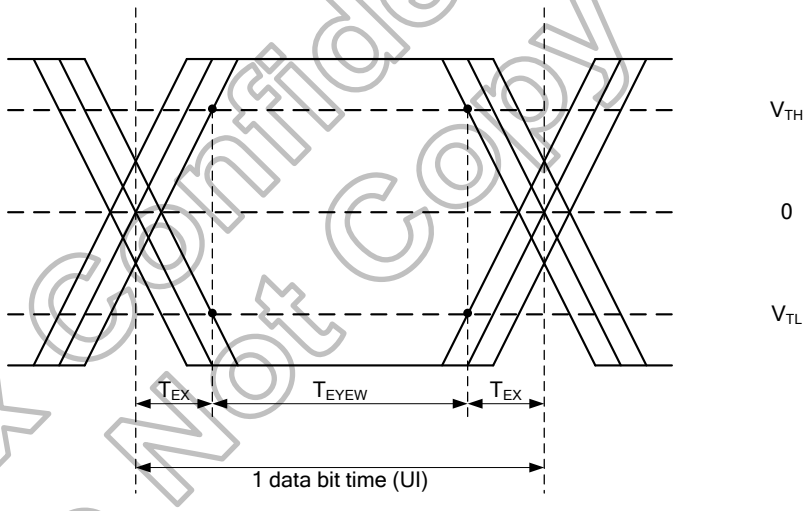


Figure 9.3: LVDS input eye diagram

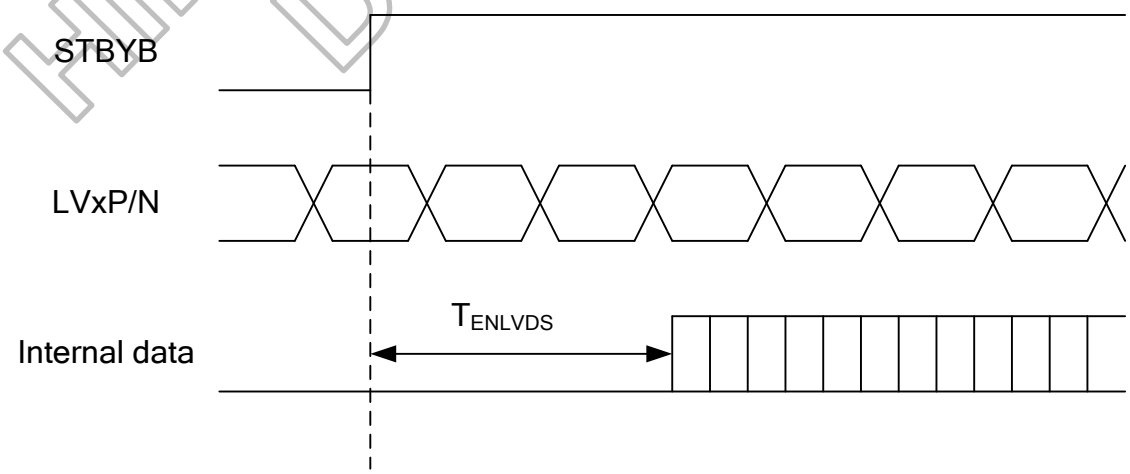


Figure 9.4: LVDS wake up time

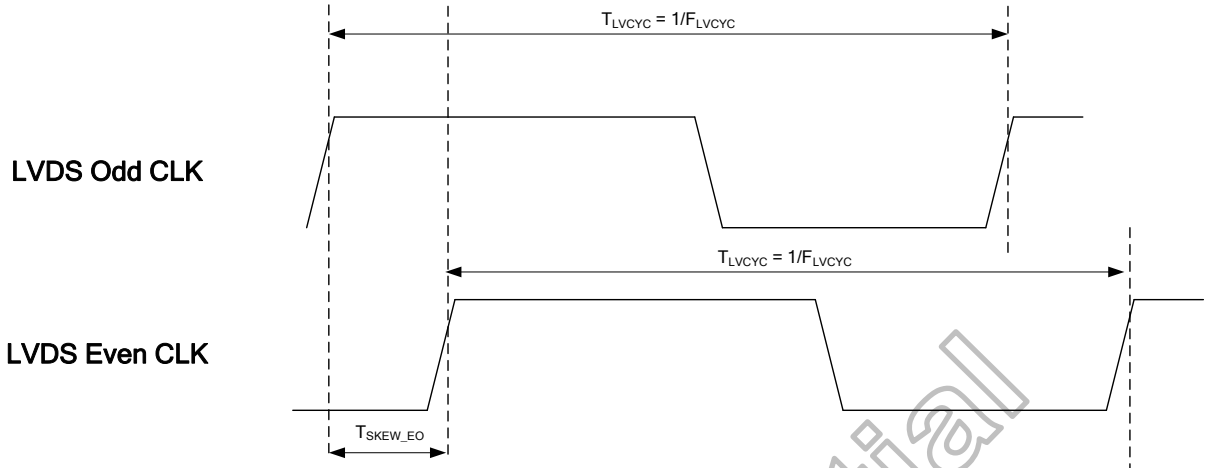


Figure 9.5: LVDS clock to clock skew

LVDS with SSC

The LVDS receiver can support spread spectrum clock **(SSC)**. Limitation is listed as below.

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Modulation frequency	SSC_{MF}	LVDS clock frequency center at ≤110MHz~80MHz	-	-	200	KHz
		LVDS clock frequency center at <80MHz~40MHz	-	-	150	KHz
		LVDS clock frequency center at <40MHz~15MHz	-	-	100	KHz
Modulation rate	SSC_{MR}	LVDS clock frequency + SSCMR in the range of 15MHz~110MHz	-	-	±3	%

Table 9.3: SSC limitation of LVDS interface

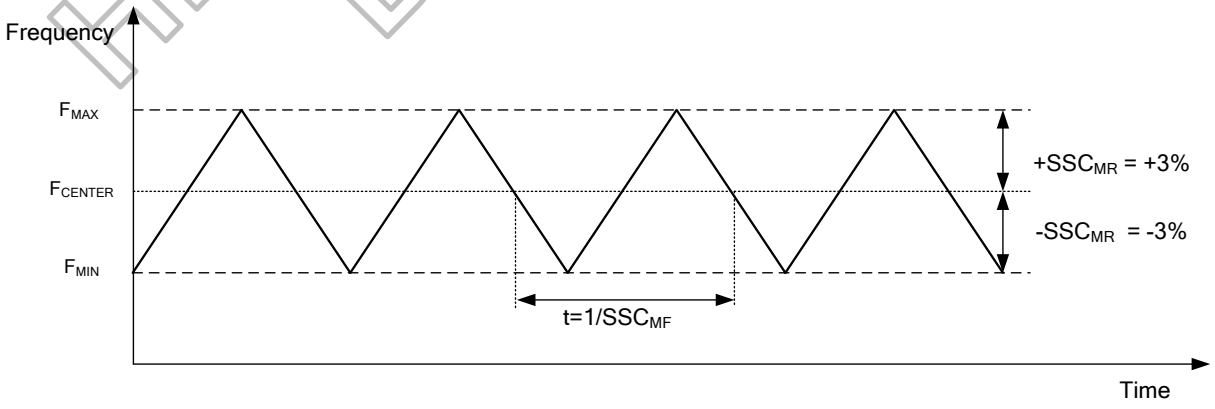


Figure 9.6: SSC figure

9.2.5. TTL mode AC electrical characteristics

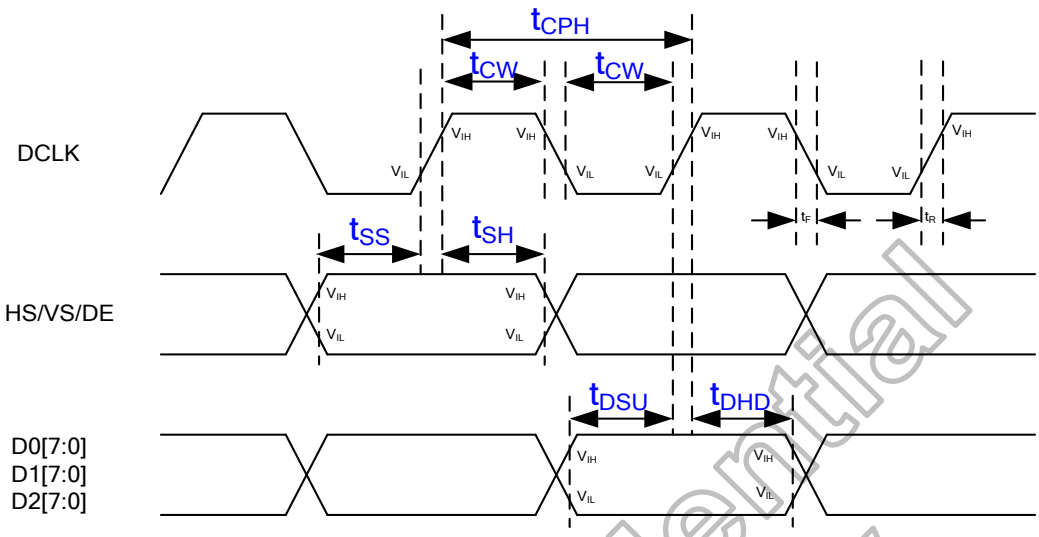


Figure 9.7: Input signal timing

Input data/Sync. parameters
(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40°C to +105°C)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK period	t_{CPH}	16.67	-	-	ns
DCLK clock high/low width	t_{CW}	6	-	-	ns
Data setup time	t_{DSU}	5	-	-	ns
Data hold time	t_{DHD}	5	-	-	ns
HS/VS/DE setup time	t_{SS}	5	-	-	ns
HS/VS/DE hold time	t_{SH}	5	-	-	ns
Input signal rising time	t_R	-	-	10	ns
Input signal falling time	t_F	-	-	10	ns

Table 9.4: Input data/Sync. parameters

9.2.6. Reset timing

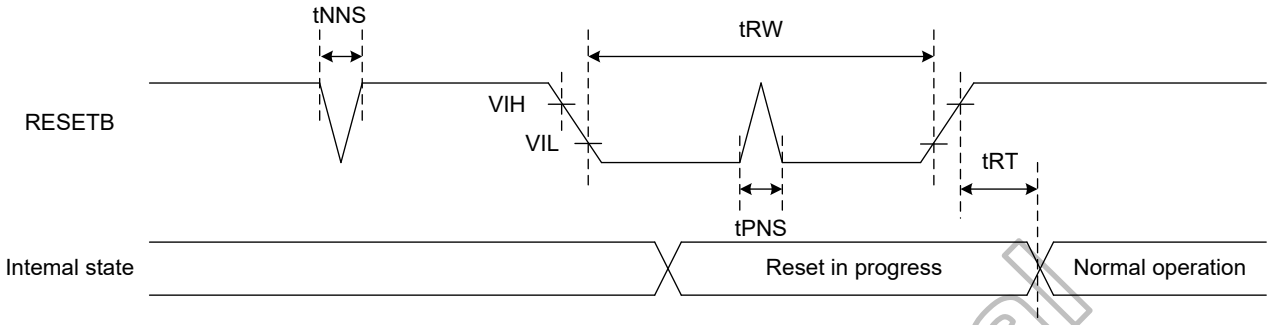


Figure 9.8: Reset timing

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40°C to +105°C)

Signal	Parameter	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
RESETB	Reset pulse width	tRW	10	-	-	µs
	Reset complete time	tRT	-	-	5	µs
	Positive spike noise width	tPNS	-	-	100	ns
	Negative spike noise width	tNNS	-	-	100	ns

Table 9.5: Reset timing parameter

9.2.7. SPI timing

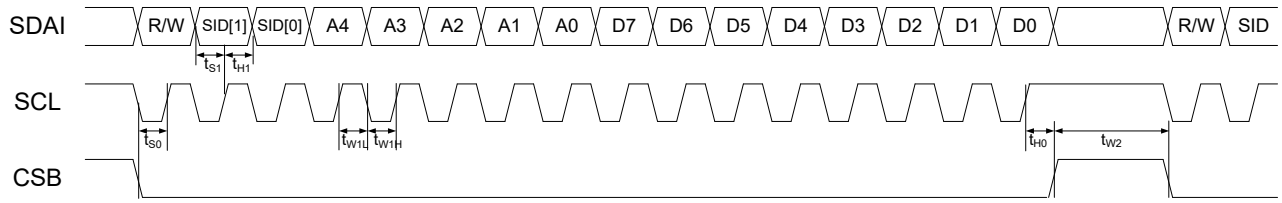


Figure 9.9: SPI signal timing

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40°C to +105°C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
SDAI setup time	t_{S0}	CSB to SCL	60	-	-	ns
	t_{S1}	SDAI to SCL	60	-	-	ns
SDAI hold time	t_{H0}	CSB to SCL	60	-	-	ns
	t_{H1}	SDAI to SCL	60	-	-	ns
Pulse width	t_{W1L}	SCL pulse width	100	-	-	ns
	t_{W1H}	SCL pulse width	100	-	-	ns
	t_{W2}	CSB pulse width	1	-	-	µs
Clock duty	-	-	40	50	60	%

Table 9.6: SPI timing parameter

9.2.8. I2C timing

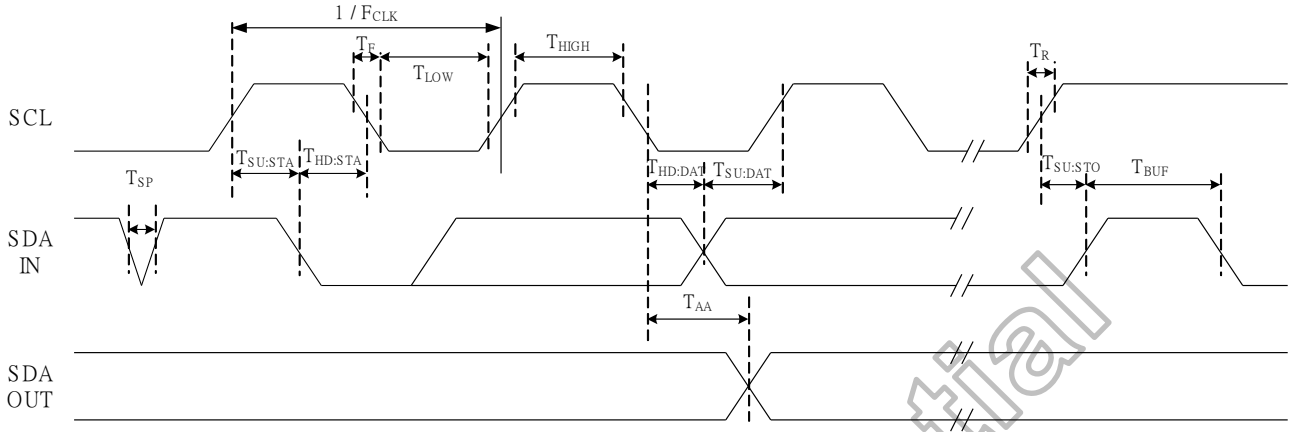


Figure 9.10: I2C signal timing

(VCC1=VCC1P=VCC2=VCCIF=3.0V to 3.6V, VSS1=VSS2=VSSA=0V, T_A=-40°C to +105°C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock frequency	F_{CLK}	-	-	-	400	KHz
Clock high time	T_{HIGH}	-	600	-	-	ns
Clock low time	T_{LOW}	-	1300	-	-	ns
SDA and SCL rise time	T_R	-	-	-	300	ns
SDA and SCL fall time	T_F	-	-	-	300	ns
Start condition hold time	$T_{HD:STA}$	-	600	-	-	ns
Start condition setup time	$T_{SU:STA}$	-	600	-	-	ns
Data input hold time	$T_{HD:DAT}$	-	0	-	-	ns
Data input setup time	$T_{SU:DAT}$	-	100	-	-	ns
Stop condition setup time	$T_{SU:STO}$	-	600	-	-	ns
Output valid from clock	T_{AA}	-	-	-	900	ns
Bus free time	T_{BUF}	Time the bus must be free before a new transmission can start	1300	-	-	ns
Input filter spike suppression	T_{SP}	SDA and SCL pins	-	-	10	ns

Table 9.7: I2C timing parameter

10. Pad Information

10.1. Chip information

Parameter	Size		Unit
	X	Y	
Chip size	28370	880	μm
Chip size **(Including scribe line)**	28450	950	

Table 10.1: Chip Information

10.2. Bump dimension

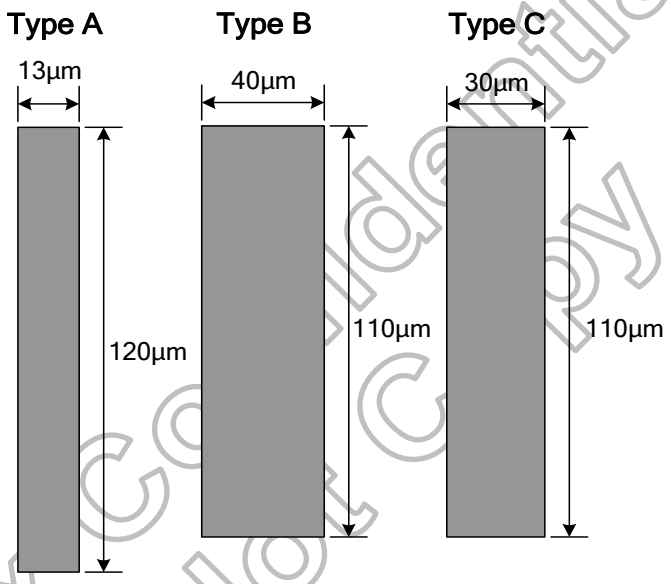


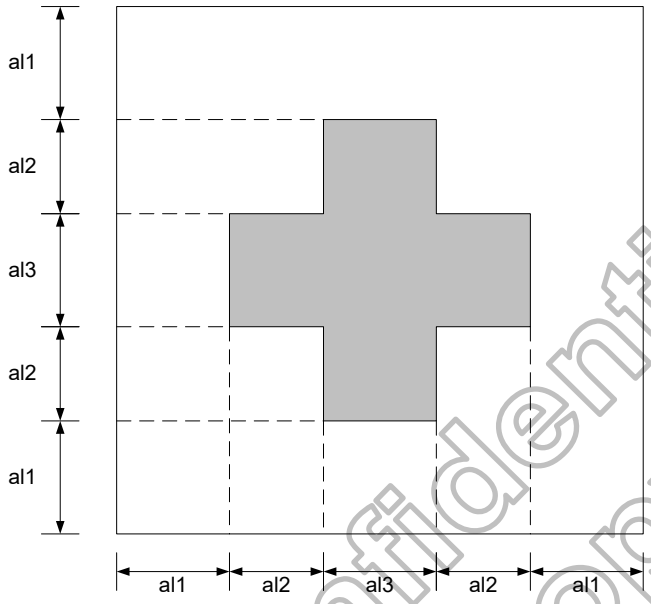
Figure 10.1: Bump dimension

10.3. Bump information

Bump height: 12±3.0μm
Bump height Co-planarity within Die: < 2μm
Hardness: 90±20Hv; 75±20Hv depends on customer
Shear stress: > 4.5g/mil^2

10.4. Alignment mark

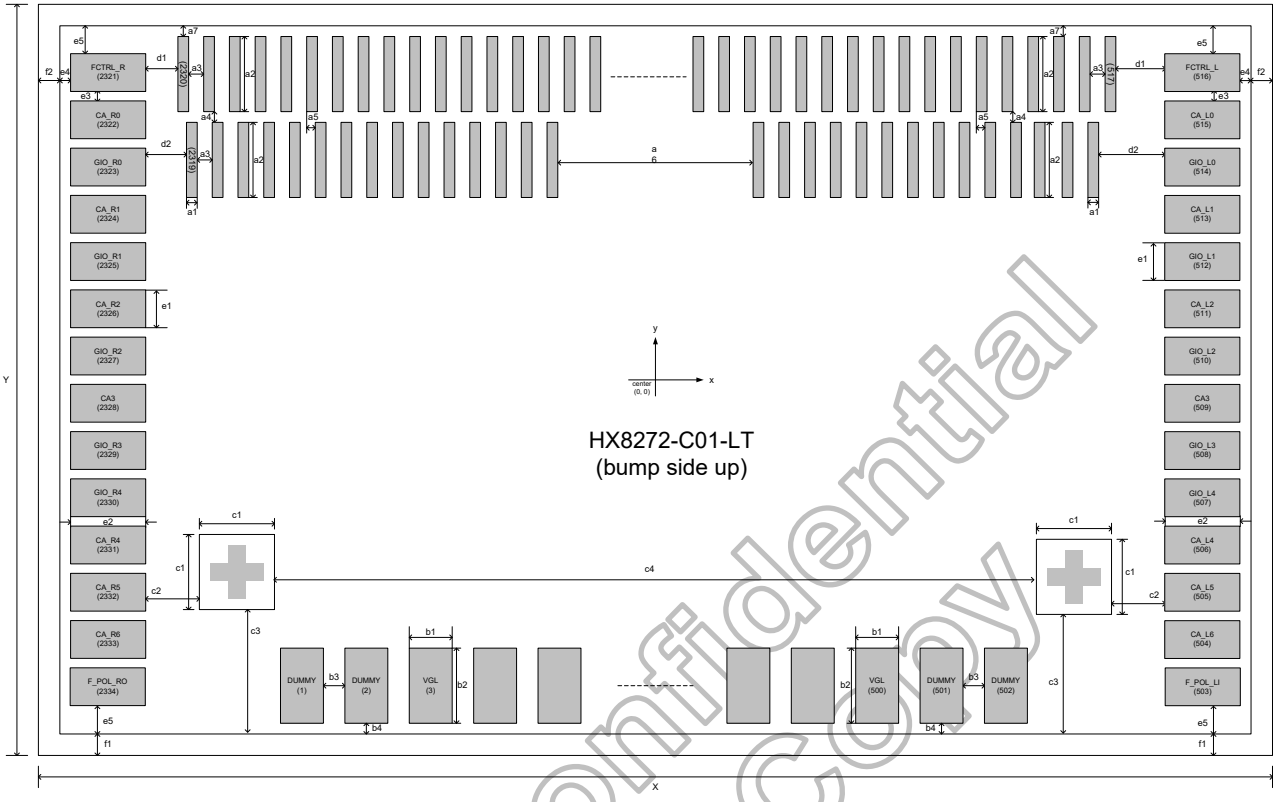
Two Alignment marks are center located at (-13881, -151) and (13881, -151).
The cross pattern is top metal layer.



Symbol	Dimension (μm)
al1	12.5
al2	33
al3	34

Table 10.2: Alignment mark dimension

10.5. Chip outline

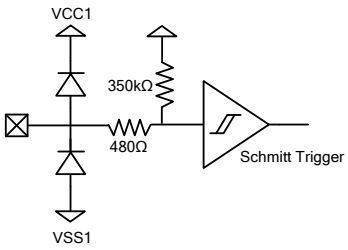
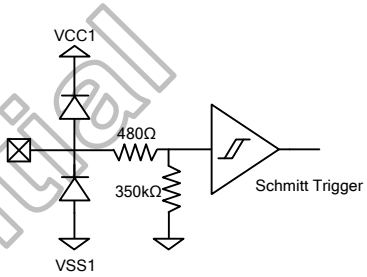
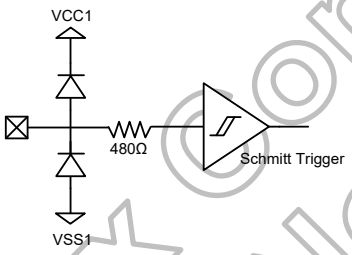
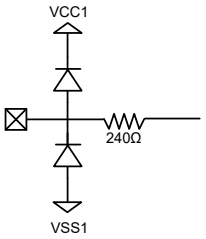
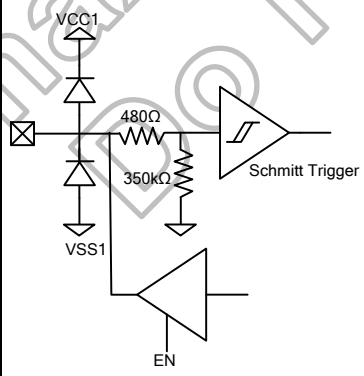
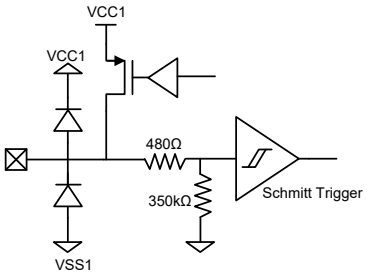


Symbol	Dimension (μm)
a1	13
a2	120
a3	15
a4	25
a5	14
a6	5139
a7	50
b1	40
b2	110
b3	15
b4	50

Symbol	Dimension (μm)
c1	125
c2	81.5
c3	226.5
c4	27637
d1	116.5
d2	130.5
e1	30
e2	110
e3	25
e4	50
e5	67.5
f1	35
f2	40

Table 10.3: Chip outline dimension

10.6. I/O structure

Signal	Input equivalent circuit	Signal	Input equivalent circuit
HS, VS, RESETB, RESETB_SLP, STBYB, FCS, SIDEN, MODE, NB, RL,TB, INV[1:0], SPI_CSB		DE,GSQ, ATREN, EXT_PWR, EXT_SDPWR, EEPEN, TR[1:0], GDSEL, GPOS[1:0], BISTEN, SPI_SCL, SPI_SDAI , I2C_SCL, I2C_SPI_SEL, ESDAI, F_POL_LI, ZZS[1:0], PTS[2:0], CA_L[2:0], CA_L[6:4], TS_H, TS_L, FMT, LANE_SW, LANE_PN	
SID[1:0], RS[3:0]		D0[7:0], D1[7:0], D2[7:0] DCLK	
I2C_SDA, GIO_L[4:0], GIO_R[4:0], ECS,ESCL, FCTRL_L, FCTRL_R		CA3	

10.7. Pad coordinates

No.	Name	X	Y	Bump size(μm)
1	DUMMY	-13777.5	-335	40 x 110
2	DUMMY	-13722.5	-335	40 x 110
3	VGL	-13667.5	-335	40 x 110
4	VGL	-13612.5	-335	40 x 110
5	VGL	-13557.5	-335	40 x 110
6	DUMMY	-13502.5	-335	40 x 110
7	VGH	-13447.5	-335	40 x 110
8	VGH	-13392.5	-335	40 x 110
9	VGH	-13337.5	-335	40 x 110
10	VGH	-13282.5	-335	40 x 110
11	VSS1	-13227.5	-335	40 x 110
12	VSS1	-13172.5	-335	40 x 110
13	VSS1	-13117.5	-335	40 x 110
14	VSS1	-13062.5	-335	40 x 110
15	DUMMY	-13007.5	-335	40 x 110
16	DUMMY	-12952.5	-335	40 x 110
17	VCOM_R	-12897.5	-335	40 x 110
18	VCOM_R	-12842.5	-335	40 x 110
19	VCOM_R	-12787.5	-335	40 x 110
20	VCOM_R	-12732.5	-335	40 x 110
21	THROUGH_1	-12677.5	-335	40 x 110
22	THROUGH_1	-12622.5	-335	40 x 110
23	DUMMY	-12567.5	-335	40 x 110
24	DUMMY	-12512.5	-335	40 x 110
25	CLN2	-12457.5	-335	40 x 110
26	CLN2	-12402.5	-335	40 x 110
27	CLN2	-12347.5	-335	40 x 110
28	CLN2	-12292.5	-335	40 x 110
29	CLP2	-12237.5	-335	40 x 110
30	CLP2	-12182.5	-335	40 x 110
31	CLP2	-12127.5	-335	40 x 110
32	CLP2	-12072.5	-335	40 x 110
33	CLP1	-12017.5	-335	40 x 110
34	CLP1	-11962.5	-335	40 x 110
35	CLP1	-11907.5	-335	40 x 110
36	CLP1	-11852.5	-335	40 x 110
37	CLN1	-11797.5	-335	40 x 110
38	CLN1	-11742.5	-335	40 x 110
39	CLN1	-11687.5	-335	40 x 110
40	CLN1	-11632.5	-335	40 x 110
41	VREGN	-11577.5	-335	40 x 110
42	VREGN	-11522.5	-335	40 x 110
43	VREGN	-11467.5	-335	40 x 110
44	VREGN	-11412.5	-335	40 x 110
45	VGL	-11357.5	-335	40 x 110
46	VGL	-11302.5	-335	40 x 110
47	VGL	-11247.5	-335	40 x 110
48	VGL	-11192.5	-335	40 x 110
49	DUMMY	-11137.5	-335	40 x 110
50	DUMMY	-11082.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
51	VGH	-11027.5	-335	40 x 110
52	VGH	-10972.5	-335	40 x 110
53	VGH	-10917.5	-335	40 x 110
54	VGH	-10862.5	-335	40 x 110
55	CHP3	-10807.5	-335	40 x 110
56	CHP3	-10752.5	-335	40 x 110
57	CHP3	-10697.5	-335	40 x 110
58	CHN3	-10642.5	-335	40 x 110
59	CHN3	-10587.5	-335	40 x 110
60	CHN3	-10532.5	-335	40 x 110
61	CHP2	-10477.5	-335	40 x 110
62	CHP2	-10422.5	-335	40 x 110
63	CHP2	-10367.5	-335	40 x 110
64	CHN2	-10312.5	-335	40 x 110
65	CHN2	-10257.5	-335	40 x 110
66	CHN2	-10202.5	-335	40 x 110
67	CHP1	-10147.5	-335	40 x 110
68	CHP1	-10092.5	-335	40 x 110
69	CHP1	-10037.5	-335	40 x 110
70	CHN1	-9982.5	-335	40 x 110
71	CHN1	-9927.5	-335	40 x 110
72	CHN1	-9872.5	-335	40 x 110
73	VREGP	-9817.5	-335	40 x 110
74	VREGP	-9762.5	-335	40 x 110
75	VREGP	-9707.5	-335	40 x 110
76	VREGP	-9652.5	-335	40 x 110
77	VSS1P	-9597.5	-335	40 x 110
78	VSS1P	-9542.5	-335	40 x 110
79	VSS1P	-9487.5	-335	40 x 110
80	VSS1P	-9432.5	-335	40 x 110
81	VSS1P	-9377.5	-335	40 x 110
82	VSS1P	-9322.5	-335	40 x 110
83	VCL	-9267.5	-335	40 x 110
84	VCL	-9212.5	-335	40 x 110
85	VCL	-9157.5	-335	40 x 110
86	VCL	-9102.5	-335	40 x 110
87	VCL	-9047.5	-335	40 x 110
88	VCL	-8992.5	-335	40 x 110
89	DUMMY	-8937.5	-335	40 x 110
90	DUMMY	-8882.5	-335	40 x 110
91	VMONN	-8827.5	-335	40 x 110
92	VMONN	-8772.5	-335	40 x 110
93	VSN	-8717.5	-335	40 x 110
94	VSN	-8662.5	-335	40 x 110
95	VSN	-8607.5	-335	40 x 110
96	VSN	-8552.5	-335	40 x 110
97	VSN	-8497.5	-335	40 x 110
98	DRVN	-8442.5	-335	40 x 110
99	DRVN	-8387.5	-335	40 x 110
100	DRVN	-8332.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
101	DRVN	-8277.5	-335	40 x 110
102	VCC1P	-8222.5	-335	40 x 110
103	VCC1P	-8167.5	-335	40 x 110
104	VCC1P	-8112.5	-335	40 x 110
105	VCC1P	-8057.5	-335	40 x 110
106	VCC1P	-8002.5	-335	40 x 110
107	VCC1P	-7947.5	-335	40 x 110
108	VSDN	-7892.5	-335	40 x 110
109	VSDN	-7837.5	-335	40 x 110
110	VSDN	-7782.5	-335	40 x 110
111	VSDN	-7727.5	-335	40 x 110
112	VSDN	-7672.5	-335	40 x 110
113	VSDN	-7617.5	-335	40 x 110
114	VSSA	-7562.5	-335	40 x 110
115	VSSA	-7507.5	-335	40 x 110
116	VSSA	-7452.5	-335	40 x 110
117	VSSA	-7397.5	-335	40 x 110
118	VSSA	-7342.5	-335	40 x 110
119	VSSA	-7287.5	-335	40 x 110
120	VSSA	-7232.5	-335	40 x 110
121	VSSA	-7177.5	-335	40 x 110
122	VSDP	-7122.5	-335	40 x 110
123	VSDP	-7067.5	-335	40 x 110
124	VSDP	-7012.5	-335	40 x 110
125	VSDP	-6957.5	-335	40 x 110
126	VSDP	-6902.5	-335	40 x 110
127	VSDP	-6847.5	-335	40 x 110
128	DRVP	-6792.5	-335	40 x 110
129	DRVP	-6737.5	-335	40 x 110
130	DRVP	-6682.5	-335	40 x 110
131	DRVP	-6627.5	-335	40 x 110
132	VSP	-6572.5	-335	40 x 110
133	VSP	-6517.5	-335	40 x 110
134	VSP	-6462.5	-335	40 x 110
135	VSP	-6407.5	-335	40 x 110
136	VSP	-6352.5	-335	40 x 110
137	VMONP	-6297.5	-335	40 x 110
138	VMONP	-6242.5	-335	40 x 110
139	DUMMY	-6187.5	-335	40 x 110
140	DUMMY	-6132.5	-335	40 x 110
141	DUMMY	-6077.5	-335	40 x 110
142	SPI_SDAO	-6022.5	-335	40 x 110
143	SPI_SDAO	-5967.5	-335	40 x 110
144	SPI_SDAI	-5912.5	-335	40 x 110
145	DUMMY	-5857.5	-335	40 x 110
146	SPI_SCL	-5802.5	-335	40 x 110
147	SPI_CSB	-5747.5	-335	40 x 110
148	DUMMY	-5692.5	-335	40 x 110
149	DUMMY	-5637.5	-335	40 x 110
150	DUMMY	-5582.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
151	I2C_SDA	-5527.5	-335	40 x 110
152	I2C_SDA	-5472.5	-335	40 x 110
153	I2C_SDA	-5417.5	-335	40 x 110
154	DUMMY	-5362.5	-335	40 x 110
155	I2C_SCL	-5307.5	-335	40 x 110
156	I2C_SPI_SEL	-5252.5	-335	40 x 110
157	DUMMY	-5197.5	-335	40 x 110
158	DUMMY	-5142.5	-335	40 x 110
159	DUMMY	-5087.5	-335	40 x 110
160	VGMNHI	-5032.5	-335	40 x 110
161	VGMNHI	-4977.5	-335	40 x 110
162	VGMNHI	-4922.5	-335	40 x 110
163	VGMNHI	-4867.5	-335	40 x 110
164	VGMNLI	-4812.5	-335	40 x 110
165	VGMNLI	-4757.5	-335	40 x 110
166	VGMNLI	-4702.5	-335	40 x 110
167	VGMNLI	-4647.5	-335	40 x 110
168	DUMMY	-4592.5	-335	40 x 110
169	DUMMY	-4537.5	-335	40 x 110
170	DUMMY	-4482.5	-335	40 x 110
171	DUMMY	-4427.5	-335	40 x 110
172	VDDD	-4372.5	-335	40 x 110
173	VDDD	-4317.5	-335	40 x 110
174	VDDD	-4262.5	-335	40 x 110
175	VDDD	-4207.5	-335	40 x 110
176	VDDD	-4152.5	-335	40 x 110
177	VSS1	-4097.5	-335	40 x 110
178	VSS1	-4042.5	-335	40 x 110
179	VSS1	-3987.5	-335	40 x 110
180	VSS1	-3932.5	-335	40 x 110
181	VSS1	-3877.5	-335	40 x 110
182	VSS1	-3822.5	-335	40 x 110
183	VCC1	-3767.5	-335	40 x 110
184	VCC1	-3712.5	-335	40 x 110
185	VCC1	-3657.5	-335	40 x 110
186	VCC1	-3602.5	-335	40 x 110
187	VCC1	-3547.5	-335	40 x 110
188	VCC1	-3492.5	-335	40 x 110
189	RESETB_SLP	-3437.5	-335	40 x 110
190	DUMMY	-3382.5	-335	40 x 110
191	VDDD	-3327.5	-335	40 x 110
192	VDDD	-3272.5	-335	40 x 110
193	VDDD	-3217.5	-335	40 x 110
194	VDDD	-3162.5	-335	40 x 110
195	VDDD	-3107.5	-335	40 x 110
196	VSS1	-3052.5	-335	40 x 110
197	VSS1	-2997.5	-335	40 x 110
198	VSS1	-2942.5	-335	40 x 110
199	VSS1	-2887.5	-335	40 x 110
200	VSS1	-2832.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
201	VCCIF	-2777.5	-335	40 x 110
202	VCCIF	-2722.5	-335	40 x 110
203	VCCIF	-2667.5	-335	40 x 110
204	VCCIF	-2612.5	-335	40 x 110
205	VCCIF	-2557.5	-335	40 x 110
206	VSS1	-2502.5	-335	40 x 110
207	VSS1	-2447.5	-335	40 x 110
208	VSS1	-2392.5	-335	40 x 110
209	VSS1	-2337.5	-335	40 x 110
210	D20	-2282.5	-335	40 x 110
211	D20	-2227.5	-335	40 x 110
212	D21	-2172.5	-335	40 x 110
213	D21	-2117.5	-335	40 x 110
214	VSS1	-2062.5	-335	40 x 110
215	VSS1	-2007.5	-335	40 x 110
216	D22	-1952.5	-335	40 x 110
217	D22	-1897.5	-335	40 x 110
218	D23	-1842.5	-335	40 x 110
219	D23	-1787.5	-335	40 x 110
220	VSS1	-1732.5	-335	40 x 110
221	VSS1	-1677.5	-335	40 x 110
222	D24	-1622.5	-335	40 x 110
223	D24	-1567.5	-335	40 x 110
224	D25	-1512.5	-335	40 x 110
225	D25	-1457.5	-335	40 x 110
226	VSS1	-1402.5	-335	40 x 110
227	VSS1	-1347.5	-335	40 x 110
228	D26	-1292.5	-335	40 x 110
229	D26	-1237.5	-335	40 x 110
230	D27	-1182.5	-335	40 x 110
231	D27	-1127.5	-335	40 x 110
232	VSS1	-1072.5	-335	40 x 110
233	VSS1	-1017.5	-335	40 x 110
234	D10	-962.5	-335	40 x 110
235	D10	-907.5	-335	40 x 110
236	D11	-852.5	-335	40 x 110
237	D11	-797.5	-335	40 x 110
238	VSS1	-742.5	-335	40 x 110
239	VSS1	-687.5	-335	40 x 110
240	D12	-632.5	-335	40 x 110
241	D12	-577.5	-335	40 x 110
242	D13	-522.5	-335	40 x 110
243	D13	-467.5	-335	40 x 110
244	VSS1	-412.5	-335	40 x 110
245	VSS1	-357.5	-335	40 x 110
246	D14	-302.5	-335	40 x 110
247	D14	-247.5	-335	40 x 110
248	D15	-192.5	-335	40 x 110
249	D15	-137.5	-335	40 x 110
250	VSS1	-82.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
251	VSS1	-27.5	-335	40 x 110
252	D16	27.5	-335	40 x 110
253	D16	82.5	-335	40 x 110
254	D17	137.5	-335	40 x 110
255	D17	192.5	-335	40 x 110
256	VSS1	247.5	-335	40 x 110
257	VSS1	302.5	-335	40 x 110
258	D00	357.5	-335	40 x 110
259	D00	412.5	-335	40 x 110
260	D01	467.5	-335	40 x 110
261	D01	522.5	-335	40 x 110
262	VSS1	577.5	-335	40 x 110
263	VSS1	632.5	-335	40 x 110
264	D02	687.5	-335	40 x 110
265	D02	742.5	-335	40 x 110
266	D03	797.5	-335	40 x 110
267	D03	852.5	-335	40 x 110
268	VSS1	907.5	-335	40 x 110
269	VSS1	962.5	-335	40 x 110
270	D04	1017.5	-335	40 x 110
271	D04	1072.5	-335	40 x 110
272	D05	1127.5	-335	40 x 110
273	D05	1182.5	-335	40 x 110
274	VSS1	1237.5	-335	40 x 110
275	VSS1	1292.5	-335	40 x 110
276	D06	1347.5	-335	40 x 110
277	D06	1402.5	-335	40 x 110
278	D07	1457.5	-335	40 x 110
279	D07	1512.5	-335	40 x 110
280	VSS1	1567.5	-335	40 x 110
281	VSS1	1622.5	-335	40 x 110
282	DCLK	1677.5	-335	40 x 110
283	DCLK	1732.5	-335	40 x 110
284	HS	1787.5	-335	40 x 110
285	HS	1842.5	-335	40 x 110
286	VS	1897.5	-335	40 x 110
287	VS	1952.5	-335	40 x 110
288	DE	2007.5	-335	40 x 110
289	DE	2062.5	-335	40 x 110
290	VSS1	2117.5	-335	40 x 110
291	VSS1	2172.5	-335	40 x 110
292	VSS1	2227.5	-335	40 x 110
293	VSS1	2282.5	-335	40 x 110
294	VSS1	2337.5	-335	40 x 110
295	VSS1	2392.5	-335	40 x 110
296	VDDD	2447.5	-335	40 x 110
297	VDDD	2502.5	-335	40 x 110
298	VDDD	2557.5	-335	40 x 110
299	VDDD	2612.5	-335	40 x 110
300	VDDD	2667.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
301	VDDD	2722.5	-335	40 x 110
302	VSS1	2777.5	-335	40 x 110
303	VSS1	2832.5	-335	40 x 110
304	VSS1	2887.5	-335	40 x 110
305	STBYB	2942.5	-335	40 x 110
306	RESETB	2997.5	-335	40 x 110
307	EEPEN	3052.5	-335	40 x 110
308	ECS	3107.5	-335	40 x 110
309	ECS	3162.5	-335	40 x 110
310	ECS	3217.5	-335	40 x 110
311	ESCL	3272.5	-335	40 x 110
312	ESCL	3327.5	-335	40 x 110
313	ESCL	3382.5	-335	40 x 110
314	ESDAO	3437.5	-335	40 x 110
315	ESDAO	3492.5	-335	40 x 110
316	ESDAI	3547.5	-335	40 x 110
317	DUMMY	3602.5	-335	40 x 110
318	DUMMY	3657.5	-335	40 x 110
319	VGMPHI	3712.5	-335	40 x 110
320	VGMPHI	3767.5	-335	40 x 110
321	VGMPHI	3822.5	-335	40 x 110
322	VGMPHI	3877.5	-335	40 x 110
323	VGMPLI	3932.5	-335	40 x 110
324	VGMPLI	3987.5	-335	40 x 110
325	VGMPLI	4042.5	-335	40 x 110
326	VGMPLI	4097.5	-335	40 x 110
327	DUMMY	4152.5	-335	40 x 110
328	DUMMY	4207.5	-335	40 x 110
329	DUMMY	4262.5	-335	40 x 110
330	DUMMY	4317.5	-335	40 x 110
331	VGMPHO	4372.5	-335	40 x 110
332	VGMPHO	4427.5	-335	40 x 110
333	VGMPHO	4482.5	-335	40 x 110
334	VGMPHO	4537.5	-335	40 x 110
335	VGMPLO	4592.5	-335	40 x 110
336	VGMPLO	4647.5	-335	40 x 110
337	VGMPLO	4702.5	-335	40 x 110
338	VGMPLO	4757.5	-335	40 x 110
339	VGMNHO	4812.5	-335	40 x 110
340	VGMNHO	4867.5	-335	40 x 110
341	VGMNHO	4922.5	-335	40 x 110
342	VGMNHO	4977.5	-335	40 x 110
343	VGMNLO	5032.5	-335	40 x 110
344	VGMNLO	5087.5	-335	40 x 110
345	VGMNLO	5142.5	-335	40 x 110
346	VGMNLO	5197.5	-335	40 x 110
347	DUMMY	5252.5	-335	40 x 110
348	DUMMY	5307.5	-335	40 x 110
349	TESTI2	5362.5	-335	40 x 110
350	TESTI1	5417.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
351	TESTI0	5472.5	-335	40 x 110
352	VCC1	5527.5	-335	40 x 110
353	VCC1	5582.5	-335	40 x 110
354	TEST7	5637.5	-335	40 x 110
355	TEST7	5692.5	-335	40 x 110
356	TEST6	5747.5	-335	40 x 110
357	TEST6	5802.5	-335	40 x 110
358	TEST5	5857.5	-335	40 x 110
359	TEST5	5912.5	-335	40 x 110
360	TEST4	5967.5	-335	40 x 110
361	TEST4	6022.5	-335	40 x 110
362	VSS1	6077.5	-335	40 x 110
363	VSS1	6132.5	-335	40 x 110
364	TEST3	6187.5	-335	40 x 110
365	TEST3	6242.5	-335	40 x 110
366	TEST2	6297.5	-335	40 x 110
367	TEST2	6352.5	-335	40 x 110
368	TP_SYNC2	6407.5	-335	40 x 110
369	TP_SYNC2	6462.5	-335	40 x 110
370	TP_SYNC1	6517.5	-335	40 x 110
371	TP_SYNC1	6572.5	-335	40 x 110
372	FAIL_DET	6627.5	-335	40 x 110
373	FAIL_DET	6682.5	-335	40 x 110
374	CABC_PWM	6737.5	-335	40 x 110
375	CABC_PWM	6792.5	-335	40 x 110
376	VSN	6847.5	-335	40 x 110
377	VSN	6902.5	-335	40 x 110
378	VSN	6957.5	-335	40 x 110
379	VSN	7012.5	-335	40 x 110
380	VSN	7067.5	-335	40 x 110
381	VSN	7122.5	-335	40 x 110
382	VSN	7177.5	-335	40 x 110
383	VSDN	7232.5	-335	40 x 110
384	VSDN	7287.5	-335	40 x 110
385	VSDN	7342.5	-335	40 x 110
386	VSDN	7397.5	-335	40 x 110
387	VSDN	7452.5	-335	40 x 110
388	VSDN	7507.5	-335	40 x 110
389	VSDN	7562.5	-335	40 x 110
390	VSSA	7617.5	-335	40 x 110
391	VSSA	7672.5	-335	40 x 110
392	VSSA	7727.5	-335	40 x 110
393	VSSA	7782.5	-335	40 x 110
394	VSSA	7837.5	-335	40 x 110
395	VSSA	7892.5	-335	40 x 110
396	VSSA	7947.5	-335	40 x 110
397	VSSA	8002.5	-335	40 x 110
398	VSDP	8057.5	-335	40 x 110
399	VSDP	8112.5	-335	40 x 110
400	VSDP	8167.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
401	VSDP	8222.5	-335	40 x 110
402	VSDP	8277.5	-335	40 x 110
403	VSDP	8332.5	-335	40 x 110
404	VSDP	8387.5	-335	40 x 110
405	VSP	8442.5	-335	40 x 110
406	VSP	8497.5	-335	40 x 110
407	VSP	8552.5	-335	40 x 110
408	VSP	8607.5	-335	40 x 110
409	VSP	8662.5	-335	40 x 110
410	VSP	8717.5	-335	40 x 110
411	VSP	8772.5	-335	40 x 110
412	TO3	8827.5	-335	40 x 110
413	TO2	8882.5	-335	40 x 110
414	TO1	8937.5	-335	40 x 110
415	TO0	8992.5	-335	40 x 110
416	DUMMY	9047.5	-335	40 x 110
417	VSS2	9102.5	-335	40 x 110
418	VSS2	9157.5	-335	40 x 110
419	VSS2	9212.5	-335	40 x 110
420	VSS2	9267.5	-335	40 x 110
421	VCC2	9322.5	-335	40 x 110
422	VCC2	9377.5	-335	40 x 110
423	VCC2	9432.5	-335	40 x 110
424	VCC2	9487.5	-335	40 x 110
425	VSS1	9542.5	-335	40 x 110
426	VSS1	9597.5	-335	40 x 110
427	VSS1	9652.5	-335	40 x 110
428	VSS1	9707.5	-335	40 x 110
429	VCC1	9762.5	-335	40 x 110
430	VCC1	9817.5	-335	40 x 110
431	VCC1	9872.5	-335	40 x 110
432	VCC1	9927.5	-335	40 x 110
433	TS_H	9982.5	-335	40 x 110
434	TS_L	10037.5	-335	40 x 110
435	FMT	10092.5	-335	40 x 110
436	LANE_SW	10147.5	-335	40 x 110
437	TB	10202.5	-335	40 x 110
438	RL	10257.5	-335	40 x 110
439	NB	10312.5	-335	40 x 110
440	MODE	10367.5	-335	40 x 110
441	LANE_PN	10422.5	-335	40 x 110
442	TR1	10477.5	-335	40 x 110
443	TR0	10532.5	-335	40 x 110
444	CABC_PWM_IN	10587.5	-335	40 x 110
445	PTS2	10642.5	-335	40 x 110
446	PTS1	10697.5	-335	40 x 110
447	PTS0	10752.5	-335	40 x 110
448	DUMMY	10807.5	-335	40 x 110
449	DUMMY	10862.5	-335	40 x 110
450	EXT_SDPWR	10917.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
451	ATREN	10972.5	-335	40 x 110
452	GSQ	11027.5	-335	40 x 110
453	SIDEN	11082.5	-335	40 x 110
454	SID1	11137.5	-335	40 x 110
455	SID0	11192.5	-335	40 x 110
456	FCS	11247.5	-335	40 x 110
457	GDSEL	11302.5	-335	40 x 110
458	ZZS1	11357.5	-335	40 x 110
459	ZZS0	11412.5	-335	40 x 110
460	DUMMY	11467.5	-335	40 x 110
461	DUMMY	11522.5	-335	40 x 110
462	BISTEN	11577.5	-335	40 x 110
463	GPOS1	11632.5	-335	40 x 110
464	GPOS0	11687.5	-335	40 x 110
465	RS3	11742.5	-335	40 x 110
466	RS2	11797.5	-335	40 x 110
467	RS1	11852.5	-335	40 x 110
468	RS0	11907.5	-335	40 x 110
469	INV1	11962.5	-335	40 x 110
470	INV0	12017.5	-335	40 x 110
471	EXT_PWR	12072.5	-335	40 x 110
472	VCOM	12127.5	-335	40 x 110
473	VCOM	12182.5	-335	40 x 110
474	VCOM	12237.5	-335	40 x 110
475	VCOM	12292.5	-335	40 x 110
476	VDD_OTP	12347.5	-335	40 x 110
477	VDD_OTP	12402.5	-335	40 x 110
478	VDD_OTP	12457.5	-335	40 x 110
479	VDD_OTP	12512.5	-335	40 x 110
480	VDD_OTP	12567.5	-335	40 x 110
481	THROUGH_2	12622.5	-335	40 x 110
482	THROUGH_2	12677.5	-335	40 x 110
483	VCOM_L	12732.5	-335	40 x 110
484	VCOM_L	12787.5	-335	40 x 110
485	VCOM_L	12842.5	-335	40 x 110
486	VCOM_L	12897.5	-335	40 x 110
487	DUMMY	12952.5	-335	40 x 110
488	DUMMY	13007.5	-335	40 x 110
489	VSS1	13062.5	-335	40 x 110
490	VSS1	13117.5	-335	40 x 110
491	VSS1	13172.5	-335	40 x 110
492	VSS1	13227.5	-335	40 x 110
493	VGH	13282.5	-335	40 x 110
494	VGH	13337.5	-335	40 x 110
495	VGH	13392.5	-335	40 x 110
496	VGH	13447.5	-335	40 x 110
497	DUMMY	13502.5	-335	40 x 110
498	VGL	13557.5	-335	40 x 110
499	VGL	13612.5	-335	40 x 110
500	VGL	13667.5	-335	40 x 110

No.	Name	X	Y	Bump size(μm)
501	DUMMY	13722.5	-335	40 x 110
502	DUMMY	13777.5	-335	40 x 110
503	F_POL_LI	14080	-357.5	110 x 30
504	CA_L6	14080	-302.5	110 x 30
505	CA_L5	14080	-247.5	110 x 30
506	CA_L4	14080	-192.5	110 x 30
507	GIO_L4	14080	-137.5	110 x 30
508	GIO_L3	14080	-82.5	110 x 30
509	CA3	14080	-27.5	110 x 30
510	GIO_L2	14080	27.5	110 x 30
511	CA_L2	14080	82.5	110 x 30
512	GIO_L1	14080	137.5	110 x 30
513	CA_L1	14080	192.5	110 x 30
514	GIO_L0	14080	247.5	110 x 30
515	CA_L0	14080	302.5	110 x 30
516	FCTRL_L	14080	357.5	110 x 30
517	GDETL[1]	13905	330	13 x 120
518	GDETL[1]	13891	185	13 x 120
519	VCOM_L	13877	330	13 x 120
520	VCOM_L	13863	185	13 x 120
521	GOUTL1	13849	330	13 x 120
522	GOUTL1	13835	185	13 x 120
523	GOUTL2	13821	330	13 x 120
524	GOUTL2	13807	185	13 x 120
525	GOUTL3	13793	330	13 x 120
526	GOUTL3	13779	185	13 x 120
527	GOUTL4	13765	330	13 x 120
528	GOUTL4	13751	185	13 x 120
529	GOUTL5	13737	330	13 x 120
530	GOUTL5	13723	185	13 x 120
531	GOUTL6	13709	330	13 x 120
532	GOUTL6	13695	185	13 x 120
533	GOUTL7	13681	330	13 x 120
534	GOUTL7	13667	185	13 x 120
535	GOUTL8	13653	330	13 x 120
536	GOUTL8	13639	185	13 x 120
537	VGL	13625	330	13 x 120
538	VGL	13611	185	13 x 120
539	VGL	13597	330	13 x 120
540	VGL	13583	185	13 x 120
541	VGL	13569	330	13 x 120
542	VGL	13555	185	13 x 120
543	VGL	13541	330	13 x 120
544	VGL	13527	185	13 x 120
545	VGL	13513	330	13 x 120
546	VGL	13499	185	13 x 120
547	GOUTL9	13485	330	13 x 120
548	GOUTL9	13471	185	13 x 120
549	GOUTL10	13457	330	13 x 120
550	GOUTL10	13443	185	13 x 120

No.	Name	X	Y	Bump size(μm)
551	GOUTL11	13429	330	13 x 120
552	GOUTL11	13415	185	13 x 120
553	GOUTL12	13401	330	13 x 120
554	GOUTL12	13387	185	13 x 120
555	GOUTL13	13373	330	13 x 120
556	GOUTL13	13359	185	13 x 120
557	GOUTL14	13345	330	13 x 120
558	GOUTL14	13331	185	13 x 120
559	GOUTL15	13317	330	13 x 120
560	GOUTL15	13303	185	13 x 120
561	GOUTL16	13289	330	13 x 120
562	GOUTL16	13275	185	13 x 120
563	GOUTL17	13261	330	13 x 120
564	GOUTL17	13247	185	13 x 120
565	GOUTL18	13233	330	13 x 120
566	GOUTL18	13219	185	13 x 120
567	GOUTL19	13205	330	13 x 120
568	GOUTL19	13191	185	13 x 120
569	GOUTL20	13177	330	13 x 120
570	GOUTL20	13163	185	13 x 120
571	VGH	13149	330	13 x 120
572	VGH	13135	185	13 x 120
573	VGH	13121	330	13 x 120
574	VGH	13107	185	13 x 120
575	GDETL[2]	13093	330	13 x 120
576	GDETL[2]	13079	185	13 x 120
577	VGH	13065	330	13 x 120
578	VGH	13051	185	13 x 120
579	VGH	13037	330	13 x 120
580	VGH	13023	185	13 x 120
581	SWL1	13009	330	13 x 120
582	SWL1	12995	185	13 x 120
583	SWL1B	12981	330	13 x 120
584	SWL1B	12967	185	13 x 120
585	SWL2	12953	330	13 x 120
586	SWL2	12939	185	13 x 120
587	SWL2B	12925	330	13 x 120
588	SWL2B	12911	185	13 x 120
589	SWL3	12897	330	13 x 120
590	SWL3	12883	185	13 x 120
591	SWL3B	12869	330	13 x 120
592	SWL3B	12855	185	13 x 120
593	DUMMY	12841	330	13 x 120
594	DUMMY	12827	185	13 x 120
595	DUMMY	12813	330	13 x 120
596	DUMMY	12799	185	13 x 120
597	VCOM_L	12785	330	13 x 120
598	VCOM_L	12771	185	13 x 120
599	VCOM_L	12757	330	13 x 120
600	VCOM_L	12743	185	13 x 120

No.	Name	X	Y	Bump size(μm)
601	THROUGH_4	12729	330	13 x 120
602	THROUGH_4	12715	185	13 x 120
603	DUMMY	12701	330	13 x 120
604	DUMMY	12687	185	13 x 120
605	DUMMY	12673	330	13 x 120
606	SZ	12659	185	13 x 120
607	S[1]	12645	330	13 x 120
608	S[2]	12631	185	13 x 120
609	S[3]	12617	330	13 x 120
610	S[4]	12603	185	13 x 120
611	S[5]	12589	330	13 x 120
612	S[6]	12575	185	13 x 120
613	S[7]	12561	330	13 x 120
614	S[8]	12547	185	13 x 120
615	S[9]	12533	330	13 x 120
616	S[10]	12519	185	13 x 120
617	S[11]	12504.5	330	13 x 120
618	S[12]	12490.5	185	13 x 120
619	S[13]	12476.5	330	13 x 120
620	S[14]	12462.5	185	13 x 120
621	S[15]	12448.5	330	13 x 120
622	S[16]	12434.5	185	13 x 120
623	S[17]	12420.5	330	13 x 120
624	S[18]	12406.5	185	13 x 120
625	S[19]	12392.5	330	13 x 120
626	S[20]	12378.5	185	13 x 120
627	S[21]	12364.5	330	13 x 120
628	S[22]	12350.5	185	13 x 120
629	S[23]	12336.5	330	13 x 120
630	S[24]	12322.5	185	13 x 120
631	S[25]	12308.5	330	13 x 120
632	S[26]	12294.5	185	13 x 120
633	S[27]	12280.5	330	13 x 120
634	S[28]	12266.5	185	13 x 120
635	S[29]	12252.5	330	13 x 120
636	S[30]	12238.5	185	13 x 120
637	S[31]	12224.5	330	13 x 120
638	S[32]	12210.5	185	13 x 120
639	S[33]	12196.5	330	13 x 120
640	S[34]	12182.5	185	13 x 120
641	S[35]	12168.5	330	13 x 120
642	S[36]	12154.5	185	13 x 120
643	S[37]	12140.5	330	13 x 120
644	S[38]	12126.5	185	13 x 120
645	S[39]	12112.5	330	13 x 120
646	S[40]	12098.5	185	13 x 120
647	S[41]	12084.5	330	13 x 120
648	S[42]	12070.5	185	13 x 120
649	S[43]	12056.5	330	13 x 120
650	S[44]	12042.5	185	13 x 120

No.	Name	X	Y	Bump size(μm)
651	S[45]	12028.5	330	13 x 120
652	S[46]	12014.5	185	13 x 120
653	S[47]	12000.5	330	13 x 120
654	S[48]	11986.5	185	13 x 120
655	S[49]	11972.5	330	13 x 120
656	S[50]	11958.5	185	13 x 120
657	S[51]	11944.5	330	13 x 120
658	S[52]	11930.5	185	13 x 120
659	S[53]	11916.5	330	13 x 120
660	S[54]	11902.5	185	13 x 120
661	S[55]	11888.5	330	13 x 120
662	S[56]	11874.5	185	13 x 120
663	S[57]	11860.5	330	13 x 120
664	S[58]	11846.5	185	13 x 120
665	S[59]	11832.5	330	13 x 120
666	S[60]	11818.5	185	13 x 120
667	S[61]	11804.5	330	13 x 120
668	S[62]	11790.5	185	13 x 120
669	S[63]	11776.5	330	13 x 120
670	S[64]	11762.5	185	13 x 120
671	S[65]	11748.5	330	13 x 120
672	S[66]	11734.5	185	13 x 120
673	S[67]	11720.5	330	13 x 120
674	S[68]	11706.5	185	13 x 120
675	S[69]	11692.5	330	13 x 120
676	S[70]	11678.5	185	13 x 120
677	S[71]	11664.5	330	13 x 120
678	S[72]	11650.5	185	13 x 120
679	S[73]	11636.5	330	13 x 120
680	S[74]	11622.5	185	13 x 120
681	S[75]	11608.5	330	13 x 120
682	S[76]	11594.5	185	13 x 120
683	S[77]	11580.5	330	13 x 120
684	S[78]	11566.5	185	13 x 120
685	S[79]	11552.5	330	13 x 120
686	S[80]	11538.5	185	13 x 120
687	S[81]	11524.5	330	13 x 120
688	S[82]	11510.5	185	13 x 120
689	S[83]	11496.5	330	13 x 120
690	S[84]	11482.5	185	13 x 120
691	S[85]	11468.5	330	13 x 120
692	S[86]	11454.5	185	13 x 120
693	S[87]	11440.5	330	13 x 120
694	S[88]	11426.5	185	13 x 120
695	S[89]	11412.5	330	13 x 120
696	S[90]	11398.5	185	13 x 120
697	S[91]	11384.5	330	13 x 120
698	S[92]	11370.5	185	13 x 120
699	S[93]	11356.5	330	13 x 120
700	S[94]	11342.5	185	13 x 120

No.	Name	X	Y	Bump size(μm)
701	S[95]	11328.5	330	13 x 120
702	S[96]	11314.5	185	13 x 120
703	S[97]	11300.5	330	13 x 120
704	S[98]	11286.5	185	13 x 120
705	S[99]	11272.5	330	13 x 120
706	S[100]	11258.5	185	13 x 120
707	S[101]	11244.5	330	13 x 120
708	S[102]	11230.5	185	13 x 120
709	S[103]	11216.5	330	13 x 120
710	S[104]	11202.5	185	13 x 120
711	S[105]	11188.5	330	13 x 120
712	S[106]	11174.5	185	13 x 120
713	S[107]	11160.5	330	13 x 120
714	S[108]	11146.5	185	13 x 120
715	S[109]	11132.5	330	13 x 120
716	S[110]	11118.5	185	13 x 120
717	S[111]	11104.5	330	13 x 120
718	S[112]	11090.5	185	13 x 120
719	S[113]	11076.5	330	13 x 120
720	S[114]	11062.5	185	13 x 120
721	S[115]	11048.5	330	13 x 120
722	S[116]	11034.5	185	13 x 120
723	S[117]	11020.5	330	13 x 120
724	S[118]	11006.5	185	13 x 120
725	S[119]	10992.5	330	13 x 120
726	S[120]	10978.5	185	13 x 120
727	S[121]	10964.5	330	13 x 120
728	S[122]	10950.5	185	13 x 120
729	S[123]	10936.5	330	13 x 120
730	S[124]	10922.5	185	13 x 120
731	S[125]	10908.5	330	13 x 120
732	S[126]	10894.5	185	13 x 120
733	S[127]	10880.5	330	13 x 120
734	S[128]	10866.5	185	13 x 120
735	S[129]	10852.5	330	13 x 120
736	S[130]	10838.5	185	13 x 120
737	S[131]	10824.5	330	13 x 120
738	S[132]	10810.5	185	13 x 120
739	S[133]	10796.5	330	13 x 120
740	S[134]	10782.5	185	13 x 120
741	S[135]	10768.5	330	13 x 120
742	S[136]	10754.5	185	13 x 120
743	S[137]	10740.5	330	13 x 120
744	S[138]	10726.5	185	13 x 120
745	S[139]	10712.5	330	13 x 120
746	S[140]	10698.5	185	13 x 120
747	S[141]	10684.5	330	13 x 120
748	S[142]	10670.5	185	13 x 120
749	S[143]	10656.5	330	13 x 120
750	S[144]	10642.5	185	13 x 120

No.	Name	X	Y	Bump size(μm)
751	S[145]	10628.5	330	13 x 120
752	S[146]	10614.5	185	13 x 120
753	S[147]	10600.5	330	13 x 120
754	S[148]	10586.5	185	13 x 120
755	S[149]	10572.5	330	13 x 120
756	S[150]	10558.5	185	13 x 120
757	S[151]	10544.5	330	13 x 120
758	S[152]	10530.5	185	13 x 120
759	S[153]	10516.5	330	13 x 120
760	S[154]	10502.5	185	13 x 120
761	S[155]	10488.5	330	13 x 120
762	S[156]	10474.5	185	13 x 120
763	S[157]	10460.5	330	13 x 120
764	S[158]	10446.5	185	13 x 120
765	S[159]	10432.5	330	13 x 120
766	S[160]	10418.5	185	13 x 120
767	S[161]	10404.5	330	13 x 120
768	S[162]	10390.5	185	13 x 120
769	S[163]	10376.5	330	13 x 120
770	S[164]	10362.5	185	13 x 120
771	S[165]	10348.5	330	13 x 120
772	S[166]	10334.5	185	13 x 120
773	S[167]	10320.5	330	13 x 120
774	S[168]	10306.5	185	13 x 120
775	S[169]	10292.5	330	13 x 120
776	S[170]	10278.5	185	13 x 120
777	S[171]	10264.5	330	13 x 120
778	S[172]	10250.5	185	13 x 120
779	S[173]	10236.5	330	13 x 120
780	S[174]	10222.5	185	13 x 120
781	S[175]	10208.5	330	13 x 120
782	S[176]	10194.5	185	13 x 120
783	S[177]	10180.5	330	13 x 120
784	S[178]	10166.5	185	13 x 120
785	S[179]	10152.5	330	13 x 120
786	S[180]	10138.5	185	13 x 120
787	S[181]	10124.5	330	13 x 120
788	S[182]	10110.5	185	13 x 120
789	S[183]	10096.5	330	13 x 120
790	S[184]	10082.5	185	13 x 120
791	S[185]	10068.5	330	13 x 120
792	S[186]	10054.5	185	13 x 120
793	S[187]	10040.5	330	13 x 120
794	S[188]	10026.5	185	13 x 120
795	S[189]	10012.5	330	13 x 120
796	S[190]	9998	185	13 x 120
797	S[191]	9984	330	13 x 120
798	S[192]	9970	185	13 x 120
799	S[193]	9956	330	13 x 120
800	S[194]	9942	185	13 x 120

No.	Name	X	Y	Bump size(μm)
801	S[195]	9928	330	13 x 120
802	S[196]	9914	185	13 x 120
803	S[197]	9900	330	13 x 120
804	S[198]	9886	185	13 x 120
805	S[199]	9872	330	13 x 120
806	S[200]	9858	185	13 x 120
807	S[201]	9844	330	13 x 120
808	S[202]	9830	185	13 x 120
809	S[203]	9816	330	13 x 120
810	S[204]	9802	185	13 x 120
811	S[205]	9788	330	13 x 120
812	S[206]	9774	185	13 x 120
813	S[207]	9760	330	13 x 120
814	S[208]	9746	185	13 x 120
815	S[209]	9732	330	13 x 120
816	S[210]	9718	185	13 x 120
817	S[211]	9704	330	13 x 120
818	S[212]	9690	185	13 x 120
819	S[213]	9676	330	13 x 120
820	S[214]	9662	185	13 x 120
821	S[215]	9648	330	13 x 120
822	S[216]	9634	185	13 x 120
823	S[217]	9620	330	13 x 120
824	S[218]	9606	185	13 x 120
825	S[219]	9592	330	13 x 120
826	S[220]	9578	185	13 x 120
827	S[221]	9564	330	13 x 120
828	S[222]	9550	185	13 x 120
829	S[223]	9536	330	13 x 120
830	S[224]	9522	185	13 x 120
831	S[225]	9508	330	13 x 120
832	S[226]	9494	185	13 x 120
833	S[227]	9480	330	13 x 120
834	S[228]	9466	185	13 x 120
835	S[229]	9452	330	13 x 120
836	S[230]	9438	185	13 x 120
837	S[231]	9424	330	13 x 120
838	S[232]	9410	185	13 x 120
839	S[233]	9396	330	13 x 120
840	S[234]	9382	185	13 x 120
841	S[235]	9368	330	13 x 120
842	S[236]	9354	185	13 x 120
843	S[237]	9340	330	13 x 120
844	S[238]	9326	185	13 x 120
845	S[239]	9312	330	13 x 120
846	S[240]	9298	185	13 x 120
847	S[241]	9284	330	13 x 120
848	S[242]	9270	185	13 x 120
849	S[243]	9256	330	13 x 120
850	S[244]	9242	185	13 x 120

No.	Name	X	Y	Bump size(μm)
851	S[245]	9228	330	13 x 120
852	S[246]	9214	185	13 x 120
853	S[247]	9200	330	13 x 120
854	S[248]	9186	185	13 x 120
855	S[249]	9172	330	13 x 120
856	S[250]	9158	185	13 x 120
857	S[251]	9144	330	13 x 120
858	S[252]	9130	185	13 x 120
859	S[253]	9116	330	13 x 120
860	S[254]	9102	185	13 x 120
861	S[255]	9088	330	13 x 120
862	S[256]	9074	185	13 x 120
863	S[257]	9060	330	13 x 120
864	S[258]	9046	185	13 x 120
865	S[259]	9032	330	13 x 120
866	S[260]	9018	185	13 x 120
867	S[261]	9004	330	13 x 120
868	S[262]	8990	185	13 x 120
869	S[263]	8976	330	13 x 120
870	S[264]	8962	185	13 x 120
871	S[265]	8948	330	13 x 120
872	S[266]	8934	185	13 x 120
873	S[267]	8920	330	13 x 120
874	S[268]	8906	185	13 x 120
875	S[269]	8892	330	13 x 120
876	S[270]	8878	185	13 x 120
877	S[271]	8864	330	13 x 120
878	S[272]	8850	185	13 x 120
879	S[273]	8836	330	13 x 120
880	S[274]	8822	185	13 x 120
881	S[275]	8808	330	13 x 120
882	S[276]	8794	185	13 x 120
883	S[277]	8780	330	13 x 120
884	S[278]	8766	185	13 x 120
885	S[279]	8752	330	13 x 120
886	S[280]	8738	185	13 x 120
887	S[281]	8724	330	13 x 120
888	S[282]	8710	185	13 x 120
889	S[283]	8696	330	13 x 120
890	S[284]	8682	185	13 x 120
891	S[285]	8668	330	13 x 120
892	S[286]	8654	185	13 x 120
893	S[287]	8640	330	13 x 120
894	S[288]	8626	185	13 x 120
895	S[289]	8612	330	13 x 120
896	S[290]	8598	185	13 x 120
897	S[291]	8584	330	13 x 120
898	S[292]	8570	185	13 x 120
899	S[293]	8556	330	13 x 120
900	S[294]	8542	185	13 x 120

No.	Name	X	Y	Bump size(μm)
901	S[295]	8528	330	13 x 120
902	S[296]	8514	185	13 x 120
903	S[297]	8500	330	13 x 120
904	S[298]	8486	185	13 x 120
905	S[299]	8472	330	13 x 120
906	S[300]	8458	185	13 x 120
907	S[301]	8444	330	13 x 120
908	S[302]	8430	185	13 x 120
909	S[303]	8416	330	13 x 120
910	S[304]	8402	185	13 x 120
911	S[305]	8388	330	13 x 120
912	S[306]	8374	185	13 x 120
913	S[307]	8360	330	13 x 120
914	S[308]	8346	185	13 x 120
915	S[309]	8332	330	13 x 120
916	S[310]	8318	185	13 x 120
917	S[311]	8304	330	13 x 120
918	S[312]	8290	185	13 x 120
919	S[313]	8276	330	13 x 120
920	S[314]	8262	185	13 x 120
921	S[315]	8248	330	13 x 120
922	S[316]	8234	185	13 x 120
923	S[317]	8220	330	13 x 120
924	S[318]	8206	185	13 x 120
925	S[319]	8192	330	13 x 120
926	S[320]	8178	185	13 x 120
927	S[321]	8164	330	13 x 120
928	S[322]	8150	185	13 x 120
929	S[323]	8136	330	13 x 120
930	S[324]	8122	185	13 x 120
931	S[325]	8108	330	13 x 120
932	S[326]	8094	185	13 x 120
933	S[327]	8080	330	13 x 120
934	S[328]	8066	185	13 x 120
935	S[329]	8052	330	13 x 120
936	S[330]	8038	185	13 x 120
937	S[331]	8024	330	13 x 120
938	S[332]	8010	185	13 x 120
939	S[333]	7996	330	13 x 120
940	S[334]	7982	185	13 x 120
941	S[335]	7968	330	13 x 120
942	S[336]	7954	185	13 x 120
943	S[337]	7940	330	13 x 120
944	S[338]	7926	185	13 x 120
945	S[339]	7912	330	13 x 120
946	S[340]	7898	185	13 x 120
947	S[341]	7884	330	13 x 120
948	S[342]	7870	185	13 x 120
949	S[343]	7856	330	13 x 120
950	S[344]	7842	185	13 x 120

No.	Name	X	Y	Bump size(μm)
951	S[345]	7828	330	13 x 120
952	S[346]	7814	185	13 x 120
953	S[347]	7800	330	13 x 120
954	S[348]	7786	185	13 x 120
955	S[349]	7772	330	13 x 120
956	S[350]	7758	185	13 x 120
957	S[351]	7744	330	13 x 120
958	S[352]	7730	185	13 x 120
959	S[353]	7716	330	13 x 120
960	S[354]	7702	185	13 x 120
961	S[355]	7688	330	13 x 120
962	S[356]	7674	185	13 x 120
963	S[357]	7660	330	13 x 120
964	S[358]	7646	185	13 x 120
965	S[359]	7632	330	13 x 120
966	S[360]	7618	185	13 x 120
967	S[361]	7604	330	13 x 120
968	S[362]	7590	185	13 x 120
969	S[363]	7576	330	13 x 120
970	S[364]	7562	185	13 x 120
971	S[365]	7548	330	13 x 120
972	S[366]	7534	185	13 x 120
973	S[367]	7520	330	13 x 120
974	S[368]	7505.5	185	13 x 120
975	S[369]	7491.5	330	13 x 120
976	S[370]	7477.5	185	13 x 120
977	S[371]	7463.5	330	13 x 120
978	S[372]	7449.5	185	13 x 120
979	S[373]	7435.5	330	13 x 120
980	S[374]	7421.5	185	13 x 120
981	S[375]	7407.5	330	13 x 120
982	S[376]	7393.5	185	13 x 120
983	S[377]	7379.5	330	13 x 120
984	S[378]	7365.5	185	13 x 120
985	S[379]	7351.5	330	13 x 120
986	S[380]	7337.5	185	13 x 120
987	S[381]	7323.5	330	13 x 120
988	S[382]	7309.5	185	13 x 120
989	S[383]	7295.5	330	13 x 120
990	S[384]	7281.5	185	13 x 120
991	S[385]	7267.5	330	13 x 120
992	S[386]	7253.5	185	13 x 120
993	S[387]	7239.5	330	13 x 120
994	S[388]	7225.5	185	13 x 120
995	S[389]	7211.5	330	13 x 120
996	S[390]	7197.5	185	13 x 120
997	S[391]	7183.5	330	13 x 120
998	S[392]	7169.5	185	13 x 120
999	S[393]	7155.5	330	13 x 120
1000	S[394]	7141.5	185	13 x 120

No.	Name	X	Y	Bump size(μm)
1001	S[395]	7127.5	330	13 x 120
1002	S[396]	7113.5	185	13 x 120
1003	S[397]	7099.5	330	13 x 120
1004	S[398]	7085.5	185	13 x 120
1005	S[399]	7071.5	330	13 x 120
1006	S[400]	7057.5	185	13 x 120
1007	S[401]	7043.5	330	13 x 120
1008	S[402]	7029.5	185	13 x 120
1009	S[403]	7015.5	330	13 x 120
1010	S[404]	7001.5	185	13 x 120
1011	S[405]	6987.5	330	13 x 120
1012	S[406]	6973.5	185	13 x 120
1013	S[407]	6959.5	330	13 x 120
1014	S[408]	6945.5	185	13 x 120
1015	S[409]	6931.5	330	13 x 120
1016	S[410]	6917.5	185	13 x 120
1017	S[411]	6903.5	330	13 x 120
1018	S[412]	6889.5	185	13 x 120
1019	S[413]	6875.5	330	13 x 120
1020	S[414]	6861.5	185	13 x 120
1021	S[415]	6847.5	330	13 x 120
1022	S[416]	6833.5	185	13 x 120
1023	S[417]	6819.5	330	13 x 120
1024	S[418]	6805.5	185	13 x 120
1025	S[419]	6791.5	330	13 x 120
1026	S[420]	6777.5	185	13 x 120
1027	S[421]	6763.5	330	13 x 120
1028	S[422]	6749.5	185	13 x 120
1029	S[423]	6735.5	330	13 x 120
1030	S[424]	6721.5	185	13 x 120
1031	S[425]	6707.5	330	13 x 120
1032	S[426]	6693.5	185	13 x 120
1033	S[427]	6679.5	330	13 x 120
1034	S[428]	6665.5	185	13 x 120
1035	S[429]	6651.5	330	13 x 120
1036	S[430]	6637.5	185	13 x 120
1037	S[431]	6623.5	330	13 x 120
1038	S[432]	6609.5	185	13 x 120
1039	S[433]	6595.5	330	13 x 120
1040	S[434]	6581.5	185	13 x 120
1041	S[435]	6567.5	330	13 x 120
1042	S[436]	6553.5	185	13 x 120
1043	S[437]	6539.5	330	13 x 120
1044	S[438]	6525.5	185	13 x 120
1045	S[439]	6511.5	330	13 x 120
1046	S[440]	6497.5	185	13 x 120
1047	S[441]	6483.5	330	13 x 120
1048	S[442]	6469.5	185	13 x 120
1049	S[443]	6455.5	330	13 x 120
1050	S[444]	6441.5	185	13 x 120

No.	Name	X	Y	Bump size(μm)
1051	S[445]	6427.5	330	13 x 120
1052	S[446]	6413.5	185	13 x 120
1053	S[447]	6399.5	330	13 x 120
1054	S[448]	6385.5	185	13 x 120
1055	S[449]	6371.5	330	13 x 120
1056	S[450]	6357.5	185	13 x 120
1057	S[451]	6343.5	330	13 x 120
1058	S[452]	6329.5	185	13 x 120
1059	S[453]	6315.5	330	13 x 120
1060	S[454]	6301.5	185	13 x 120
1061	S[455]	6287.5	330	13 x 120
1062	S[456]	6273.5	185	13 x 120
1063	S[457]	6259.5	330	13 x 120
1064	S[458]	6245.5	185	13 x 120
1065	S[459]	6231.5	330	13 x 120
1066	S[460]	6217.5	185	13 x 120
1067	S[461]	6203.5	330	13 x 120
1068	S[462]	6189.5	185	13 x 120
1069	S[463]	6175.5	330	13 x 120
1070	S[464]	6161.5	185	13 x 120
1071	S[465]	6147.5	330	13 x 120
1072	S[466]	6133.5	185	13 x 120
1073	S[467]	6119.5	330	13 x 120
1074	S[468]	6105.5	185	13 x 120
1075	S[469]	6091.5	330	13 x 120
1076	S[470]	6077.5	185	13 x 120
1077	S[471]	6063.5	330	13 x 120
1078	S[472]	6049.5	185	13 x 120
1079	S[473]	6035.5	330	13 x 120
1080	S[474]	6021.5	185	13 x 120
1081	S[475]	6007.5	330	13 x 120
1082	S[476]	5993.5	185	13 x 120
1083	S[477]	5979.5	330	13 x 120
1084	S[478]	5965.5	185	13 x 120
1085	S[479]	5951.5	330	13 x 120
1086	S[480]	5937.5	185	13 x 120
1087	S[481]	5923.5	330	13 x 120
1088	S[482]	5909.5	185	13 x 120
1089	S[483]	5895.5	330	13 x 120
1090	S[484]	5881.5	185	13 x 120
1091	S[485]	5867.5	330	13 x 120
1092	S[486]	5853.5	185	13 x 120
1093	S[487]	5839.5	330	13 x 120
1094	S[488]	5825.5	185	13 x 120
1095	S[489]	5811.5	330	13 x 120
1096	S[490]	5797.5	185	13 x 120
1097	S[491]	5783.5	330	13 x 120
1098	S[492]	5769.5	185	13 x 120
1099	S[493]	5755.5	330	13 x 120
1100	S[494]	5741.5	185	13 x 120

No.	Name	X	Y	Bump size(μm)
1101	S[495]	5727.5	330	13 x 120
1102	S[496]	5713.5	185	13 x 120
1103	S[497]	5699.5	330	13 x 120
1104	S[498]	5685.5	185	13 x 120
1105	S[499]	5671.5	330	13 x 120
1106	S[500]	5657.5	185	13 x 120
1107	S[501]	5643.5	330	13 x 120
1108	S[502]	5629.5	185	13 x 120
1109	S[503]	5615.5	330	13 x 120
1110	S[504]	5601.5	185	13 x 120
1111	S[505]	5587.5	330	13 x 120
1112	S[506]	5573.5	185	13 x 120
1113	S[507]	5559.5	330	13 x 120
1114	S[508]	5545.5	185	13 x 120
1115	S[509]	5531.5	330	13 x 120
1116	S[510]	5517.5	185	13 x 120
1117	S[511]	5503.5	330	13 x 120
1118	S[512]	5489.5	185	13 x 120
1119	S[513]	5475.5	330	13 x 120
1120	S[514]	5461.5	185	13 x 120
1121	S[515]	5447.5	330	13 x 120
1122	S[516]	5433.5	185	13 x 120
1123	S[517]	5419.5	330	13 x 120
1124	S[518]	5405.5	185	13 x 120
1125	S[519]	5391.5	330	13 x 120
1126	S[520]	5377.5	185	13 x 120
1127	S[521]	5363.5	330	13 x 120
1128	S[522]	5349.5	185	13 x 120
1129	S[523]	5335.5	330	13 x 120
1130	S[524]	5321.5	185	13 x 120
1131	S[525]	5307.5	330	13 x 120
1132	S[526]	5293.5	185	13 x 120
1133	S[527]	5279.5	330	13 x 120
1134	S[528]	5265.5	185	13 x 120
1135	S[529]	5251.5	330	13 x 120
1136	S[530]	5237.5	185	13 x 120
1137	S[531]	5223.5	330	13 x 120
1138	S[532]	5209.5	185	13 x 120
1139	S[533]	5195.5	330	13 x 120
1140	S[534]	5181.5	185	13 x 120
1141	S[535]	5167.5	330	13 x 120
1142	S[536]	5153.5	185	13 x 120
1143	S[537]	5139.5	330	13 x 120
1144	S[538]	5125.5	185	13 x 120
1145	S[539]	5111.5	330	13 x 120
1146	S[540]	5097.5	185	13 x 120
1147	S[541]	5083.5	330	13 x 120
1148	S[542]	5069.5	185	13 x 120
1149	S[543]	5055.5	330	13 x 120
1150	S[544]	5041.5	185	13 x 120

No.	Name	X	Y	Bump size(μm)
1151	S[545]	5027.5	330	13 x 120
1152	S[546]	5013.5	185	13 x 120
1153	S[547]	4999	330	13 x 120
1154	S[548]	4985	185	13 x 120
1155	S[549]	4971	330	13 x 120
1156	S[550]	4957	185	13 x 120
1157	S[551]	4943	330	13 x 120
1158	S[552]	4929	185	13 x 120
1159	S[553]	4915	330	13 x 120
1160	S[554]	4901	185	13 x 120
1161	S[555]	4887	330	13 x 120
1162	S[556]	4873	185	13 x 120
1163	S[557]	4859	330	13 x 120
1164	S[558]	4845	185	13 x 120
1165	S[559]	4831	330	13 x 120
1166	S[560]	4817	185	13 x 120
1167	S[561]	4803	330	13 x 120
1168	S[562]	4789	185	13 x 120
1169	S[563]	4775	330	13 x 120
1170	S[564]	4761	185	13 x 120
1171	S[565]	4747	330	13 x 120
1172	S[566]	4733	185	13 x 120
1173	S[567]	4719	330	13 x 120
1174	S[568]	4705	185	13 x 120
1175	S[569]	4691	330	13 x 120
1176	S[570]	4677	185	13 x 120
1177	S[571]	4663	330	13 x 120
1178	S[572]	4649	185	13 x 120
1179	S[573]	4635	330	13 x 120
1180	S[574]	4621	185	13 x 120
1181	S[575]	4607	330	13 x 120
1182	S[576]	4593	185	13 x 120
1183	S[577]	4579	330	13 x 120
1184	S[578]	4565	185	13 x 120
1185	S[579]	4551	330	13 x 120
1186	S[580]	4537	185	13 x 120
1187	S[581]	4523	330	13 x 120
1188	S[582]	4509	185	13 x 120
1189	S[583]	4495	330	13 x 120
1190	S[584]	4481	185	13 x 120
1191	S[585]	4467	330	13 x 120
1192	S[586]	4453	185	13 x 120
1193	S[587]	4439	330	13 x 120
1194	S[588]	4425	185	13 x 120
1195	S[589]	4411	330	13 x 120
1196	S[590]	4397	185	13 x 120
1197	S[591]	4383	330	13 x 120
1198	S[592]	4369	185	13 x 120
1199	S[593]	4355	330	13 x 120
1200	S[594]	4341	185	13 x 120

No.	Name	X	Y	Bump size(μm)
1201	S[595]	4327	330	13 x 120
1202	S[596]	4313	185	13 x 120
1203	S[597]	4299	330	13 x 120
1204	S[598]	4285	185	13 x 120
1205	S[599]	4271	330	13 x 120
1206	S[600]	4257	185	13 x 120
1207	S[601]	4243	330	13 x 120
1208	S[602]	4229	185	13 x 120
1209	S[603]	4215	330	13 x 120
1210	S[604]	4201	185	13 x 120
1211	S[605]	4187	330	13 x 120
1212	S[606]	4173	185	13 x 120
1213	S[607]	4159	330	13 x 120
1214	S[608]	4145	185	13 x 120
1215	S[609]	4131	330	13 x 120
1216	S[610]	4117	185	13 x 120
1217	S[611]	4103	330	13 x 120
1218	S[612]	4089	185	13 x 120
1219	S[613]	4075	330	13 x 120
1220	S[614]	4061	185	13 x 120
1221	S[615]	4047	330	13 x 120
1222	S[616]	4033	185	13 x 120
1223	S[617]	4019	330	13 x 120
1224	S[618]	4005	185	13 x 120
1225	S[619]	3991	330	13 x 120
1226	S[620]	3977	185	13 x 120
1227	S[621]	3963	330	13 x 120
1228	S[622]	3949	185	13 x 120
1229	S[623]	3935	330	13 x 120
1230	S[624]	3921	185	13 x 120
1231	S[625]	3907	330	13 x 120
1232	S[626]	3893	185	13 x 120
1233	S[627]	3879	330	13 x 120
1234	S[628]	3865	185	13 x 120
1235	S[629]	3851	330	13 x 120
1236	S[630]	3837	185	13 x 120
1237	S[631]	3823	330	13 x 120
1238	S[632]	3809	185	13 x 120
1239	S[633]	3795	330	13 x 120
1240	S[634]	3781	185	13 x 120
1241	S[635]	3767	330	13 x 120
1242	S[636]	3753	185	13 x 120
1243	S[637]	3739	330	13 x 120
1244	S[638]	3725	185	13 x 120
1245	S[639]	3711	330	13 x 120
1246	S[640]	3697	185	13 x 120
1247	S[641]	3683	330	13 x 120
1248	S[642]	3669	185	13 x 120
1249	S[643]	3655	330	13 x 120
1250	S[644]	3641	185	13 x 120

No.	Name	X	Y	Bump size(μm)
1251	S[645]	3627	330	13 x 120
1252	S[646]	3613	185	13 x 120
1253	S[647]	3599	330	13 x 120
1254	S[648]	3585	185	13 x 120
1255	S[649]	3571	330	13 x 120
1256	S[650]	3557	185	13 x 120
1257	S[651]	3543	330	13 x 120
1258	S[652]	3529	185	13 x 120
1259	S[653]	3515	330	13 x 120
1260	S[654]	3501	185	13 x 120
1261	S[655]	3487	330	13 x 120
1262	S[656]	3473	185	13 x 120
1263	S[657]	3459	330	13 x 120
1264	S[658]	3445	185	13 x 120
1265	S[659]	3431	330	13 x 120
1266	S[660]	3417	185	13 x 120
1267	S[661]	3403	330	13 x 120
1268	S[662]	3389	185	13 x 120
1269	S[663]	3375	330	13 x 120
1270	S[664]	3361	185	13 x 120
1271	S[665]	3347	330	13 x 120
1272	S[666]	3333	185	13 x 120
1273	S[667]	3319	330	13 x 120
1274	S[668]	3305	185	13 x 120
1275	S[669]	3291	330	13 x 120
1276	S[670]	3277	185	13 x 120
1277	S[671]	3263	330	13 x 120
1278	S[672]	3249	185	13 x 120
1279	S[673]	3235	330	13 x 120
1280	S[674]	3221	185	13 x 120
1281	S[675]	3207	330	13 x 120
1282	S[676]	3193	185	13 x 120
1283	S[677]	3179	330	13 x 120
1284	S[678]	3165	185	13 x 120
1285	S[679]	3151	330	13 x 120
1286	S[680]	3137	185	13 x 120
1287	S[681]	3123	330	13 x 120
1288	S[682]	3109	185	13 x 120
1289	S[683]	3095	330	13 x 120
1290	S[684]	3081	185	13 x 120
1291	S[685]	3067	330	13 x 120
1292	S[686]	3053	185	13 x 120
1293	S[687]	3039	330	13 x 120
1294	S[688]	3025	185	13 x 120
1295	S[689]	3011	330	13 x 120
1296	S[690]	2997	185	13 x 120
1297	S[691]	2983	330	13 x 120
1298	S[692]	2969	185	13 x 120
1299	S[693]	2955	330	13 x 120
1300	S[694]	2941	185	13 x 120

No.	Name	X	Y	Bump size(μm)
1301	S[695]	2927	330	13 x 120
1302	S[696]	2913	185	13 x 120
1303	S[697]	2899	330	13 x 120
1304	S[698]	2885	185	13 x 120
1305	S[699]	2871	330	13 x 120
1306	S[700]	2857	185	13 x 120
1307	S[701]	2843	330	13 x 120
1308	S[702]	2829	185	13 x 120
1309	S[703]	2815	330	13 x 120
1310	S[704]	2801	185	13 x 120
1311	S[705]	2787	330	13 x 120
1312	S[706]	2773	185	13 x 120
1313	S[707]	2759	330	13 x 120
1314	S[708]	2745	185	13 x 120
1315	S[709]	2731	330	13 x 120
1316	S[710]	2717	185	13 x 120
1317	S[711]	2703	330	13 x 120
1318	S[712]	2689	185	13 x 120
1319	S[713]	2675	330	13 x 120
1320	S[714]	2661	185	13 x 120
1321	S[715]	2647	330	13 x 120
1322	S[716]	2633	185	13 x 120
1323	S[717]	2619	330	13 x 120
1324	S[718]	2605	185	13 x 120
1325	S[719]	2591	330	13 x 120
1326	S[720]	2577	185	13 x 120
1327	DUMMY	2563	330	13 x 120
1328	DUMMY	2535	330	13 x 120
1329	DUMMY	2506.5	330	13 x 120
1330	DUMMY	2478.5	330	13 x 120
1331	DUMMY	2450.5	330	13 x 120
1332	DUMMY	2422.5	330	13 x 120
1333	DUMMY	2394.5	330	13 x 120
1334	DUMMY	2366.5	330	13 x 120
1335	DUMMY	2338.5	330	13 x 120
1336	DUMMY	2310.5	330	13 x 120
1337	DUMMY	2282.5	330	13 x 120
1338	DUMMY	2254.5	330	13 x 120
1339	DUMMY	2226.5	330	13 x 120
1340	DUMMY	2198.5	330	13 x 120
1341	DUMMY	2170.5	330	13 x 120
1342	DUMMY	2142.5	330	13 x 120
1343	DUMMY	2114.5	330	13 x 120
1344	DUMMY	2086.5	330	13 x 120
1345	DUMMY	2058.5	330	13 x 120
1346	DUMMY	2030.5	330	13 x 120
1347	DUMMY	2002.5	330	13 x 120
1348	DUMMY	1974.5	330	13 x 120
1349	DUMMY	1946.5	330	13 x 120
1350	DUMMY	1918.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1351	DUMMY	1890.5	330	13 x 120
1352	DUMMY	1862.5	330	13 x 120
1353	DUMMY	1834.5	330	13 x 120
1354	DUMMY	1806.5	330	13 x 120
1355	DUMMY	1778.5	330	13 x 120
1356	DUMMY	1750.5	330	13 x 120
1357	DUMMY	1722.5	330	13 x 120
1358	DUMMY	1694.5	330	13 x 120
1359	DUMMY	1666.5	330	13 x 120
1360	DUMMY	1638.5	330	13 x 120
1361	DUMMY	1610.5	330	13 x 120
1362	DUMMY	1582.5	330	13 x 120
1363	DUMMY	1554.5	330	13 x 120
1364	DUMMY	1526.5	330	13 x 120
1365	DUMMY	1498.5	330	13 x 120
1366	DUMMY	1470.5	330	13 x 120
1367	DUMMY	1442.5	330	13 x 120
1368	DUMMY	1414.5	330	13 x 120
1369	DUMMY	1386.5	330	13 x 120
1370	DUMMY	1358.5	330	13 x 120
1371	DUMMY	1330.5	330	13 x 120
1372	DUMMY	1302.5	330	13 x 120
1373	DUMMY	1274.5	330	13 x 120
1374	DUMMY	1246.5	330	13 x 120
1375	DUMMY	1218.5	330	13 x 120
1376	DUMMY	1190.5	330	13 x 120
1377	DUMMY	1162.5	330	13 x 120
1378	DUMMY	1134.5	330	13 x 120
1379	DUMMY	1106.5	330	13 x 120
1380	DUMMY	1078.5	330	13 x 120
1381	DUMMY	1050.5	330	13 x 120
1382	DUMMY	1022.5	330	13 x 120
1383	DUMMY	994.5	330	13 x 120
1384	DUMMY	966.5	330	13 x 120
1385	DUMMY	938.5	330	13 x 120
1386	DUMMY	910.5	330	13 x 120
1387	DUMMY	882.5	330	13 x 120
1388	DUMMY	854.5	330	13 x 120
1389	DUMMY	826.5	330	13 x 120
1390	DUMMY	798.5	330	13 x 120
1391	DUMMY	770.5	330	13 x 120
1392	DUMMY	742.5	330	13 x 120
1393	DUMMY	714.5	330	13 x 120
1394	DUMMY	686.5	330	13 x 120
1395	DUMMY	658.5	330	13 x 120
1396	DUMMY	630.5	330	13 x 120
1397	DUMMY	602.5	330	13 x 120
1398	DUMMY	574.5	330	13 x 120
1399	DUMMY	546.5	330	13 x 120
1400	DUMMY	518.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1401	DUMMY	490.5	330	13 x 120
1402	DUMMY	462.5	330	13 x 120
1403	DUMMY	434.5	330	13 x 120
1404	DUMMY	406.5	330	13 x 120
1405	DUMMY	378.5	330	13 x 120
1406	DUMMY	350.5	330	13 x 120
1407	DUMMY	322.5	330	13 x 120
1408	DUMMY	294.5	330	13 x 120
1409	DUMMY	266.5	330	13 x 120
1410	DUMMY	238.5	330	13 x 120
1411	DUMMY	210.5	330	13 x 120
1412	DUMMY	182.5	330	13 x 120
1413	DUMMY	154.5	330	13 x 120
1414	DUMMY	126.5	330	13 x 120
1415	DUMMY	98.5	330	13 x 120
1416	DUMMY	70.5	330	13 x 120
1417	DUMMY	42.5	330	13 x 120
1418	DUMMY	14.5	330	13 x 120
1419	DUMMY	-14.5	330	13 x 120
1420	DUMMY	-42.5	330	13 x 120
1421	DUMMY	-70.5	330	13 x 120
1422	DUMMY	-98.5	330	13 x 120
1423	DUMMY	-126.5	330	13 x 120
1424	DUMMY	-154.5	330	13 x 120
1425	DUMMY	-182.5	330	13 x 120
1426	DUMMY	-210.5	330	13 x 120
1427	DUMMY	-238.5	330	13 x 120
1428	DUMMY	-266.5	330	13 x 120
1429	DUMMY	-294.5	330	13 x 120
1430	DUMMY	-322.5	330	13 x 120
1431	DUMMY	-350.5	330	13 x 120
1432	DUMMY	-378.5	330	13 x 120
1433	DUMMY	-406.5	330	13 x 120
1434	DUMMY	-434.5	330	13 x 120
1435	DUMMY	-462.5	330	13 x 120
1436	DUMMY	-490.5	330	13 x 120
1437	DUMMY	-518.5	330	13 x 120
1438	DUMMY	-546.5	330	13 x 120
1439	DUMMY	-574.5	330	13 x 120
1440	DUMMY	-602.5	330	13 x 120
1441	DUMMY	-630.5	330	13 x 120
1442	DUMMY	-658.5	330	13 x 120
1443	DUMMY	-686.5	330	13 x 120
1444	DUMMY	-714.5	330	13 x 120
1445	DUMMY	-742.5	330	13 x 120
1446	DUMMY	-770.5	330	13 x 120
1447	DUMMY	-798.5	330	13 x 120
1448	DUMMY	-826.5	330	13 x 120
1449	DUMMY	-854.5	330	13 x 120
1450	DUMMY	-882.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1451	DUMMY	-910.5	330	13 x 120
1452	DUMMY	-938.5	330	13 x 120
1453	DUMMY	-966.5	330	13 x 120
1454	DUMMY	-994.5	330	13 x 120
1455	DUMMY	-1022.5	330	13 x 120
1456	DUMMY	-1050.5	330	13 x 120
1457	DUMMY	-1078.5	330	13 x 120
1458	DUMMY	-1106.5	330	13 x 120
1459	DUMMY	-1134.5	330	13 x 120
1460	DUMMY	-1162.5	330	13 x 120
1461	DUMMY	-1190.5	330	13 x 120
1462	DUMMY	-1218.5	330	13 x 120
1463	DUMMY	-1246.5	330	13 x 120
1464	DUMMY	-1274.5	330	13 x 120
1465	DUMMY	-1302.5	330	13 x 120
1466	DUMMY	-1330.5	330	13 x 120
1467	DUMMY	-1358.5	330	13 x 120
1468	DUMMY	-1386.5	330	13 x 120
1469	DUMMY	-1414.5	330	13 x 120
1470	DUMMY	-1442.5	330	13 x 120
1471	DUMMY	-1470.5	330	13 x 120
1472	DUMMY	-1498.5	330	13 x 120
1473	DUMMY	-1526.5	330	13 x 120
1474	DUMMY	-1554.5	330	13 x 120
1475	DUMMY	-1582.5	330	13 x 120
1476	DUMMY	-1610.5	330	13 x 120
1477	DUMMY	-1638.5	330	13 x 120
1478	DUMMY	-1666.5	330	13 x 120
1479	DUMMY	-1694.5	330	13 x 120
1480	DUMMY	-1722.5	330	13 x 120
1481	DUMMY	-1750.5	330	13 x 120
1482	DUMMY	-1778.5	330	13 x 120
1483	DUMMY	-1806.5	330	13 x 120
1484	DUMMY	-1834.5	330	13 x 120
1485	DUMMY	-1862.5	330	13 x 120
1486	DUMMY	-1890.5	330	13 x 120
1487	DUMMY	-1918.5	330	13 x 120
1488	DUMMY	-1946.5	330	13 x 120
1489	DUMMY	-1974.5	330	13 x 120
1490	DUMMY	-2002.5	330	13 x 120
1491	DUMMY	-2030.5	330	13 x 120
1492	DUMMY	-2058.5	330	13 x 120
1493	DUMMY	-2086.5	330	13 x 120
1494	DUMMY	-2114.5	330	13 x 120
1495	DUMMY	-2142.5	330	13 x 120
1496	DUMMY	-2170.5	330	13 x 120
1497	DUMMY	-2198.5	330	13 x 120
1498	DUMMY	-2226.5	330	13 x 120
1499	DUMMY	-2254.5	330	13 x 120
1500	DUMMY	-2282.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1501	DUMMY	-2310.5	330	13 x 120
1502	DUMMY	-2338.5	330	13 x 120
1503	DUMMY	-2366.5	330	13 x 120
1504	DUMMY	-2394.5	330	13 x 120
1505	DUMMY	-2422.5	330	13 x 120
1506	DUMMY	-2450.5	330	13 x 120
1507	DUMMY	-2478.5	330	13 x 120
1508	DUMMY	-2506.5	330	13 x 120
1509	DUMMY	-2535	330	13 x 120
1510	DUMMY	-2563	330	13 x 120
1511	S[721]	-2577	185	13 x 120
1512	S[722]	-2591	330	13 x 120
1513	S[723]	-2605	185	13 x 120
1514	S[724]	-2619	330	13 x 120
1515	S[725]	-2633	185	13 x 120
1516	S[726]	-2647	330	13 x 120
1517	S[727]	-2661	185	13 x 120
1518	S[728]	-2675	330	13 x 120
1519	S[729]	-2689	185	13 x 120
1520	S[730]	-2703	330	13 x 120
1521	S[731]	-2717	185	13 x 120
1522	S[732]	-2731	330	13 x 120
1523	S[733]	-2745	185	13 x 120
1524	S[734]	-2759	330	13 x 120
1525	S[735]	-2773	185	13 x 120
1526	S[736]	-2787	330	13 x 120
1527	S[737]	-2801	185	13 x 120
1528	S[738]	-2815	330	13 x 120
1529	S[739]	-2829	185	13 x 120
1530	S[740]	-2843	330	13 x 120
1531	S[741]	-2857	185	13 x 120
1532	S[742]	-2871	330	13 x 120
1533	S[743]	-2885	185	13 x 120
1534	S[744]	-2899	330	13 x 120
1535	S[745]	-2913	185	13 x 120
1536	S[746]	-2927	330	13 x 120
1537	S[747]	-2941	185	13 x 120
1538	S[748]	-2955	330	13 x 120
1539	S[749]	-2969	185	13 x 120
1540	S[750]	-2983	330	13 x 120
1541	S[751]	-2997	185	13 x 120
1542	S[752]	-3011	330	13 x 120
1543	S[753]	-3025	185	13 x 120
1544	S[754]	-3039	330	13 x 120
1545	S[755]	-3053	185	13 x 120
1546	S[756]	-3067	330	13 x 120
1547	S[757]	-3081	185	13 x 120
1548	S[758]	-3095	330	13 x 120
1549	S[759]	-3109	185	13 x 120
1550	S[760]	-3123	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1551	S[761]	-3137	185	13 x 120
1552	S[762]	-3151	330	13 x 120
1553	S[763]	-3165	185	13 x 120
1554	S[764]	-3179	330	13 x 120
1555	S[765]	-3193	185	13 x 120
1556	S[766]	-3207	330	13 x 120
1557	S[767]	-3221	185	13 x 120
1558	S[768]	-3235	330	13 x 120
1559	S[769]	-3249	185	13 x 120
1560	S[770]	-3263	330	13 x 120
1561	S[771]	-3277	185	13 x 120
1562	S[772]	-3291	330	13 x 120
1563	S[773]	-3305	185	13 x 120
1564	S[774]	-3319	330	13 x 120
1565	S[775]	-3333	185	13 x 120
1566	S[776]	-3347	330	13 x 120
1567	S[777]	-3361	185	13 x 120
1568	S[778]	-3375	330	13 x 120
1569	S[779]	-3389	185	13 x 120
1570	S[780]	-3403	330	13 x 120
1571	S[781]	-3417	185	13 x 120
1572	S[782]	-3431	330	13 x 120
1573	S[783]	-3445	185	13 x 120
1574	S[784]	-3459	330	13 x 120
1575	S[785]	-3473	185	13 x 120
1576	S[786]	-3487	330	13 x 120
1577	S[787]	-3501	185	13 x 120
1578	S[788]	-3515	330	13 x 120
1579	S[789]	-3529	185	13 x 120
1580	S[790]	-3543	330	13 x 120
1581	S[791]	-3557	185	13 x 120
1582	S[792]	-3571	330	13 x 120
1583	S[793]	-3585	185	13 x 120
1584	S[794]	-3599	330	13 x 120
1585	S[795]	-3613	185	13 x 120
1586	S[796]	-3627	330	13 x 120
1587	S[797]	-3641	185	13 x 120
1588	S[798]	-3655	330	13 x 120
1589	S[799]	-3669	185	13 x 120
1590	S[800]	-3683	330	13 x 120
1591	S[801]	-3697	185	13 x 120
1592	S[802]	-3711	330	13 x 120
1593	S[803]	-3725	185	13 x 120
1594	S[804]	-3739	330	13 x 120
1595	S[805]	-3753	185	13 x 120
1596	S[806]	-3767	330	13 x 120
1597	S[807]	-3781	185	13 x 120
1598	S[808]	-3795	330	13 x 120
1599	S[809]	-3809	185	13 x 120
1600	S[810]	-3823	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1601	S[811]	-3837	185	13 x 120
1602	S[812]	-3851	330	13 x 120
1603	S[813]	-3865	185	13 x 120
1604	S[814]	-3879	330	13 x 120
1605	S[815]	-3893	185	13 x 120
1606	S[816]	-3907	330	13 x 120
1607	S[817]	-3921	185	13 x 120
1608	S[818]	-3935	330	13 x 120
1609	S[819]	-3949	185	13 x 120
1610	S[820]	-3963	330	13 x 120
1611	S[821]	-3977	185	13 x 120
1612	S[822]	-3991	330	13 x 120
1613	S[823]	-4005	185	13 x 120
1614	S[824]	-4019	330	13 x 120
1615	S[825]	-4033	185	13 x 120
1616	S[826]	-4047	330	13 x 120
1617	S[827]	-4061	185	13 x 120
1618	S[828]	-4075	330	13 x 120
1619	S[829]	-4089	185	13 x 120
1620	S[830]	-4103	330	13 x 120
1621	S[831]	-4117	185	13 x 120
1622	S[832]	-4131	330	13 x 120
1623	S[833]	-4145	185	13 x 120
1624	S[834]	-4159	330	13 x 120
1625	S[835]	-4173	185	13 x 120
1626	S[836]	-4187	330	13 x 120
1627	S[837]	-4201	185	13 x 120
1628	S[838]	-4215	330	13 x 120
1629	S[839]	-4229	185	13 x 120
1630	S[840]	-4243	330	13 x 120
1631	S[841]	-4257	185	13 x 120
1632	S[842]	-4271	330	13 x 120
1633	S[843]	-4285	185	13 x 120
1634	S[844]	-4299	330	13 x 120
1635	S[845]	-4313	185	13 x 120
1636	S[846]	-4327	330	13 x 120
1637	S[847]	-4341	185	13 x 120
1638	S[848]	-4355	330	13 x 120
1639	S[849]	-4369	185	13 x 120
1640	S[850]	-4383	330	13 x 120
1641	S[851]	-4397	185	13 x 120
1642	S[852]	-4411	330	13 x 120
1643	S[853]	-4425	185	13 x 120
1644	S[854]	-4439	330	13 x 120
1645	S[855]	-4453	185	13 x 120
1646	S[856]	-4467	330	13 x 120
1647	S[857]	-4481	185	13 x 120
1648	S[858]	-4495	330	13 x 120
1649	S[859]	-4509	185	13 x 120
1650	S[860]	-4523	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1651	S[861]	-4537	185	13 x 120
1652	S[862]	-4551	330	13 x 120
1653	S[863]	-4565	185	13 x 120
1654	S[864]	-4579	330	13 x 120
1655	S[865]	-4593	185	13 x 120
1656	S[866]	-4607	330	13 x 120
1657	S[867]	-4621	185	13 x 120
1658	S[868]	-4635	330	13 x 120
1659	S[869]	-4649	185	13 x 120
1660	S[870]	-4663	330	13 x 120
1661	S[871]	-4677	185	13 x 120
1662	S[872]	-4691	330	13 x 120
1663	S[873]	-4705	185	13 x 120
1664	S[874]	-4719	330	13 x 120
1665	S[875]	-4733	185	13 x 120
1666	S[876]	-4747	330	13 x 120
1667	S[877]	-4761	185	13 x 120
1668	S[878]	-4775	330	13 x 120
1669	S[879]	-4789	185	13 x 120
1670	S[880]	-4803	330	13 x 120
1671	S[881]	-4817	185	13 x 120
1672	S[882]	-4831	330	13 x 120
1673	S[883]	-4845	185	13 x 120
1674	S[884]	-4859	330	13 x 120
1675	S[885]	-4873	185	13 x 120
1676	S[886]	-4887	330	13 x 120
1677	S[887]	-4901	185	13 x 120
1678	S[888]	-4915	330	13 x 120
1679	S[889]	-4929	185	13 x 120
1680	S[890]	-4943	330	13 x 120
1681	S[891]	-4957	185	13 x 120
1682	S[892]	-4971	330	13 x 120
1683	S[893]	-4985	185	13 x 120
1684	S[894]	-4999	330	13 x 120
1685	S[895]	-5013.5	185	13 x 120
1686	S[896]	-5027.5	330	13 x 120
1687	S[897]	-5041.5	185	13 x 120
1688	S[898]	-5055.5	330	13 x 120
1689	S[899]	-5069.5	185	13 x 120
1690	S[900]	-5083.5	330	13 x 120
1691	S[901]	-5097.5	185	13 x 120
1692	S[902]	-5111.5	330	13 x 120
1693	S[903]	-5125.5	185	13 x 120
1694	S[904]	-5139.5	330	13 x 120
1695	S[905]	-5153.5	185	13 x 120
1696	S[906]	-5167.5	330	13 x 120
1697	S[907]	-5181.5	185	13 x 120
1698	S[908]	-5195.5	330	13 x 120
1699	S[909]	-5209.5	185	13 x 120
1700	S[910]	-5223.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1701	S[911]	-5237.5	185	13 x 120
1702	S[912]	-5251.5	330	13 x 120
1703	S[913]	-5265.5	185	13 x 120
1704	S[914]	-5279.5	330	13 x 120
1705	S[915]	-5293.5	185	13 x 120
1706	S[916]	-5307.5	330	13 x 120
1707	S[917]	-5321.5	185	13 x 120
1708	S[918]	-5335.5	330	13 x 120
1709	S[919]	-5349.5	185	13 x 120
1710	S[920]	-5363.5	330	13 x 120
1711	S[921]	-5377.5	185	13 x 120
1712	S[922]	-5391.5	330	13 x 120
1713	S[923]	-5405.5	185	13 x 120
1714	S[924]	-5419.5	330	13 x 120
1715	S[925]	-5433.5	185	13 x 120
1716	S[926]	-5447.5	330	13 x 120
1717	S[927]	-5461.5	185	13 x 120
1718	S[928]	-5475.5	330	13 x 120
1719	S[929]	-5489.5	185	13 x 120
1720	S[930]	-5503.5	330	13 x 120
1721	S[931]	-5517.5	185	13 x 120
1722	S[932]	-5531.5	330	13 x 120
1723	S[933]	-5545.5	185	13 x 120
1724	S[934]	-5559.5	330	13 x 120
1725	S[935]	-5573.5	185	13 x 120
1726	S[936]	-5587.5	330	13 x 120
1727	S[937]	-5601.5	185	13 x 120
1728	S[938]	-5615.5	330	13 x 120
1729	S[939]	-5629.5	185	13 x 120
1730	S[940]	-5643.5	330	13 x 120
1731	S[941]	-5657.5	185	13 x 120
1732	S[942]	-5671.5	330	13 x 120
1733	S[943]	-5685.5	185	13 x 120
1734	S[944]	-5699.5	330	13 x 120
1735	S[945]	-5713.5	185	13 x 120
1736	S[946]	-5727.5	330	13 x 120
1737	S[947]	-5741.5	185	13 x 120
1738	S[948]	-5755.5	330	13 x 120
1739	S[949]	-5769.5	185	13 x 120
1740	S[950]	-5783.5	330	13 x 120
1741	S[951]	-5797.5	185	13 x 120
1742	S[952]	-5811.5	330	13 x 120
1743	S[953]	-5825.5	185	13 x 120
1744	S[954]	-5839.5	330	13 x 120
1745	S[955]	-5853.5	185	13 x 120
1746	S[956]	-5867.5	330	13 x 120
1747	S[957]	-5881.5	185	13 x 120
1748	S[958]	-5895.5	330	13 x 120
1749	S[959]	-5909.5	185	13 x 120
1750	S[960]	-5923.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1751	S[961]	-5937.5	185	13 x 120
1752	S[962]	-5951.5	330	13 x 120
1753	S[963]	-5965.5	185	13 x 120
1754	S[964]	-5979.5	330	13 x 120
1755	S[965]	-5993.5	185	13 x 120
1756	S[966]	-6007.5	330	13 x 120
1757	S[967]	-6021.5	185	13 x 120
1758	S[968]	-6035.5	330	13 x 120
1759	S[969]	-6049.5	185	13 x 120
1760	S[970]	-6063.5	330	13 x 120
1761	S[971]	-6077.5	185	13 x 120
1762	S[972]	-6091.5	330	13 x 120
1763	S[973]	-6105.5	185	13 x 120
1764	S[974]	-6119.5	330	13 x 120
1765	S[975]	-6133.5	185	13 x 120
1766	S[976]	-6147.5	330	13 x 120
1767	S[977]	-6161.5	185	13 x 120
1768	S[978]	-6175.5	330	13 x 120
1769	S[979]	-6189.5	185	13 x 120
1770	S[980]	-6203.5	330	13 x 120
1771	S[981]	-6217.5	185	13 x 120
1772	S[982]	-6231.5	330	13 x 120
1773	S[983]	-6245.5	185	13 x 120
1774	S[984]	-6259.5	330	13 x 120
1775	S[985]	-6273.5	185	13 x 120
1776	S[986]	-6287.5	330	13 x 120
1777	S[987]	-6301.5	185	13 x 120
1778	S[988]	-6315.5	330	13 x 120
1779	S[989]	-6329.5	185	13 x 120
1780	S[990]	-6343.5	330	13 x 120
1781	S[991]	-6357.5	185	13 x 120
1782	S[992]	-6371.5	330	13 x 120
1783	S[993]	-6385.5	185	13 x 120
1784	S[994]	-6399.5	330	13 x 120
1785	S[995]	-6413.5	185	13 x 120
1786	S[996]	-6427.5	330	13 x 120
1787	S[997]	-6441.5	185	13 x 120
1788	S[998]	-6455.5	330	13 x 120
1789	S[999]	-6469.5	185	13 x 120
1790	S[1000]	-6483.5	330	13 x 120
1791	S[1001]	-6497.5	185	13 x 120
1792	S[1002]	-6511.5	330	13 x 120
1793	S[1003]	-6525.5	185	13 x 120
1794	S[1004]	-6539.5	330	13 x 120
1795	S[1005]	-6553.5	185	13 x 120
1796	S[1006]	-6567.5	330	13 x 120
1797	S[1007]	-6581.5	185	13 x 120
1798	S[1008]	-6595.5	330	13 x 120
1799	S[1009]	-6609.5	185	13 x 120
1800	S[1010]	-6623.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1801	S[1011]	-6637.5	185	13 x 120
1802	S[1012]	-6651.5	330	13 x 120
1803	S[1013]	-6665.5	185	13 x 120
1804	S[1014]	-6679.5	330	13 x 120
1805	S[1015]	-6693.5	185	13 x 120
1806	S[1016]	-6707.5	330	13 x 120
1807	S[1017]	-6721.5	185	13 x 120
1808	S[1018]	-6735.5	330	13 x 120
1809	S[1019]	-6749.5	185	13 x 120
1810	S[1020]	-6763.5	330	13 x 120
1811	S[1021]	-6777.5	185	13 x 120
1812	S[1022]	-6791.5	330	13 x 120
1813	S[1023]	-6805.5	185	13 x 120
1814	S[1024]	-6819.5	330	13 x 120
1815	S[1025]	-6833.5	185	13 x 120
1816	S[1026]	-6847.5	330	13 x 120
1817	S[1027]	-6861.5	185	13 x 120
1818	S[1028]	-6875.5	330	13 x 120
1819	S[1029]	-6889.5	185	13 x 120
1820	S[1030]	-6903.5	330	13 x 120
1821	S[1031]	-6917.5	185	13 x 120
1822	S[1032]	-6931.5	330	13 x 120
1823	S[1033]	-6945.5	185	13 x 120
1824	S[1034]	-6959.5	330	13 x 120
1825	S[1035]	-6973.5	185	13 x 120
1826	S[1036]	-6987.5	330	13 x 120
1827	S[1037]	-7001.5	185	13 x 120
1828	S[1038]	-7015.5	330	13 x 120
1829	S[1039]	-7029.5	185	13 x 120
1830	S[1040]	-7043.5	330	13 x 120
1831	S[1041]	-7057.5	185	13 x 120
1832	S[1042]	-7071.5	330	13 x 120
1833	S[1043]	-7085.5	185	13 x 120
1834	S[1044]	-7099.5	330	13 x 120
1835	S[1045]	-7113.5	185	13 x 120
1836	S[1046]	-7127.5	330	13 x 120
1837	S[1047]	-7141.5	185	13 x 120
1838	S[1048]	-7155.5	330	13 x 120
1839	S[1049]	-7169.5	185	13 x 120
1840	S[1050]	-7183.5	330	13 x 120
1841	S[1051]	-7197.5	185	13 x 120
1842	S[1052]	-7211.5	330	13 x 120
1843	S[1053]	-7225.5	185	13 x 120
1844	S[1054]	-7239.5	330	13 x 120
1845	S[1055]	-7253.5	185	13 x 120
1846	S[1056]	-7267.5	330	13 x 120
1847	S[1057]	-7281.5	185	13 x 120
1848	S[1058]	-7295.5	330	13 x 120
1849	S[1059]	-7309.5	185	13 x 120
1850	S[1060]	-7323.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1851	S[1061]	-7337.5	185	13 x 120
1852	S[1062]	-7351.5	330	13 x 120
1853	S[1063]	-7365.5	185	13 x 120
1854	S[1064]	-7379.5	330	13 x 120
1855	S[1065]	-7393.5	185	13 x 120
1856	S[1066]	-7407.5	330	13 x 120
1857	S[1067]	-7421.5	185	13 x 120
1858	S[1068]	-7435.5	330	13 x 120
1859	S[1069]	-7449.5	185	13 x 120
1860	S[1070]	-7463.5	330	13 x 120
1861	S[1071]	-7477.5	185	13 x 120
1862	S[1072]	-7491.5	330	13 x 120
1863	S[1073]	-7505.5	185	13 x 120
1864	S[1074]	-7520	330	13 x 120
1865	S[1075]	-7534	185	13 x 120
1866	S[1076]	-7548	330	13 x 120
1867	S[1077]	-7562	185	13 x 120
1868	S[1078]	-7576	330	13 x 120
1869	S[1079]	-7590	185	13 x 120
1870	S[1080]	-7604	330	13 x 120
1871	S[1081]	-7618	185	13 x 120
1872	S[1082]	-7632	330	13 x 120
1873	S[1083]	-7646	185	13 x 120
1874	S[1084]	-7660	330	13 x 120
1875	S[1085]	-7674	185	13 x 120
1876	S[1086]	-7688	330	13 x 120
1877	S[1087]	-7702	185	13 x 120
1878	S[1088]	-7716	330	13 x 120
1879	S[1089]	-7730	185	13 x 120
1880	S[1090]	-7744	330	13 x 120
1881	S[1091]	-7758	185	13 x 120
1882	S[1092]	-7772	330	13 x 120
1883	S[1093]	-7786	185	13 x 120
1884	S[1094]	-7800	330	13 x 120
1885	S[1095]	-7814	185	13 x 120
1886	S[1096]	-7828	330	13 x 120
1887	S[1097]	-7842	185	13 x 120
1888	S[1098]	-7856	330	13 x 120
1889	S[1099]	-7870	185	13 x 120
1890	S[1100]	-7884	330	13 x 120
1891	S[1101]	-7898	185	13 x 120
1892	S[1102]	-7912	330	13 x 120
1893	S[1103]	-7926	185	13 x 120
1894	S[1104]	-7940	330	13 x 120
1895	S[1105]	-7954	185	13 x 120
1896	S[1106]	-7968	330	13 x 120
1897	S[1107]	-7982	185	13 x 120
1898	S[1108]	-7996	330	13 x 120
1899	S[1109]	-8010	185	13 x 120
1900	S[1110]	-8024	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1901	S[1111]	-8038	185	13 x 120
1902	S[1112]	-8052	330	13 x 120
1903	S[1113]	-8066	185	13 x 120
1904	S[1114]	-8080	330	13 x 120
1905	S[1115]	-8094	185	13 x 120
1906	S[1116]	-8108	330	13 x 120
1907	S[1117]	-8122	185	13 x 120
1908	S[1118]	-8136	330	13 x 120
1909	S[1119]	-8150	185	13 x 120
1910	S[1120]	-8164	330	13 x 120
1911	S[1121]	-8178	185	13 x 120
1912	S[1122]	-8192	330	13 x 120
1913	S[1123]	-8206	185	13 x 120
1914	S[1124]	-8220	330	13 x 120
1915	S[1125]	-8234	185	13 x 120
1916	S[1126]	-8248	330	13 x 120
1917	S[1127]	-8262	185	13 x 120
1918	S[1128]	-8276	330	13 x 120
1919	S[1129]	-8290	185	13 x 120
1920	S[1130]	-8304	330	13 x 120
1921	S[1131]	-8318	185	13 x 120
1922	S[1132]	-8332	330	13 x 120
1923	S[1133]	-8346	185	13 x 120
1924	S[1134]	-8360	330	13 x 120
1925	S[1135]	-8374	185	13 x 120
1926	S[1136]	-8388	330	13 x 120
1927	S[1137]	-8402	185	13 x 120
1928	S[1138]	-8416	330	13 x 120
1929	S[1139]	-8430	185	13 x 120
1930	S[1140]	-8444	330	13 x 120
1931	S[1141]	-8458	185	13 x 120
1932	S[1142]	-8472	330	13 x 120
1933	S[1143]	-8486	185	13 x 120
1934	S[1144]	-8500	330	13 x 120
1935	S[1145]	-8514	185	13 x 120
1936	S[1146]	-8528	330	13 x 120
1937	S[1147]	-8542	185	13 x 120
1938	S[1148]	-8556	330	13 x 120
1939	S[1149]	-8570	185	13 x 120
1940	S[1150]	-8584	330	13 x 120
1941	S[1151]	-8598	185	13 x 120
1942	S[1152]	-8612	330	13 x 120
1943	S[1153]	-8626	185	13 x 120
1944	S[1154]	-8640	330	13 x 120
1945	S[1155]	-8654	185	13 x 120
1946	S[1156]	-8668	330	13 x 120
1947	S[1157]	-8682	185	13 x 120
1948	S[1158]	-8696	330	13 x 120
1949	S[1159]	-8710	185	13 x 120
1950	S[1160]	-8724	330	13 x 120

No.	Name	X	Y	Bump size(μm)
1951	S[1161]	-8738	185	13 x 120
1952	S[1162]	-8752	330	13 x 120
1953	S[1163]	-8766	185	13 x 120
1954	S[1164]	-8780	330	13 x 120
1955	S[1165]	-8794	185	13 x 120
1956	S[1166]	-8808	330	13 x 120
1957	S[1167]	-8822	185	13 x 120
1958	S[1168]	-8836	330	13 x 120
1959	S[1169]	-8850	185	13 x 120
1960	S[1170]	-8864	330	13 x 120
1961	S[1171]	-8878	185	13 x 120
1962	S[1172]	-8892	330	13 x 120
1963	S[1173]	-8906	185	13 x 120
1964	S[1174]	-8920	330	13 x 120
1965	S[1175]	-8934	185	13 x 120
1966	S[1176]	-8948	330	13 x 120
1967	S[1177]	-8962	185	13 x 120
1968	S[1178]	-8976	330	13 x 120
1969	S[1179]	-8990	185	13 x 120
1970	S[1180]	-9004	330	13 x 120
1971	S[1181]	-9018	185	13 x 120
1972	S[1182]	-9032	330	13 x 120
1973	S[1183]	-9046	185	13 x 120
1974	S[1184]	-9060	330	13 x 120
1975	S[1185]	-9074	185	13 x 120
1976	S[1186]	-9088	330	13 x 120
1977	S[1187]	-9102	185	13 x 120
1978	S[1188]	-9116	330	13 x 120
1979	S[1189]	-9130	185	13 x 120
1980	S[1190]	-9144	330	13 x 120
1981	S[1191]	-9158	185	13 x 120
1982	S[1192]	-9172	330	13 x 120
1983	S[1193]	-9186	185	13 x 120
1984	S[1194]	-9200	330	13 x 120
1985	S[1195]	-9214	185	13 x 120
1986	S[1196]	-9228	330	13 x 120
1987	S[1197]	-9242	185	13 x 120
1988	S[1198]	-9256	330	13 x 120
1989	S[1199]	-9270	185	13 x 120
1990	S[1200]	-9284	330	13 x 120
1991	S[1201]	-9298	185	13 x 120
1992	S[1202]	-9312	330	13 x 120
1993	S[1203]	-9326	185	13 x 120
1994	S[1204]	-9340	330	13 x 120
1995	S[1205]	-9354	185	13 x 120
1996	S[1206]	-9368	330	13 x 120
1997	S[1207]	-9382	185	13 x 120
1998	S[1208]	-9396	330	13 x 120
1999	S[1209]	-9410	185	13 x 120
2000	S[1210]	-9424	330	13 x 120

No.	Name	X	Y	Bump size(μm)
2001	S[1211]	-9438	185	13 x 120
2002	S[1212]	-9452	330	13 x 120
2003	S[1213]	-9466	185	13 x 120
2004	S[1214]	-9480	330	13 x 120
2005	S[1215]	-9494	185	13 x 120
2006	S[1216]	-9508	330	13 x 120
2007	S[1217]	-9522	185	13 x 120
2008	S[1218]	-9536	330	13 x 120
2009	S[1219]	-9550	185	13 x 120
2010	S[1220]	-9564	330	13 x 120
2011	S[1221]	-9578	185	13 x 120
2012	S[1222]	-9592	330	13 x 120
2013	S[1223]	-9606	185	13 x 120
2014	S[1224]	-9620	330	13 x 120
2015	S[1225]	-9634	185	13 x 120
2016	S[1226]	-9648	330	13 x 120
2017	S[1227]	-9662	185	13 x 120
2018	S[1228]	-9676	330	13 x 120
2019	S[1229]	-9690	185	13 x 120
2020	S[1230]	-9704	330	13 x 120
2021	S[1231]	-9718	185	13 x 120
2022	S[1232]	-9732	330	13 x 120
2023	S[1233]	-9746	185	13 x 120
2024	S[1234]	-9760	330	13 x 120
2025	S[1235]	-9774	185	13 x 120
2026	S[1236]	-9788	330	13 x 120
2027	S[1237]	-9802	185	13 x 120
2028	S[1238]	-9816	330	13 x 120
2029	S[1239]	-9830	185	13 x 120
2030	S[1240]	-9844	330	13 x 120
2031	S[1241]	-9858	185	13 x 120
2032	S[1242]	-9872	330	13 x 120
2033	S[1243]	-9886	185	13 x 120
2034	S[1244]	-9900	330	13 x 120
2035	S[1245]	-9914	185	13 x 120
2036	S[1246]	-9928	330	13 x 120
2037	S[1247]	-9942	185	13 x 120
2038	S[1248]	-9956	330	13 x 120
2039	S[1249]	-9970	185	13 x 120
2040	S[1250]	-9984	330	13 x 120
2041	S[1251]	-9998	185	13 x 120
2042	S[1252]	-10012.5	330	13 x 120
2043	S[1253]	-10026.5	185	13 x 120
2044	S[1254]	-10040.5	330	13 x 120
2045	S[1255]	-10054.5	185	13 x 120
2046	S[1256]	-10068.5	330	13 x 120
2047	S[1257]	-10082.5	185	13 x 120
2048	S[1258]	-10096.5	330	13 x 120
2049	S[1259]	-10110.5	185	13 x 120
2050	S[1260]	-10124.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
2051	S[1261]	-10138.5	185	13 x 120
2052	S[1262]	-10152.5	330	13 x 120
2053	S[1263]	-10166.5	185	13 x 120
2054	S[1264]	-10180.5	330	13 x 120
2055	S[1265]	-10194.5	185	13 x 120
2056	S[1266]	-10208.5	330	13 x 120
2057	S[1267]	-10222.5	185	13 x 120
2058	S[1268]	-10236.5	330	13 x 120
2059	S[1269]	-10250.5	185	13 x 120
2060	S[1270]	-10264.5	330	13 x 120
2061	S[1271]	-10278.5	185	13 x 120
2062	S[1272]	-10292.5	330	13 x 120
2063	S[1273]	-10306.5	185	13 x 120
2064	S[1274]	-10320.5	330	13 x 120
2065	S[1275]	-10334.5	185	13 x 120
2066	S[1276]	-10348.5	330	13 x 120
2067	S[1277]	-10362.5	185	13 x 120
2068	S[1278]	-10376.5	330	13 x 120
2069	S[1279]	-10390.5	185	13 x 120
2070	S[1280]	-10404.5	330	13 x 120
2071	S[1281]	-10418.5	185	13 x 120
2072	S[1282]	-10432.5	330	13 x 120
2073	S[1283]	-10446.5	185	13 x 120
2074	S[1284]	-10460.5	330	13 x 120
2075	S[1285]	-10474.5	185	13 x 120
2076	S[1286]	-10488.5	330	13 x 120
2077	S[1287]	-10502.5	185	13 x 120
2078	S[1288]	-10516.5	330	13 x 120
2079	S[1289]	-10530.5	185	13 x 120
2080	S[1290]	-10544.5	330	13 x 120
2081	S[1291]	-10558.5	185	13 x 120
2082	S[1292]	-10572.5	330	13 x 120
2083	S[1293]	-10586.5	185	13 x 120
2084	S[1294]	-10600.5	330	13 x 120
2085	S[1295]	-10614.5	185	13 x 120
2086	S[1296]	-10628.5	330	13 x 120
2087	S[1297]	-10642.5	185	13 x 120
2088	S[1298]	-10656.5	330	13 x 120
2089	S[1299]	-10670.5	185	13 x 120
2090	S[1300]	-10684.5	330	13 x 120
2091	S[1301]	-10698.5	185	13 x 120
2092	S[1302]	-10712.5	330	13 x 120
2093	S[1303]	-10726.5	185	13 x 120
2094	S[1304]	-10740.5	330	13 x 120
2095	S[1305]	-10754.5	185	13 x 120
2096	S[1306]	-10768.5	330	13 x 120
2097	S[1307]	-10782.5	185	13 x 120
2098	S[1308]	-10796.5	330	13 x 120
2099	S[1309]	-10810.5	185	13 x 120
2100	S[1310]	-10824.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
2101	S[1311]	-10838.5	185	13 x 120
2102	S[1312]	-10852.5	330	13 x 120
2103	S[1313]	-10866.5	185	13 x 120
2104	S[1314]	-10880.5	330	13 x 120
2105	S[1315]	-10894.5	185	13 x 120
2106	S[1316]	-10908.5	330	13 x 120
2107	S[1317]	-10922.5	185	13 x 120
2108	S[1318]	-10936.5	330	13 x 120
2109	S[1319]	-10950.5	185	13 x 120
2110	S[1320]	-10964.5	330	13 x 120
2111	S[1321]	-10978.5	185	13 x 120
2112	S[1322]	-10992.5	330	13 x 120
2113	S[1323]	-11006.5	185	13 x 120
2114	S[1324]	-11020.5	330	13 x 120
2115	S[1325]	-11034.5	185	13 x 120
2116	S[1326]	-11048.5	330	13 x 120
2117	S[1327]	-11062.5	185	13 x 120
2118	S[1328]	-11076.5	330	13 x 120
2119	S[1329]	-11090.5	185	13 x 120
2120	S[1330]	-11104.5	330	13 x 120
2121	S[1331]	-11118.5	185	13 x 120
2122	S[1332]	-11132.5	330	13 x 120
2123	S[1333]	-11146.5	185	13 x 120
2124	S[1334]	-11160.5	330	13 x 120
2125	S[1335]	-11174.5	185	13 x 120
2126	S[1336]	-11188.5	330	13 x 120
2127	S[1337]	-11202.5	185	13 x 120
2128	S[1338]	-11216.5	330	13 x 120
2129	S[1339]	-11230.5	185	13 x 120
2130	S[1340]	-11244.5	330	13 x 120
2131	S[1341]	-11258.5	185	13 x 120
2132	S[1342]	-11272.5	330	13 x 120
2133	S[1343]	-11286.5	185	13 x 120
2134	S[1344]	-11300.5	330	13 x 120
2135	S[1345]	-11314.5	185	13 x 120
2136	S[1346]	-11328.5	330	13 x 120
2137	S[1347]	-11342.5	185	13 x 120
2138	S[1348]	-11356.5	330	13 x 120
2139	S[1349]	-11370.5	185	13 x 120
2140	S[1350]	-11384.5	330	13 x 120
2141	S[1351]	-11398.5	185	13 x 120
2142	S[1352]	-11412.5	330	13 x 120
2143	S[1353]	-11426.5	185	13 x 120
2144	S[1354]	-11440.5	330	13 x 120
2145	S[1355]	-11454.5	185	13 x 120
2146	S[1356]	-11468.5	330	13 x 120
2147	S[1357]	-11482.5	185	13 x 120
2148	S[1358]	-11496.5	330	13 x 120
2149	S[1359]	-11510.5	185	13 x 120
2150	S[1360]	-11524.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
2151	S[1361]	-11538.5	185	13 x 120
2152	S[1362]	-11552.5	330	13 x 120
2153	S[1363]	-11566.5	185	13 x 120
2154	S[1364]	-11580.5	330	13 x 120
2155	S[1365]	-11594.5	185	13 x 120
2156	S[1366]	-11608.5	330	13 x 120
2157	S[1367]	-11622.5	185	13 x 120
2158	S[1368]	-11636.5	330	13 x 120
2159	S[1369]	-11650.5	185	13 x 120
2160	S[1370]	-11664.5	330	13 x 120
2161	S[1371]	-11678.5	185	13 x 120
2162	S[1372]	-11692.5	330	13 x 120
2163	S[1373]	-11706.5	185	13 x 120
2164	S[1374]	-11720.5	330	13 x 120
2165	S[1375]	-11734.5	185	13 x 120
2166	S[1376]	-11748.5	330	13 x 120
2167	S[1377]	-11762.5	185	13 x 120
2168	S[1378]	-11776.5	330	13 x 120
2169	S[1379]	-11790.5	185	13 x 120
2170	S[1380]	-11804.5	330	13 x 120
2171	S[1381]	-11818.5	185	13 x 120
2172	S[1382]	-11832.5	330	13 x 120
2173	S[1383]	-11846.5	185	13 x 120
2174	S[1384]	-11860.5	330	13 x 120
2175	S[1385]	-11874.5	185	13 x 120
2176	S[1386]	-11888.5	330	13 x 120
2177	S[1387]	-11902.5	185	13 x 120
2178	S[1388]	-11916.5	330	13 x 120
2179	S[1389]	-11930.5	185	13 x 120
2180	S[1390]	-11944.5	330	13 x 120
2181	S[1391]	-11958.5	185	13 x 120
2182	S[1392]	-11972.5	330	13 x 120
2183	S[1393]	-11986.5	185	13 x 120
2184	S[1394]	-12000.5	330	13 x 120
2185	S[1395]	-12014.5	185	13 x 120
2186	S[1396]	-12028.5	330	13 x 120
2187	S[1397]	-12042.5	185	13 x 120
2188	S[1398]	-12056.5	330	13 x 120
2189	S[1399]	-12070.5	185	13 x 120
2190	S[1400]	-12084.5	330	13 x 120
2191	S[1401]	-12098.5	185	13 x 120
2192	S[1402]	-12112.5	330	13 x 120
2193	S[1403]	-12126.5	185	13 x 120
2194	S[1404]	-12140.5	330	13 x 120
2195	S[1405]	-12154.5	185	13 x 120
2196	S[1406]	-12168.5	330	13 x 120
2197	S[1407]	-12182.5	185	13 x 120
2198	S[1408]	-12196.5	330	13 x 120
2199	S[1409]	-12210.5	185	13 x 120
2200	S[1410]	-12224.5	330	13 x 120

No.	Name	X	Y	Bump size(μm)
2201	S[1411]	-12238.5	185	13 x 120
2202	S[1412]	-12252.5	330	13 x 120
2203	S[1413]	-12266.5	185	13 x 120
2204	S[1414]	-12280.5	330	13 x 120
2205	S[1415]	-12294.5	185	13 x 120
2206	S[1416]	-12308.5	330	13 x 120
2207	S[1417]	-12322.5	185	13 x 120
2208	S[1418]	-12336.5	330	13 x 120
2209	S[1419]	-12350.5	185	13 x 120
2210	S[1420]	-12364.5	330	13 x 120
2211	S[1421]	-12378.5	185	13 x 120
2212	S[1422]	-12392.5	330	13 x 120
2213	S[1423]	-12406.5	185	13 x 120
2214	S[1424]	-12420.5	330	13 x 120
2215	S[1425]	-12434.5	185	13 x 120
2216	S[1426]	-12448.5	330	13 x 120
2217	S[1427]	-12462.5	185	13 x 120
2218	S[1428]	-12476.5	330	13 x 120
2219	S[1429]	-12490.5	185	13 x 120
2220	S[1430]	-12504.5	330	13 x 120
2221	S[1431]	-12519	185	13 x 120
2222	S[1432]	-12533	330	13 x 120
2223	S[1433]	-12547	185	13 x 120
2224	S[1434]	-12561	330	13 x 120
2225	S[1435]	-12575	185	13 x 120
2226	S[1436]	-12589	330	13 x 120
2227	S[1437]	-12603	185	13 x 120
2228	S[1438]	-12617	330	13 x 120
2229	S[1439]	-12631	185	13 x 120
2230	S[1440]	-12645	330	13 x 120
2231	DUMMY	-12659	185	13 x 120
2232	DUMMY	-12673	330	13 x 120
2233	DUMMY	-12687	185	13 x 120
2234	DUMMY	-12701	330	13 x 120
2235	THROUGH_3	-12715	185	13 x 120
2236	THROUGH_3	-12729	330	13 x 120
2237	VCOM_R	-12743	185	13 x 120
2238	VCOM_R	-12757	330	13 x 120
2239	VCOM_R	-12771	185	13 x 120
2240	VCOM_R	-12785	330	13 x 120
2241	DUMMY	-12799	185	13 x 120
2242	DUMMY	-12813	330	13 x 120
2243	DUMMY	-12827	185	13 x 120
2244	DUMMY	-12841	330	13 x 120
2245	SWR3B	-12855	185	13 x 120
2246	SWR3B	-12869	330	13 x 120
2247	SWR3	-12883	185	13 x 120
2248	SWR3	-12897	330	13 x 120
2249	SWR2B	-12911	185	13 x 120
2250	SWR2B	-12925	330	13 x 120

No.	Name	X	Y	Bump size(μm)
2251	SWR2	-12939	185	13 x 120
2252	SWR2	-12953	330	13 x 120
2253	SWR1B	-12967	185	13 x 120
2254	SWR1B	-12981	330	13 x 120
2255	SWR1	-12995	185	13 x 120
2256	SWR1	-13009	330	13 x 120
2257	VGH	-13023	185	13 x 120
2258	VGH	-13037	330	13 x 120
2259	VGH	-13051	185	13 x 120
2260	VGH	-13065	330	13 x 120
2261	GDETR[2]	-13079	185	13 x 120
2262	GDETR[2]	-13093	330	13 x 120
2263	VGH	-13107	185	13 x 120
2264	VGH	-13121	330	13 x 120
2265	VGH	-13135	185	13 x 120
2266	VGH	-13149	330	13 x 120
2267	GOUTR20	-13163	185	13 x 120
2268	GOUTR20	-13177	330	13 x 120
2269	GOUTR19	-13191	185	13 x 120
2270	GOUTR19	-13205	330	13 x 120
2271	GOUTR18	-13219	185	13 x 120
2272	GOUTR18	-13233	330	13 x 120
2273	GOUTR17	-13247	185	13 x 120
2274	GOUTR17	-13261	330	13 x 120
2275	GOUTR16	-13275	185	13 x 120
2276	GOUTR16	-13289	330	13 x 120
2277	GOUTR15	-13303	185	13 x 120
2278	GOUTR15	-13317	330	13 x 120
2279	GOUTR14	-13331	185	13 x 120
2280	GOUTR14	-13345	330	13 x 120
2281	GOUTR13	-13359	185	13 x 120
2282	GOUTR13	-13373	330	13 x 120
2283	GOUTR12	-13387	185	13 x 120
2284	GOUTR12	-13401	330	13 x 120
2285	GOUTR11	-13415	185	13 x 120
2286	GOUTR11	-13429	330	13 x 120
2287	GOUTR10	-13443	185	13 x 120
2288	GOUTR10	-13457	330	13 x 120
2289	GOUTR9	-13471	185	13 x 120
2290	GOUTR9	-13485	330	13 x 120
2291	VGL	-13499	185	13 x 120
2292	VGL	-13513	330	13 x 120
2293	VGL	-13527	185	13 x 120
2294	VGL	-13541	330	13 x 120
2295	VGL	-13555	185	13 x 120
2296	VGL	-13569	330	13 x 120
2297	VGL	-13583	185	13 x 120
2298	VGL	-13597	330	13 x 120
2299	VGL	-13611	185	13 x 120
2300	VGL	-13625	330	13 x 120

No.	Name	X	Y	Bump size(μm)
2301	GOUTR8	-13639	185	13 x 120
2302	GOUTR8	-13653	330	13 x 120
2303	GOUTR7	-13667	185	13 x 120
2304	GOUTR7	-13681	330	13 x 120
2305	GOUTR6	-13695	185	13 x 120
2306	GOUTR6	-13709	330	13 x 120
2307	GOUTR5	-13723	185	13 x 120
2308	GOUTR5	-13737	330	13 x 120
2309	GOUTR4	-13751	185	13 x 120
2310	GOUTR4	-13765	330	13 x 120
2311	GOUTR3	-13779	185	13 x 120
2312	GOUTR3	-13793	330	13 x 120
2313	GOUTR2	-13807	185	13 x 120
2314	GOUTR2	-13821	330	13 x 120
2315	GOUTR1	-13835	185	13 x 120
2316	GOUTR1	-13849	330	13 x 120
2317	VCOM_R	-13863	185	13 x 120
2318	VCOM_R	-13877	330	13 x 120
2319	GDETR[1]	-13891	185	13 x 120
2320	GDETR[1]	-13905	330	13 x 120
2321	FCTRL_R	-14080	357.5	110 x 30
2322	CA_R0	-14080	302.5	110 x 30
2323	GIO_R0	-14080	247.5	110 x 30
2324	CA_R1	-14080	192.5	110 x 30
2325	GIO_R1	-14080	137.5	110 x 30
2326	CA_R2	-14080	82.5	110 x 30
2327	GIO_R2	-14080	27.5	110 x 30
2328	CA3	-14080	-27.5	110 x 30
2329	GIO_R3	-14080	-82.5	110 x 30
2330	GIO_R4	-14080	-137.5	110 x 30
2331	CA_R4	-14080	-192.5	110 x 30
2332	CA_R5	-14080	-247.5	110 x 30
2333	CA_R6	-14080	-302.5	110 x 30
2334	F_POL_RO	-14080	-357.5	110 x 30

11. Ordering Information

Part no.	Package
HX8272-C01DPDxxxy-LT	00: mean chip version D: mean fab code PD: mean COG xxx: mean chip thickness **(μm)** y: mean value of bump compensation LT: mean low temperature
HX8272-C01DPDxxxy-LTP	00: mean chip version D: mean fab code PD: mean COG xxx: mean chip thickness **(μm)** y: mean value of bump compensation LT: mean low temperature P: mean polish