CDTech(H.K.)Electronics Limited

Product Specification

Model Name	S035GV09HS
Description	TFT LCD Module 3.5" VGA 480(RGB)x640 Dots
Date	2018/02/08
Version	3.0

Approved by/Date	**Check by/Date**	**Prepared by/Date**
Sam 2018/02/08	Borger 2018/02/08	Jack Guo 2018/02/08

Customer Approval	
Date	

CDTech(H.K.)Electronics Limited

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1. Record of Revision

Rev	Issued Date	Description	Editor
1.0	2016/11/30	First Release.	Jack Guo
2.0	2016/12/6	Update Surface luminance.	Jack Guo
3.0	2018/02/08	Update Interface Timing.	Jack Guo

2. General Specifications

Feature		Spec
Characteristics	Size	3.5 inch
	Resolution	480(horizontal)*640(Vertical)
	Interface	18bit-RGB
	Connect type	Connector
	Color Depth	16.7M
	Technology type	a-Si
	Pixel pitch (mm)	0.111*0.111
	Pixel Configuration	R.G.B.-Stripe
	Display Mode	Normally White
	Driver IC	ILI9805C
	Viewing Direction	6 O'clock
Mechanical	LCM (W x H x D) (mm)	64.00*85.00*2.90
	Active Area(mm)	53.269*71.04
	With /Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	8 LEDs

Note 1: Requirements on Environmental Protection: RoHs
Note 2: LCM weight tolerance: +/- 5%

3. Input/Output Terminals

No.	Symbol	Description
1~2	GND	System Ground
3~4	VDD	Power supply.
5	NC	-
6	RESETB	Reset signal.
7	HSYNC	Horizontal sync.
8	VSYNC	Vertical sync.
9	CLK	Dot clock signal.
10	VSS	System Ground
11	D0(B2)	6bits Blue Data
12	D1(B3)	6bits Blue Data
13	D2(B4)	6bits Blue Data
14	D3(B5)	6bits Blue Data
15	D4(B6)	6bits Blue Data
16	D5(B7)	6bits Blue Data
17	D10(G2)	6bits Green Data
18	D11(G3)	6bits Green Data
19	D12(G4)	6bits Green Data
20	D13(G5)	6bits Green Data
21	D14(G6)	6bits Green Data
22	D15(G7)	6bits Green Data
23	D20(R2)	6bits Red Data
24	D21(R3)	6bits Red Data
25	D22(R4)	6bits Red Data
26	D23(R5)	6bits Red Data
27	D24(R6)	6bits Red Data
28	D25(R7)	6bits Red Data
29	VSS	System Ground
30	DE	Data enable signal.
31	STBYB	Standby signal(Hi:Normal operation,LO: Standby operation)
32	TEST1	-
33	XL	Touch panel terminal
34	YD	Touch panel terminal
35	XR	Touch panel terminal

36	YU	Touch panel terminal
37	TEST2	-
38	BLH	LED Anode
39	BLL	LED Cathode.

4. Absolute Maximum Rating

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	V_{DD}	-0.3	-	5.5	V	-
Operating Temperature	T_{OPR}	-20	-	70	℃	-
Storage Temperature	T_{STG}	-30	-	80	℃	

5. Timing characteristics

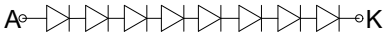
5.1 ELECTRICAL CHARACTERISTICS

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		V_{cc}	2.3	2.8	3.3	V	
		IOVCC	1.65	1.8	3.3		
Input Signal Voltage	Low Leve	V_{IL}	VSS	-	0.3VDDI	V	
	High Level	V_{IH}	0.7VDDI	-	VDDI	V	
Output Signal Voltage	Low Leve	V_{OL}	VSS	-	0.2VDDI	V	
	High Level	V_{OH}	0.8VDDI	-	VDDI	V	
Supply current		I_{DD}	-	33	50	mA	

5.2 LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	-	mA	
Forward Voltage	V_F	24	25.6	-	V	
LED Lifetime		-	50000	-	Hrs	

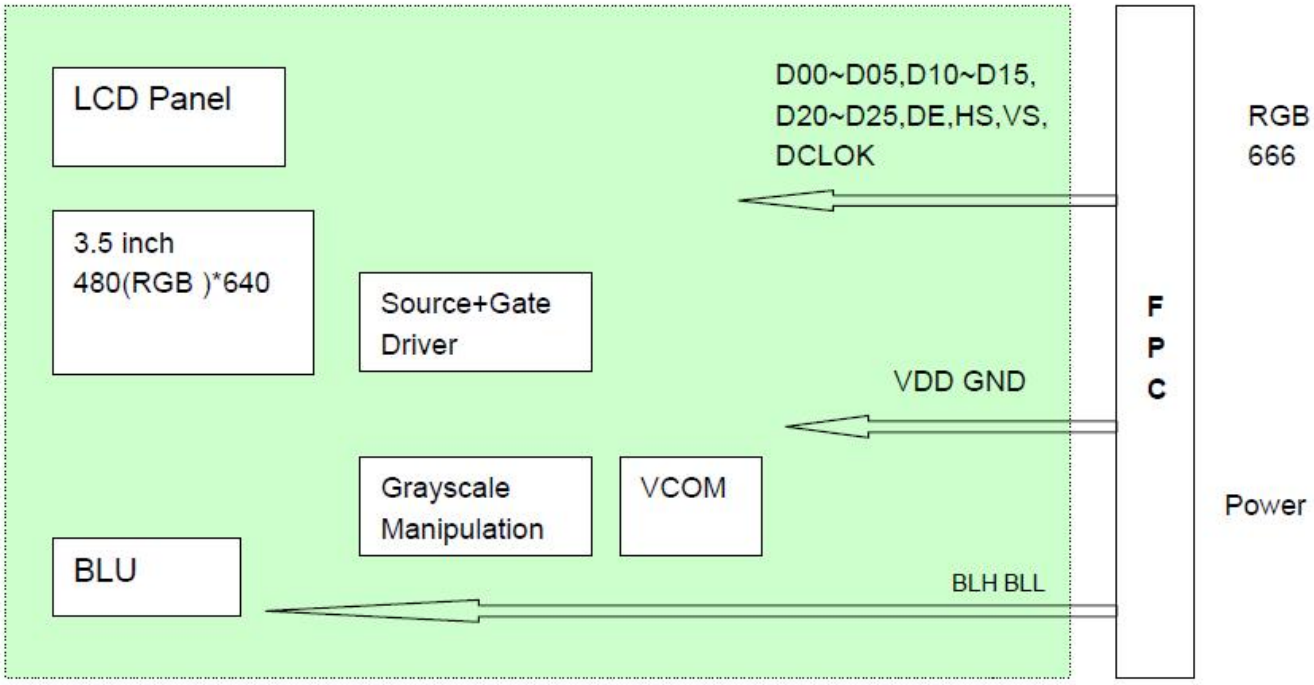
Note 1: Each LED: IF =20 mA, VF =3.2+/0.2V.
Note 2: Optical performance should be evaluated at Ta=25℃ only.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.



BL CIRCUIT DIAGRAM

Figure: LED connection of backlight(Constant Current)

5.3 Block Diagram



6 Interface Timing

6.1 DC characteristics

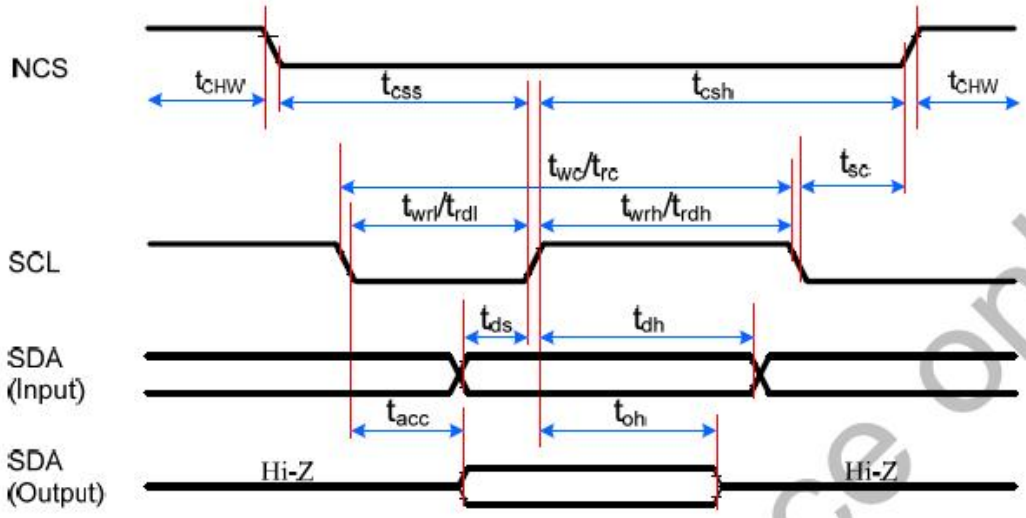
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.6	2.8	3.6	V	
Logic operating voltage	HS_VCC	-	1.65	2.8	3.3	V	
Logic operating voltage	IOVCC	-	1.65	1.8	3.3	V	Note1,2
OTP Supply voltage	VPP_OTP	-	4.5	5	6.6	V	Note1
Logic High level input voltage	V_{IH}	-	0.7*IOVCC		IOVCC	V	Note1
Logic Low level input voltage	V_{IL}	-	-0.3		0.3*IOVCC	V	Note1
Logic High level output voltage TE, SDO (SDA) , CABC_PWM_OUT	V_{OH}	IOH = -1.0mA	0.8*IOVCC		IOVCC	V	Note1
Logic Low level output voltage TE, SDO (SDA) , CABC_PWM_OUT	V_{OL}	IOL = +1.0mA	0		0.2*IOVCC	V	Note1
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	
Driver Supply Voltage	-	|VGH-VGL|	16	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-3.0	-	-0.06	V	Note3
Source Driver							
Source Output Range	V_{SOUT}	-	0.1	-	VREG1OUT-0.1	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.687	-	5.5	V	
Negative Gamma Reference Voltage	VREG2OUT	-	-5.5	-	-3.687	V	
Source Output Setting Time	Tr	Below with 99% precision	-	10	-	uS	Note3.4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	(TBD)	mV	Note3
		4.2V>Sout>0.8V	-	-	(TBD)	mV	
Output Offset Voltage	V_{OFFSET}	-	-	-	(TBD)	mV	Note3
Booster Operation							
Booster (VCIx2) Voltage	DDVDH	-			6	V	
Booster (VCIx2) Voltage	DDVDL	-	-6			V	
Booster (VCIx2 Drop Voltage)	VCI1x2 drop	loading=1mA	-	-	5	%	
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	
Standby mode current consumption							
Sleep In mode	$I_{(IOVCC\ SLP\ IN)}$	Ta = 25 °C VCI=2.8V IOVCC=1.8V	-	0	-	uA	
	$I_{(VCI\ SLP\ IN)}$		-	(TBD)	(TBD)	uA	
Deep Standby mode	$I_{(IOVCC\ DSTB)}$		-	1	-	uA	
	$I_{(VCI\ DSTB)}$		-	1	-	uA	

Notes:

1. Ta = -30 to 70 °C (to 85 °C no damage), IOVCC = 1.65V to 3.3V, VCI = 2.6V to 3.6V, HS_VSS = DGND = 0V.
2. Supply digital IOVCC voltage equal or less than analog VCI voltage.
3. Source channel loading = 10KΩ, 40pF/channel
4. The maximum value is between with 10KΩ, 40pF/channel and Gamma setting value

6.2 AC Characteristics

6.2.1 Display Serial Interface Timing Characteristics (3-line SPI System)

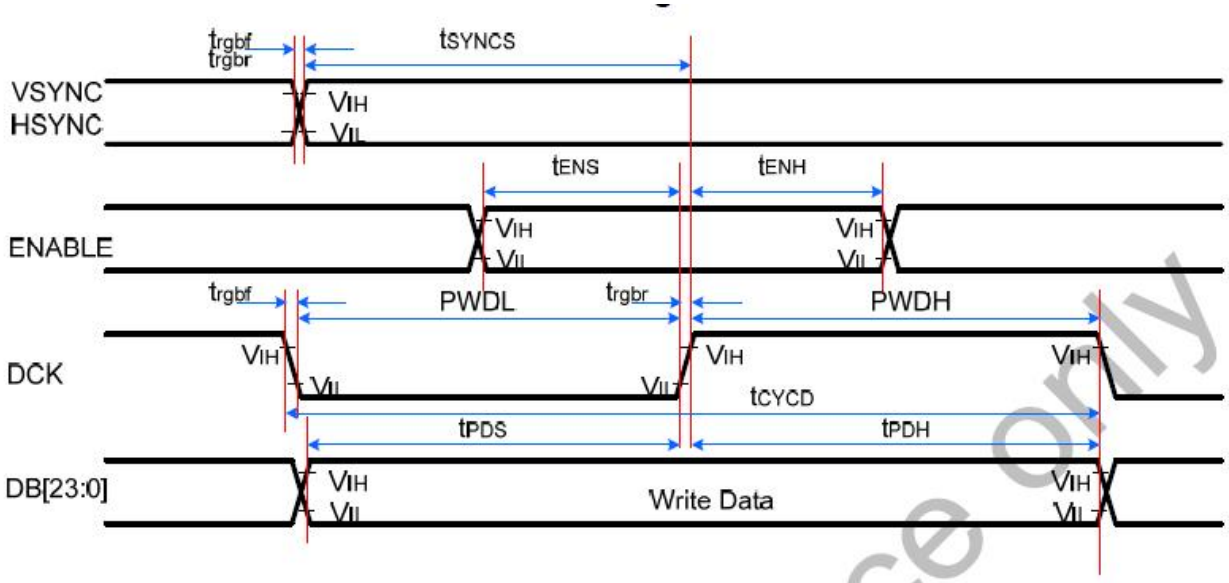


Signal	Symbol	Parameter	min	max	Unit	Description
NCS	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS "H" pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	80	-	ns	
	twrh	SCL "H" pulse width (Write)	30	-	ns	
	twrl	SCL "L" pulse width (Write)	30	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL = 30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL = 8pF

Notes:

1. Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.6V to 3.6V, HS_VSS = DGND = 0V, T = 10+/-0.5ns.
2. Does not include signal rising and falling times.

6.2.2 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	5	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	5	-	ns	
	t_{ENH}	ENABLE hold time	5	-	ns	
DB [17:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
DCK	PWDH	DCK high-level period	13	-	ns	
	PWDL	DCK low-level period	13	-	ns	
	t_{CYCD}	DCK cycle time	28	-	ns	
	t_{rgbr}, t_{rgbf}	DCK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC = 1.65V to 3.3V, VCI = 2.6V to 3.6V, HS_VSS = DGND = 0V

The timing chart of 24-/18-/16-bit DPI interface mode is illustrated in Figure 12.

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		50	-	70	fps
Horizontal Low Pulse Width	HLW		5	-	80	DOTCLK
Horizontal Back Porch	HBP		10	-	85	DOTCLK
Horizontal Address	HACT		-	480	-	DOTCLK
Horizontal Front Porch	HFP		5	-	80	DOTCLK
Horizontal Blanking Period	HBP + HFP		60		90	DOTCLK
Vertical Low Pulse Width*	VLW		2	-	4	Line
Vertical Back Porch*	VBP		4	-	6	Line
Vertical Address	VACT		-	864	-	Line
Vertical Front Porch	VFP		2	-	4	Line
Vertical Blanking Period	VBP + VFP		6		12	Line
Data Clock	DCK		23.5	-	34.9	MHz

*: Vertical Back Porch(VBP) ≧ Vertical Low Pulse Width(VLW)

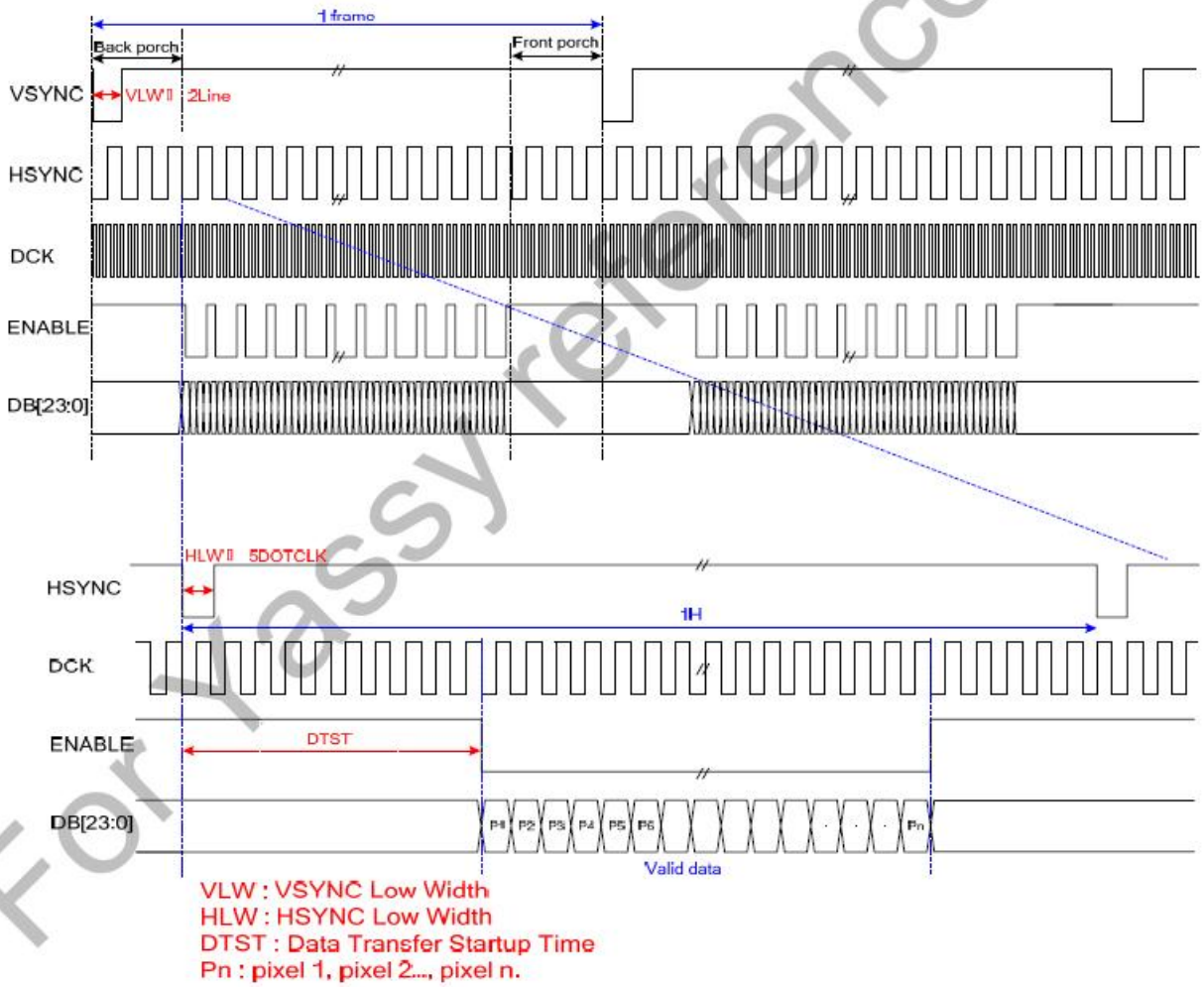


Figure 12: DPI Interface Timing Diagram

Note: VSPL = 0, HSPL = 0, DPL = 0 and EPL = 0 of "Interface Mode Control B0h" command.

6.3 Power ON/OFF Sequence

IOVCC and VCI can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VCI and IOVCC can be powered down with minimum 0msec after NRESET has been released.
NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

Note:

1. *There will be no damage to ILI9805C if the power sequences are not met.*
2. *There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*
3. *There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*
4. *If NRESET line is not held stable by host during Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*
5. *Keep data pins DB[23:0] at low level, when VCI or IOVCC comes later.*

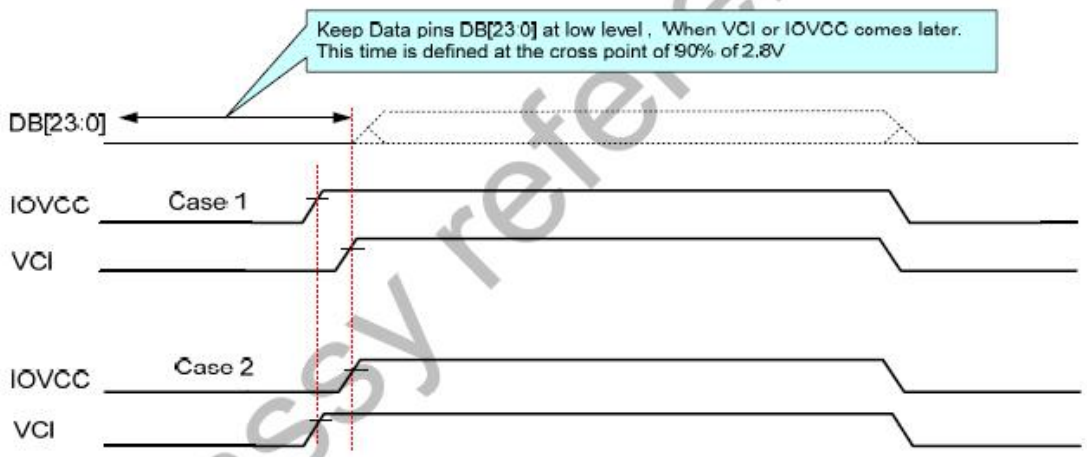


Figure 104: Data pins DB[23:0] keep low before VCI and IOVCC be applied

6.4 Reset Timing

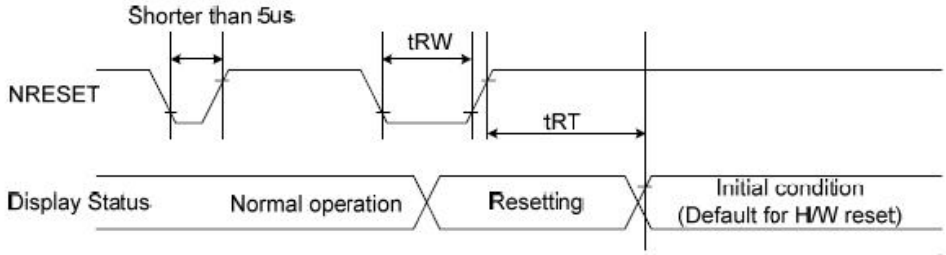


Figure 113: Reset Timing

Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
NRESET	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of NRESET.
2. Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the Table 40.

Table 40: Reset Descript

NRESET Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

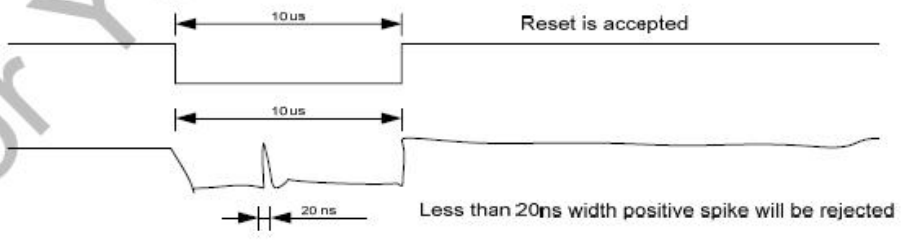


Figure 114: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7 Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	-	-	30	-	ms	FIG.1	Note4
Contrast Ratio		CR		400	-	-	-	FIG.2	Note1
Surface luminance		LV	θ =0°	-	500	-	cd/m2	FIG.2	Note2
Luminance uniformity		Yu	θ =0°	-	-	-	%	FIG.2	Note3
NTSC		-	θ =0°	-	50	-	%	FIG.2	Note5
Viewing angle		θ Cr>10	∅ =90°	-	65	-	deg	FIG.3	Note6
			∅ =270°	-	55	-	deg	FIG.3	
			∅ =0°	-	65	-	deg	FIG.3	
			∅ =180°	-	65	-	deg	FIG.3	
Chromaticity	Red	R_X	θ =0° ∅ =0° Ta=25°	0.56	0.59	0.62	-	FIG.2 CIE1931	Note5
		R_Y		0.28	0.31	0.34	-		
	Green	G_X		0.29	0.32	0.35	-		
		G_Y		0.50	0.53	0.56	-		
	Blue	B_X		0.12	0.15	0.18	-		
		B_Y		0.06	0.09	0.12	-		
	White	W_X		0.26	0.27	0.32	-		
		W_Y		0.28	0.30	0.34	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON’s BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (Tr) is the time between photo detector output intensity changed from 90% to 10%. And fall time (Tf) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers’s ConoScope or DMS series Instruments or compatible.

FIG.1.The definition of response Time

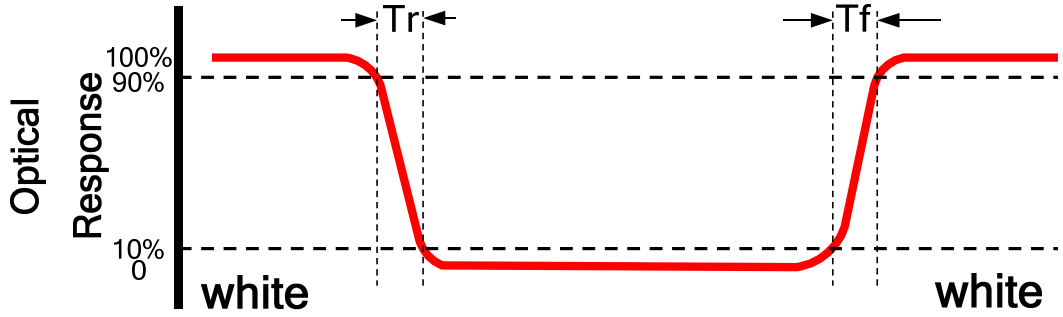


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

Size : S≤5"(see Figure a) A : 5 mm B : 5 mm
H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure a.
measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

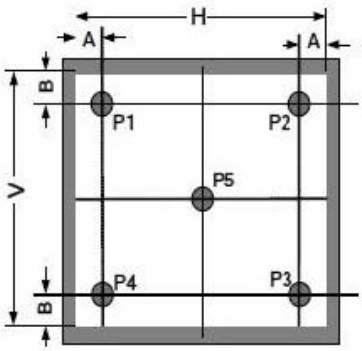


Figure a

Size : 5"＜S≤12.3"(see Figure b) H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure b.
measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

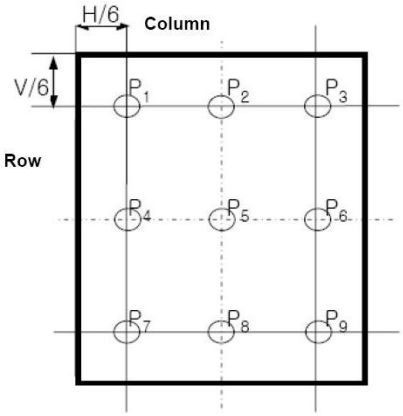


Figure b

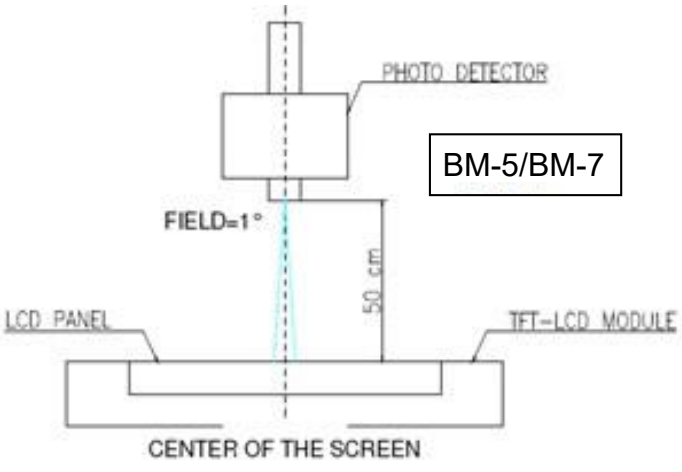
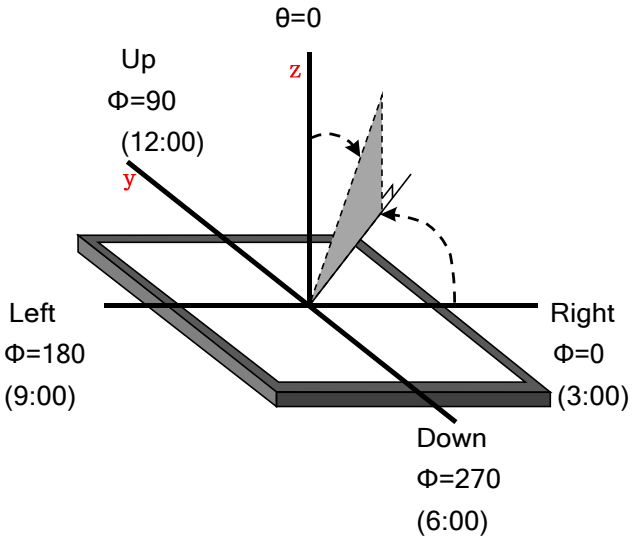


Figure c

FIG.3.The definition of viewing angle

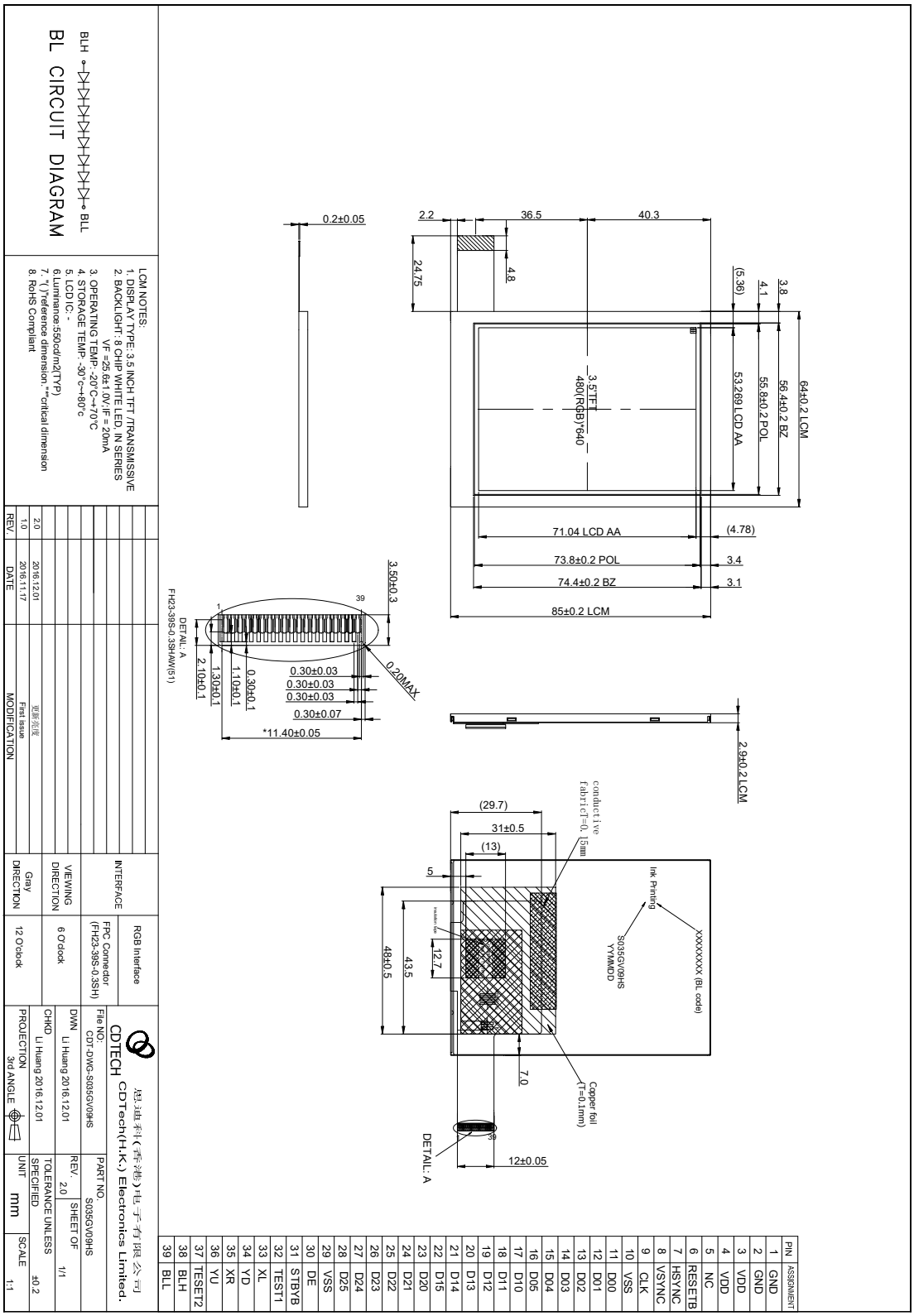


8 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 96hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 96hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max,96 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-20℃ 30 min ~ +60℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

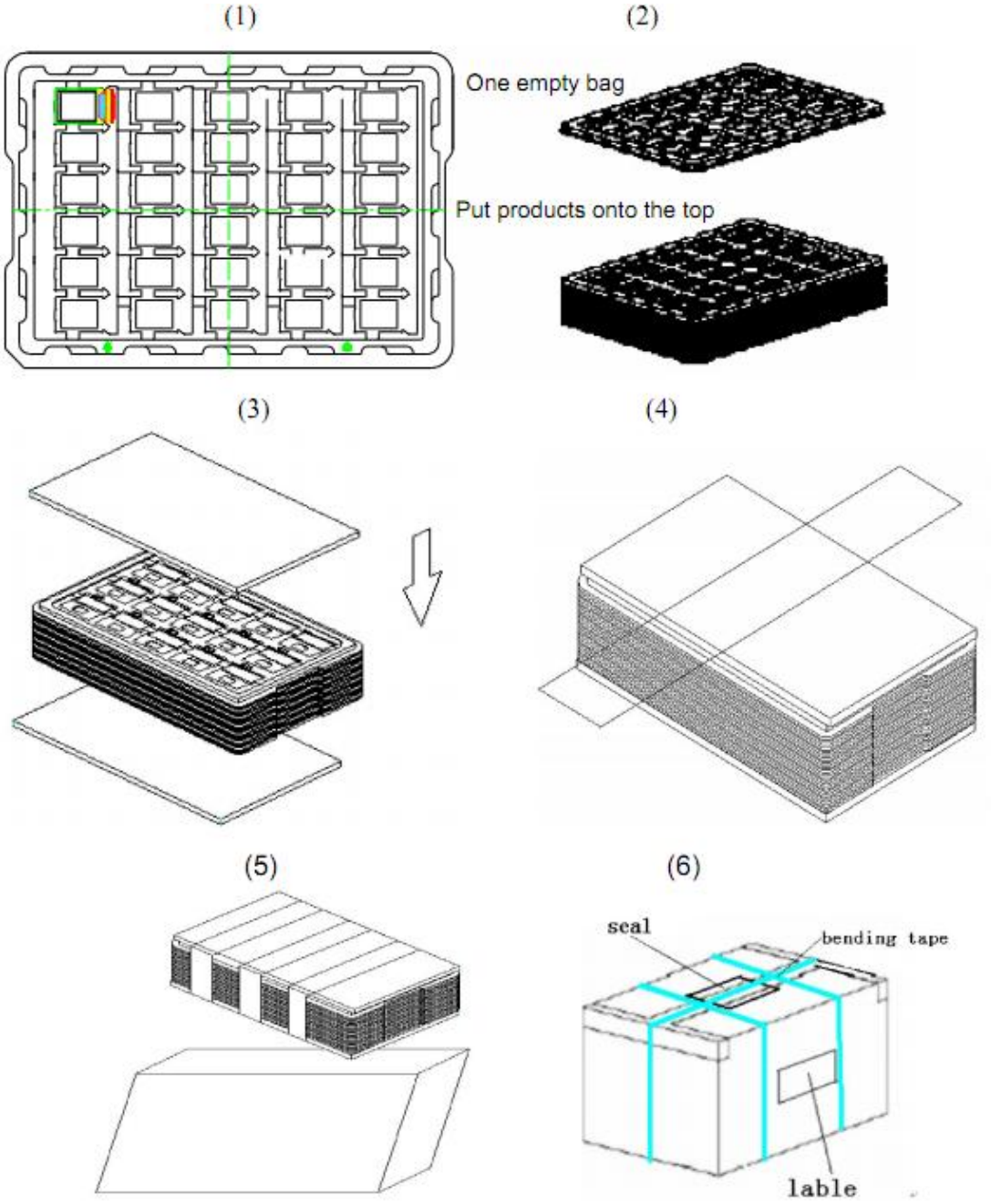
Note:1. Ts is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.
3. The size of sample is 5pcs.

9 Mechanical Drawing



10 Packing

Packing Method



1. Put module into tray cavity:
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above:
4. Fix the cardboard to the tray stack with adhesive tape:
5. Put the tray stack into carton.
6. Carton sealing with adhesive tape.

11. Precautions for Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

11.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.