南京观海微电子有限公司
GoHi Microelectronics Co., Ltd.

GH8323-i1 Datasheet

1366RGBx768 dots,
16.7M color,α-Si TFT
LCD single chip driver
(preliminary v0.12)

Revision History

Version	Date	Description of modification
Preliminary v0.0	2023/06/01	New setup
Preliminary v0.10	2023/07/04	Fix Source channel select
Preliminary v0.11	2023/07/10	Fix Pin Description
Preliminary v0.12	2023/07/17	Update multiple points

Contents

1 General Description

The GH8323-i1 is a highly integrated solution for small size to middle size α-Si & LTPS TFT-LCD panels. This chip integrates 2054 channel source driver a timing controller for color TFT LCD panel. The chip support LVDS & MIPI & RGB interface. And support the function setting through R/W SPI/3-wire serial interface.

2 Features

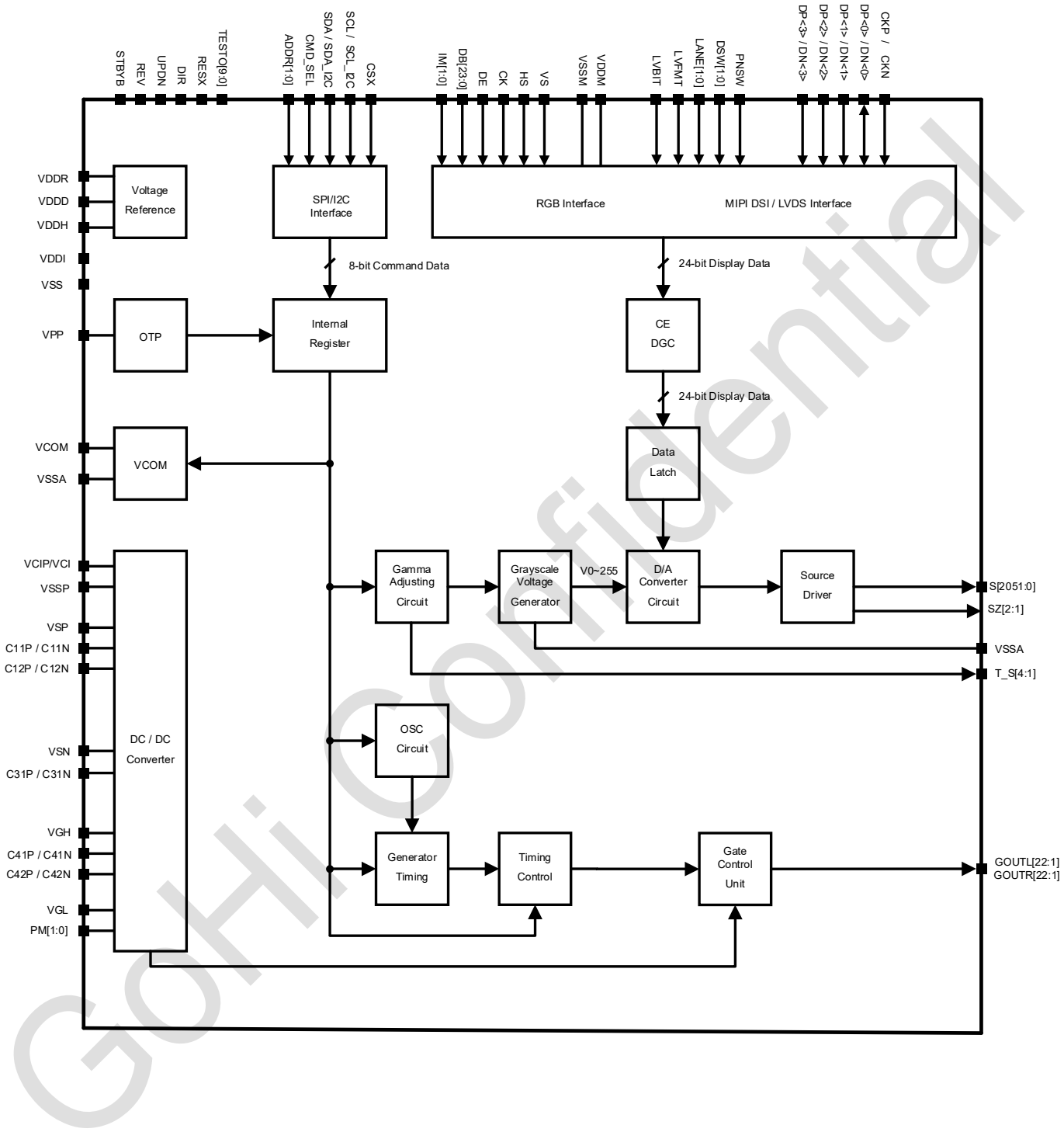
- Single chip solution for a WXGA a-Si type LCD display
- Integrate 2054 channel source driver and timing controller
- Display resolution:
  - Dual gate (Gate Ln*2,max2400)
    - 1366 RGB x 768
    - 1280 RGB x 800
    - 1024 RGB x 600
    - 960 RGB x 640
    - 800 RGB x 600
- Display interface (support 6/8 bits)
  - RGB interface
    - SYNC + DE mode
    - SYNC only mode
  - MIPI-DSI(Display Serial Interface)interface
    - Support DSI Version 1.1
    - Support D-PHY version 1.00
  - LVDS interface(VESA/JEIDA)
- Support normally black and white panel
- Provide total 17 register value for gamma correction adjustment
- Support BIST mode
- Support GAS function for abnormal power off
- Support SPI/I2C interface
- Support dual gate
- Support Zigzag
- Support CABC
- Support eye protection mode
- Source driver output with 8-bit DAC
- OTP memory to store initialization register settings
  - OTP for GOA setting
  - OTP for gamma setting
  - 3 times OTP for VCOM setting
- Input power supply:

- VDDR = 1.65V to 3.6V (power supply for digital circuit)
- VDDI = 1.65V to 3.6V (power for interface circuit)
- VDDM = 1.65V to 3.6V (power for high speed interface)
- VCIP/VCI = 2.5V to 3.6V (power supply for analog/charge pump circuit)
- VCOM = 0V to -3.0V
- VSP = 4.5V to 6V (power supply for source circuit)
- VSN = -4.5V to -6V (power supply for source circuit)
- VGH = 8V to 20V (power supply for GOA circuit)
- VGL = -6V to -18V (power supply for GOA circuit)
- VGH, VGL: VGH-VGL<32V

- Output voltage ranges:
  - Analog voltage range for VSP:4.5V to 6.0V
  - Analog voltage range for VSP:4.5V to 6.0V
  - Positive source output voltage level: VGMP = 3V to VSP-0.2V
  - Negative source output voltage level: VGMN = -3V to VSN+0.2V
  - Positive gate driver output volage level: VGH = 8V to 20V
  - Negative gate driver output voltage level: VGL= -6V to -18V
  - VCOM = 0V to -3V
  - VGH, VGL: VGH - VGL<32V
- COG package
- Operating temperature (T_A): -30℃ to + 105℃
- Storage temperature (T_{STG}): -55℃ to + 125℃

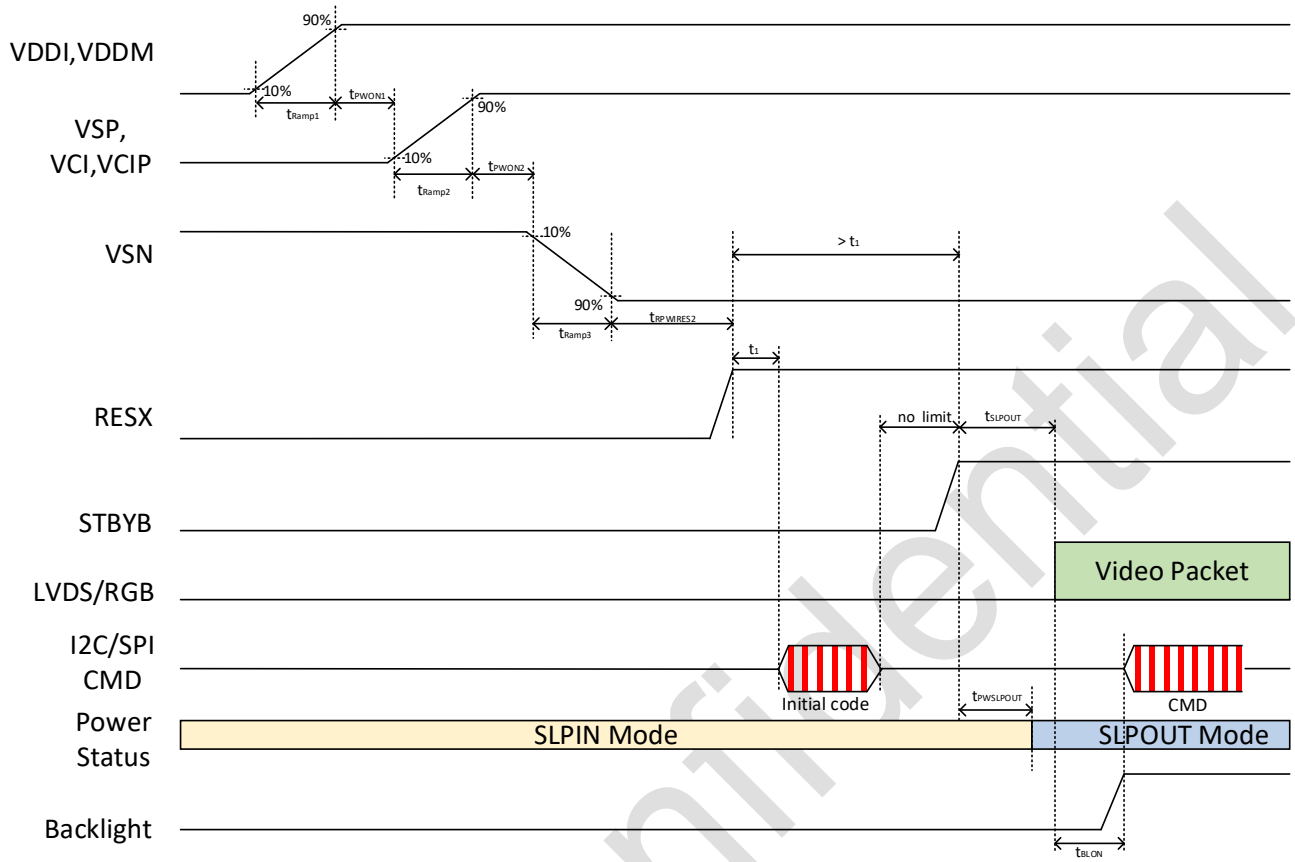
3 Device Overview

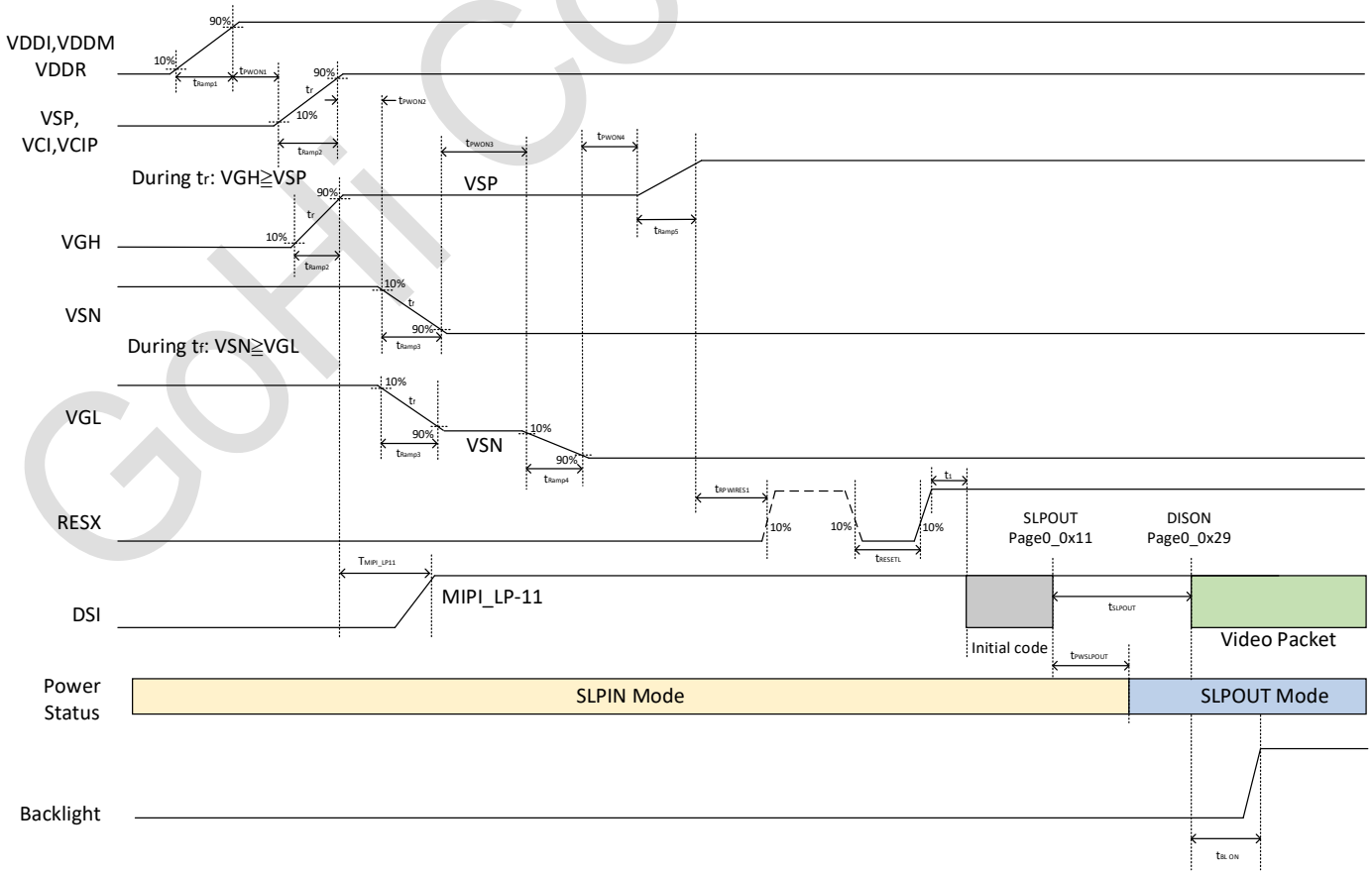
3.1 Device Block Diagram



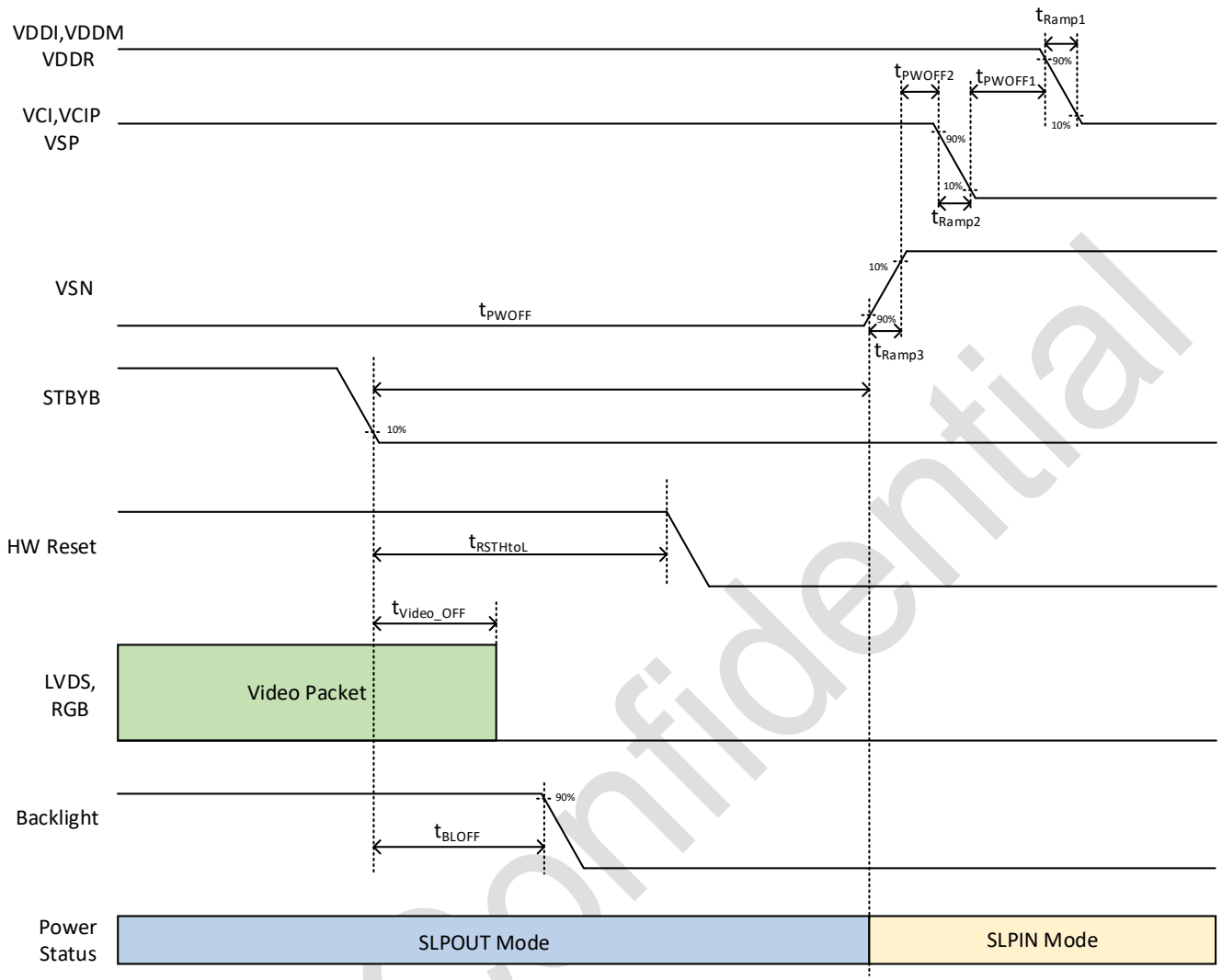
3.2 Power on/off sequence

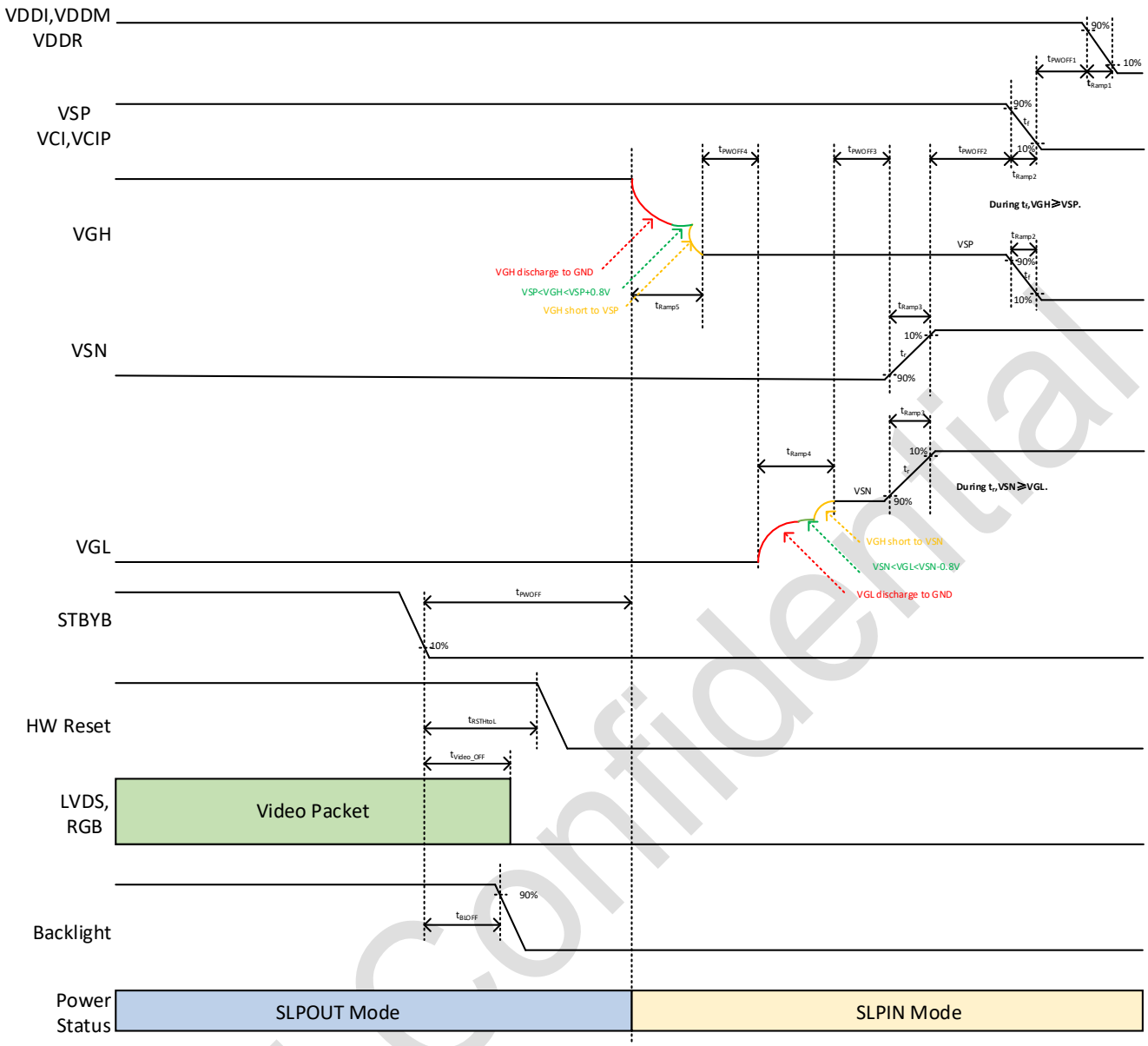
3.2.1 Power on sequence





3.2.2 Power off sequence





3.3 Output voltage range

GH8323-I1 generates corresponding voltage with α-Si LCD panel by internal power supply circuit. Please set up each voltage output according to the LCD panel.

Name	Function	Set up value	Note
VSP	DC/DC converter circuit output	+4.5V ~ +6.0V	
VSN	DC/DC converter circuit output	-4.5V ~ -6.0V	
VGMP	Reference voltage for gamma circuit	+3.0V ~ VSP-0.2V	Reference register
VGMN	Reference voltage for gamma circuit	-3.0V ~ VSN+0.2V	Reference register
VGH	Positive gate driver output voltage level	+8V ~ +20V	Depend on VSP & VSN
VGL	Negative gate driver output voltage level	-6V ~ -18V	Depend on VSP & VSN
VCOM	VCOM DC voltage	0V ~ -3V	
VDDH	Analog power for High speed interface circuit	1.5V	Depend on DSI I/F
VDDD	Digital power for internal digital circuit.	1.5V	

3.4 LCD Power Generation Scheme

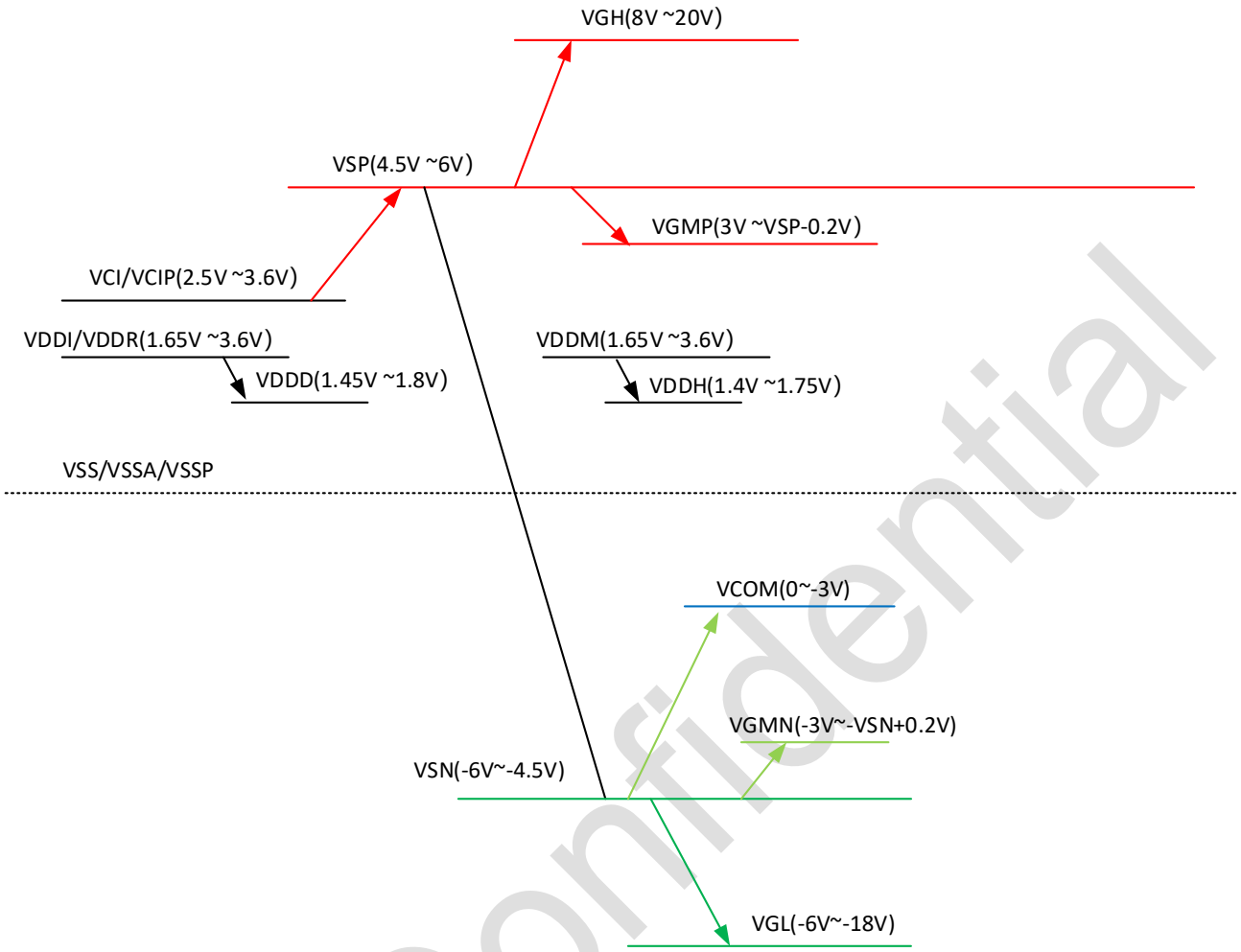


Figure 3.1: Power generation scheme

3.5 DC/DC Converter Circuit

3.5.1 DC/DC power mode 1 (VSP/VSN/VGH/VGL external power)

PM[1:0]=00 (5 power mode)

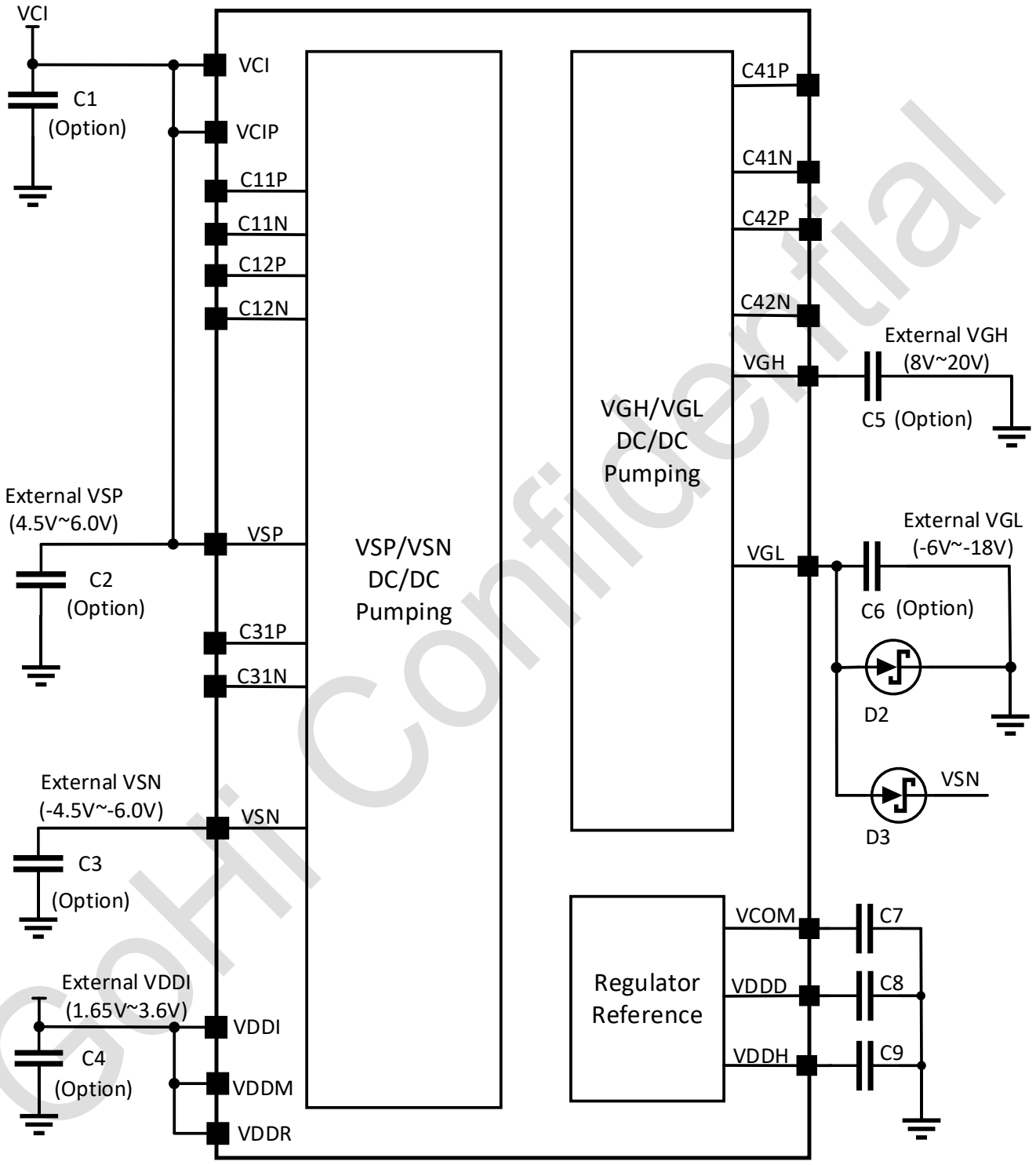


Figure 3.2: VSP/VSN/VGH/VGL external power

3.5.2 External component table for VSP/VSN/VGH/VGL external power

Pad Name	Symbol	Connection	Typical Value
VCI / VCIP	C1 (Option)	Connect to Capacitor: VCI/VCIP ---(+)----| |--- (-)---------- VSSA	2.2 μF / 6.3V
VSP	C2 (Option)	Connect to Capacitor: VSN ---(+)----| |--- (-)---------- VSSA	2.2 μF / 10V
VSN	C3 (Option)	Connect to Capacitor: VSP ---(+)----| |--- (-)----------VSSA	2.2 μF / 10V
VDDI / VDDR / VDDM	C4 (Option)	Connect to Capacitor: VDDI ---(+)----| |--- (-)----------VSSA	2.2 μF / 6.3V
VGH	C5 (Option)	Connect to Capacitor: VGH ---(+)----| |--- (-) ----------VSSA	2.2 μF / 25V
VGL	C6 (Option)	Connect to Capacitor: VGL ---(-)----| |--- (+)----------VSSA	2.2 μF / 25V
	D2	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►∫--- (+) ----------VSSA	VF < 0.4V / 20mA @ 25°C,VR ≥30V (Recommended diode: RB521S-30)
	D3	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►∫--- (+) ----------VSN	VF < 0.4V / 20mA @ 25°C,VR ≥30V (Recommended diode: RB521S-30)
VCOM	C7	Connect to Capacitor: VCOM ---(-)----| |--- (+)----------VSSA	2.2 μF / 6.3V
VDDD	C8	Connect to Capacitor: VDD ---(+)----| |--- (-) ----------VSS	2.2 μF / 6.3V
VDDH	C9	Connect to Capacitor: VDDH ---(+)----| |--- (-) ----------VSSM	2.2 μF / 6.3V

3.5.3 DC/DC power mode 2(VSP/VSN Internal Charge Pump)

PM[1:0]=01 (2 power mode)

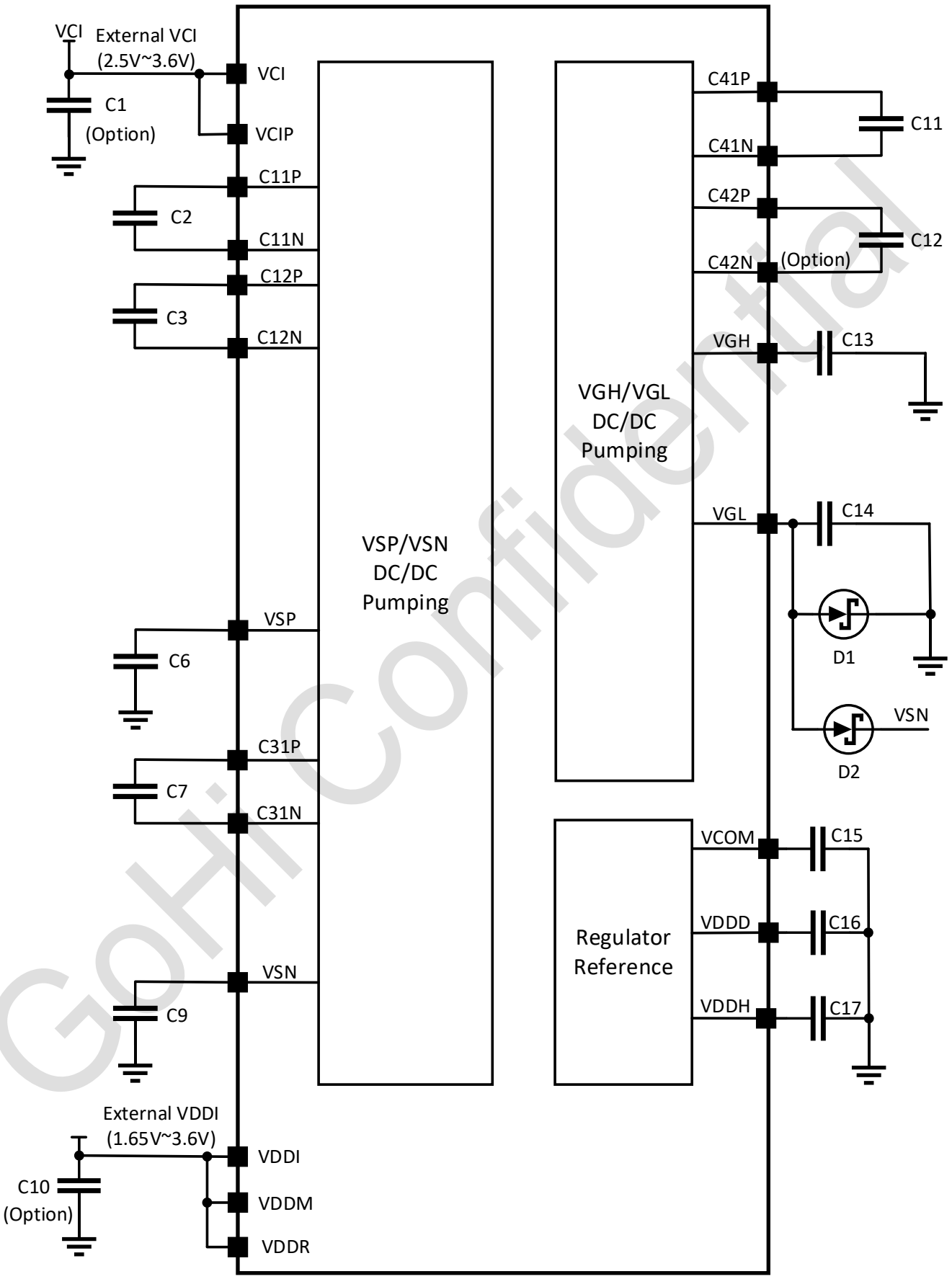


Figure 3.3: VSP/VSN Internal charge pump

3.5.4 External component table for VSP/VSN Internal Charge Pump

Pad Name	Symbol	Connection	Typical Value
VCI / VCIP	C1 (Option)	Connect to Capacitor: VCI/VCIP ---(+)----| |--- (-) ----------VSSA	2.2 μF / 6.3V
C11P –C11N	C2	Connect to Capacitor: C11P ---(+)----| |--- (-)---------- C11N	1.0 μF / 10V
C12P – C12N	C3	Connect to Capacitor: C12P ---(+)----| |--- (-)---------- C12N	1.0 μF / 10V
VSP	C6	Connect to Capacitor: VSN ---(+)----| |--- (-) ---------- VSSA	2.2 μF / 10V
C31P – C31N	C7	Connect to Capacitor: C31P ---(+)----| |--- (-)---------- C31N	1.0 μF / 10V
VSN	C9	Connect to Capacitor: VSP ---(+)----| |--- (-) ---------- VSSA	2.2 μF / 10V
VDDI / VDDR / VDDM	C10 (Option)	Connect to Capacitor: VDDI ---(+)----| |--- (-) ----------VSSA	2.2 μF / 6.3V
C41P – C41N	C11	Connect to Capacitor: C41P ---(+)----| |--- (-)---------- C41N	1.0 μF / 25V
C42P – C42N	C12	Connect to Capacitor: C42P ---(+)----| |--- (-)---------- C42N	1.0 μF / 25V
VGH	C13	Connect to Capacitor: VGH ---(+)----| |--- (-)---------- VSSA	2.2 μF / 25V
VGL	C14	Connect to Capacitor: NC ---(+)----| |--- (-) ---------- NC	1.0 μF / 25V
	D1	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►|--- (+) ---------- VSSA	VF < 0.4V / 20mA@ 25°C,VR ≥30V (Recommended diode: RB521S-30)
	D2	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►|--- (+) ---------- VSN	VF < 0.4V / 20mA @ 25°C,VR ≥30V (Recommended diode: RB521S-30)
VCOM	C15	Connect to Capacitor: VCOM ---(-)----| |--- (+) ---------- VSSA	2.2 μF / 6.3V
VDDD	C16	Connect to Capacitor: VDD ---(+)----| |--- (-)----------VSS	2.2 μF / 6.3V
VDDH	C17	Connect to Capacitor: VDDH ---(+)----| |--- (-)---------- VSSM	2.2 μF / 6.3V

3.5.5 DC/DC power mode 3 (VSP/VSN external power with GH6121)

PM[1:0]=10 (2 power mode)

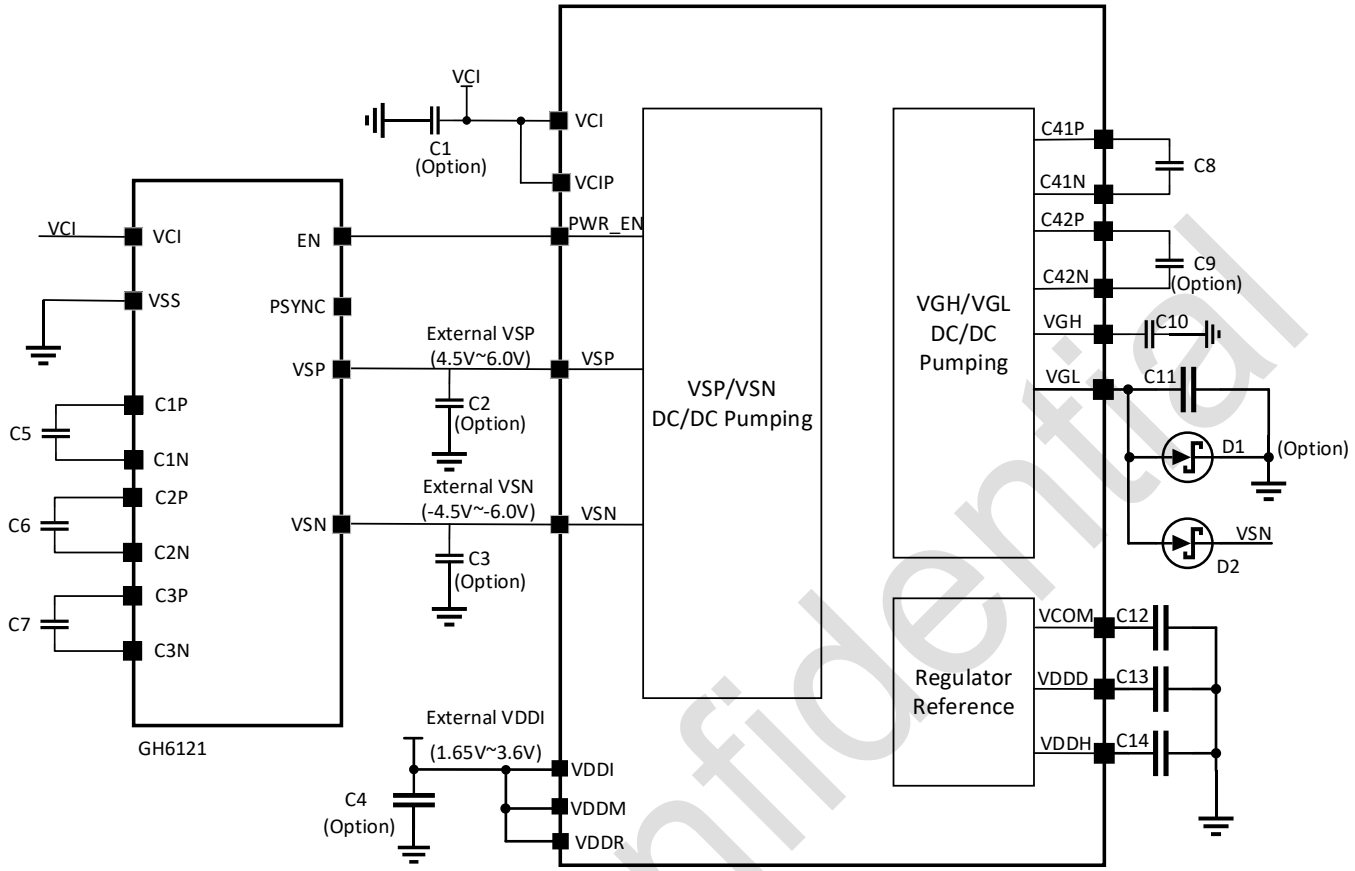


Figure 3.4: VSP/VSN external power with GH6121 power IC

3.5.6 External component table for VSP/VSN external power with GH6121

Pad Name	Symbol	Connection	Typical Value
VCI / VCIP	C1 (Option)	Connect to Capacitor: VCI/VCIP ---(+)----| |--- (-)---------- VSSA	2.2 μF / 6.3V
VSP	C2 (Option)	Connect to Capacitor: VSN ---(+)----| |--- (-) ----------VSSA	2.2 μF / 10V
VSN	C3 (Option)	Connect to Capacitor: VSP ---(+)----| |--- (-)---------- VSSA	2.2 μF / 10V
VDDI / VDDR/ VDDM	C4 (Option)	Connect to Capacitor: VDDI ---(+)----| |--- (-) ---------- VSSA	2.2 μF / 6.3V
C41P – C41N	C8	Connect to Capacitor: C41P ---(+)----| |--- (-) ---------- C41N	1.0 μF / 25V
C42P – C42N	C9	Connect to Capacitor: C42P ---(+)----| |--- (-) ---------- C42N	1.0 μF / 25V
VGH	C10	Connect to Capacitor: VGH ---(+)----| |--- (-) ---------- VSSA	2.2 μF / 25V
VGL	C11	Connect to Capacitor: VGL ---(-)----| |--- (+)---------- VSSA	2.2 μF / 25V
	D1 (Option)	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►|--- (+)---------- VSSA	VF < 0.4V / 20mA @ 25°C,VR ≥30V (Recommended diode: RB521S-30)
	D2	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►|--- (+)---------- VSN	VF < 0.4V / 20mA @ 25°C,VR ≥30V (Recommended diode: RB521S-30)
VCOM	C12	Connect to Capacitor: VCOM ---(-)----| |--- (+)----------VSSA	2.2 μF / 6.3V
VDDD	C13	Connect to Capacitor: VDD ---(+)----| |--- (-) ---------- VSS	2.2 μF / 6.3V
VDDH	C14	Connect to Capacitor: VDDH ---(+)----| |--- (-) ---------- VSSM	2.2 μF / 6.3V

3.5.7 DC/DC power mode 4(VSP/VSN external power)

PM[1:0]=11 (3 power mode)

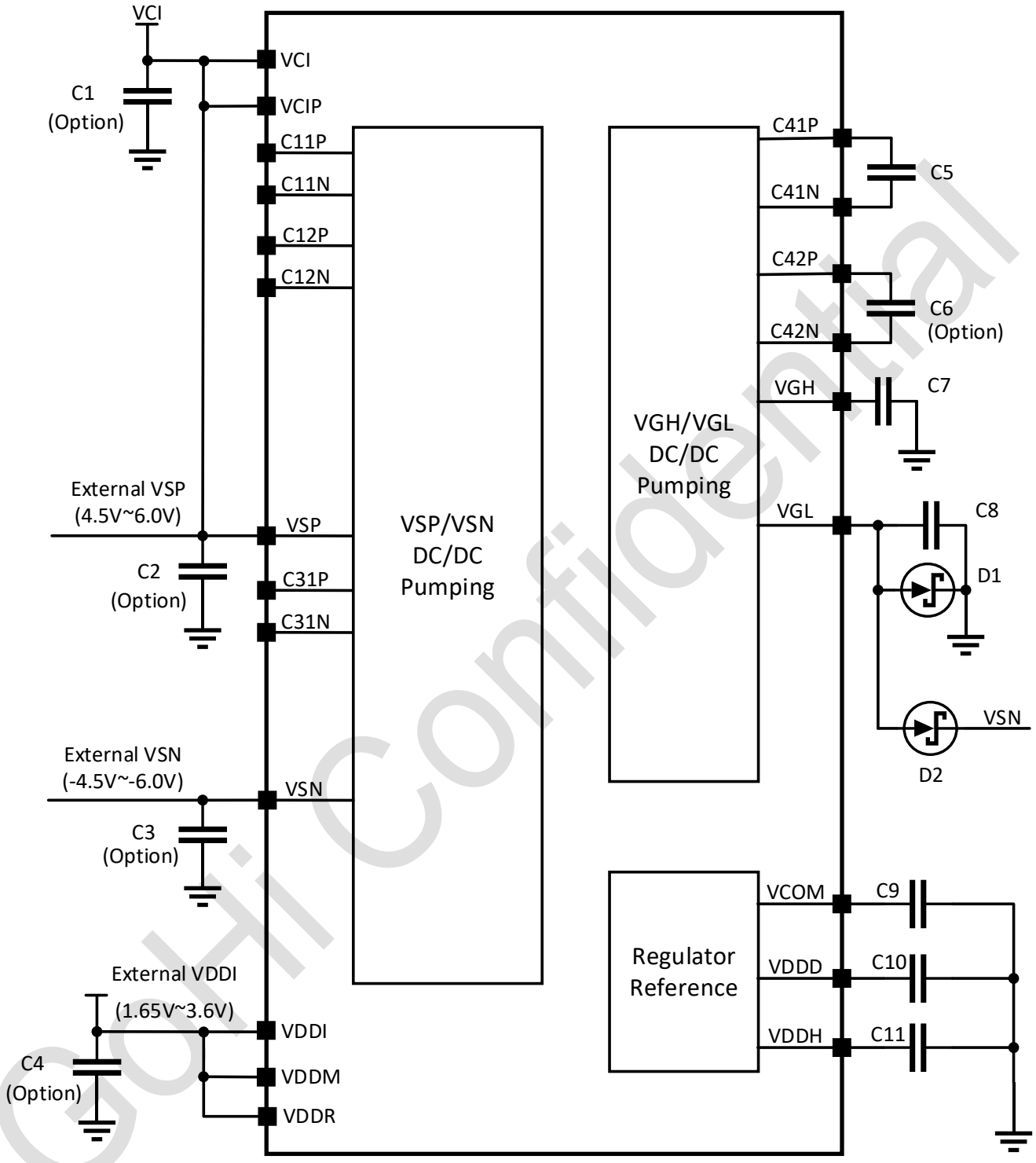


Figure 3.5: VSP/VSN external power

3.5.8 External component table for VSP/VSN external power

Pad Name	Symbol	Connection	Typical Value
VCI / VCIP	C1 (Option)	Connect to Capacitor: VCI/VCIP ---(+)----| |--- (-)---------- VSSA	2.2 μF / 6.3V
VSP	C2 (Option)	Connect to Capacitor: VSN ---(+)----| |--- (-)---------- VSSA	2.2 μF / 10V
VSN	C3 (Option)	Connect to Capacitor: VSP ---(+)----| |--- (-) ---------- VSSA	2.2 μF / 10V
VDDI / VDDR / VDDM	C4 (Option)	Connect to Capacitor: VDDI ---(+)----| |--- (-)---------- VSSA	2.2 μF / 6.3V
C41P – C41N	C5	Connect to Capacitor: C41P ---(+)----| |--- (-) ---------- C41N	1.0 μF / 16V
C42P – C42N	C6	Connect to Capacitor: C42P ---(+)----| |--- (-) ---------- C42N	1.0 μF / 16V
VGH	C7	Connect to Capacitor: VGH ---(+)----| |--- (-)---------- VSSA	2.2 μF / 25V
VGL	C8	Connect to Capacitor: VGL ---(-)----| |--- (+) ----------VSSA	2.2 μF / 25V
	D1	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►∫--- (+) ---------- VSSA	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
	D2	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►∫--- (+) ---------- VSN	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VCOM	C9	Connect to Capacitor: VCOM ---(-)----| |--- (+) ---------- VSSA	2.2 μF / 6.3V
VDDD	C10	Connect to Capacitor: VDD ---(+)----| |--- (-)----------VSS	2.2 μF / 6.3V
VDDH	C11	Connect to Capacitor: VDDH ---(+)----| |--- (-) ----------VSSM	2.2 μF / 6.3V

4 Maximum Layout Resistance

Name	Pin Definition	Maximum series resistance	Unit
VCI/VCIP, VDDI, VDDM, VDDR	Power supply	5	Ω
VCOM	Output, Capacitor Connection	5	Ω
VDDD, VDDH	Output, Capacitor Connection	5	Ω
VGMP,VGMN	Input / Output	5	Ω
VSP, VSN	Input / Output, Capacitor Connection	5	Ω
VGH, VGL	Input / Output, Capacitor Connection	10	Ω
C11P, C11N, C12P, C12N, C31P, C31N, C41P, C41N, C42P, C42N,	Capacitor Connection	5	Ω
VSS, VSSA, VSSM, VSSP	Power Supply	5	Ω
VPP	OTP Power Supply	20	Ω
DSW [1:0], IM[1:0], ADDR[1:0], PM[1:0], LANE[1:0], GIP_LRSEL[1:0]	Input	100	Ω
DIR, UPDN, REV, STBYB, LVFMT, LVBIT, CMD_SEL,BIST, DITHER_EN, HFRC_EN，CS_GIP, CAS, PNSW	Input	100	Ω
CSX, RESX, SCL, SCL_I2C	Input	100	Ω
SDA, SDA_I2C	Input / Output	100	Ω
DB[23:0], CK, VS, HS, DE	Input	100	Ω
DP<0>, DN<0>	Input / Output	5	Ω
DP<1>, DN<1>	Input	5	Ω
DP<2>, DN<2>	Input	5	Ω
DP<3>, DN<3>	Input	5	Ω
CKP, CKN	Input	5	Ω
TEST_EN	Input	100	Ω
TSOP, TSON, PWR_EN, TESTO[9:0], TE, ERR, LEDPWM, LEDON, T_S[4:1]	Output	100	Ω
SYNC_L[4:0], SYNC_R[4:0]	Input / Output	10	Ω
GOUTL[22:1], GOUTR[22:1]	Output	10	Ω
PASS1_R, PASS2_R, PASS1_L, PASS2_L	Input / Output	5	Ω

5 Pin Description

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>DP [0]/DN [0]
DP [1]/DN [1]
DP [2]/DN [2]
DP [3]/DN [3]</td><td>Input</td><td>MIPI or LVDS data input
Select by LANE[1:0]</td></tr>
<tr><td>CKP/CKN</td><td>Input</td><td>MIPI/LVDS clock Input</td></tr>
<tr><td>DB[23:0]</td><td>Input</td><td>Display data input in RGB interface, Let it to open or GND, if not used.</td></tr>
<tr><td>CK</td><td>Input</td><td>Pixel clock input in RGB interface. Must be connected to GND or open if not used.</td></tr>
<tr><td>DE</td><td>Input</td><td>Data enable input in RGB interface. Must be connected to GND or open if not used.</td></tr>
<tr><td>HS</td><td>Input</td><td>Horizontal sync input in RGB interface. Must be connected to GND or open if not used.</td></tr>
<tr><td>VS</td><td>Input</td><td>Vertical sync input in RGB interface. Must be connected to GND or open if not used.</td></tr>
<tr><td>IM[1:0]</td><td>Input</td><td>MIPI/LVDS Interface selection
<table>
<tr><td>IM[1:0]</td><td>Interface</td></tr>
<tr><td>00</td><td>MIPI</td></tr>
<tr><td>01</td><td>LVDS(default)</td></tr>
<tr><td>10</td><td>RGB</td></tr>
<tr><td>11</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>DSW[1:0]</td><td>Input</td><td>MIPI data lane swapping selection pins (default:00)
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<tr><td colspan="12">MIPI interface</td></tr>
<tr><td>DSW<1:0></td><td>PNSW</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>CKP</td><td>CKN</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td rowspan="2">2'b00</td><td>0</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>CKP</td><td>CKN</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>1</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td><td>CKN</td><td>CKP</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td></tr>
<tr><td rowspan="2">2'b01</td><td>0</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>CKP</td><td>CKN</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
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<tr><td rowspan="2">2'b10</td><td>0</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>CKP</td><td>CKN</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr>
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<tr><td rowspan="2">2'b11</td><td>0</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>CKP</td><td>CKN</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr>
<tr><td>1</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td><td>CKN</td><td>CKP</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td></tr>
</table>
LVDS data/clk Lane swapping selection pins (default:00)
<table>
<tr><td colspan="12">LVDS interface</td></tr>
<tr><td>DSW<1:0></td><td>PNSW</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>CKP</td><td>CKN</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td rowspan="2">2'b00</td><td>0</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td><td>CKP</td><td>CKN</td></tr>
<tr><td>1</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td><td>CKN</td><td>CKP</td></tr>
<tr><td rowspan="2">2'b01</td><td>0</td><td>CKP</td><td>CKN</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>1</td><td>CKN</td><td>CKP</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td></tr>
<tr><td rowspan="2">2'b10</td><td>0</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>CKP</td><td>CKN</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>1</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td><td>CKN</td><td>CKP</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td></tr>
<tr><td rowspan="2">2'b11</td><td>0</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>CKP</td><td>CKN</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr>
<tr><td>1</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td><td>CKN</td><td>CKP</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td></tr>
</table></td></tr>
<tr><td>PNSW</td><td>Input</td><td>MIPI/LVDS polarity selection pin (default:0)</td></tr>
<tr><td>RES[2:0]</td><td></td><td>Dummy pin (Let it open)</td></tr>
<tr><td>DIR</td><td>Input</td><td>The shift direction of device internal shift register is controlled by this as shown below: Normally pull high.
<table>
<tr><td>DIR</td><td>Function</td></tr>
<tr><td>H</td><td>S[0,1,2]->… ->S[2049,2050,2051] (default)</td></tr>
<tr><td>L</td><td>S[2049,2050,2051]->… ->S[0,1,2]</td></tr>
</table></td></tr>
<tr><td>UPDN</td><td>Input</td><td>Gate driver scan direction on panel module
If “UPDN”=“H”, support backward scan
If “UPDN”=“L”, support forward scan(default)</td></tr>
<tr><td>CS_SD</td><td></td><td>Dummy pin (Let it open)</td></tr>
<tr><td>REV</td><td>Input</td><td>Control whether the data of D0~D3 are inverted or not, Normally pull low.
When “REV=1” these data will be inverted. Ex. “00”->”FF“, “AA”->”55”,and so on.</td></tr>
<tr><td>PM[1:0]</td><td>Input</td><td>Power mode:
<table>
<tr><td>PM[1:0]</td><td>VDDI</td><td>VCI</td><td>VSP/VSN</td><td>VGH/VGL</td></tr>
<tr><td>00</td><td>External</td><td>VSP</td><td>External</td><td>External</td></tr>
<tr><td>01</td><td>External</td><td>External</td><td>Internal</td><td>Internal</td></tr>
<tr><td>10</td><td>External</td><td>External</td><td>PMIC</td><td>Internal</td></tr>
<tr><td>11</td><td>External</td><td>VSP</td><td>External</td><td>Internal</td></tr>
</table></td></tr>
<tr><td>DVCOM_WP</td><td>Input</td><td>Dummy pin (Let it open)</td></tr>
<tr><td>DVCOM</td><td>Input</td><td>DVCOM selection:</td></tr>
</table>

		DVCOM: Function H: Enable DVCOM L: Disable DVCOM (VCOM input from external power)
INV_SEL[0:1]	Input	Dummy pin (Let it open)
GIP_LRSEL[1:0]	Input	GIP Level shift selection: Normally pull high 00: Disable GIP level shift function 01: Enable GIP level shift on left side(right off) 10: Enable GIP level shift on right side(left off) 11: Enable GIP level shift on left and right side (default)
LANE[1:0]	Input	Select the lane mode as listed below: 00: 1 01: 2 10: 3 11: 4 (default)
ADDR[1:0]	Input	Address for I2C and SPI. Source driver location definition pin. (For CAS mode, single chip pull high)
CAS	Input	Cascade mode selection H: Cascade mode（default） L: Normal mode Refer to application Block diagram
RESX	Input	Global reset pin. Normally pull high. H: Normal operation(default) L: The controller is in reset state
STBYB	input	Standby mode. Normally pull high. STBYB=L, timing controller, source driver will turn off, all outputs are High-Z. STBYB=H. normal operation.(default)
LVFMT	Input	8-bit input format select for LVDS. Normally pull high. (only for LVDS) H: VESA format(default) L: JEIDA format
LVBIT	Input	6-bit/8-bit input select for LVDS mode. Normally pull high H: 8-bit(default) L: 6-bit
ZIGZAG	Input	Dummy pin (Let it open)
ZTPYE	Input	Dummy pin (Let it open)
CMD_SEL	Input	Command interface selection H: I2C L: 3-wire
BIST	Input	Normal Operation/BIST pattern select. Normally pull low H: BIST mode L: Normal operation (default)
DITHER_EN	Input	Dithering function enable control. Normally pull low. In LVDS 6-bit mode, IC don't care DITHER and HFRC setting. H: Enable internal dithering function L: Disable internal dithering function
HFRC_EN	Input	H-FRC selection. Normally pull low

<table>
<tr><td></td><td></td><td><table><tr><td>H</td><td>H-FRC enable</td></tr><tr><td>L</td><td>Disable H-FRC</td></tr></table></td></tr>
<tr><td>CSX</td><td>Input</td><td>Chip select pin
0: chip can be accessed
1: chip cannot be accessed.
If this pin is not used. Please connect it to VDDI.</td></tr>
<tr><td>SCL</td><td>Input</td><td>Serial clock input in SPI interface.
If not use, let it open.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Serial data input/output pin in SPI interface operation.
If not use, let it open.</td></tr>
<tr><td>SCL_I2C</td><td>I</td><td>Serial clock input in IIC interface.
If not use, please connect it to VDDI.</td></tr>
<tr><td>SDA_I2C</td><td>I/O</td><td>Serial data input/output pin in IIC interface operation.
If not use, please connect it to VDDI.</td></tr>
<tr><td>LEDON</td><td>Output</td><td>Back-light enable signal.</td></tr>
<tr><td>LEDPWM</td><td>Output</td><td>This pin is connected to the External LED driver.
PWM type control signal for brightness of the LED backlight.
If not used, please float this pin.</td></tr>
<tr><td>PWR_EN</td><td>Output</td><td>Enable power for external power IC</td></tr>
<tr><td>S[2051:0]</td><td>Output</td><td>Source output.
<table>
<tr><td>Channel select</td><td>Source channel</td><td>Disable channel</td></tr>
<tr><td>2049</td><td>S[2051:0]</td><td>-</td></tr>
<tr><td>1920</td><td>S[2051:1092] and S[959:0]</td><td>S[1091:960]</td></tr>
<tr><td>1800</td><td>S[2051:1152] and S[899:0]</td><td>S[1151:900]</td></tr>
<tr><td>1620</td><td>S[2051:1248] and S[815:0]</td><td>S[1247:816]</td></tr>
<tr><td>1602</td><td>S[2051:1248] and S[803:0]</td><td>S[1247:804]</td></tr>
<tr><td>1536</td><td>S[2051:1284] and S[767:0]</td><td>S[1283:768]</td></tr>
<tr><td>1440</td><td>S[2051:1332] and S[719:0]</td><td>S[1331:720]</td></tr>
<tr><td>1296</td><td>S[2051:1404] and S[647:0]</td><td>S[1403:648]</td></tr>
<tr><td>1284</td><td>S[2051:1404] and S[635:0]</td><td>S[1403:636]</td></tr>
<tr><td>1200</td><td>S[2051:1452] and S[599:0]</td><td>S[1451:600]</td></tr>
<tr><td>1152</td><td>S[2051:1476] and S[575:0]</td><td>S[1475:576]</td></tr>
<tr><td>1128</td><td>S[2051:1488] and S[563:0]</td><td>S[1487:564]</td></tr>
<tr><td>1080</td><td>S[2051:1512] and S[539:0]</td><td>S[1511:540]</td></tr>
<tr><td>960</td><td>S[2051:1572] and S[479:0]</td><td>S[1571:480]</td></tr>
<tr><td>810</td><td>S[2051:1644] and S[407:0]</td><td>S[1643:408]</td></tr>
<tr><td>768</td><td>S[2051:1668] and S[383:0]</td><td>S[1667:384]</td></tr>
</table></td></tr>
<tr><td>GOUTL[22:1]</td><td>Output</td><td>These pins are used for panel gate control signals. If not used, let it open.</td></tr>
<tr><td>GOUTR[22:1]</td><td>Output</td><td>These pins are used for panel gate control signals. If not used, let it open.</td></tr>
<tr><td>SYNC_L[4:0]</td><td>I/O</td><td>Sync signal for IC control(for cascade mode)</td></tr>
<tr><td>SYNC_R[4:0]</td><td>I/O</td><td>Sync signal for IC control(for cascade mode)</td></tr>
<tr><td>TSO[9:0]</td><td>T</td><td>Test pin. Float these pins for normal operation.</td></tr>
<tr><td>T_S[4:1]</td><td>T</td><td>Test pin. Float these pins for normal operation.</td></tr>
<tr><td>TEST_EN</td><td>T</td><td>Test pin. Float these pins for normal operation.</td></tr>
<tr><td>CS_GIP</td><td>T</td><td>Test pin. Float these pins for normal operation.</td></tr>
<tr><td>ERR</td><td>Output</td><td>Test pin. Float these pins for normal operation.</td></tr>
<tr><td>TE</td><td>Output</td><td>Sync pin</td></tr>
<tr><td>TP[n]</td><td></td><td>Dummy pin</td></tr>
<tr><td>DUM/DUMMY</td><td></td><td>Dummy pin</td></tr>
<tr><td>PASS1_R
PASS2_R</td><td></td><td>Pass line</td></tr>
<tr><td>PASS1_L
PASS2_L</td><td></td><td>Pass line</td></tr>
<tr><td colspan="3">Power</td></tr>
<tr><td>VDDR</td><td>PI</td><td>A power supply for analog circuit. VDDR=1.65V to 3.6V</td></tr>
<tr><td>VDDD</td><td>PO</td><td>Internal power supply for logic circuits. Connect to a stabilizing capacitor.</td></tr>
<tr><td>VSS</td><td>PI</td><td>GND for the internal logic. VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.</td></tr>
<tr><td>VDDM</td><td>PI</td><td>Interface and I/O supply for the LVDS/MIPI power regulator circuits. VDDM=1.65V to 3.6V</td></tr>
<tr><td>VDDH</td><td>PO</td><td>Internal power supply for LVDS/MIPI. Connect to a stabilizing capacitor.</td></tr>
</table>

VSSM	PI	GND for LVDS/MIPI. VSSM=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VDDI	PI	A power supply for the I/O circuit. VDDI=1.65V to 3.6V
VCI/VCIP	PI	A power for analog circuit. VCI=2.5V to 3.6V
VSSA	PI	Analog ground. VSSA=0V
VSSP	PI	Ground for charge pump
VSP	PI/PO	Positive power.
VSN	PI/PO	Negative power.
VGMP	PO	Positive regulated voltage output(3V to 6.2V).
VGMN	PO	Negative regulated voltage output(-3V to -6.2V).
VGH	PO	Output voltage from the step-up circuit. Connect to a stabilizing capacitor between VGH and system ground.
VGL	PO	Output voltage from the step-up circuit. Connect to a stabilizing capacitor between VGL and system ground.
VCOM	PO	The power supply of common voltage in DC com driving. Connect to a stabilizing capacitor between VCOM and system ground.
VPP	I	External High voltage pin is used in OTP program mode. The power is operate at 8.25V. If not used. let them open.
DC/DC pumping		
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	I/O	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VSP voltage. If not used let them open.
C31P, C31N C32P, C32N	I/O	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VSN voltage. If not used let them open.
C41P, C41N C42P, C42N	I/O	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH/VGL voltage. If not used let them open.

6 Interface

The GH8323-I1 supports SPI / I2C(Command W/R), RGB, LVDS, DSI(Display Serial Interface). The interface mode can be selected by IM[1:0] and CMD_SEL pins setting as show in Table 6.1.

CMD_SEL	Command IF
0	I2C
1	SPI

IM[1:0]		Display IF
0	0	DSI
0	1	LVDS
1	0	RGB
1	1	Not used

Table 6.1: Interface selection

6.1 SPI Interface

GH8323-I1 use the 3-Wire serial port as communication interface for all the function and command setting. 3-Wire communication can be bi-directional controlled by the “R/W command index”.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

6.1.1 SPI interface write mode

Write command + data protocol:

Byte	Command + Data	
	Value	Description
1	0xF1	WR command index
2	0x4C	Data index
3	0x02	Data number
4	0xB0	Command address
5	0x12	Data 1
6	0x34	Data 2

Byte	Command Only	
	Value	Description
1	0xF1	WR command index
2	0x4C	Data index
3	0x00	Data number
4	0x11	Command address

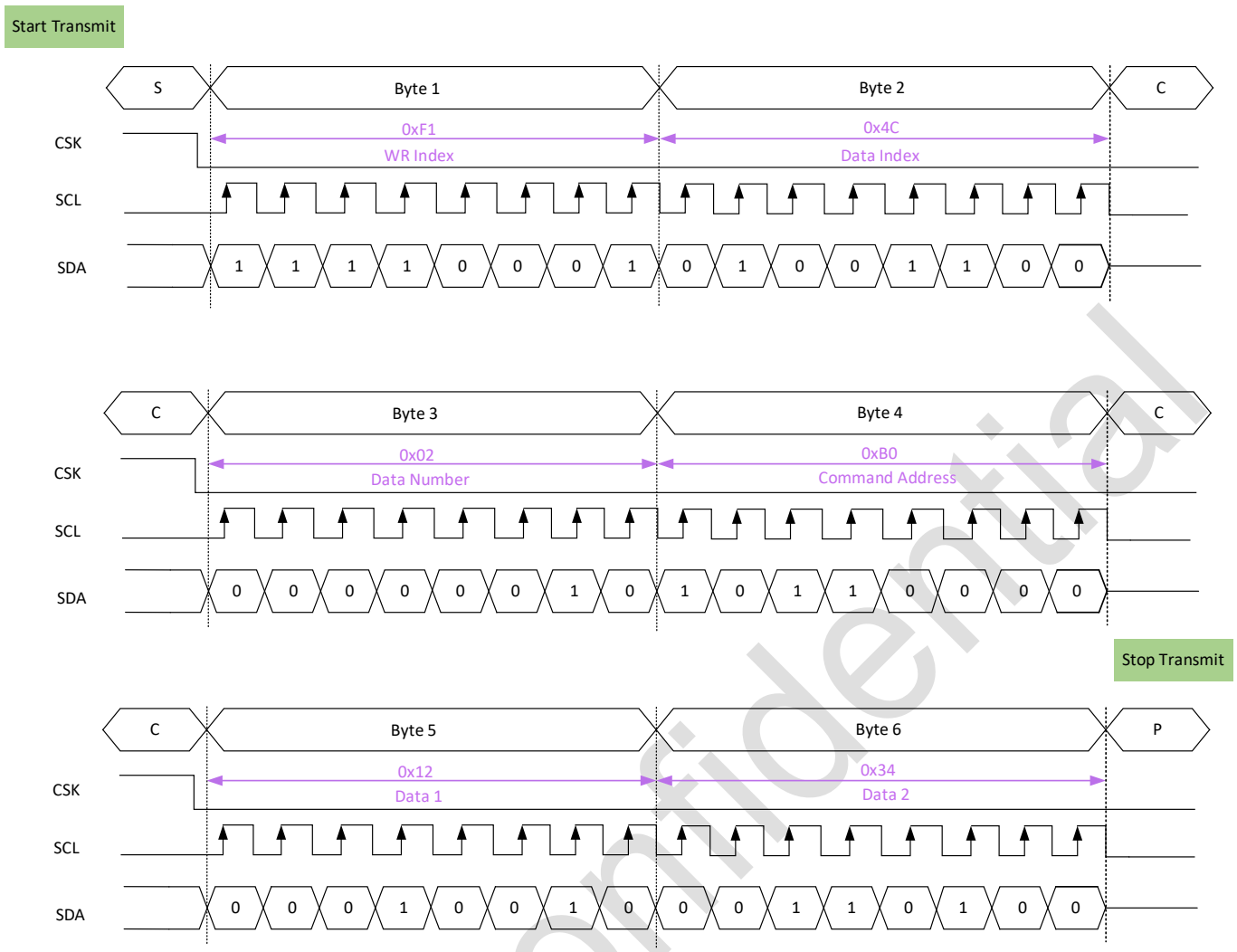


Figure 6.1: SPI Write Command + Data transmitter

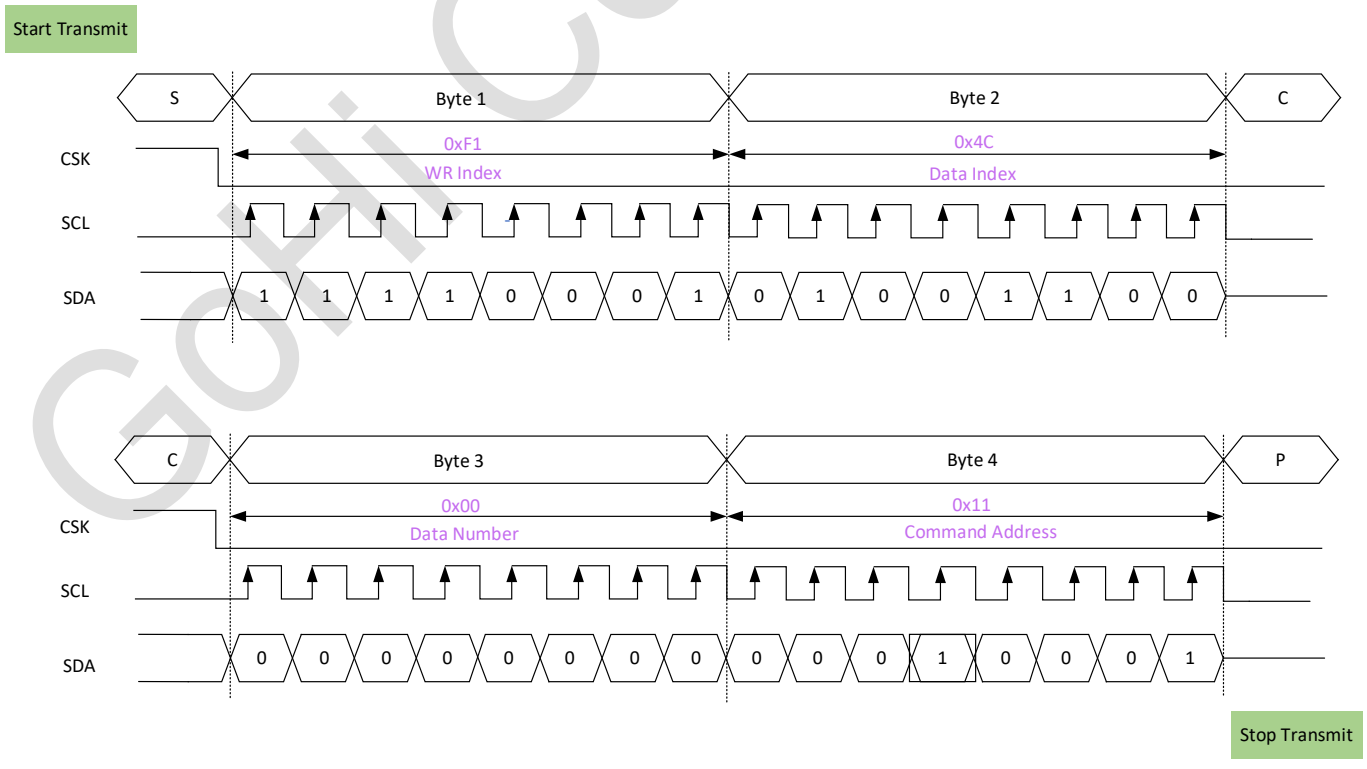


Figure 6.2: SPI Write Command Only transmitter

6.1.2 SPI interface read mode

Read command + data protocol:

Byte	Command + Data	
	Value	Description
1	0xF2	RD command index
2	0x01	Data index
3	0x02	Data number
4	0xB0	Command address
5	X	Read Data 1
6	X	Read Data 2

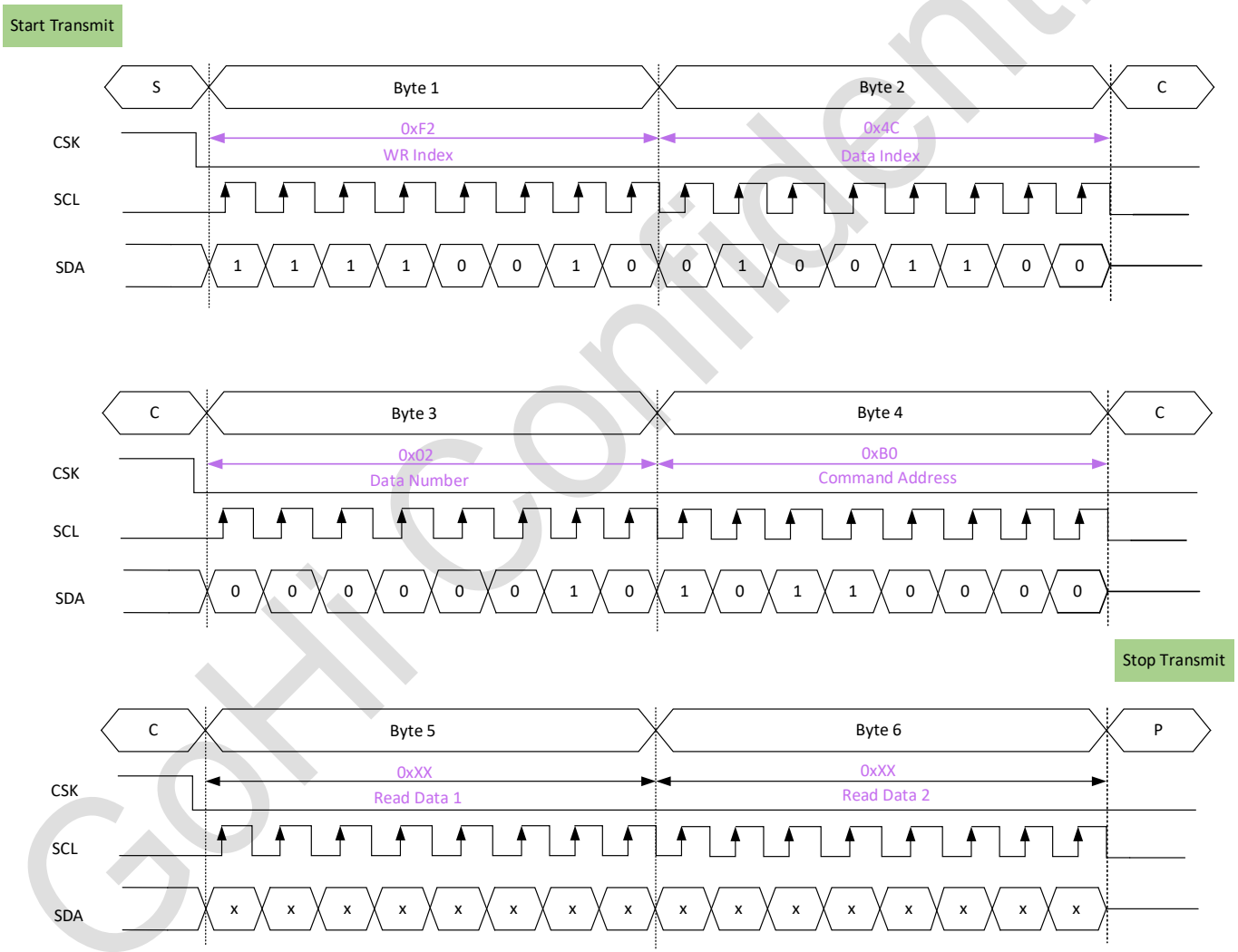


Figure 6.3: SPI Read Command + Data transmitter

6.2 I2C Interface

6.2.1 I2C format

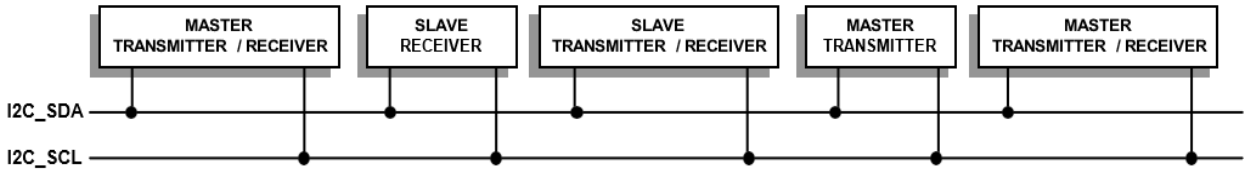
The I2C-bus is for bi-directional, two-line communication between different lcd or modules. The two lines are the Serial Data line (I2C_SDA) and the Serial Clock Line (I2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

I2C-Bus Protocol:

Before any data is transmitted on the I2C-bus, the device which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

Definitions:

- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



6.2.2 Command Write Sequence of I2C Interface

GH8323-I1 supports register write sequence via I2C-bus transfer. The register writing support single register write mode and multi-register write mode. The detail transference sequences are illustrated and described as below.

1) Data transfers for register writing follow the format is shown in below.
2) After the START condition (S), a slave address is sent. R/W bit is setting to “0” for WRITE.
3) The slave issues an ACK to master.
4) 8 bits command address transfer first then transfer the register data parameter.
5) A data transfer is always terminated by a STOP condition.
6) GH8323-I1 DA[6:0] = 100_1000(0x48, ADDR pin = ”0”) or DA[6:0] = 100_1001(0x49, ADDR pin=”1”)

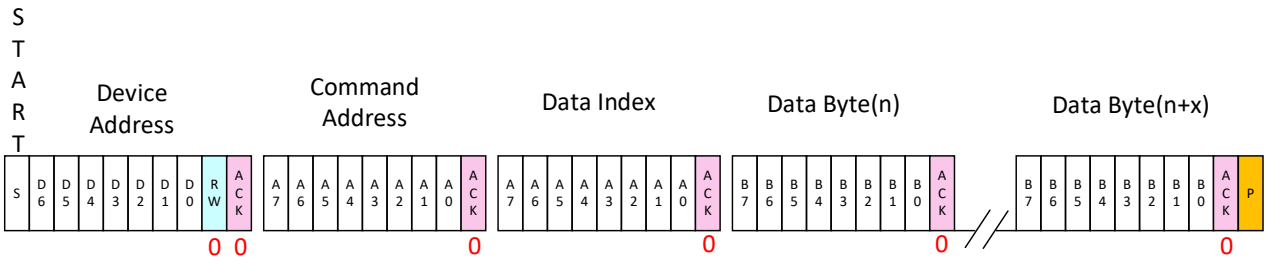


Figure 6.4: I2C Write Command + Data transmitter

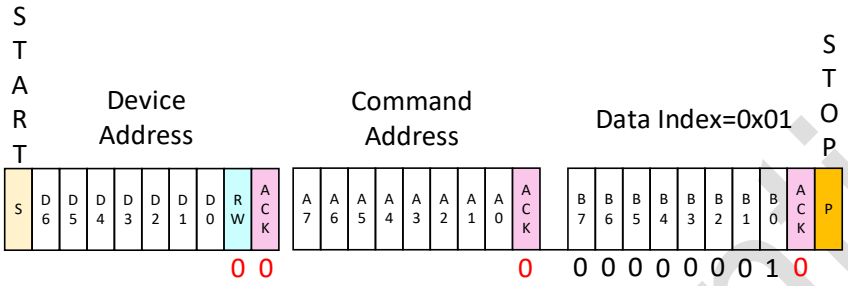


Figure 6.5: I2C Write Command Only transmitter

6.2.3 Command Read Sequence of I2C Interface

GH8323-I1 supports register read sequence via I2C-bus transfer. Register data reading transfers follow the format and is shown in below.

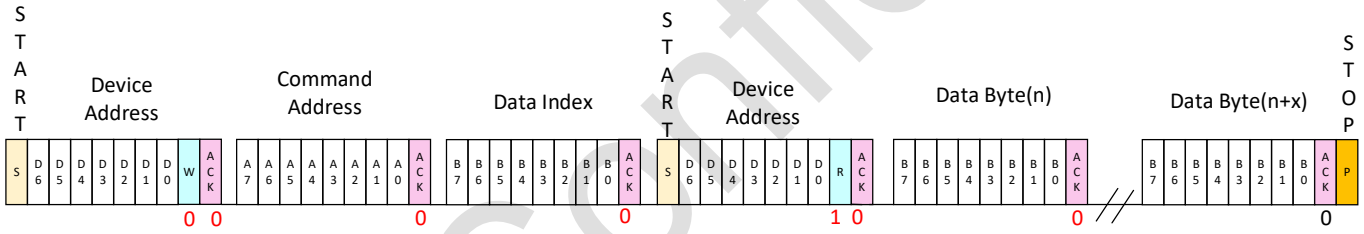


Figure 6.6:I2C Read Command + Data transmitter

6.3 RGB interface

6.3.1 General timing diagram

The image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). If it is returned from out of the range to in range timings, then the correct display image must be displayed automatically (by the display module) on the next frame (vertical sync.).

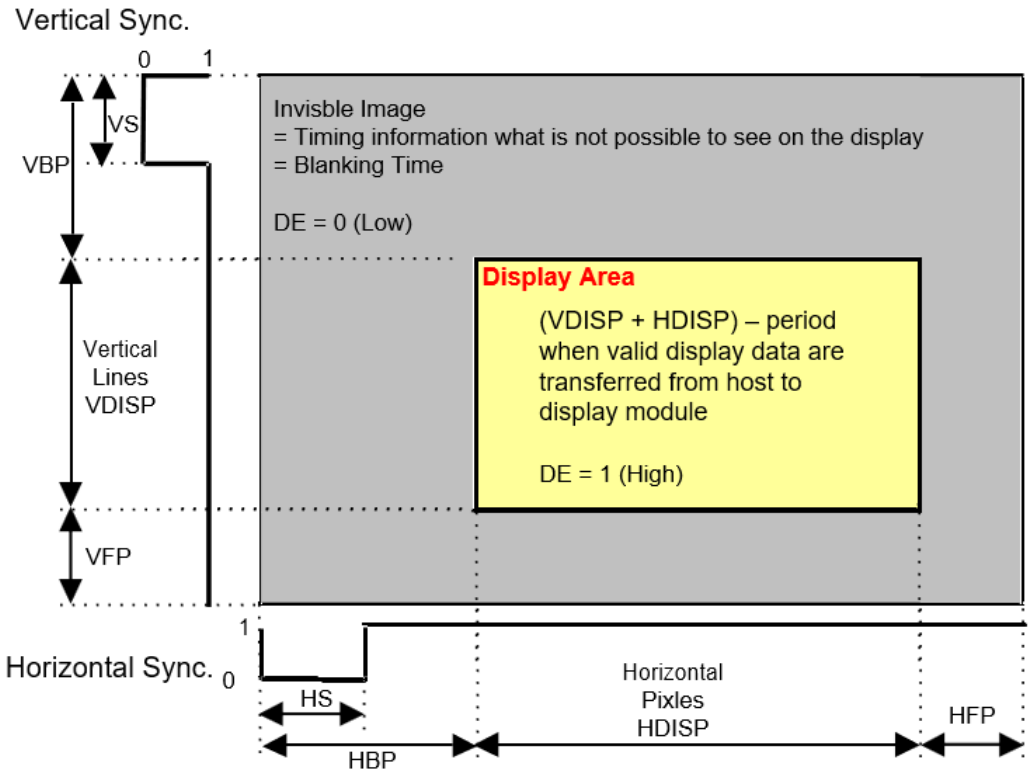


Figure 6.7: General timing diagram

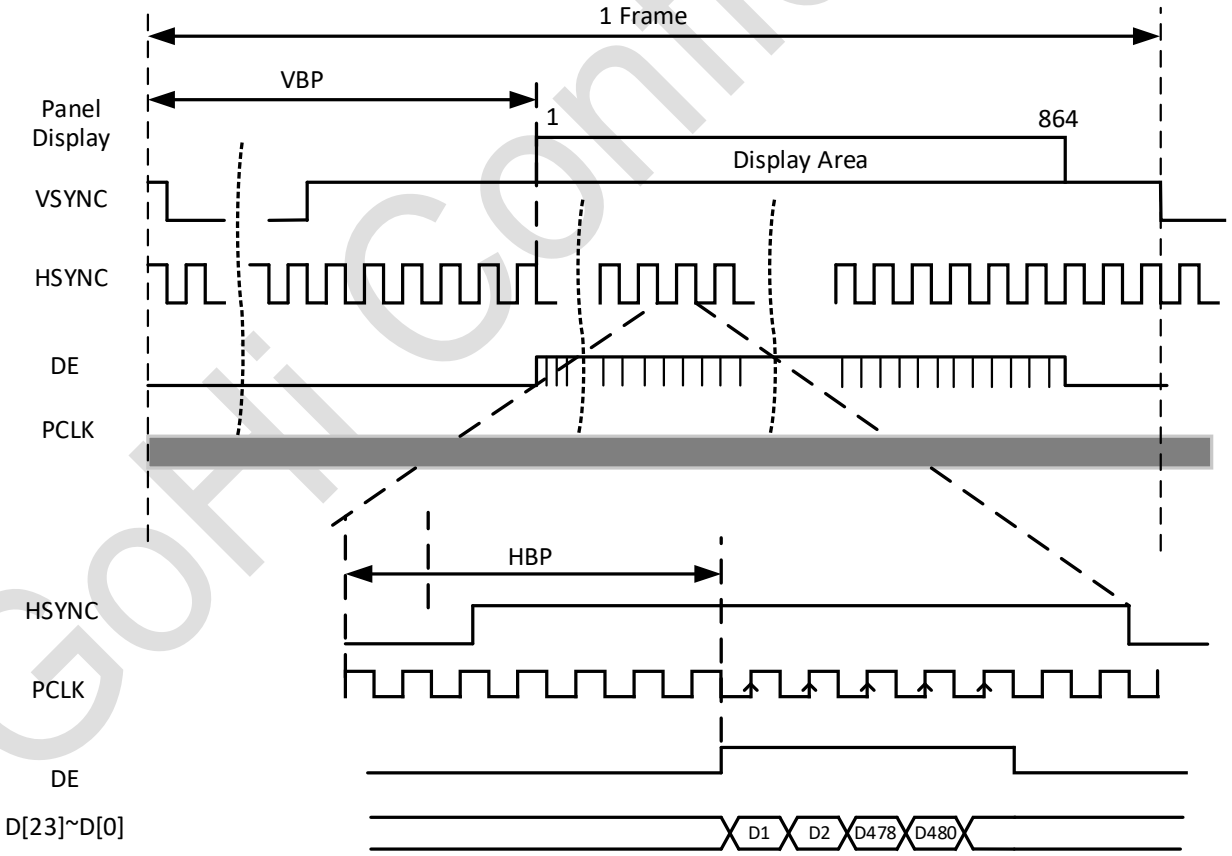


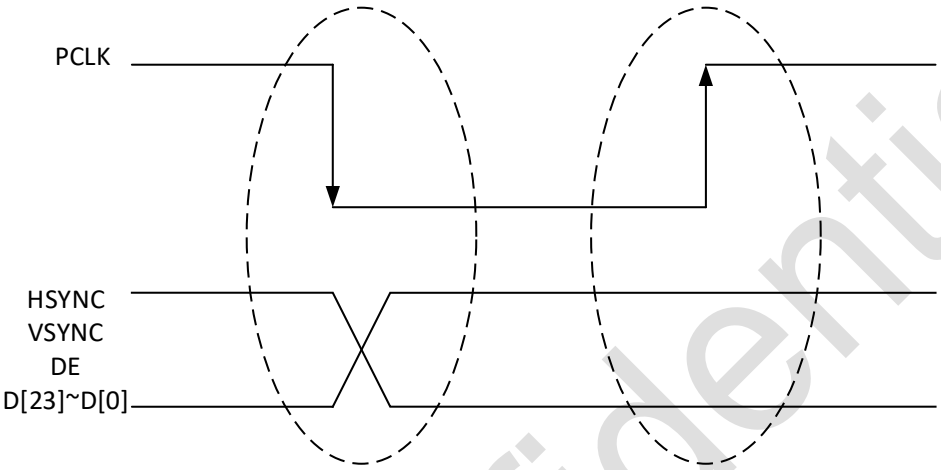
Figure 6.8: RGB (800RGB x 480) timing diagram

6.3.2 RGB Data format

The GH8323-I1 supports 16-bit, 18-bit or 24-bit parallel RGB interface which includes: HS, VS, DE, CK, DB[23:0]. The interface is active after Power On sequence. Pixel clock (CK) is

running all the time without stopping and it is used to entering HS, VS, DE and D[23:0] lines states when there is a rising edge of the CK. The CK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In– mode etc. Vertical synchronization (VS) is start signal to receive a “new frame” of the display. This is negative (“-“, “0”, low) active by rising edge of the CK-line. Horizontal synchronization (HS) is start signal to receive a “new line” of the frame. This is negative (“-“, “0”, low) active by rising edge of the CK- line. Data enable (DE) is used to receive RGB information that should be transferred on the display. This is positive (“+”, “1”, high) active by rising edge of the CK-line.

The pixel clock cycle is described in the following figure.



Note: CK is an unsynchronized signal (It can be stopped).

Figure 6.9: CK cycle

Data format	DB 23	DB 22	DB 21	DB 20	DB 19	DB 18	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 09	DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00
24bit (3Ah=0x70)	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18bit (3Ah=0x60)	R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0		
16bit (3Ah=0x50)	R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0			

Table 6.2: RGB Interface data format

6.3.3 RGB interface mode select

GH8323-I1 support RGB interface mode 1(SYNC + DE mode) and mode 2(SYNC only mode), it is select by USER command.

In RGB mode 1(SYNC + DE mode), writing data to line buffer is done by CK and Video Data Bus (D[23] to D[0]), when DE is high state. The external clocks (CK, VS and HS) are used for internal displaying clock. So, controller must always transfer CK, VS and HS signal to GH8323-I1.

In RGB mode 2(SYNC only mode), back porch of VS VBP is defined by VBP[7:0]. And back porch of HS HBP is defined by HBP[7:0]. Front porch of VS VFP is defined by VFP[7:0]. And front porch of HS HFP is defined by HFP[7:0].

RGB mode	VS	HS	DE	CK	D[23] ~ D[0]	Register VFP[7:0] ,VBP[7:0], HFP[7:0], HBP[7:0]
Mode 1	Used	Used	Used	Used	Used	Not used
Mode 2	Used	Used	Not used	Used	Used	Used

6.4 LVDS interface

6.4.1 LVDS Data format

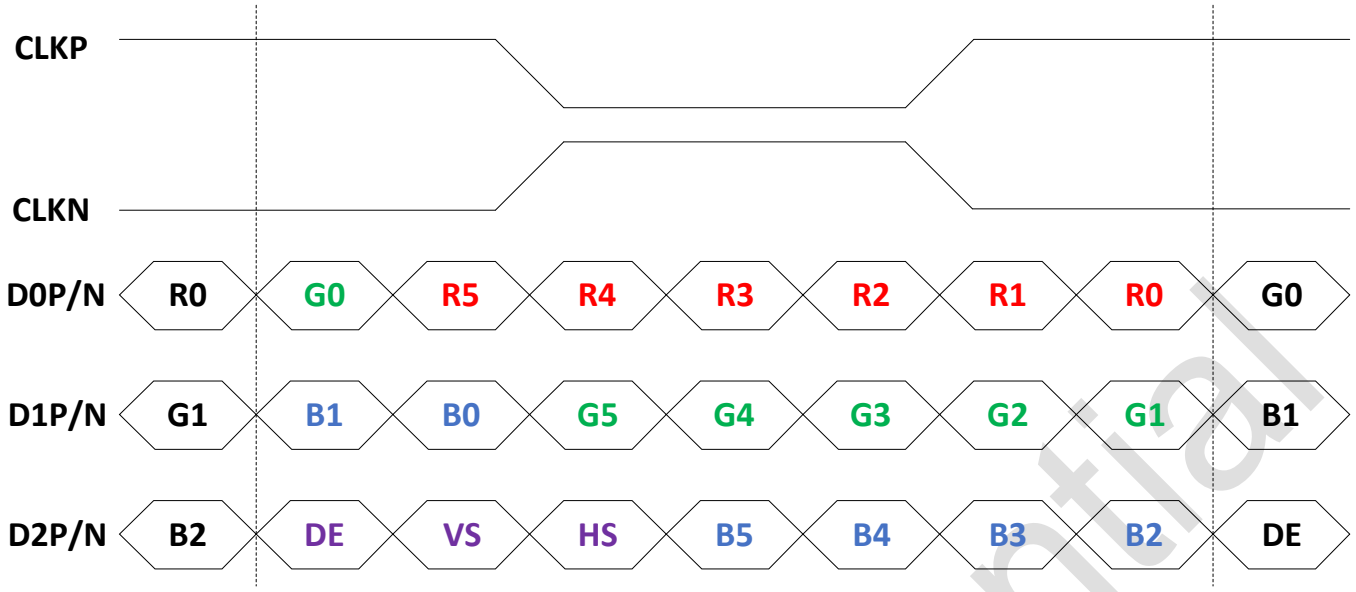


Figure 6.10: 6-bit LVDS input (IM[1:0]=01, LANE[1:0]=10, LVFMT=Don't care)

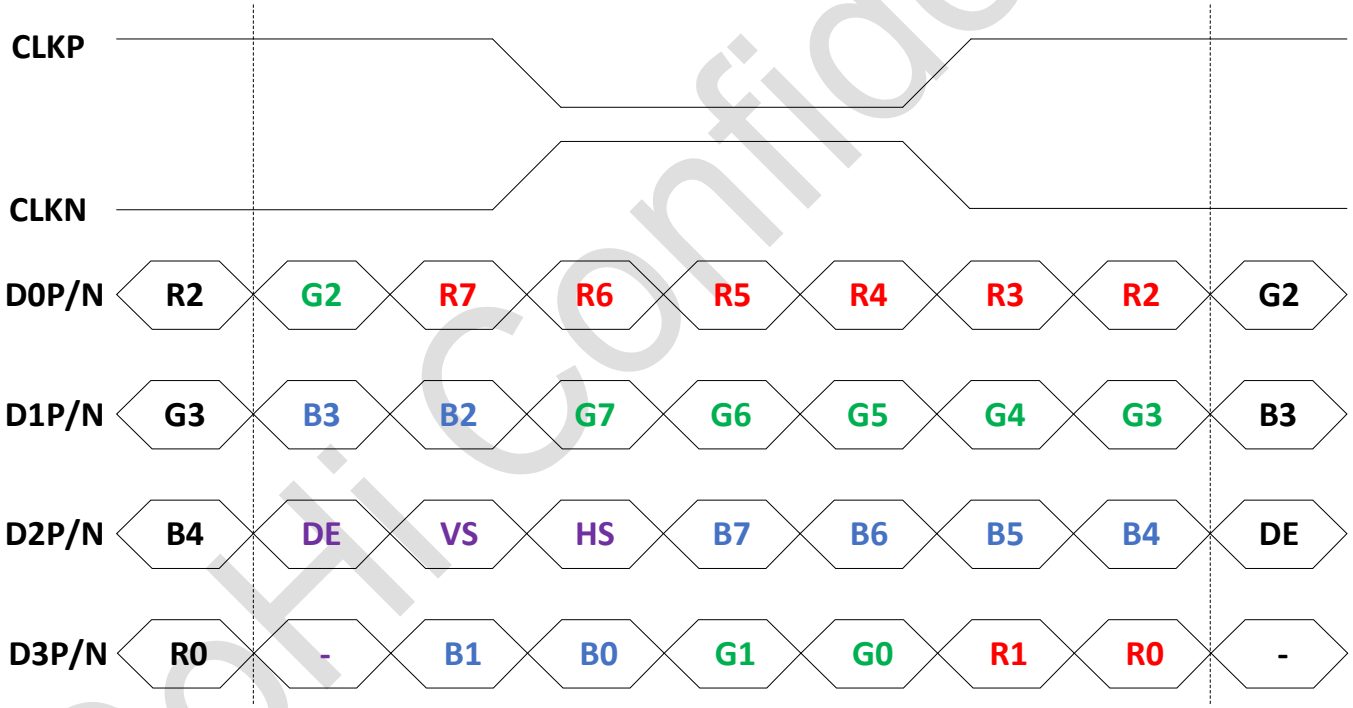


Figure 6.11: 8-bit LVDS input (IM[1:0]=01, LANE[1:0]=11, LVFMT=1(JEIDA))

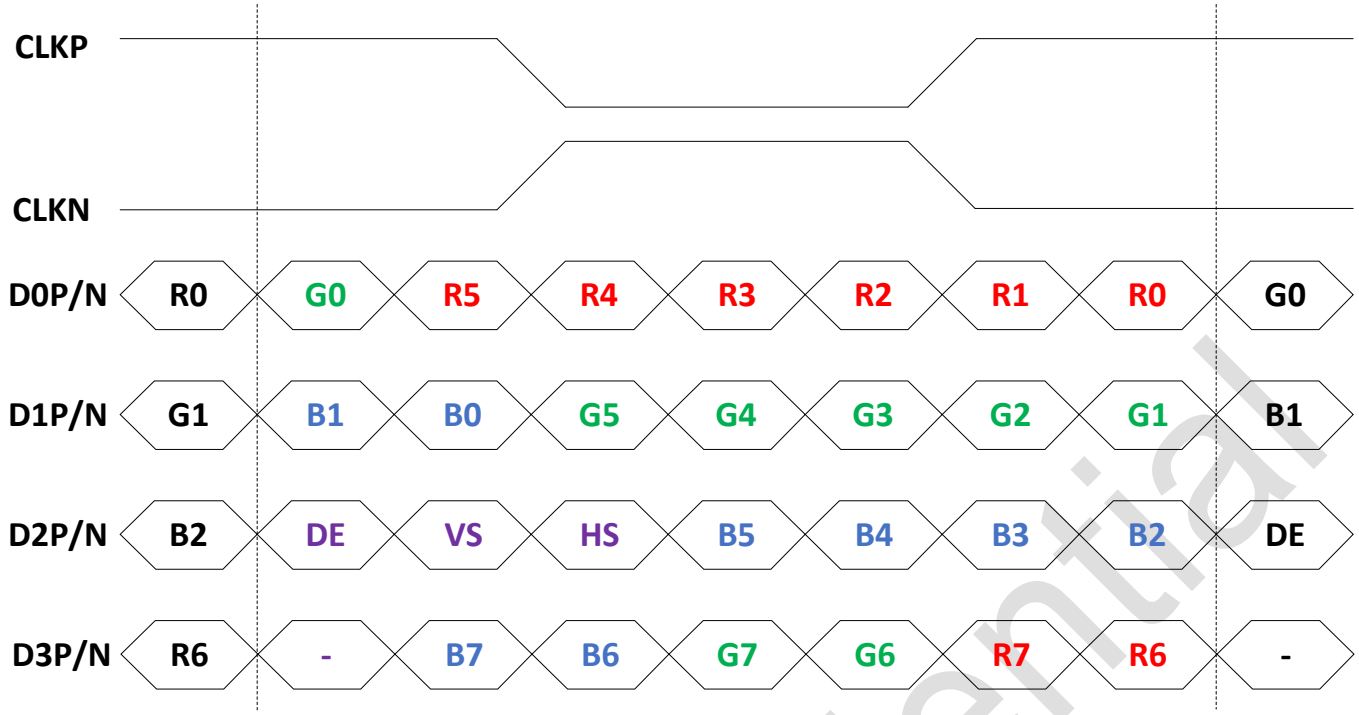


Figure 6.12: 8-bit LVDS input (IM[1:0]=01, LANE[1:0]=11, LVFMT=0(VESA))

6.4.2 LVDS Input Timing Table

For 1366RGBx768

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	69.7	75	80.9	MHz
HSYNC period time		T_H	1468	1550	1596	DCLK
Horizontal display area		T_{HD}	1366			DCLK
HSYNC pulse width	Min.	T_{HPW}	2			
	Typ.		-			
	Max.		40			
HSYNC back porch(with pulse width)		T_{HFP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	14	96	142	DCLK
VSYNC period time		T_V	792	806	840	H
Vertical display area		T_{VD}	768			H
VSYNC pulse width	Min.	TV_{PW}	2			H
	Typ.		-			
	Max.		20			
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

For 1280RGBx800

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	66.3	72.4	78.9	MHz
HSYNC period time		T_H	1380	1440	1500	DCLK
Horizontal display area		T_{HD}	1280			DCLK
HSYNC pulse width	Min.	T_{HPW}	2			
	Typ.		-			
	Max.		40			
HSYNC back porch(with pulse width)		T_{HFP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	14	72	132	DCLK
VSYNC period time		T_v	824	838	872	H
Vertical display area		T_{VD}	800			H
VSYNC pulse width	Min.	T_{VPW}	2			H
	Typ.		-			
	Max.		20			
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

6.5 DSI system interface

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards.

Figure 7.13 DSI transmitter and receiver interface shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.

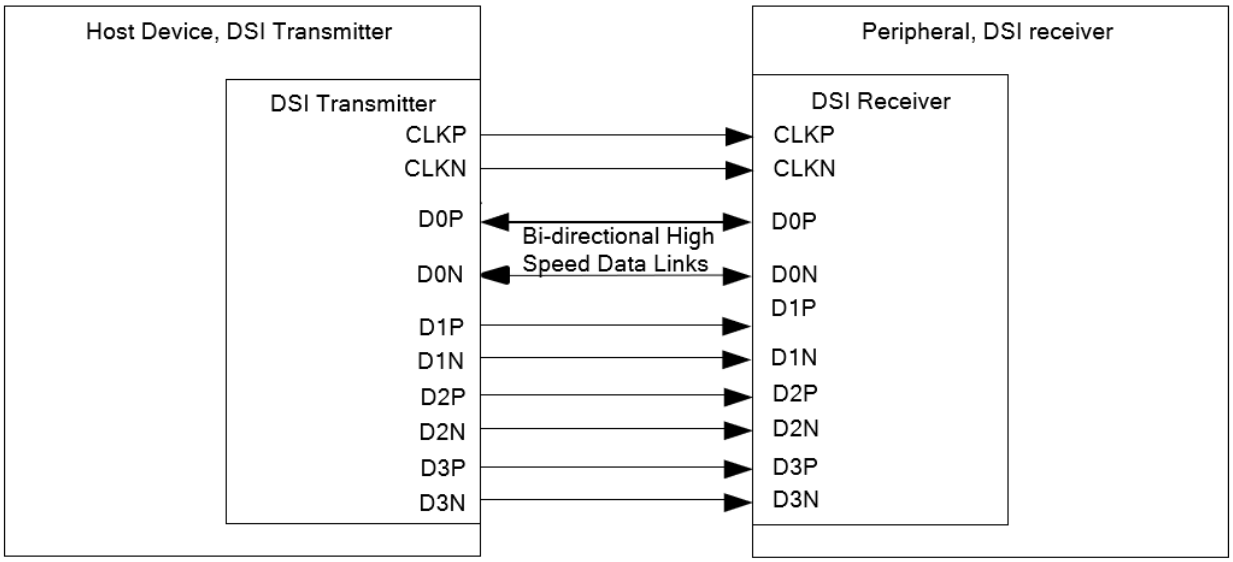


Figure 6.13 DSI transmitter and receiver interface

A conceptual vide of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown in Figure 6.14.

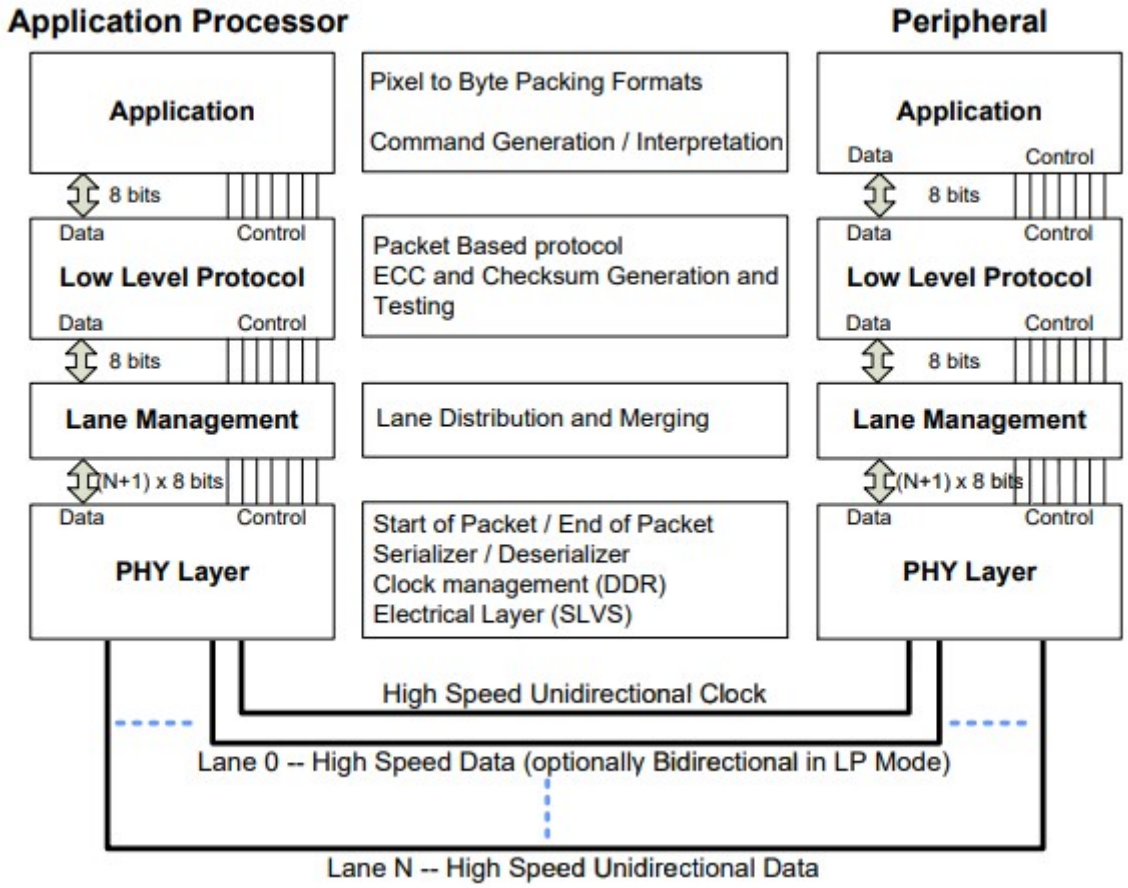


Figure 6.14: DSI Layer

PHY Layer: The PHY Layer specifies transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures “ones” and “zeroes” from the serial bit stream. Bit-level and byte-level synchronization mechanisms are included as part of the PHY.

Lane Management Layer: DSI is Lane-scalable for increased performance. The number of data signals may be 1, 2, 3, or 4 depending on the bandwidth requirements of the application. The transmitter side of the interface distributes the outgoing data stream to one or more Lanes (“distributor” function). On the receiving end, the interface collects bytes from the Lanes and merges them together into a recombined data stream that restores the original stream sequence (“merger” function).

Protocol Layer: At the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets. The protocol defines required headers for each packet, and how header information is generated and interpreted. The transmitting side of the interface appends header and error-checking information to data being transmitted. On the receiving side, the header is stripped off and interpreted by corresponding logic in the receiver. Error-checking information may be used to test the integrity of incoming data. DSI protocol also documents how packets may be tagged for interleaving multiple command or data streams to separate destinations using a single DSI.

Application Layer: This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module. The DSI specification describes the mapping of pixel values, commands and command parameters to bytes in the packet assembly.

6.5.1 Command mode, Video mode and Virtual Channel

DSI-compliant peripheral support either of two basic modes of operation: Command Mode

and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Virtual Channel Capability

While this specification only addresses the connection of a host processor to a single peripheral, DSI incorporates a virtual channel capability for communication between a host processor and multiple, physical display modules. Since interface bandwidth is shared between peripherals, there are constraints that limit the physical extent and performance of multiple-peripheral systems. The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a common DSI Link. The DSI specification makes no requirements on the specific value assigned to each virtual channel used to designate interlaced fields, For clarity, the first interlaced video field may be assigned as DI[7:6] = 2'b00 and the second interlaced video field may be assigned DI[7:6] = 2'b01.

Note1: GH8323-I1 support both command mode and video mode.

6.5.2 Power-up Sequence Example

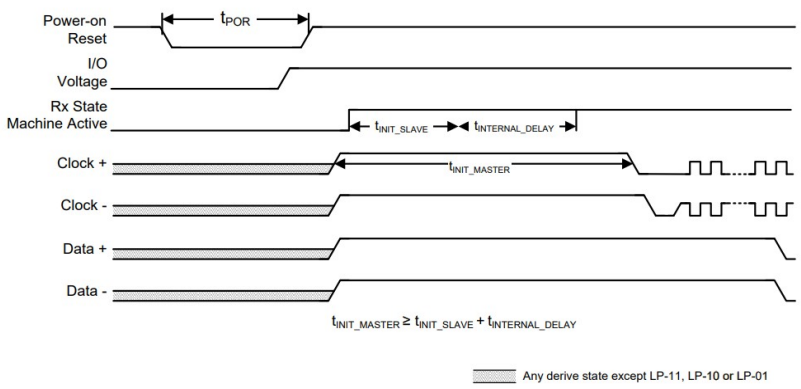


Figure 6.15: Peripheral Power-Up Sequencing Example

6.5.3 DSI Format

Information is transferred between host processor and peripheral using one or more serial data signals and accompanying serial clock. The action of sending high-speed serial data across the bus is called a HS transmission or burst. Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 7.4 shows the basic structure of a HS transmission. N is the total number of bytes sent in the transmission

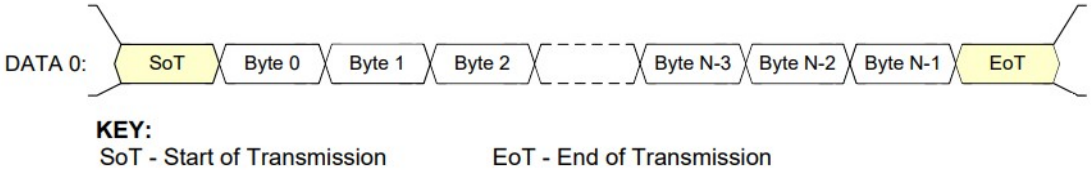


Figure 6.16: Basic HS Transmission Structure

Multi Lane Distribution and Merging

DSI is a Lane-scalable interface. Applications requiring more bandwidth than that provided by one Data Lane may expand the data path to two, three, or four Lanes wide and obtain approximately linear increases in peak bus bandwidth.

Multi-Lane implementations shall use a single common clock signal, shared by all Data Lanes. Conceptually, between the PHY and higher functional blocks is a layer that enables multi-Lane operation.

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission. Figure 6.17 & Figure 6.18 illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

Number of Bytes, N transmitted is an integer multiple of the number of lanes:

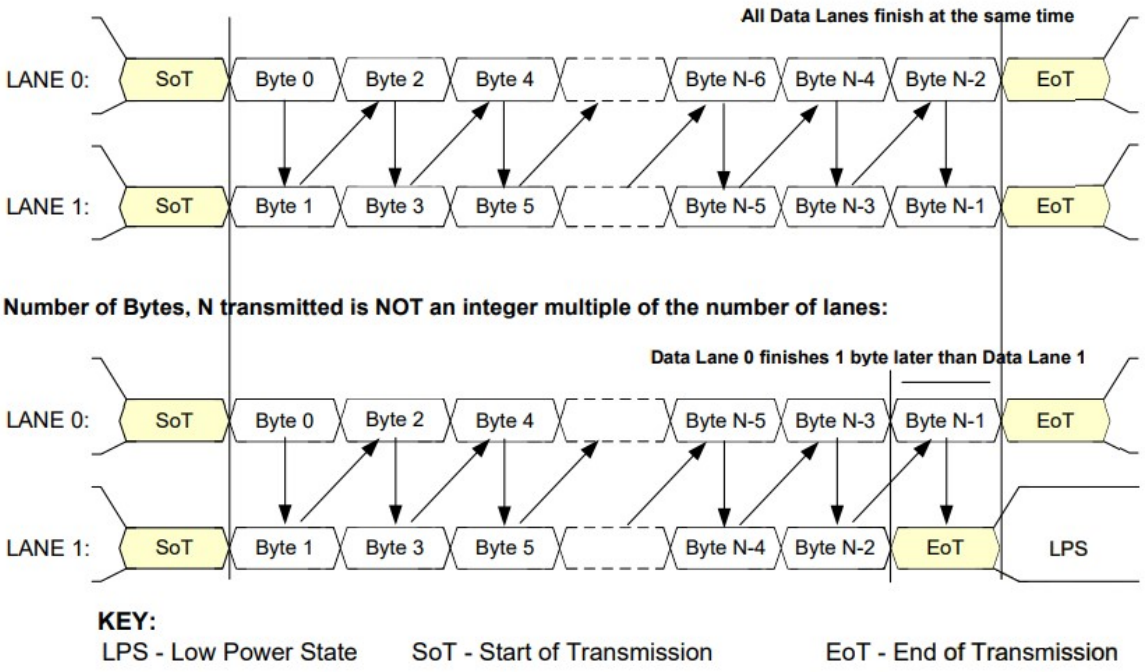


Figure 6.17: Two Lane HS Transmission Example

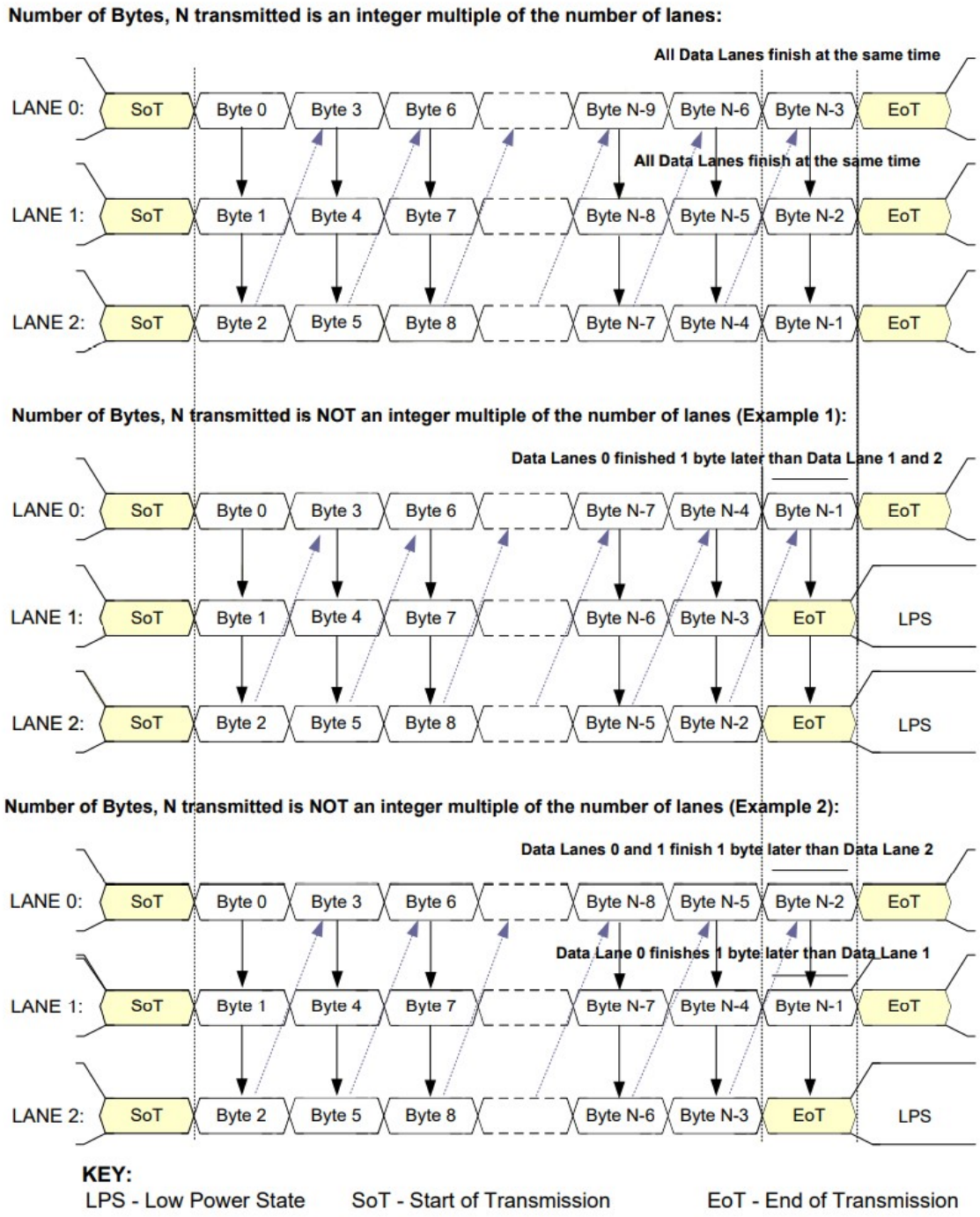


Figure 6.18: Three Lane HS Transmission Example

6.5.4 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets, following the packet organization documented in this section. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY.

6.5.5 Multiple Packets per Transmission

In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many

registers may be loaded with separate write commands at system startup.

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled. The method of enabling or disabling this capability is out of scope for this document.

The top diagram in Figure 7.19 illustrates a case where multiple packets are being sent separately with EoTp support disabled. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets. This constraint does not apply to LP transmissions. The bottom diagram in Figure 7.19 demonstrates a case where multiple packets are concatenated within a single HS transmission.

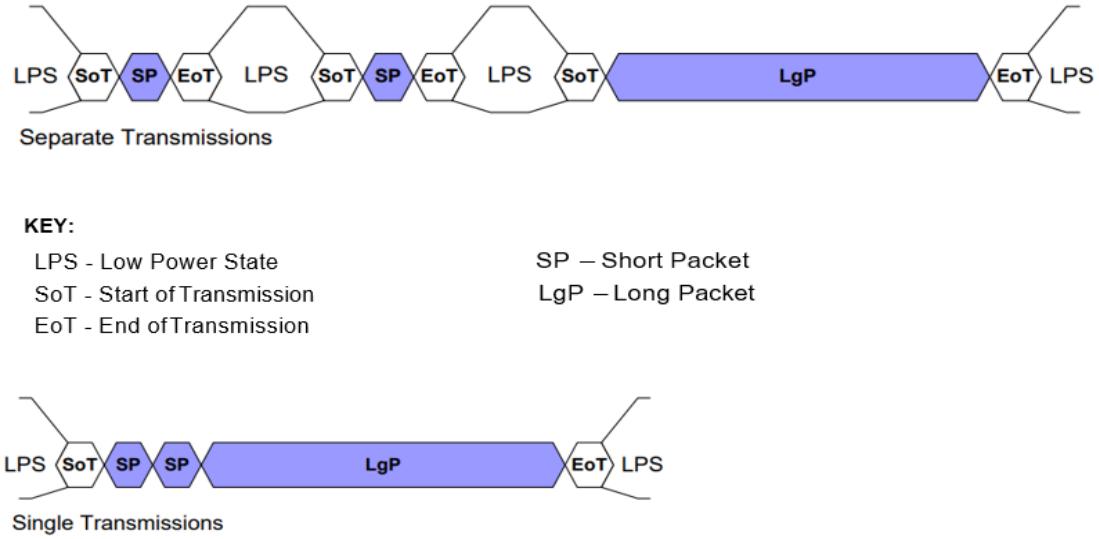


Figure 6.19: HS Transmission Examples with EoTp disabled

Figure 6.20 depicts HS transmission cases where EoTp generation is enabled. In the figure, EoT short packets are highlighted in red. The top diagram illustrates a case where a host is intending to send a short packet followed by a long packet using two separate transmissions. In this case, an additional EoT short packet is generated before each transmission ends. This mechanism provides a more robust environment, at the expense of increased overhead (four extra bytes per transmission) compared to cases where EoTp generation is disabled, i.e. the system only relies on the PHY layer EoT sequence for signaling the end of HS transmission. The overhead imposed by enabling EoTp can be minimized by sending multiple long and short packets within a single transmission as illustrated by the bottom diagram in Figure 6.8.

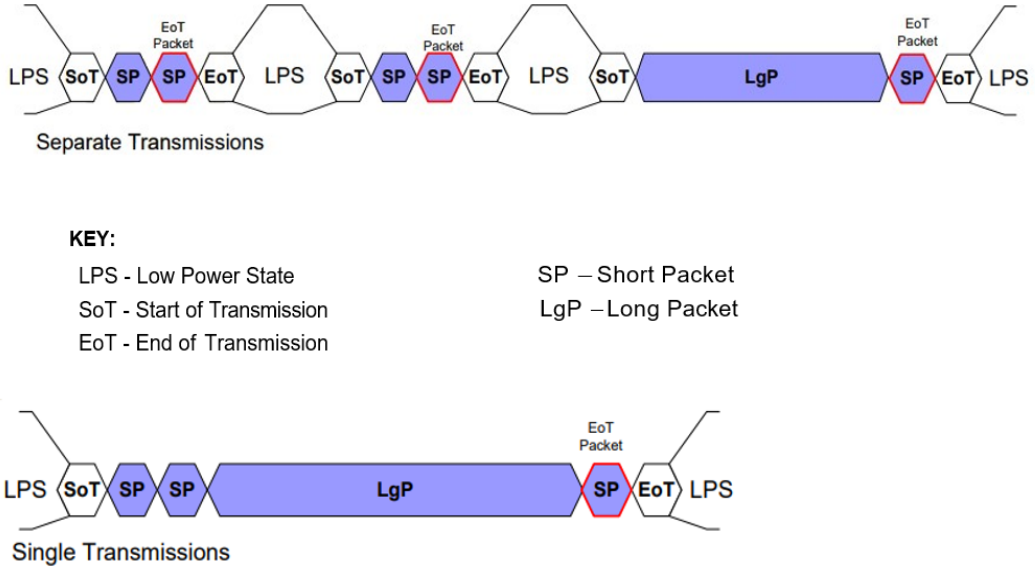


Figure 6.20: HS Transmission Examples with EoTp enabled

6.5.6 Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure 6.21 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

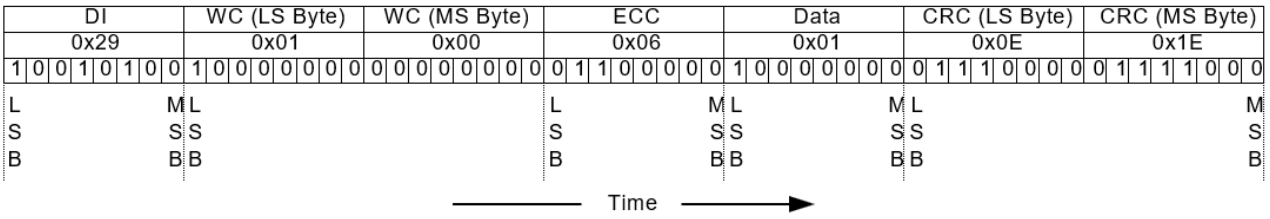


Figure 6.21: Endian Example (Long Packet)

6.5.7 Packet Structure

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Packet sizes fall into two categories:

•**Long packets** specify the payload length using a two-byte Word Count field. Payloads may be from 0 to 216- 1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

•**Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

6.5.8 Long Packet

Figure 6.22 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable

number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length

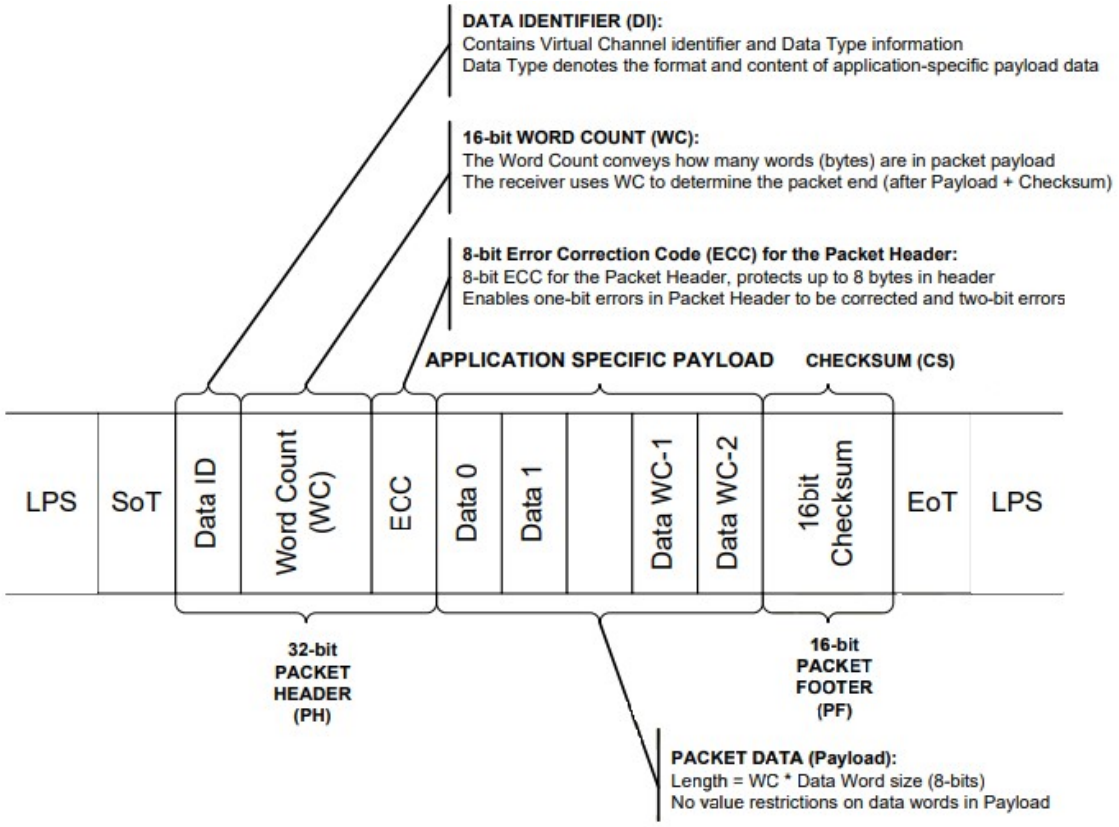


Figure6.22: Long Packet Structure

The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data.

The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count.

The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields.

After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used.

Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (0xFFFF). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0x0000). In the generic case, the length of the Data Payload shall be a multiple of bytes.

Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first.

6.5.9 Short Packet

Figure 6.23 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

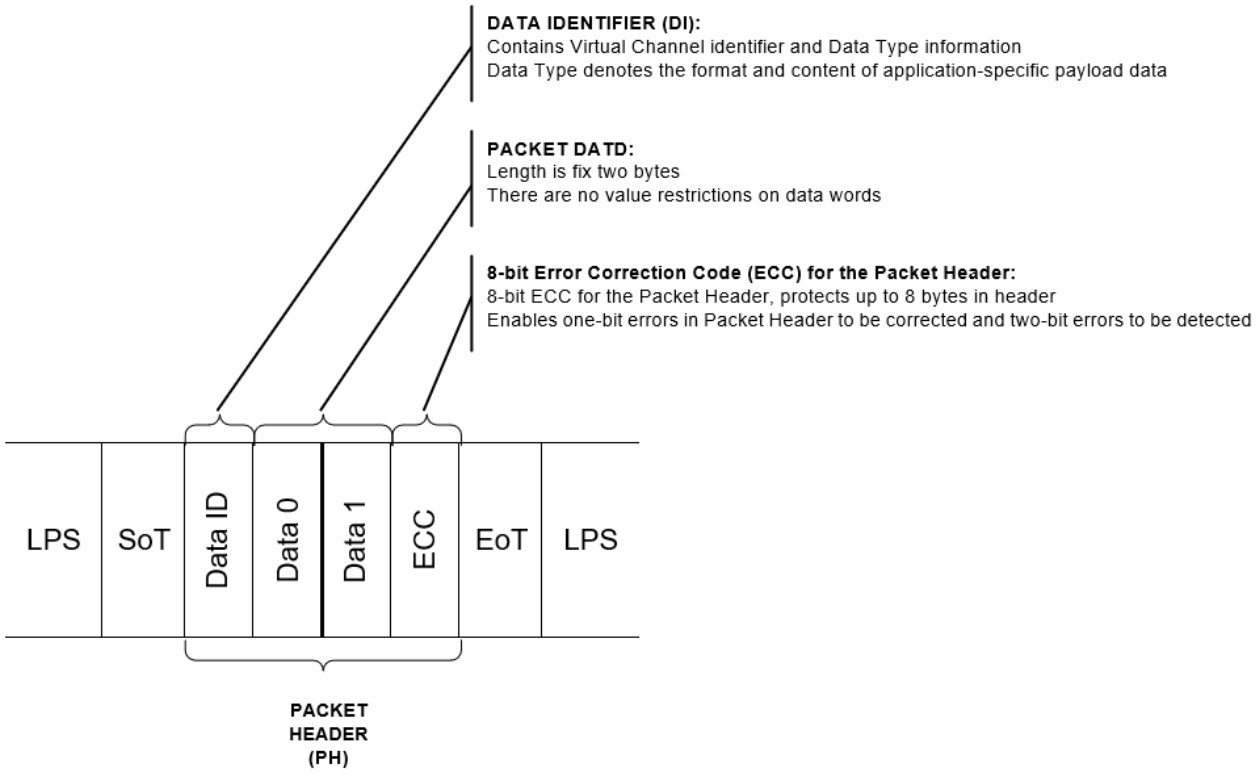


Figure 6.23: Short Packet Structure

6.5.10 Common Packet Elements

Long and Short packets have several common elements that are described in this section.

6.5.11 Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 6.12 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels. DI[5:0]: These six bits specify the Data Type.

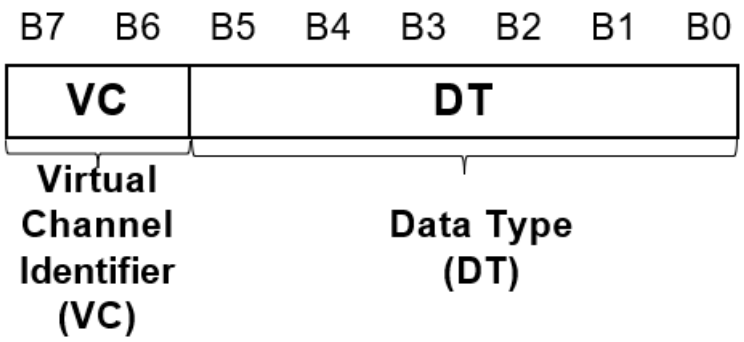


Figure 6.24: Data Identifier Byte

6.5.12 Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel.

6.5.13 Data Type Field DT[5:0]

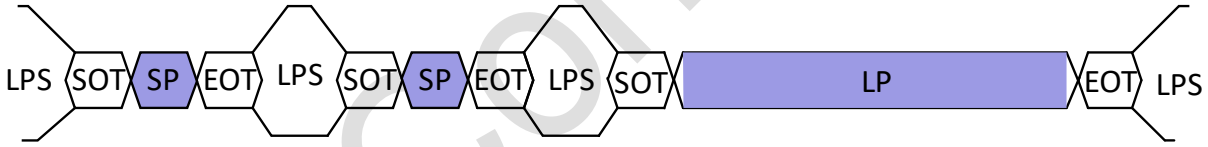
The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

6.5.14 ECC

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

6.5.15 DSI packet

The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Below figure illustrates multiple HS Transmission packets.



LPS：Low power state

SOT：Start of Transmission

SP：Short Packet

LP：Long Packet

EOT：End of Transmission

6.5.16 Processor-sourced Packets

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 6.4.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x02	00 0010	Color Mode (CM) Off Command	Short
0x12	01 0010	Color Mode (CM) On Command	Short
0x22	10 0010	Shut Down Peripheral Command	Short
0x32	11 0010	Turn On Peripheral Command	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short

0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write/write_LUT Command Packet	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
0xX0 and 0xXF unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

6.5.17 Packed Pixel Stream, 16-bit Format, Long Packet

Packed Pixel Stream 16-Bit Format shown in Figure 6.25 is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Within a color component, the LSB is sent first, the MSB last. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

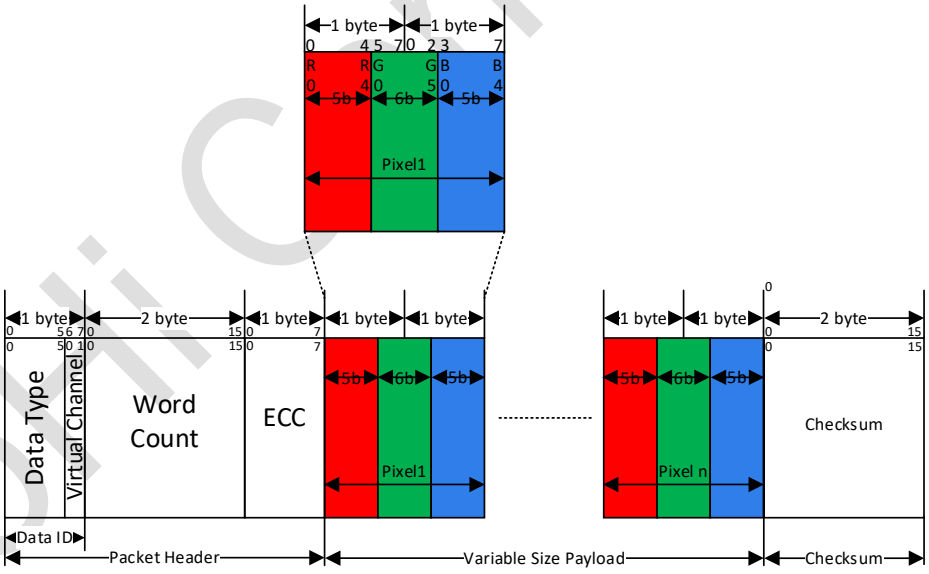


Figure6.25: 16-bit per Pixel – RGB Color Format, Long Packet

6.5.18 Packed Pixel Stream, 18-bit Format, Long Packet

Packed Pixel Stream 18-Bit Format (Packed) shown in Figure 6.26 is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly

divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. Peripheral will not display the fill pixels when refreshing the display device.

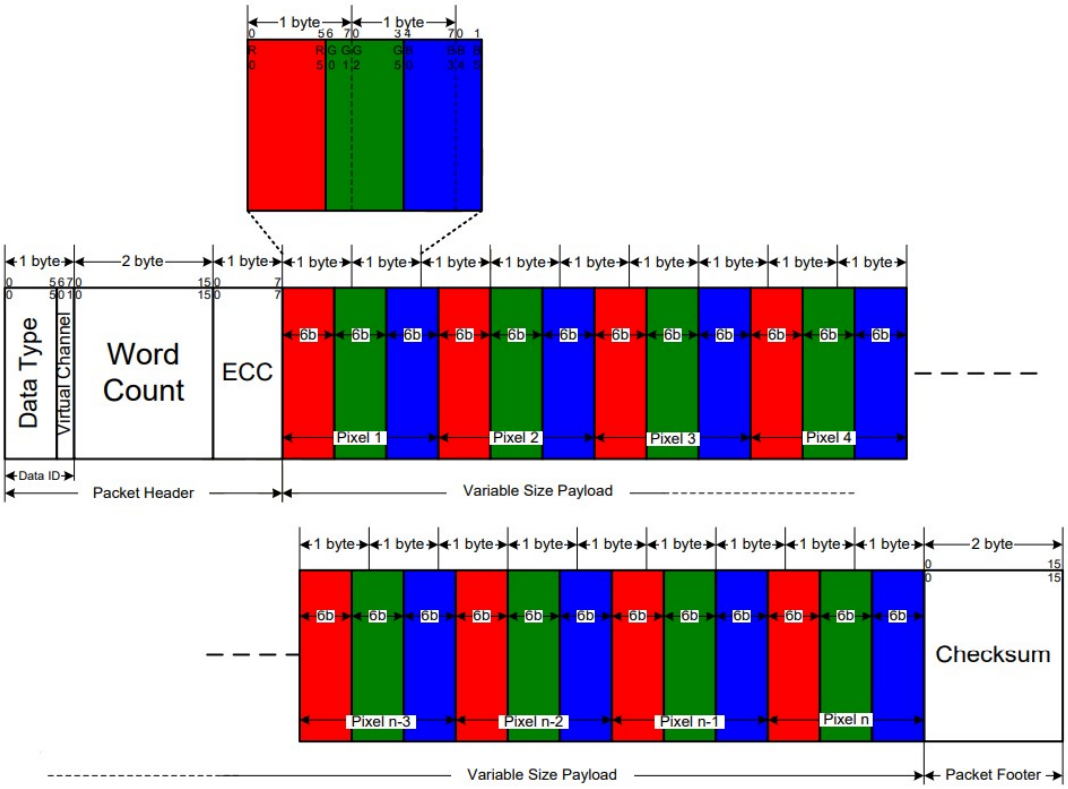


Figure 6.26: 18-bit per Pixel (Packed) – RGB Color Format, Long Packet

6.5.19 Pixel Stream, 18-bit Loosely Format, Long Packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits, but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte as shown in Figure 6.27. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

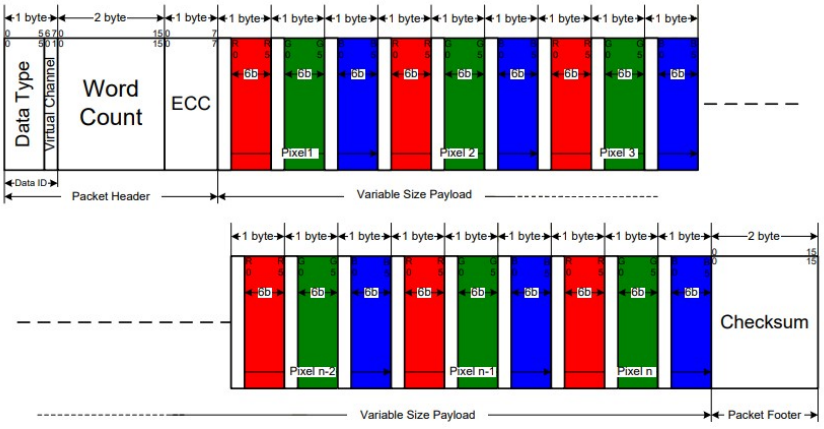


Figure 6.27: 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet

6.5.20 Packed Pixel Stream, 24-bit Format, Long Packet

Packed Pixel Stream 24-Bit Format shown in Figure 6.28 is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

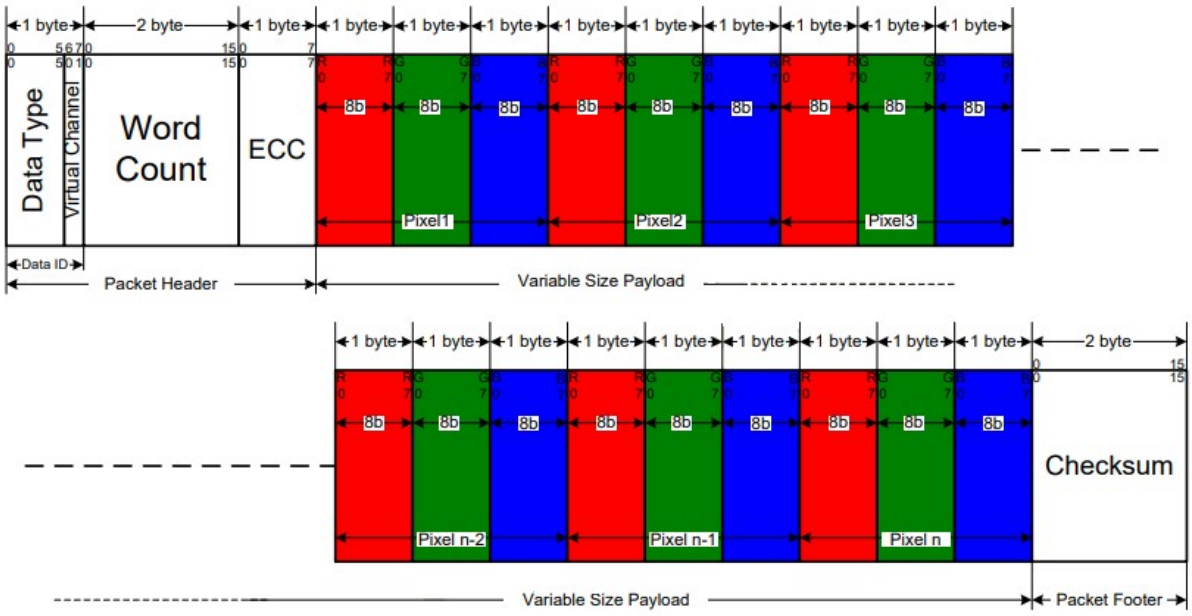


Figure 6.28: 24-bit per Pixel – RGB Color Format, Long Packet

6.5.21 Peripheral to Processor Transmission

GH8323-I1 has bidirectional capability for returning READ data, acknowledge, or error information to the host processor. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

Peripheral-to-processor transactions are of four basic types:

•**Tearing Effect (TE)** is a Trigger message sent to convey display timing information to the host processor. Trigger messages are single byte packets sent by a peripheral's PHY layer in response to a signal from the DSI protocol layer.

•**Acknowledge** is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, i.e. either triggers or packets, is received by the peripheral with no errors.

•**Acknowledge and Error Report** is a Short packet sent if any errors were detected in preceding transmissions from the host processor. Once reported, accumulated errors in the error register are cleared.

•**Response to Read Request** may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

6.5.22 Appropriate Responses to Commands and ACK Requests

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

•Following a non-Read command, the peripheral shall respond with Acknowledge if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

•Following a Read request, the peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

•Following a Read request if only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte Acknowledge and Error Report packet in the same LP transmission. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a non-Read command if only a single-bit ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a Read request, if multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following any command, if SoT Error, SoT Sync Error or DSI VC ID Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response, with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication, in the two-byte error field. Only the Acknowledge and Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

•Following any command, if EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication. For a read command, only the Acknowledge and Error Report packet shall be transmitted; no read data shall be sent by the peripheral in response.

Once reported to the host processor, all errors documented in this section are cleared from the Error Register.

6.5.23 Peripheral-to-Processor Packet Description

Table 6.5 presents the complete set of peripheral-to-processor Data Types.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x02	00 0010a	Acknowledge and Error Report	Short
0x08	00 1000	End of Transmission packet	Short
0x1C	01 1100	DCS Long READ Response	Long

Table 6.5: Data Types for Peripheral-sourced Packets

6.5.24 Format of Acknowledge and Error Report and Read Response Data Type

Acknowledge is sent using a Trigger message.

Byte 0: 00100001 (shown here in first bit [left] to last bit [right] sequence)

Response to Read Request returns data requested by the preceding READ command from the processor. These may be short or Long packets. The format for short READ packet responses is:

•Byte 0: Data Identifier (Virtual Channel ID + Data Type)

•Bytes 1, 2: READ data, may be one or two bytes. For single byte parameters, the parameter shall be returned in Byte 1 and Byte 2 shall be set to 0x00.

•ECC byte covering the header

Acknowledge and Error Report confirms that the preceding command or data sent from the host processor to a peripheral was received, and indicates what types of error were detected on the transmission and any preceding transmissions. Note that if errors accumulate from multiple preceding transmissions, it may be difficult or impossible to identify which transmission contained the error. This message is a Short packet of four bytes, taking the form:

•Byte 0: Data Identifier (Virtual Channel ID + Acknowledge Data Type)

•Byte 1: Error Report bits 0-7

•Byte 2: Error Report bits 8-15

•ECC byte covering the header

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. Table 6.6 shows the bit assignment for all error reporting.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, Single-bit (detected and corrected)
9	ECC Error, Multi-bit (detected, not corrected)

10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Table 6.6: Error Report Bit Definitions

The first eight bits, bit 0 through bit 7, are related to the physical layer errors. Bits 8 and 9 are related to single-bit and multi-bit ECC errors. The remaining bits indicate DSI protocol-specific errors.

6.5.25 Video Mode Interface Timing

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

6.5.26 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

•**Non-Burst Mode with Sync Pulses –** enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

•**Non-Burst Mode with Sync Events –** similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

•**Burst mode –** RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral.

To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. The host processor should return to LP state once per scanline during the horizontal blanking time.

During the BLLP the DSI Link may do any of the following:

•Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX

•Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode

•Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

•If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode

•Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with VSE or HSS. Note that the position of synchronization packets, such

as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet.

Transmission packet components used in the figures in this section are defined in Figure 6.29 Video Mode Interface Timing Legend unless otherwise specified.

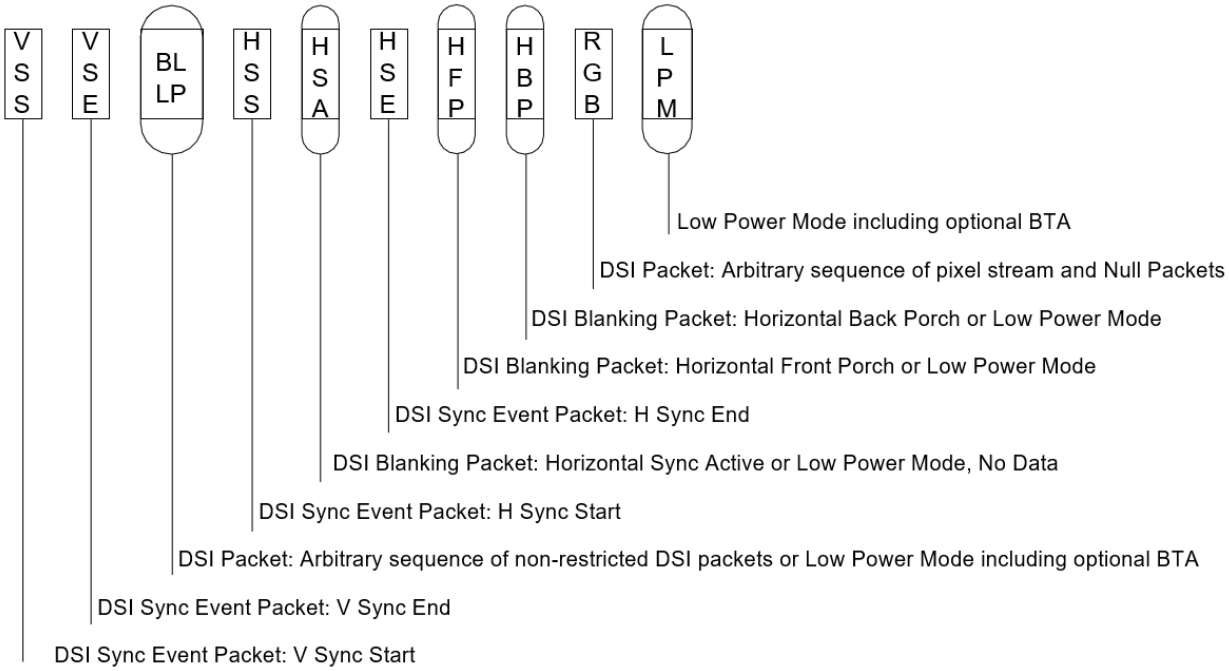


Figure 6.29 Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

6.5.27 Non-Burst sync pulse mode

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure 6.30.

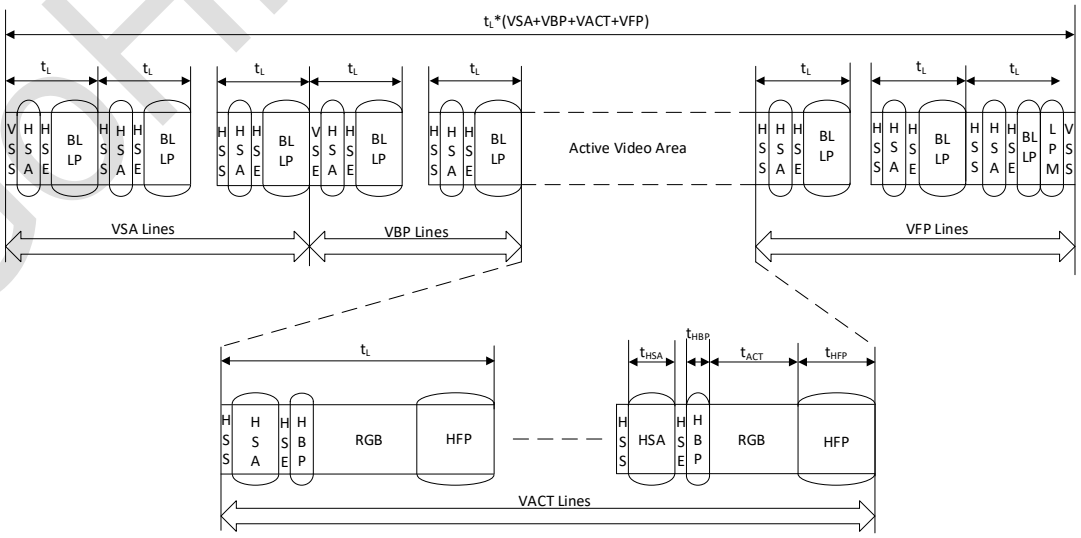


Figure 6.30: Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power. During HSA, HBP and HFP periods, the bus should stay in the LP-11 state.

6.5.28 Non-Burst sync event mode

This mode is a simplification of the "Non-Burst Mode with Sync Pulses" format. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. An example of this mode is shown in Figure 6.31.

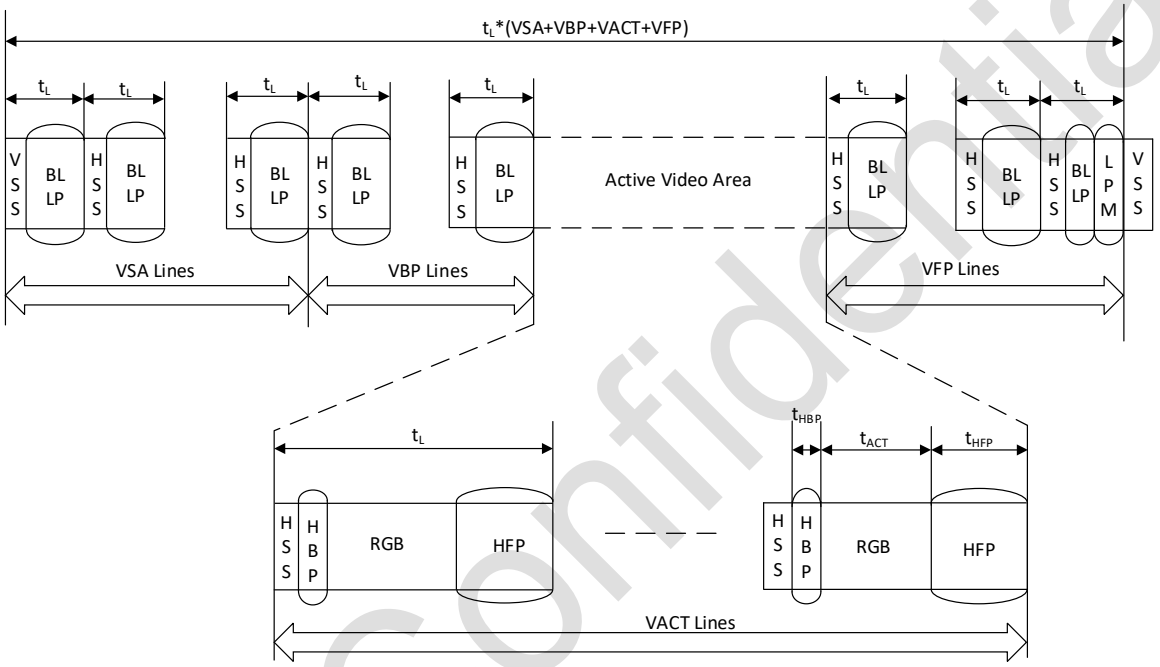


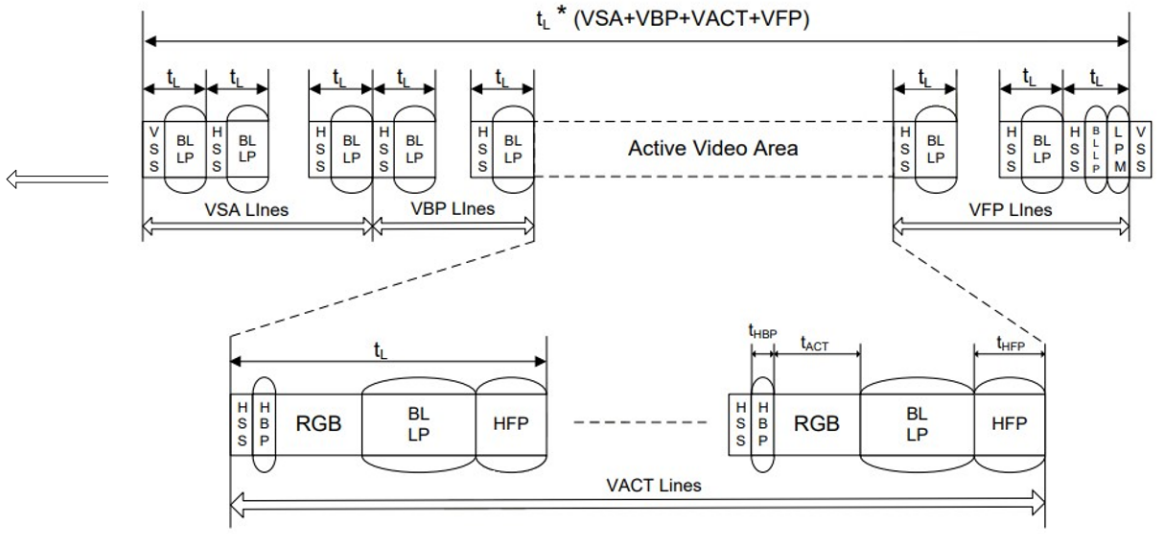
Figure 6.31: Video Mode Interface Timing: Non-burst Transmission with Sync Events

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

6.5.29 Burst mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

Following HS pixel data transmission, the bus may stay in HS Mode for sending blanking packets or go to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is



Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

6.6 Error-Correcting Code and Checksum

6.6.1 Error-Correcting Code(ECC)

MIPI DSI uses Hamming Code Theory as ECC generate rule. The parity of each bits in ECC are showed as below.

P7=0

P6=0P5=D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4=D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3=D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2=D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1=D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0=D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

ECC is generated from the twenty-four bits with in the Packet Header as illustrated in Figure 6.33, which also serves as an ECC calculation example.

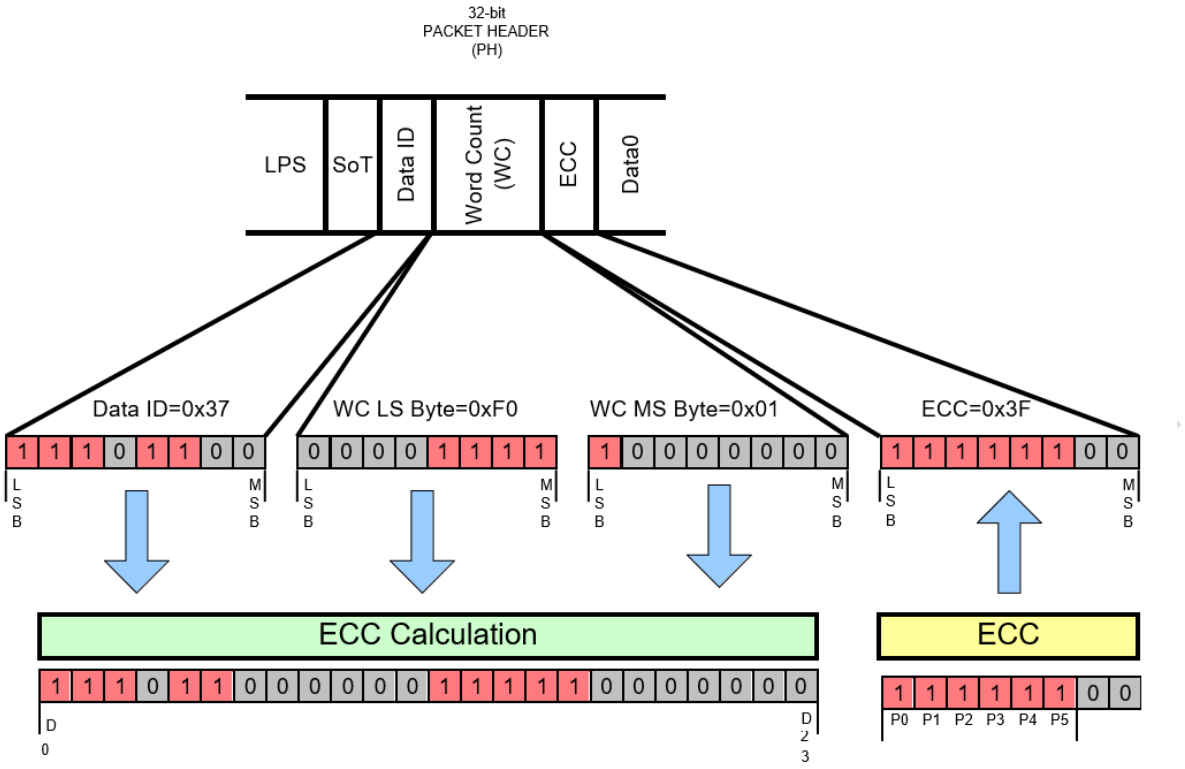


Figure 6.33: 24-bit ECC generation Example

6.6.2 Checksum Generation for Long Packet Payloads

To detect errors in transmission of Long packets, a checksum is calculated over the payload portion of the data packet. Note that, for the special case of a zero- length payload, the 2-byte checksum is set to 0xFFFF. The checksum shall be realized as a 16-bit CRC with a generator polynomial of x^16+x^12+x^5+x^0

The transmission of the checksum is illustrated in Figure 7.34. The LS byte is sent first, followed by the MS byte. Note that within the byte, the LS bit is sent first.

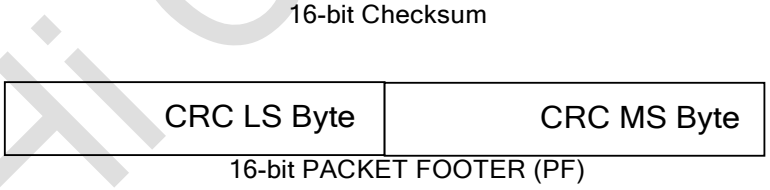


Figure 6.34: Checksum Transmission

The CRC implementation is presented in Figure 6.35. The CRC shift register shall be initialized to 0xFFFF before packet data enters. Packet data not including the Packet Header then enters as a bitwise data stream from the left, LS bit first. Each bit is fed through the CRC shift register before it is passed to the output for transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift register, the shift register contains the checksum. C15 contains the checksum's MSB and C0 the LSB of the 16-bit checksum. The checksum is then appended to the data stream and sent to the receiver. The receiver uses its own generated CRC to verify that no errors have occurred in transmission.

Polynomial: x^16+x^12+x^5+x^0

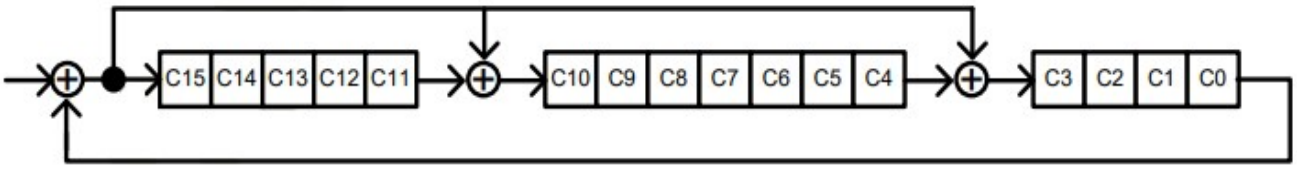


Figure 6.35: 16-bit CRC Generation Using a Shift Register

6.7 DPHY

6.7.1 Lane Module

A PHY configuration contains a Clock Lane Module and one or more Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect wires simultaneously, one or more single-ended Low-Powe functions operating on each of the interconnect wires individually, and control & interface logic. For proper operation, the set of functions in the Lane Modules on both sides of the Lane Interconnect has to be matched.

6.7.2 Lane Module Type of Clock Lane, Data0, Data1 and Data2

The required functions in a Lane Module depend on the Lane type and which side (master or slave) of the Lane Interconnect the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and Bi-directional Data Lane. Several PHY configurations can be constructed with these Lane types. In GH8323-I1 Below show the lane module architecture of each lane.

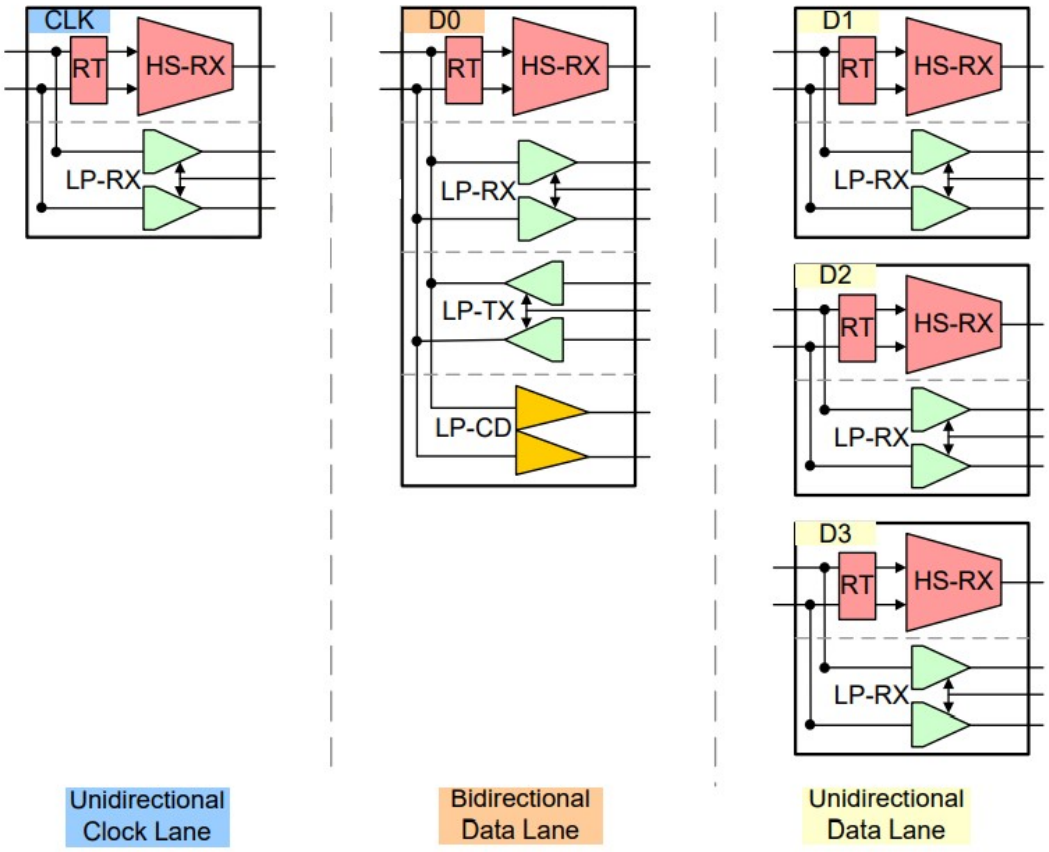


Figure 6.36: Lane Module Type

6.7.3 Master and Slave

Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. The main direction of data communication, from source to sink, is denoted as the Forward direction. Data communication in the opposite direction is called Reverse transmission. Only bi-directional Data Lanes can transmit in the Reverse direction. In all cases, the Clock Lane remains in the Forward direction, but bi-directional Data Lane(s) can be turned around, sourcing data from the Slave side.

GH8323-I1 serves as Slave side.

6.7.4 Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High- Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential- 0 and Differential-1. The interpretation of Low-Power Lane states depends on the mode of operation. The LP-Receivers shall always interpret both High-Speed differential states as LP-00.

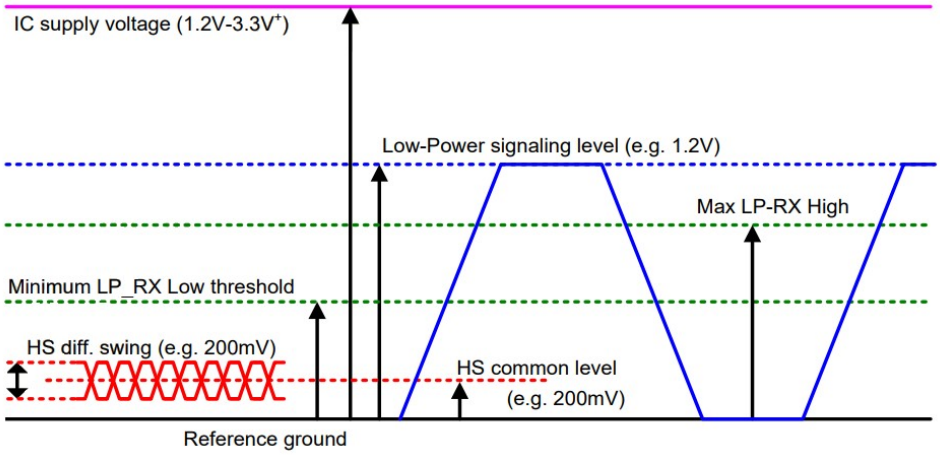


Figure 6.37: Line Levels

The Stop state has a very exclusive and central function. If the Line levels show a Stop state for the minimum required time, the PHY state machine shall return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. Table 6.7 lists all the states that can appear on a Lane during normal operation. All LP state periods shall be at least TLPX in duration. State transitions shall be smooth and exclude glitch effects.A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines. Ideally, the reconstructed clock has a duration of at least 2*TLPX, but may have a duty cycle other than 50% due to signal slope and trip levels effects.

Start Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

6.7.5 Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Notice that Master and Slave side shall not be changed by Turnaround.

Figure 6.38 shows the Turnaround procedure graphically.

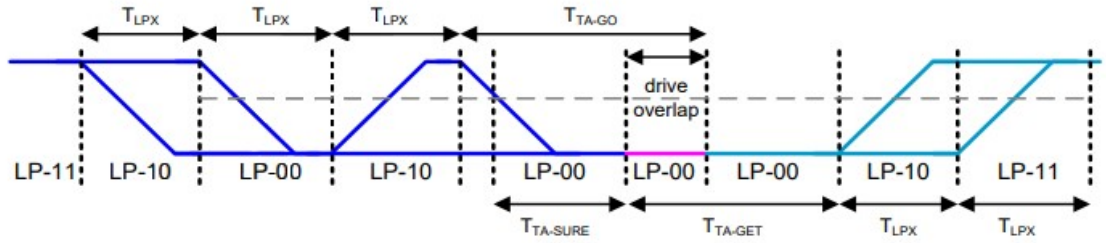


Figure 6.38: Turnaround Procedure

6.8 Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00,LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command, by Spaced-One-Hot coding, to indicate the requested action. Table 6.8 lists all supported Escape mode commands and actions.

Spaced-One-Hot coding means that each Mark state is interleaved with a Space state. Each symbol consists therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0 followed by a Space to transmit a ‘zero-bit’ and it shall send a Mark-1 followed by a Space to transmit a ‘one-bit’. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not followed by a Space state.

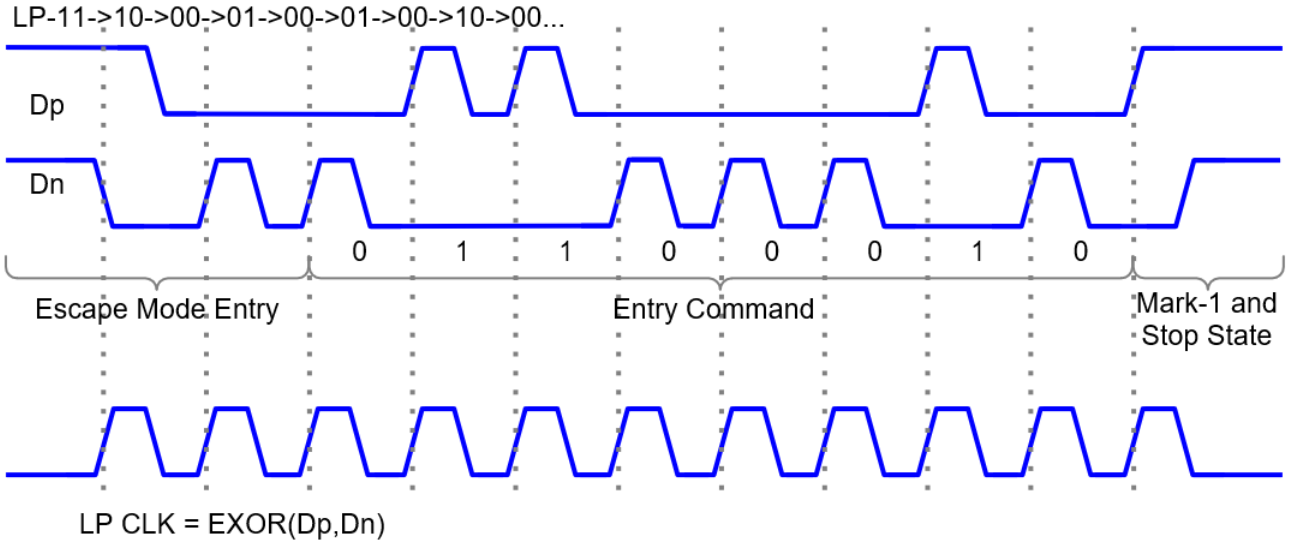


Figure 6.39: Trigger-Reset Command in Escape Mode

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low power State	mode	00011110
Reset-Trigger	Trigger	01100010
TE-Trigger	Trigger	01011101
Acknowledge	Trigger	00100001

Table 6.8: Escape Entry Codes

6.9 Remote Trigger

Trigger signaling is the mechanism to send a flag to the protocol at the receiving side, on request of the protocol on the transmitting side. This can be either in the Forward or Reverse direction depending on the direction of operation and available Escape mode functionality. Trigger signaling requires Escape mode capability and at least one matching Trigger Escape Entry Command on both sides of the interface. Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

6.10 Low-Power Data Transmission(LPDT)

If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode. Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. The data is self-clocked by the applied bit encoding and does not rely on the Clock Lane. The Lane can pause while using LPDT by maintaining a Space state on the Lines. A Stop state on the Lines stops LPDT, exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a Mark-1 state, which does not represent a data-bit. At the end of LPDT the Lane shall return to the Stop state.

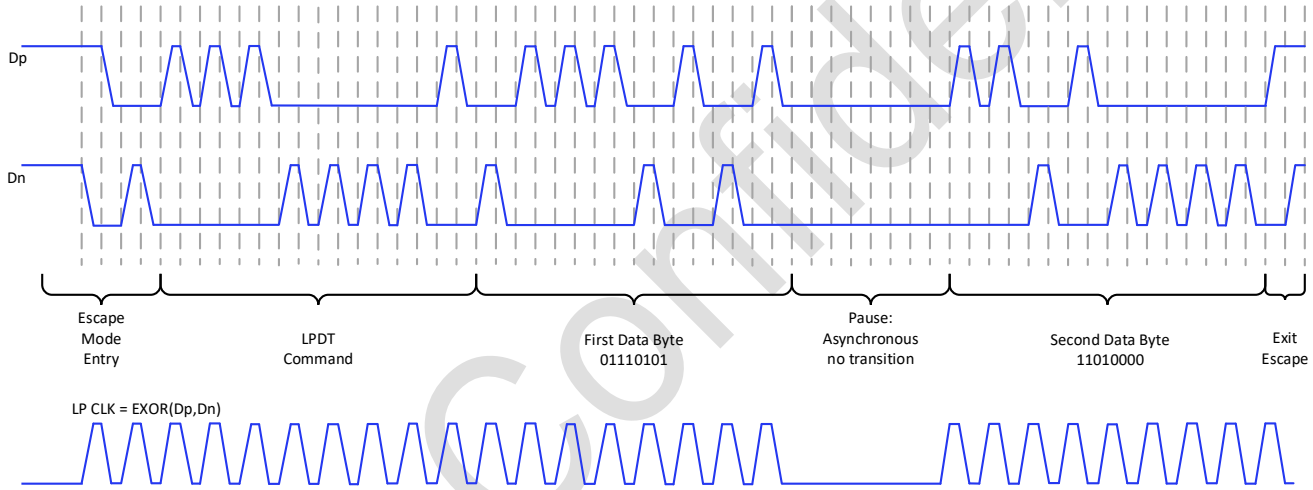


Figure 6.40: Two Data Byte Low-Power Data Transmission Example

6.11 Ultra-Low Power State(ULPS)

If the Ultra-Low Power State Entry Command is sent after an Escape mode Entry command, the Lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

6.12 TE Trigger

A Command Mode display module has its own timing controller and local frame buffer for display refresh. In some cases the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bidirectional Data Lane.

For polling to the display module, the host processor shall detect the current scan line information with a DCS command such as get_scan_line to avoid Tearing Effects. For TE-

reporting from the display module, the TE-reporting function is enabled and disabled by three DCS commands to the display module's controller: set_tear_on, set_tear_scanline, and set_tear_off.

set_tear_on and set_tear_scanline are sent to the display module as DSI Data Type 0x15 (DCS Short Write, one parameter) and DSI Data Type 0x39 (DCS Long Write/write_LUT), respectively. The host processor ends the transmission with Bus Turn-Around asserted, giving bus possession to the display module. Since the display module's DSI Protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with a normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession.

To enable TE-reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE reporting has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) Bus Turn-Around signal to its D-PHY functional block. The PHY layer will then initiate a Bus Turn-Around sequence in LP mode, which gives bus possession to the display module.

Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait for up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or requests to the display module, because it does not have bus possession.

When the TE event takes place the display module shall send TE event information in LP mode using a specified trigger message available with D-PHY protocol via the following sequence:

•The display module shall send the LP Escape Mode sequence

•The display module shall then send the trigger message byte 01011101 (shown here in first bit to last bit sequence)

•The display module shall then return bus possession to the host processor

This Trigger Message is reserved by DSI for TE signaling only and shall not be used for any other purpose in a DSI-compliant interface.

6.13 High Speed Transmission

6.13.1 Burst Payload Data

The payload data of a burst shall always represent an integer number of payload data bytes with a minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data.

There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the practical BER will not be zero. Therefore, it is important to consider for every individual protocol what the best choice is for maximum burst length.

6.13.2 Start-of-Transmission

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure. Table 6.6 describes the sequence of events on TX and RX side.

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS-PREPARE}$	Observes transition from LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D-TERM-EN}$
Enables High-Speed driver and disables Low-Powerdrivers simultaneously.	
Drives HS-0 for a time $T_{HS-ZERO}$	Enables HS-RX and waits for timer $T_{HS-SETTLE}$ to expire in order to neglect transition effects
	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence '00011101' beginning on a rising Clock edge	
	Synchronizes upon recognition of Leader Sequence '011101'
Continues to Transmit High-Speed payload data	
	Receives payload data

Table 6.9: Start-of-Transmission Sequence

6.13.3 End-of-Transmission

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 6.7 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

TX Side	RX Side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS-SKIP}$ to hide transition effects
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

6.13.4 High Speed Data Transmission

Figure 6.41 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane.

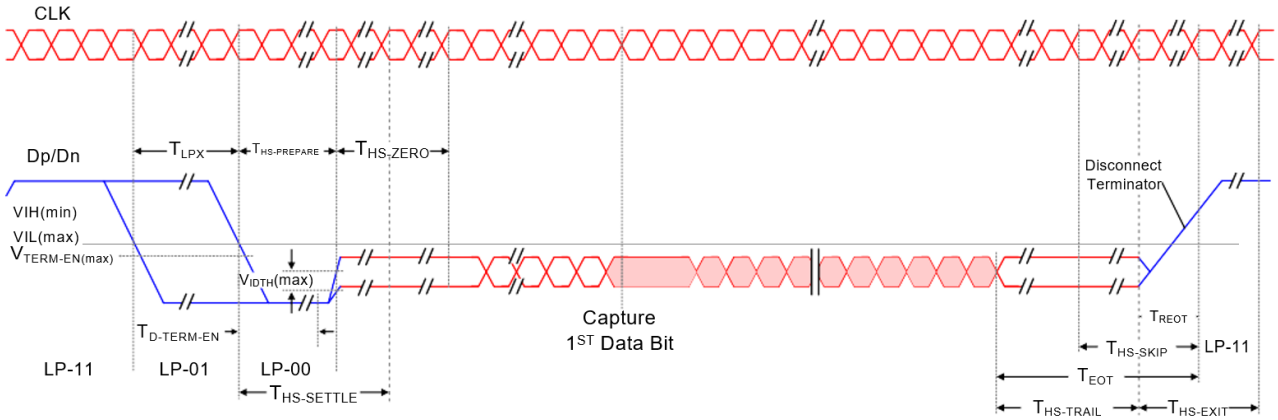


Figure 6.41: High-Speed Data Transmission in Bursts

6.13.5 High Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of the first transmitted bit of a burst. The detail Clock Start and Stop procedures are shown in Figure 6.42.

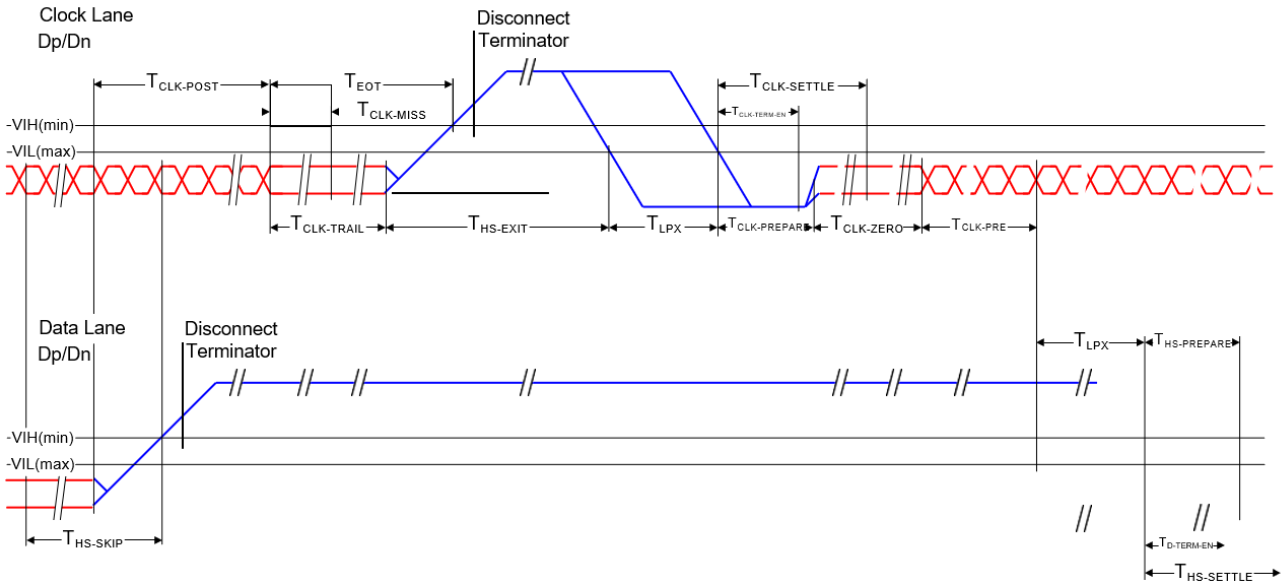


Figure 6.42: Switching the Clock Lane between Clock Transmission and Low-Power Mode

6.14 System Power state

Each Lane within a PHY configuration, that is powered and enabled, has potentially three different power consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low Power State.

6.15 Initialization

After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer then TINIT. The first Stop state longer than the specified TINIT is called the Initialization period. The Master side shall ensure that a Stop State longer than TINIT does not occur on the Lines before the Master is initialized.

TINIT must larger than 500us.

6.16 Global Operation Flow Diagram

Figure 6.43 shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround, and Initialization.

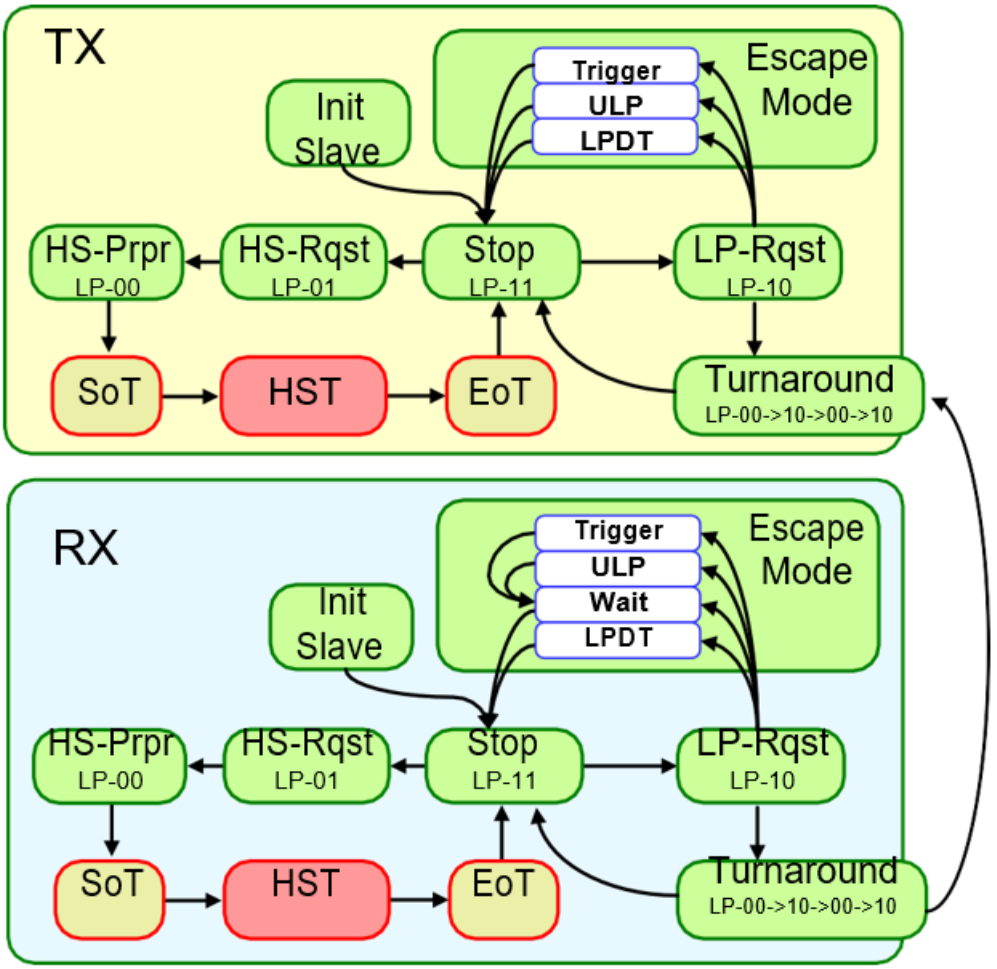


Figure 6.43: Data Lane Module State Diagram

Figure 6.44 shows the state diagram for a Clock Lane Module. The Clock Lane Module has four major operational states: Init (of unspecified duration), Low-Power Stop state, Ultra-Low Power state, and High- Speed clock transmission.

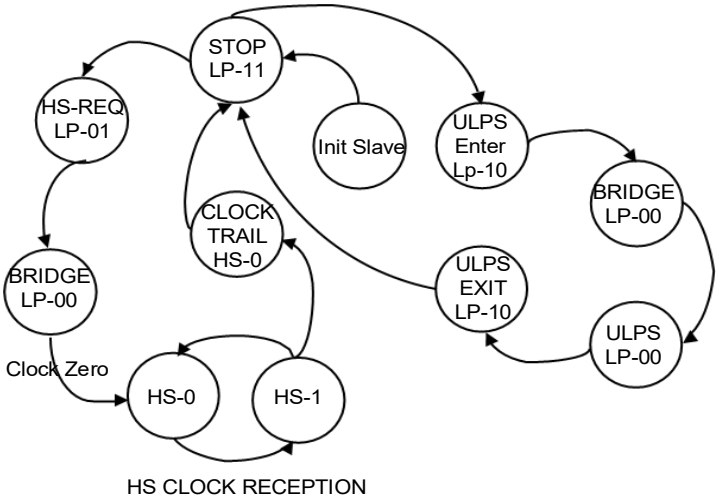
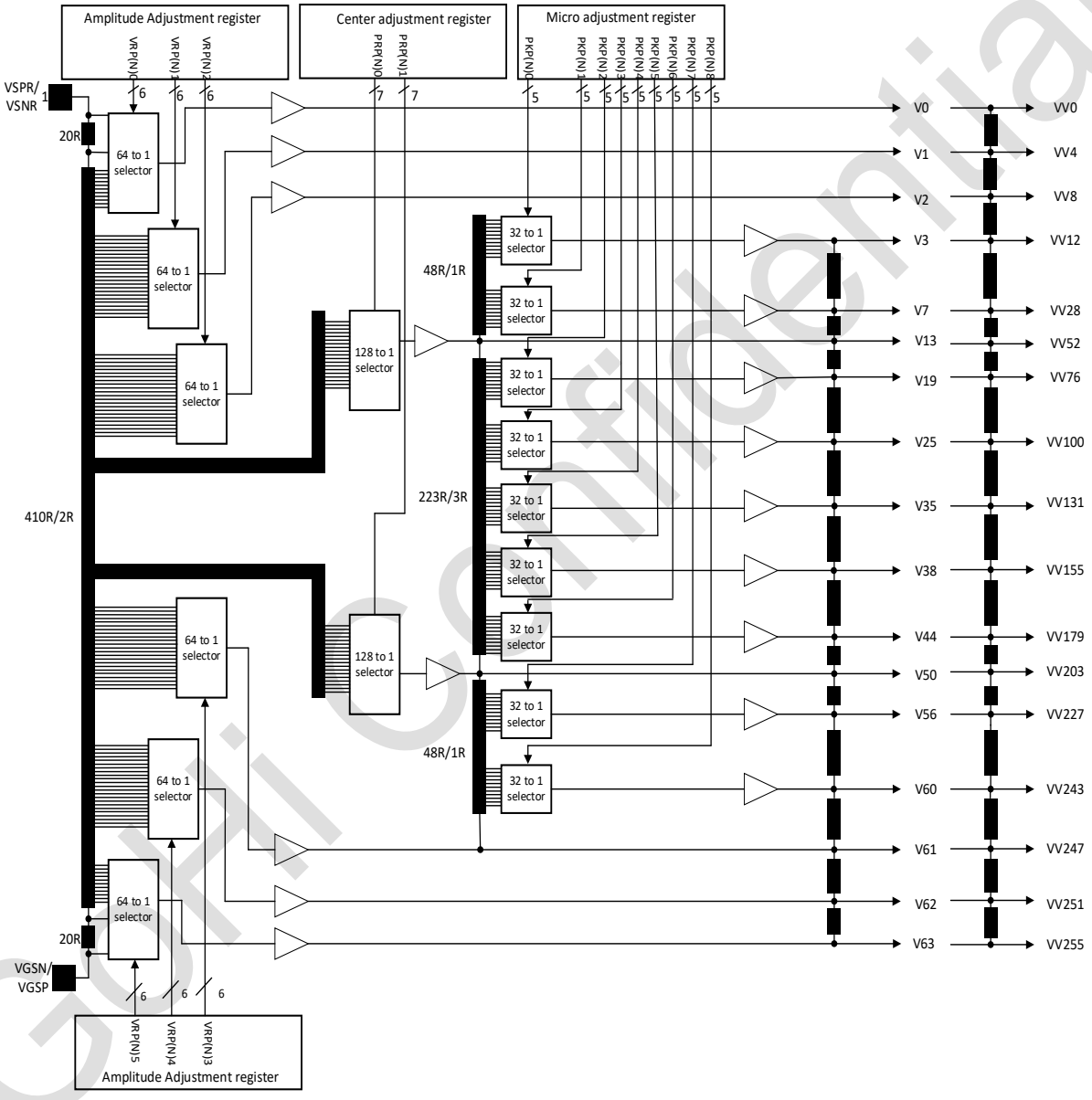


Figure 6.44: Clock Lane Module State Diagram

7 Gamma characteristic correction function

The GH8323-I1 incorporates gamma adjustment function for the 16.7m-color display. Gamma adjustment operation is implemented by deciding the 17 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including 17 gamma reference voltages. VGM P/N (0, 4, 8, 12, 28, 52, 76, 100, 131, 155, 179, 203, 227, 273, 247, 251, 255).

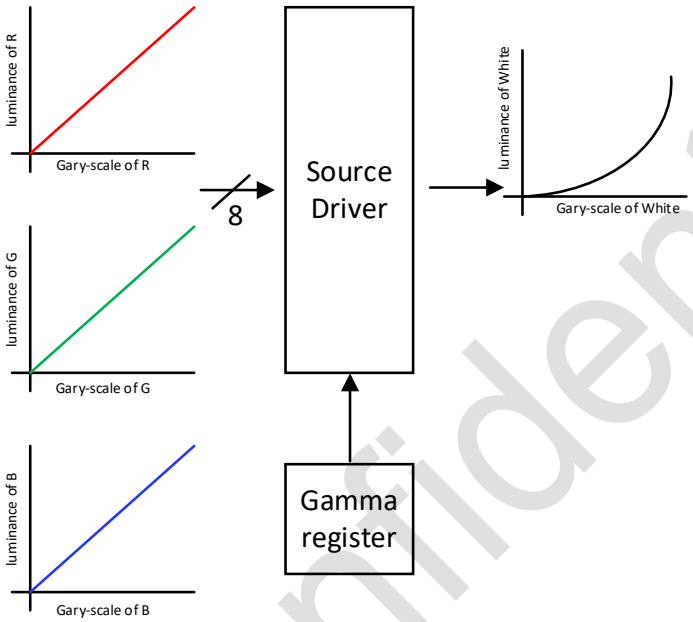


8 Function Description

8.1 Digital Gamma (separate RGB gamma)

The GH8323-I1 offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through analog gamma circuit directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is selected by internal register DGC_EN bit.

1) Gamma adjustment of Source Driver



2) Gamma adjustment of Digital Gamma Correction

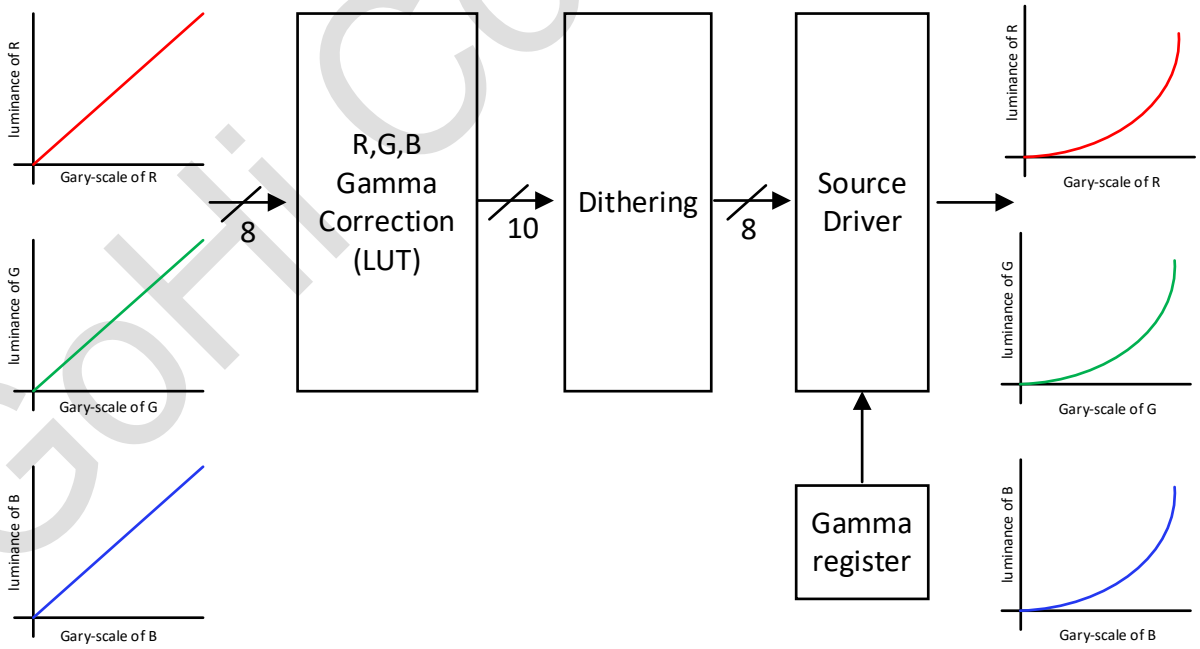


Figure 8.1: Gamma adjustments different of source driver with digital gamma correction

8.2 CABC

The CABC, a dynamic backlight control function, drastically reduces power consumption of the luminance source. The GH8323-I1 wll refer the gray scale content of the display image to output the LEDPWM pulse to the LED driver. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of theimage.

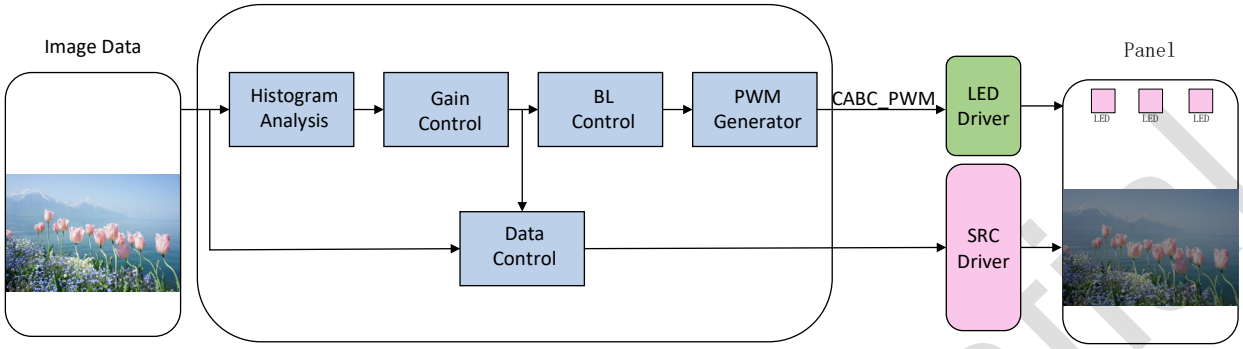


Figure 8.2: CABC Block Diagram

The GH8323-I1 can calculate the backlight brightness level and send a LEDPWM pulse to the LED driver via LEDPWIM pacfor backlight brightness control purposes. The PWM frequency can be adjusted by PWM DIV parameters, and the calculating equation is shown below.

$$f_{LEDPWM} = \frac{32MHz}{PWM\_DIV[7:0]+1} \times PWM\_DUTY\_PRECISOIN$$

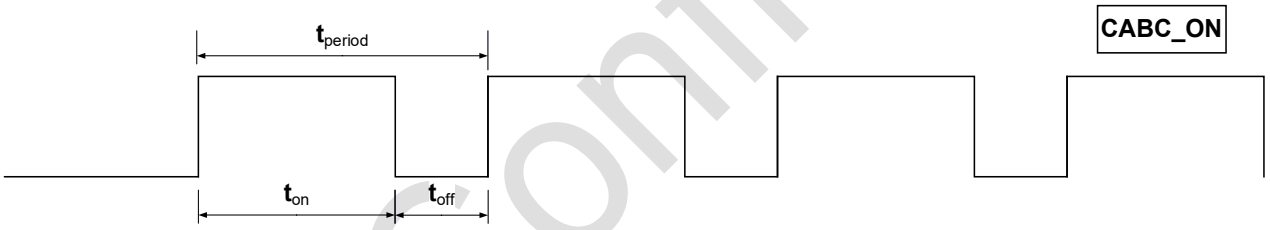
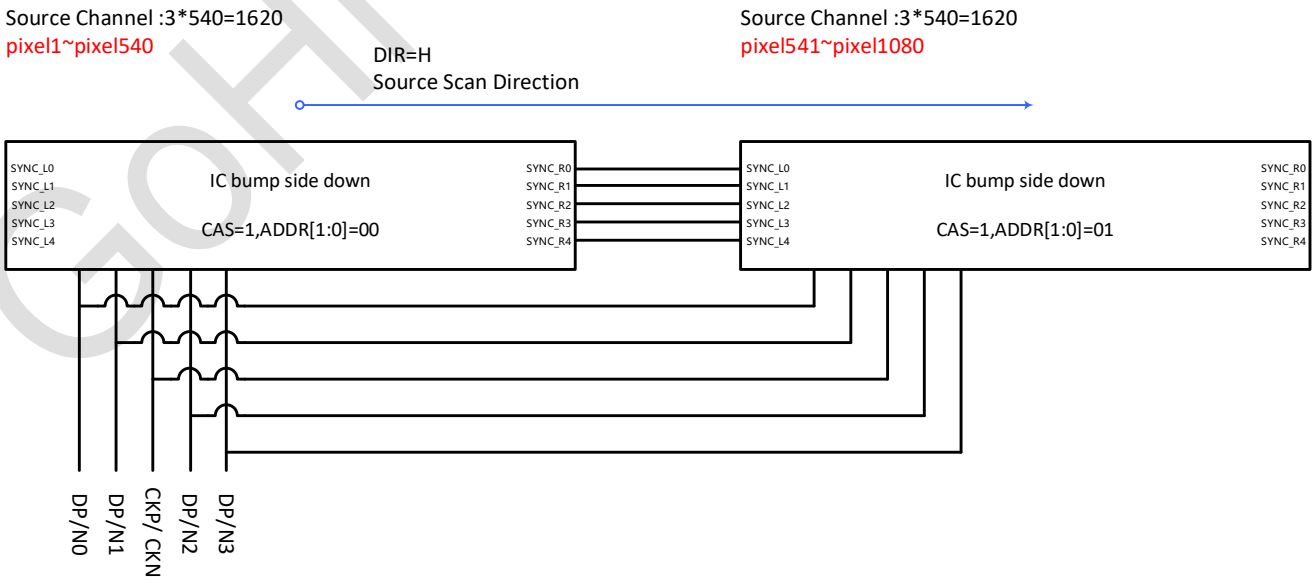
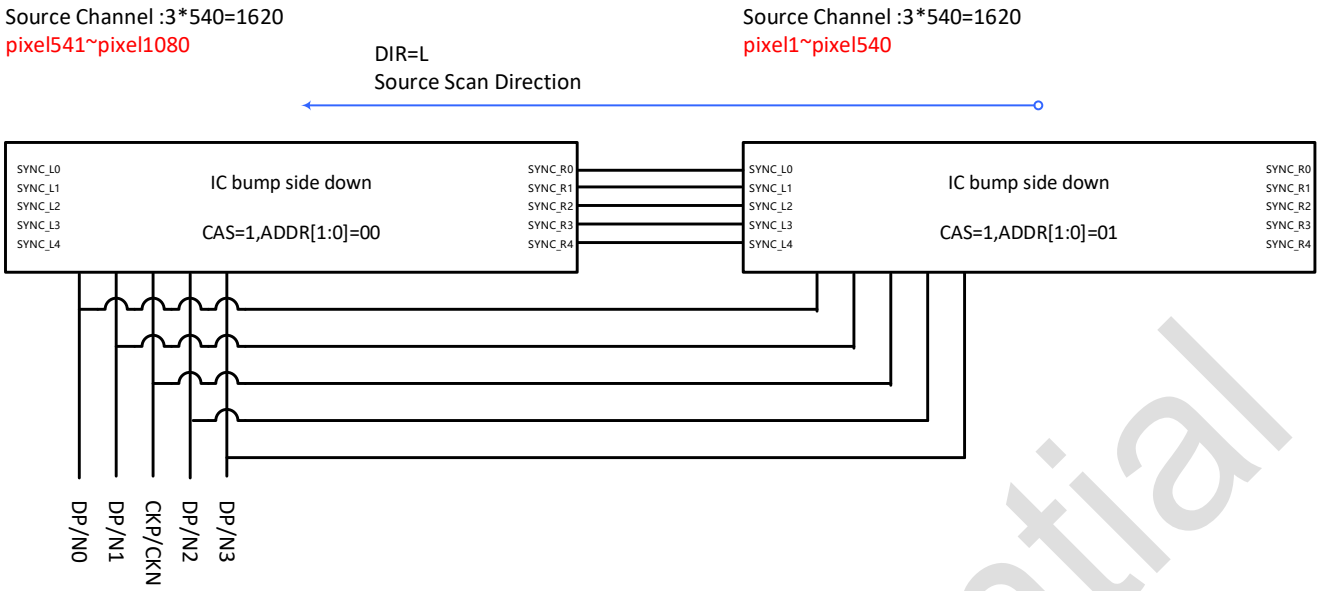


Figure 8.3：LEDPWM on/off period

8.3 Cascade



LVDS Resolution :1080RGB=pixel1~pixel1080



LVDS Resolution :1080RGB=pixel1~pixel1080

8.4 BIST

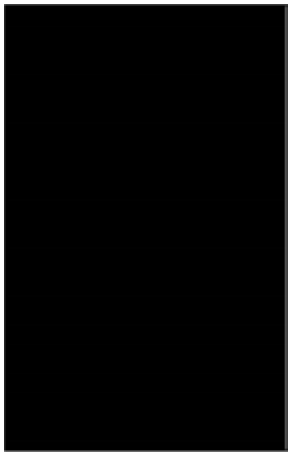
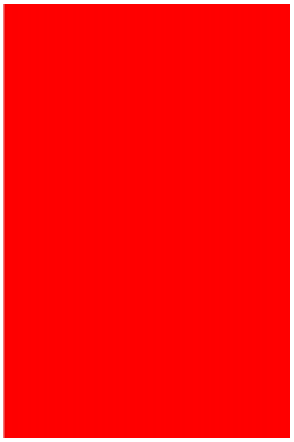
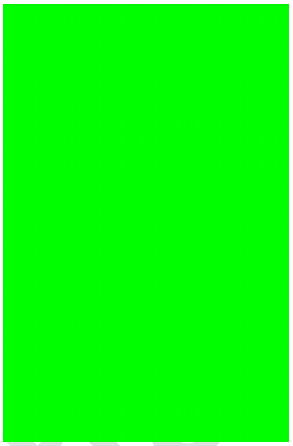
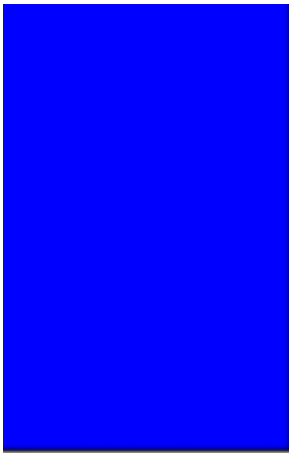
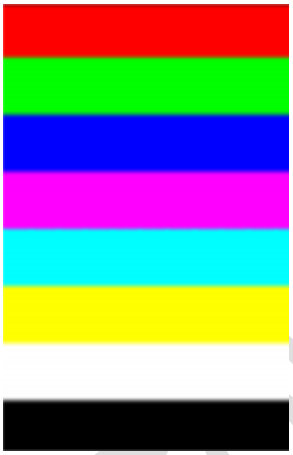
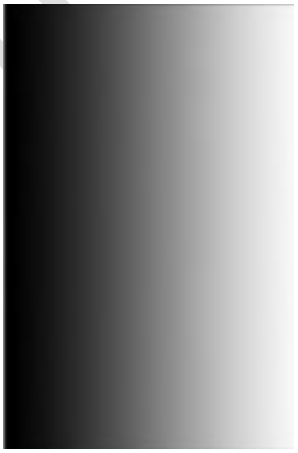
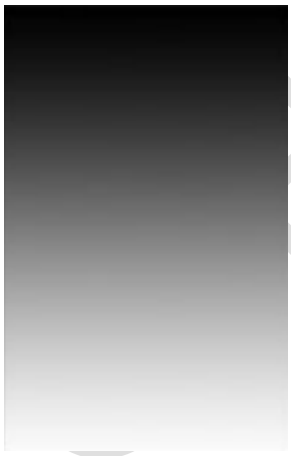
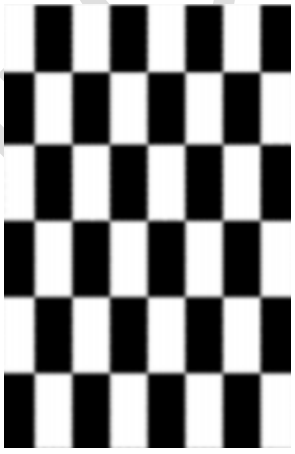
8.4.1 BIST function

When BIST is trigger to low, then GH8323-I1 will leave normal operation mode and starts to generate the BIST pattern to LCD panel without MIPI input signals.

8.4.2 BIST pattern

We support the BIST mode to test panel and debug. It can stop pattern at any time while BISTB set to low. The pattern sequence is listed below.

Configuration reg_bist_pause[3:0],Different patterns can be displayed.

Black=4'h0	White=4'h1	Red=4'h2	Green=4'h3
			
Blue=4'h4	Color Bar=4'h5	Frame edge=4'h6	Gray level H=4'h7
			
Gray level V=4'h8	Chessboard=4'h9		
			

9 Command

9.1 Command List

9.1.1 Standard command

	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function
00	NOP	W	0	0	0	0	0	0	0	0	No Operation
01	SWRESET	W	0	0	0	0	0	0	0	1	Software Reset
04	RDDIDIF	W	0	0	0	0	0	1	0	0	Read Display Identification Information
		R	ID1[7:0]								
		R	ID2[7:0]								
		R	ID3[7:0]								
05	RDDST	W	0	0	0	0	1	0	0	1	Read Display Status
		R	D[31:24]								
		R	D[23:16]								
		R	D[15:8]								
		R	D[7:0]								
06	RDDPM	W	0	0	0	0	1	0	1	0	Read display power mode
		R	D7	D6	D5	D4	D3	D2	0	0	
07	RDDMADCTL	W	0	0	0	0	1	0	1	1	Read display MADCTL
		R	D7	D6	D5	D4	D3	D2	D1	D0	
08	RDDCOLMOD	W	0	0	0	0	1	1	0	0	Read display pixel format
		R	0	D6	D5	D4	0	D2	D1	D0	
09	RDDIM	W	0	0	0	0	1	1	0	1	Read display image mode
		R	D7	D6	D5	D4	D3	D2	D1	D0	
10	RDDSM	W	0	0	0	0	1	1	1	0	Read display signal mode
		R	D7	D6	D5	D4	D3	D2	D1	D0	
0A	RDDSDR	W	0	0	0	0	1	1	1	1	Read display self-diagnostic result
		R	D7	D6	D5	D4	0	0	0	D0	
0B	SLPIN	W	0	0	0	1	0	0	0	0	Sleep In

11	SLPOUT	W	0	0	0	1	0	0	0	1	Sleep Out
13	NORON	W	0	0	0	1	0	0	1	1	Normal display mode on
20	INVOFF	W	0	0	1	0	0	0	0	0	Display inversion off
21	INVON	W	0	0	1	0	0	0	0	1	Display inversion on
22	ALLPOFF	W	0	0	1	0	0	0	1	0	All Pixel Off
23	ALLPON	W	0	0	1	0	0	0	1	1	All Pixel On
26	GAMSET	W	0	0	1	0	0	1	1	0	Gamma set-
		W	CG[7:0]								
28	DISPOFF	W	0	0	1	0	1	0	0	0	Display off
29	DISPON	W	0	0	1	0	1	0	0	1	Display on
34	TEOFF	W	0	0	1	1	0	1	0	0	Tearing Effect Line OFF
35	TEON	W	0	0	1	1	0	1	0	1	Tearing Effect Line ON
		W	X	X	X	X	X	X	X	M	
36	MADCTL	W	0	0	1	1	0	1	1	0	Memory Access Control
		W	MY	MX	X	X	BGR	-	LR	UD	
38	IDMOFF	W	0	0	1	1	1	0	0	0	Idle mode off
39	IDMON	W	0	0	1	1	1	0	0	1	Idle mode on
3A	COLMOD	W	0	0	1	1	1	0	1	0	Interface Pixel Format,
		W	X	D6	D5	D4	X	X	X	X	
44	TESL	W	0	1	0	0	0	1	0	0	Set Tear Effect Scan Lines
		W	TELINE[15:8]								
		W	TELINE[7:0]								
45	GETSCAN	W	0	1	0	0	0	1	0	1	Return the current scanline
		R	SLN[15:8]								
		R	SLN[7:0]								
51	WRDISBV	W	0	1	0	1	0	0	0	1	Write Display Brightness
		W	DBV[7:0]								
52	RDDISBV	W	0	1	0	1	0	0	1	0	Read Display Brightness Value
		R	DBV[7:0]								
53	WRCTRLD	W	0	1	0	1	0	0	1	1	Write CTRL Display
		W	X	X	BCTRL	X	DD	BL	X	X	
54	RDCTRLD	W	0	1	0	1	0	0	1	1	Read Control Value Display-
		R	X	X	BCTRL	0	DD	BL	0	0	
DA	RDID1	W	1	1	0	1	1	0	1	0	Read ID1
		R	module's manufacturer[7:0]								

DB	RDID2	W	1	1	0	1	1	0	1	1	Read ID2
		R	LCD module/driver version [7:0]								
DC	RDID3	W	1	1	0	1	1	1	0	0	Read ID3
		R	LCD module/driver ID[7:0]								
A1	RDDDB	W	1	0	1	0	0	0	0	1	Read the DDB from the provided location.
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
A8	RDDDBCON	W	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
AA	RDFCS	W	1	0	1	0	1	0	1	0	Read First Checksum
		R	FCS[7:0]								
AF	RDCCS	W	1	0	1	0	1	1	1	1	Read Continue Checksum
		R	CCS[7:0]								

9.1.2 Standard Command Accessibility

Hex Code	Operation code	Normal Mode On, Idle Mode Off, Sleep Mode Off	Normal Mode On, Idle Mode On, Sleep Mode Off	Partial Mode On, Idle Mode Off, Sleep Mode Off	Partial Mode On, Idle Mode On, Sleep Mode Off	Sleep Mode On
00	NOP	Yes	Yes	Yes	Yes	Yes
01	SWRESET	Yes	Yes	Yes	Yes	Yes
04	RDDIDIF	Yes	Yes	Yes	Yes	Yes
05	RDDST	Yes	Yes	N/A	N/A	Yes
06	RDDPM	Yes	Yes	Yes	Yes	Yes
07	RDDMADCTL	Yes	Yes	Yes	Yes	Yes
08	RDDCOLMOD	Yes	Yes	Yes	Yes	Yes
09	RDDIM	Yes	Yes	Yes	Yes	Yes
0A	RDDSM	Yes	Yes	Yes	Yes	Yes
0B	RDDSDR	Yes	Yes	Yes	Yes	Yes
0C	SLPIN	Yes	Yes	Yes	Yes	Yes
0D	SLPOUT	Yes	Yes	Yes	Yes	Yes
0E	PTLON	Yes	Yes	Yes	Yes	Yes
0F	INVOFF	Yes	Yes	Yes	Yes	Yes
10	INVON	Yes	Yes	Yes	Yes	Yes
11	ALLPOFF	Yes	Yes	N/A	N/A	Yes
12	ALLPON	Yes	Yes	N/A	N/A	Yes
20	GAMSET	Yes	Yes	Yes	Yes	Yes
21	DISPOFF	Yes	Yes	Yes	Yes	Yes
22	DISPON	Yes	Yes	Yes	Yes	Yes
23	TEOFF	Yes	Yes	Yes	Yes	Yes
26	TEON	Yes	Yes	Yes	Yes	Yes
28	MADCTL	Yes	Yes	Yes	Yes	Yes
29	IDMOFF	Yes	Yes	Yes	Yes	Yes
34	IDMON	Yes	Yes	Yes	Yes	Yes
35	COLMOD	Yes	Yes	Yes	Yes	Yes
36	TESL	Yes	Yes	Yes	Yes	Yes
38	GETSCAN	Yes	Yes	Yes	Yes	Yes
39	WRDISBV	Yes	Yes	Yes	Yes	Yes
3A	RDDISBV	Yes	Yes	Yes	Yes	Yes
44	WRCTRLD	Yes	Yes	Yes	Yes	Yes
45	RDCTRLD	Yes	Yes	Yes	Yes	Yes
51	RDID1	Yes	Yes	Yes	Yes	Yes
52	RDID2	Yes	Yes	Yes	Yes	Yes
53	RDID3	Yes	Yes	Yes	Yes	Yes
54	RDDDB	Yes	Yes	Yes	Yes	Yes
DA	RDDDBCON	Yes	Yes	Yes	Yes	Yes
DB	RDFCS	Yes	Yes	Yes	Yes	Yes
DC	RDCCS	Yes	Yes	Yes	Yes	Yes

9.1.3 Standard Command Default Modes and Values

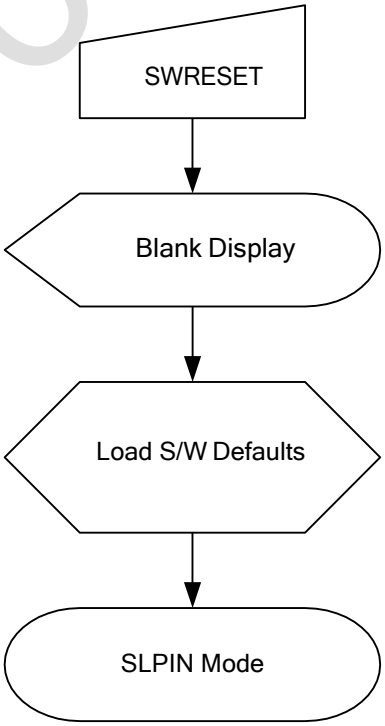
Hex Code	Operation code	Parameters	Power-on Sequence	SW Reset	HW Reset
00	**NOP**	None	N/A	N/A	N/A
01	**SWRESET**	None	N/A	N/A	N/A
04	**RDDIDIF**	3	OTP Value	OTP Value	OTP Value
05	**RDDST**	1	Refer to corresponding command parameters	Refer to corresponding command parameters	Refer to corresponding command parameters
06	**RDDPM**	1	08h	08h	08h
07	**RDDMADCTL**	1	00h	Refer to corresponding command parameters	00h
08	**RDDCOLMOD**	1	07h	07h	07h
09	**RDDIM**	1	00h	00h	00h
0A	**RDDSM**	1	00h	00h	00h
0B	**RDDSDR**	1	00h	00h	00h
0C	**SLPIN**	None	Sleep In Mode	Sleep In Mode	Sleep In Mode
0D	**SLPOUT**	None	Sleep In Mode	Sleep In Mode	Sleep In Mode
0E	**PTLON**	None			
0F	**INVOFF**	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
10	**INVON**	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
11	**ALLPOFF**	None	All Pixel Off	All Pixel Off	All Pixel Off
12	**ALLPON**	None	All Pixel Off	All Pixel Off	All Pixel Off
20	**GAMSET**	1	01h	01h	01h
21	**DISPOFF**	None	Display Off	Display Off	Display Off
22	**DISPON**	None	Display Off	Display Off	Display Off
23	**TEOFF**	None	TE Off	TE Off	TE Off
26	**TEON**	1	TE Off	TE Off	TE Off
28	**MADCTL**	1	00h	No Change	00h
29	**IDMOFF**	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
34	**IDMON**	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
35	**COLMOD**	1	07h	No Change	07h
36	**TESL**	2	0000h	0000h	0000h
38	**GETSCAN**	2	0000h	0000h	0000h
39	**WRDISBV**	1	00h	00h	00h
3A	**RDDISBV**	1	00h	00h	00h
44	**WRCTRLD**	1	00h	00h	00h
45	**RDCTRLD**	1	00h	00h	00h
51	**RDID1**	1	OTP Value	OTP Value	OTP Value
52	**RDID2**	1	OTP Value	OTP Value	OTP Value
53	**RDID3**	1	OTP Value	OTP Value	OTP Value
54	**RDDDB**	All	OTP Value	OTP Value	OTP Value
DA	**RDDDBCON**	All	OTP Value	OTP Value	OTP Value
DB	**RDFCS**	1	00h	00h	00h
DC	**RDCCS**	1	00h	00h	00h

9.2 Command Description

9.2.1 NoP (00h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	0	0	0	0	00
Description	This command does not have any effect on the display module. The NOP command may be used to terminate a Frame Memory Read or Frame Memory Write.									
Restriction	-									
Flow Chart	-									

9.2.2 SWRESET: Software Reset (01h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	0	0	0	1	01
Description	The display module performs a software reset. Registers are written with their SW Reset default values. The Frame Memory contents are unaffected by this command									
Restriction	The host processor must wait 5 milliseconds before sending any new commands to a display module following this command. The display module updates the registers during this time. If a SWRESET is sent when the display module is in SLPIN Mode, the host processor must wait 120 milliseconds before sending an SLPOUT command. SWRESET should not be sent when the display module is not in SLPIN mode.									
Flow Chart										

9.2.3 RDDIDIF: Read Display Identification Information (04h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	0	1	0	0	04
Parameter 1	**R**	ID1[7:0]								
Parameter 2	**R**	ID2[7:0]								
Parameter 3	**R**	ID3[7:0]								

Description

This read byte returns 24-bit display identification information.

The 1st Parameter identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.

The 2nd Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Color). Bits 6~0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:

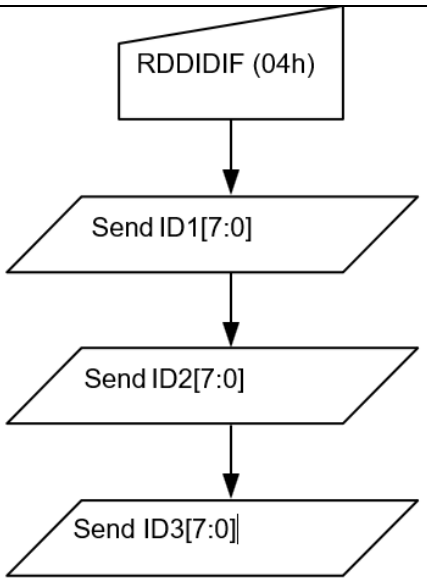
ID Byte Value V[7:0]	Version	Changes
80h		
81h		
82h		
83h		
84h		
85h		

The 3rd parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.

Restriction

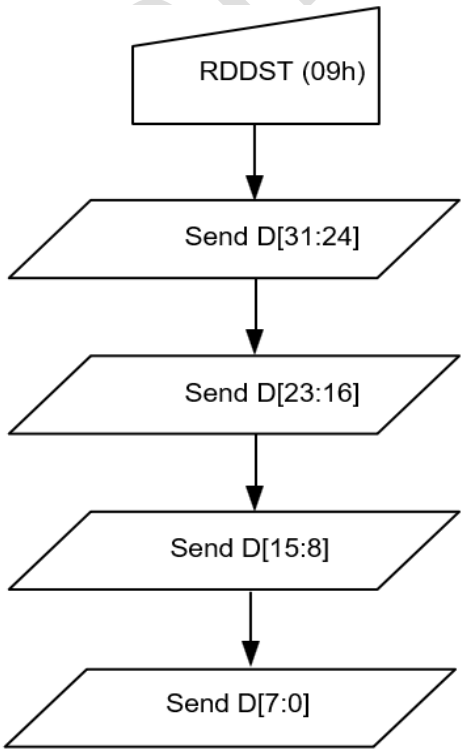
-

Flow Chart

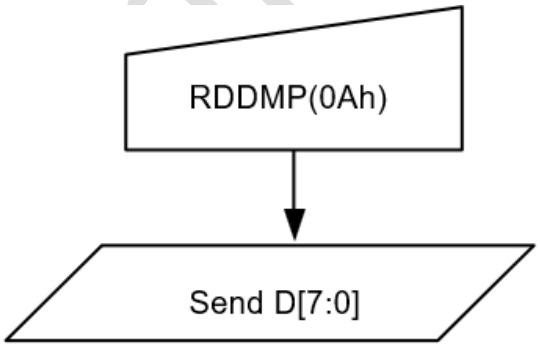


9.2.4 RDDST: Read Display Status (09h)

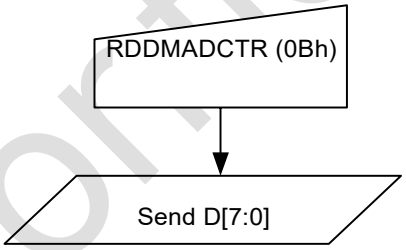
<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>09</td></tr>
<tr><td>Parameter 1</td><td>R</td><td colspan="8">D[31:24]</td><td></td></tr>
<tr><td>Parameter 2</td><td>R</td><td colspan="8">D[23:16]</td><td></td></tr>
<tr><td>Parameter 3</td><td>R</td><td colspan="8">D[15:8]</td><td></td></tr>
<tr><td>Parameter 4</td><td>R</td><td colspan="8">D[7:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D31</td><td>Booster Voltage Status</td><td>‘0’ = Booster Off.
‘1’ = Booster On.</td></tr>
<tr><td>D30</td><td>Page Address Order</td><td>‘0’ = Top to Bottom (MADCTL B7=’0’).
‘1’ = Bottom to Top (MADCTL B7=’1’).</td></tr>
<tr><td>D29</td><td>Column Address Order</td><td>‘0’ = Left to Right (MADCTL B6=’0’).
‘1’ = Right to Left (MADCTL B6=’1’)</td></tr>
<tr><td>D28</td><td>Page/Column Order</td><td>‘0’ = Normal (MADCTL B5=’0’).
‘1’ = Rotation (MADCTL B5=’1’).</td></tr>
<tr><td>D27</td><td>Display Device Line Refresh Order</td><td>‘0’ = Refresh Top to Bottom (MADCTL B4=’0’).
‘1’ = Refresh Bottom to Top (MADCTL B4=’1’).</td></tr>
<tr><td>D26</td><td>RGB/BGR Order</td><td>‘0’ = RGB (MADCTL B3=’0’).
‘1’ = BGR (MADCTL B3=’1’).</td></tr>
<tr><td>D25</td><td>Display Data Latch Data Order</td><td>‘0’ = Refresh Left to Right (MADCTL B2=’0’).
‘1’ = Refresh Right to Left (MADCTL B2=’1’).</td></tr>
<tr><td>D24</td><td>Source san sequence</td><td>‘0’ = Source output Left to Right (MADCTL B1=’0’).
‘1’ = Source output Right to Left (MADCTL B1=’1’)</td></tr>
<tr><td>D23</td><td>Gate san sequence</td><td>‘0’ = Gate output Top to Bottom (MADCTL B0=’0’).
‘1’ = Gate output Bottom to Top (MADCTL B0=’1’)</td></tr>
<tr><td>D22
D21
D20</td><td>Interface Colo
Pixel Format Definition</td><td>
<table>
<tr><th>Interface Format</th><th>D22</th><th>D21</th><th>D20</th></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 Bit/Pixel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 Bit/Pixel</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>24 Bit/Pixel</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>D19</td><td>Idle Mode On/Off</td><td>‘0’ = Idle Mode Off. ‘1’ = Idle Mode On.</td></tr>
<tr><td>D18</td><td>Partial Mode On/Off</td><td>‘0’ = Partial Mode Off, ‘1’ = Partial Mode On.</td></tr>
<tr><td>D17</td><td>Sleep In/Out</td><td>‘0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.</td></tr>
<tr><td>D16</td><td>Display Normal Mode On/Off</td><td>‘0’ = Partial or Scrolling Mode.
‘1’ = Normal Mode.</td></tr>
<tr><td>D15</td><td>Vertical Scrolling Status</td><td>‘0’ = Vertical Scrolling is Off.
‘1’ = Vertical Scrolling is On.</td></tr>
<tr><td>D14</td><td>Horizontal Scrolling Status</td><td>This bit is not applicable for this project, so it is set to ‘0’</td></tr>
<tr><td>D13</td><td>Inversion Status</td><td>‘0’ = Inversion is Off.
‘1’ = Inversion is On.</td></tr>
<tr><td>D12</td><td>All Pixels On</td><td>‘0’ = Normal mode.
‘1’ = All Pixels On.</td></tr>
<tr><td>D11</td><td>All Pixels Off</td><td>0’ = Normal mode.
‘1’ = All Pixels Off.</td></tr>
<tr><td>D10</td><td>Display On/Off</td><td>‘0’ = Display is Off.
‘1’ = Display is On.</td></tr>
</table>
</td></tr>
</table>

	D9	Tearing Effect Line On/Off	‘0’ =Tearing Effect Line Off. ‘1’ = Tearing Effect On.			
	D8		Gamma Curve Selected Gamma Curve 1	B8 0	B7 0	B6 0
			Gamma Curve 2	0	0	1
			Gamma Curve 3	0	1	0
	D7	Gamma Curve Selection	Gamma Curve 4	0	1	1
			Not Defined	1	0	0
			Not Defined	1	0	1
	D6		Not Defined Not Defined	1 1	1 1	0 1
	D5	Tearing Effect Output Line Mode	‘0’ = Mode 1, V-Blanking only. ‘1’ = Mode 2, both H-Blanking and V-Blanking.			
	D4	Horizontal Sync. (HS, DPI I/F)	‘0’ = Horizontal Sync. line is Off (“Low”). ‘1’ = Horizontal Sync. line is On (“High”).			
	D3	Vertical Sync. (VS, DPI I/F)	‘0’ = Vertical Sync. line is Off (“Low”). ‘1’ = Vertical Sync. line is On (“High”).			
	D2	Pixel Clock (DCK, DPI I/F)	‘0’ = CK line is Off (“Low”). ‘1’ = CK line is On (“High”).			
	D1	Reserved	Always = ‘0’			
	D0	Parity Error on DSI	‘0’=No Parity Error. ‘1’=Parity Error.			
	Note: This bit indicates current status of the line when this command has been sent.					
Restriction	-					
Flow Chart						

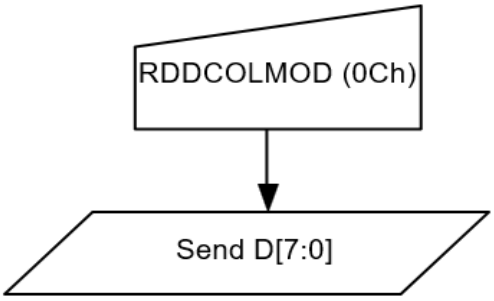
9.2.5 RDDPM: Read Display Power Mode (0Ah)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>Parameter 1</td><td>R</td><td></td><td>D7</td><td>D6</td><td>0</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td></td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td>‘0’ = Idle Mode Off.
‘1’ = Idle Mode On.</td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td>0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.</td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td>‘0’ = Display Normal Mode Off.
‘1’ = Display Normal Mode On.</td></tr>
<tr><td>D2</td><td>Display On/Off</td><td>‘0’ = Display is Off.
‘1’ = Display is On.</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td><td colspan="9">-</td></tr>
<tr><td>Flow Chart</td><td></td><td colspan="9"> 
</td></tr>
</table>

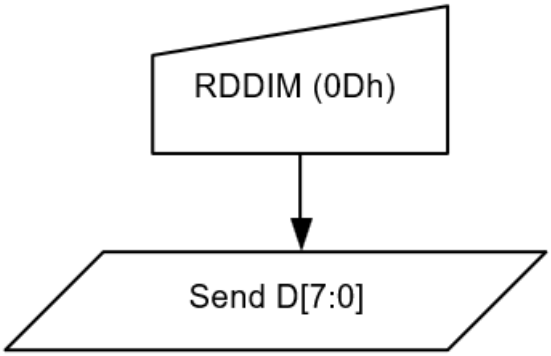
9.2.6 RDDMATCDL: Read Display MADCTL (0Bh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>D7</td><td>D6</td><td>0</td><td>0</td><td>D3</td><td>0</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td>‘0’ = Top to Bottom (When MADCTL B7=’0’).
‘1’ = Bottom to Top (When MADCTL B7=’1’).</td></tr>
<tr><td>D6</td><td>Column Address Order</td><td>‘0’ = Left to Right (When MADCTL B6=’0’).
‘1’ = Right to Left (When MADCTL B6=’1’).</td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td>‘0’ = RGB (When MADCTL B3=’0’).
‘1’ = BGR (When MADCTL B3=’1’).</td></tr>
<tr><td>D1</td><td>Source san sequence</td><td>‘0’ = Source output Left to Right (When MADCTL B1=’0’).
‘1’ = Source output Right to Left (When MADCTL B1=’1’).</td></tr>
<tr><td>D0</td><td>Gate san sequence</td><td>‘0’ = Gate output Top to Bottom (When MADCTL B0=’0’).
‘1’ = Gate output Bottom to Top (When MADCTL B0=’1’).</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

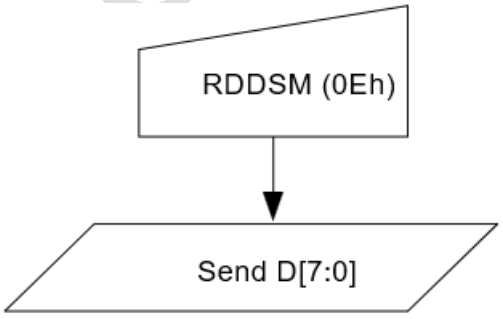
9.2.7 RDDCOLMOD: Read Display COLMOD (0Ch)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	1	1	0	0	0C
Parameter 1	**R**	-	D6	D5	D4	-	D2	D1	D0	
Description	This command gets the pixel format for the RGB image data used by the interface. D[6:4] – DPI Interface Color Pixel Format Definition, fixed @111 D[2:0] – DBI Interface Color Pixel Format Definition, fixed @000. If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module are undefined. Therefore, for a DBI display module, the Host shall ignore D[6:4] and for a DPI display module, the Host shall ignore D[2:0].									
Restriction	-									
Flow Chart										

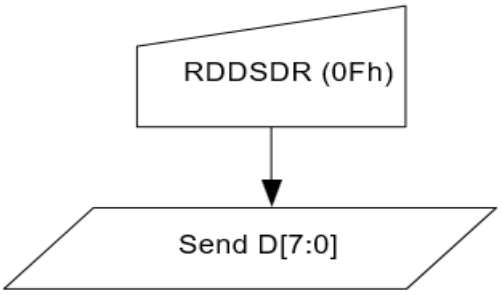
9.2.8 Read Display Image Mode (0Dh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0D</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>0</td><td>0</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D5</td><td>Inversion On/Off</td><td>‘0’ = Inversion is Off.
‘1’ = Inversion is On.</td></tr>
<tr><td>D4</td><td>All Pixels On</td><td>‘0’ = Normal Display
‘1’ = White Display</td></tr>
<tr><td>D3</td><td>All Pixels Off</td><td>‘0’ = Normal Display
‘1’ = Black Display</td></tr>
<tr><td>D2
D1
D0</td><td>Gamma Curve Selection</td><td>
<table>
<tr><th>Gamma Curve Selected</th><th>D2</th><th>D1</th><th>D0</th><th>Gamma Set(26h)</th></tr>
<tr><td>Gamma Curve1</td><td>0</td><td>0</td><td>0</td><td>CG0</td></tr>
<tr><td>Gamma Curve2</td><td>0</td><td>0</td><td>1</td><td>CG1</td></tr>
<tr><td>Gamma Curve3</td><td>0</td><td>1</td><td>0</td><td>CG2</td></tr>
<tr><td>Gamma Curve4</td><td>0</td><td>1</td><td>1</td><td>CG3</td></tr>
<tr><td>Not defined</td><td>1</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Not defined</td><td>1</td><td>0</td><td>1</td><td></td></tr>
<tr><td>Not defined</td><td>1</td><td>1</td><td>0</td><td></td></tr>
<tr><td>Not defined</td><td>1</td><td>1</td><td>1</td><td></td></tr>
</table>
</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

9.2.9 RDDSM: Read Display Signal Mode (0Eh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0E</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>‘0’ = Tearing Effect Line Off.
‘1’ = Tearing Effect On.</td></tr>
<tr><td>D6</td><td>Tearing Effect Line Output Mode</td><td>‘0’ = Mode 1.
‘1’ = Mode 2.</td></tr>
<tr><td>D5</td><td>Horizontal Sync. (RGB I/F) On/Off.</td><td>‘0’ = Horizontal Sync. Line is Off (“Low”).
‘1’ = Horizontal Sync. Line is On (“High”).</td></tr>
<tr><td>D4</td><td>Vertical Sync. (RGB I/F) On/Off.</td><td>‘0’ = Vertical Sync. Line is Off (“Low”).
‘1’ = Vertical Sync. Line is On (“High”).</td></tr>
<tr><td>D3</td><td>Pixel Clock (CK, RGB I/F) On/Off.</td><td>‘0’ = CK line is Off (“Low”).
‘1’ = CK line is On (“High”).</td></tr>
<tr><td>D2</td><td>Data Enable (DE, RGB I/F)) On/Off.</td><td>‘0’ = DE line is Off (“Low”).
‘1’ = DE line is On (“High”).</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>for future use and are set to ‘0’.</td></tr>
<tr><td>D0</td><td>Parity Error on DSI</td><td>‘0’=No Parity Error.
‘1’=Parity Error.</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

9.2.10 RDDSDR: Read Display Self-Diagnostic Result (0Fh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0F</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">The display module returns the self-diagnostic results following a SLPOUT command.
See section “0
Self-diagnostic Functions” for a description
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Register Loading Detection</td><td rowspan="2">See section “Sleep Out –command and self-diagnostic functions of the display module”</td></tr>
<tr><td>D6</td><td>Functionality Detection</td></tr>
<tr><td>D5</td><td>Chip Attachment Detection</td><td>Set to ‘0’ if feature unimplemented.</td></tr>
<tr><td>D4</td><td>Display Glass Break Detection</td><td>Set to ‘0’ if feature unimplemented.</td></tr>
<tr><td>D3</td><td rowspan="4">Reserved</td><td>Set to ‘0’.</td></tr>
<tr><td>D2</td><td>Set to ‘0’.</td></tr>
<tr><td>D1</td><td>Set to ‘0’.</td></tr>
<tr><td>D0</td><td>Set to ‘0’.</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

9.2.11 LPIN: Enter Sleep In Mode (10h)

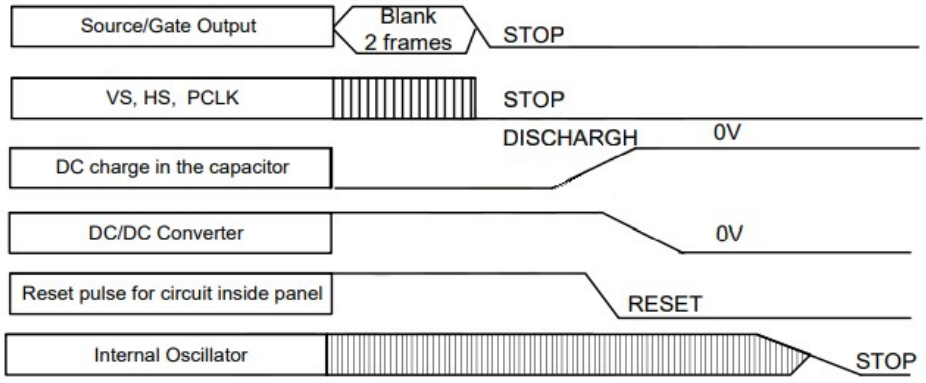
CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	1	0	0	0	0	10

Description

This command causes the LCD module to enter the minimum power consumption mode. In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports.

DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send CK, HS and VS information to DPI IF for two frames after this command is sent when the display module is in Normal mode.

In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.

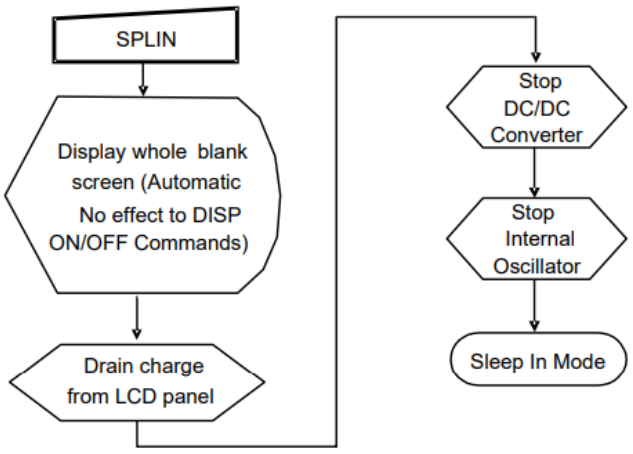


Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.

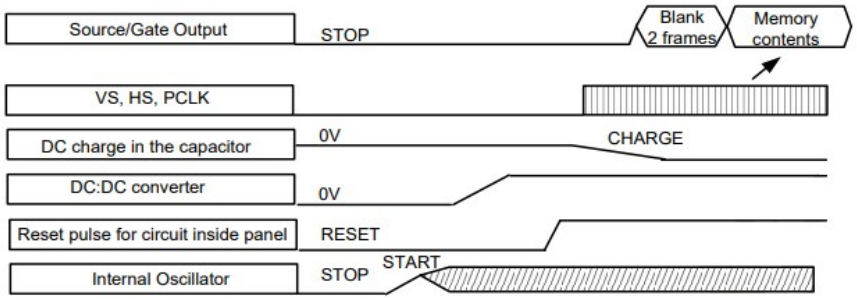


9.2.12 LPOUT:Exit Sleep In Mode(11h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	1	0	0	0	1	11

Description

This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.



User can start to send CK, HS and VS information on DPI IF before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In -mode to Sleep Out-mode in Normal Mode On. There is used an internal oscillator for blank display.

Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).

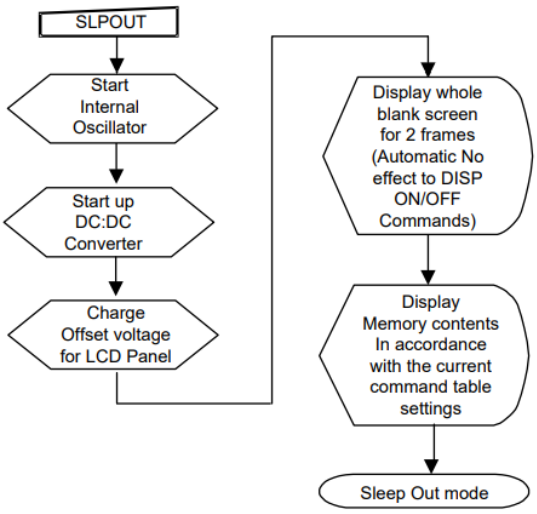
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.

The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Flow Chart

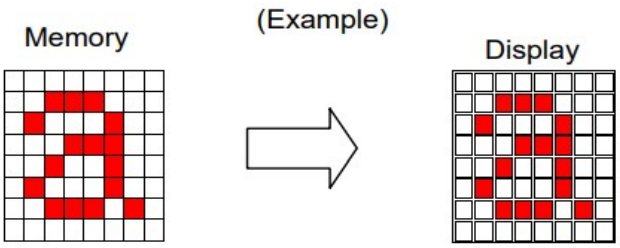
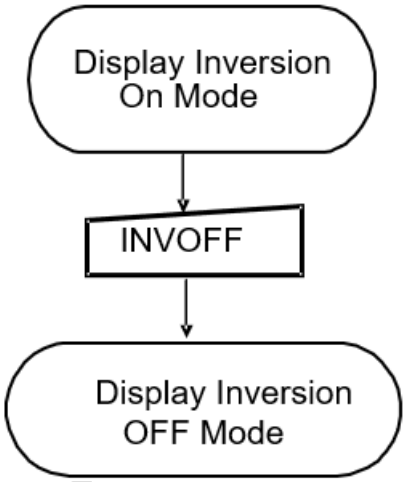
It takes 120msec to become Sleep Out mode after SLPOUT command issued.



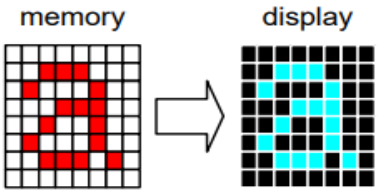
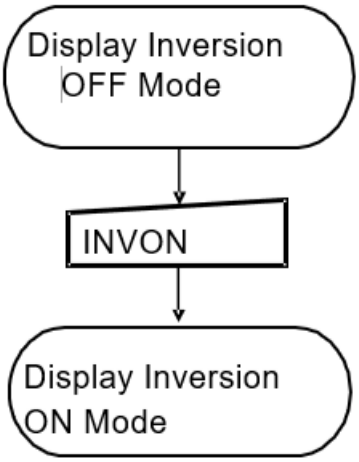
9.2.13 NORON: Enter Normal Mode (13h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	1	0	0	1	1	13
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off. There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.									
Restriction	This command has no effect when Normal Display mode is active.									
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.									

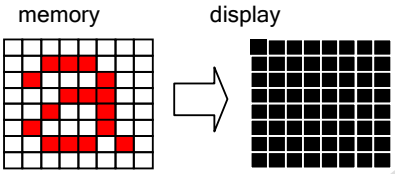
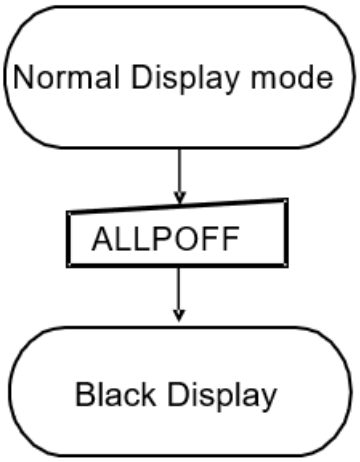
9.2.14 INVOFF: Display Inversion Off (20h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	0	0	0	0	20
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. 									
Restriction	This command has no effect when module is already in inversion off mode.									
Flow Chart										

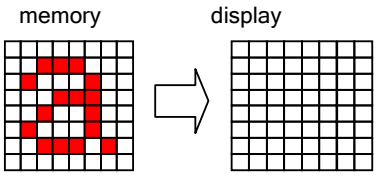
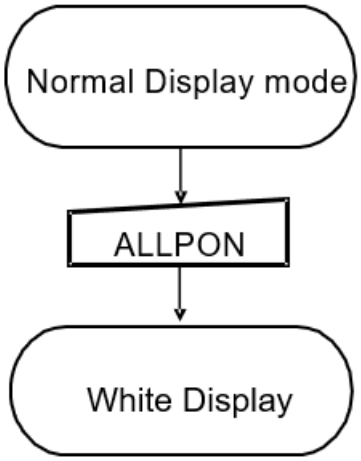
9.2.15 INVON: Display Inversion On (21h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	0	0	0	1	21
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in inversion on mode.									
Flow Chart										

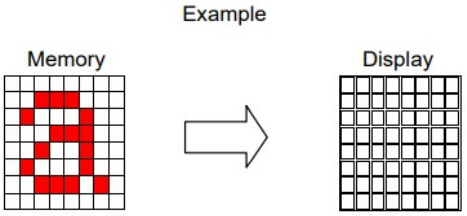
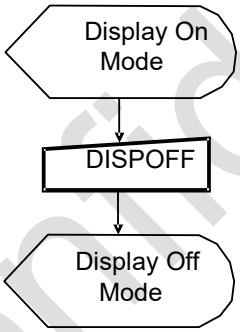
9.2.16 ALLPOFF: All Pixel Off (22h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	0	0	1	0	22
Description	This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status (Example)  'All Pixels On', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display panel is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' -commands.									
Restriction	This command has no effect when module is already in All Pixel Off mode.									
Flow Chart										

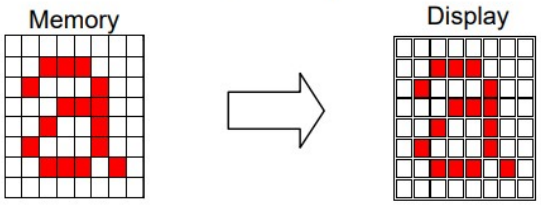
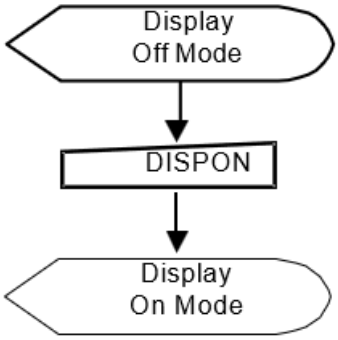
9.2.17 ALLPON: All Pixel On (23h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	0	0	1	1	23
Description	This command turns the display panel white in ‘Sleep out ‘ –mode and a status of the ‘Display On/Off’ –register can be ‘on’ or ‘off’. This command makes no change of contents of frame memory. This command does not change any other status. (Example)  ‘All Pixels Off’, ’Normal Display Mode On’ or ’Partial Mode On’ – commands are used to leave this mode. The display is showing the content of the frame memory after ‘Normal Display Mode On’ and ‘Partial Mode On’ –commands.									
Restriction	This command has no effect when module is already in all Pixel On mode.									
Flow Chart	 									

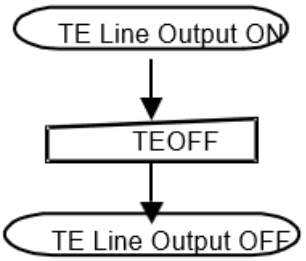
9.2.18 DISPOFF: Display Off (28h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	1	0	0	0	28
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. 									
Restriction	This command has no effect when module is already in display off mode.									
Flow Chart										

9.2.19 DISPON: Display On (29h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	1	0	0	1	29
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in display on mode.									
Flow Chart										

9.2.20 TEOFF: Tearing Effect Line OFF (34h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	0	1	0	0	34
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									
Flow Chart										

9.2.21 TEON: Tearing Effect Line ON (35h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	0	1	0	1	35
Parameter 1	**W**	X	X	X	X	X	X	X	M	

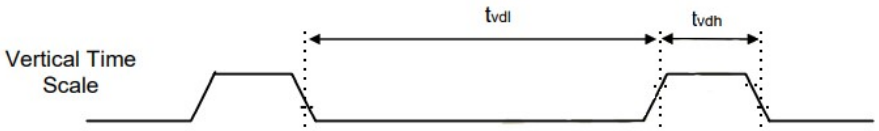
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

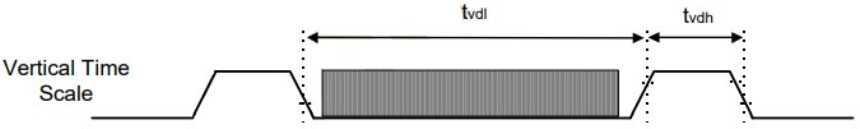
When M=0:

The Tearing Effect Output line consists of V-Blanking information only:



When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

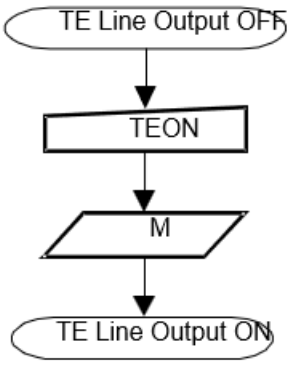


Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

Flow Chart



9.2.22 MADCTL: Memory Access Control(36h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	0	1	1	0	36
Parameter 1	**W**	B7	B6	0	0	B3	0	B1	B0	

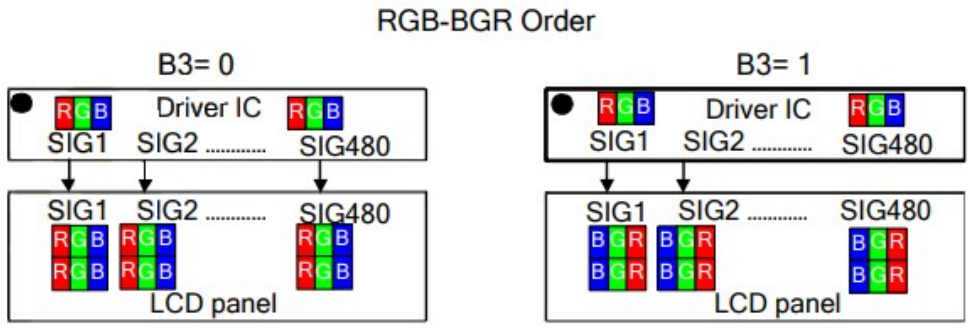
Description

This command defines read/write scanning direction of frame memory.

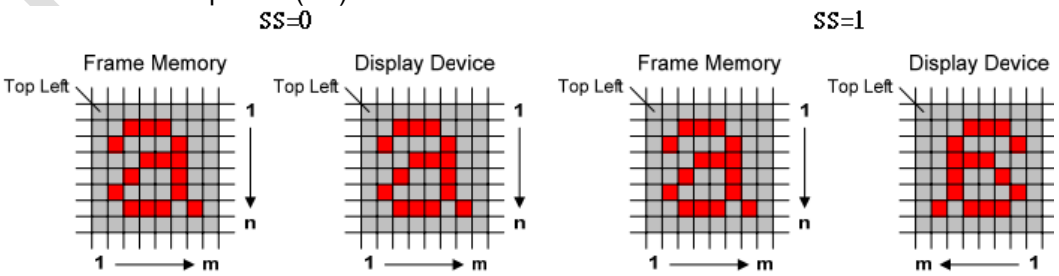
This command makes no change on the other driver status.

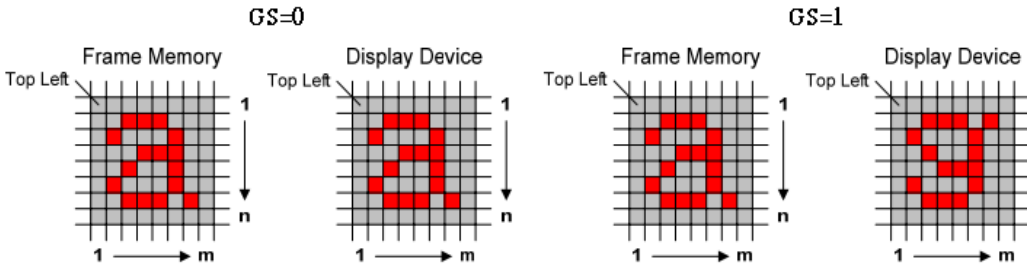
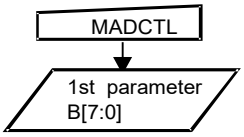
Bit	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	Select the Gate driver scan direction on panel module
B6	COLUMN ADDRESS ORDER (MX)	Select the Source driver scan direction on panel module
B3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
B1	Flip Horizontal (LR)	Select the Source driver scan direction on panel module
B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module

RGB-BGR ORDER (BGR):

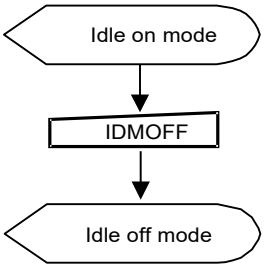


Source scan sequence (LR):



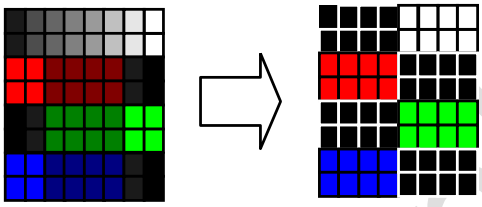
	Gate scan sequence (UD):  Note: Top-Left (0,0) means a physical memory location.
Restriction	-
Flow Chart	

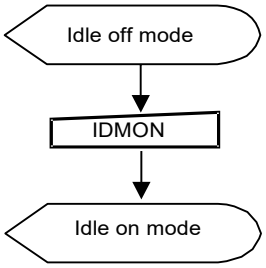
9.2.23 IDMOFF: Idle Mode Off (38h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	1	0	0	0	38
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors.									
Restriction	This command has no effect when module is already in idle off mode.									
Flow Chart										

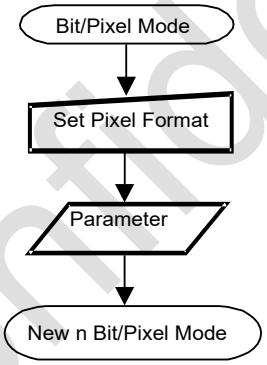
9.2.24 IDMON: Idle Mode On (39h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>39</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

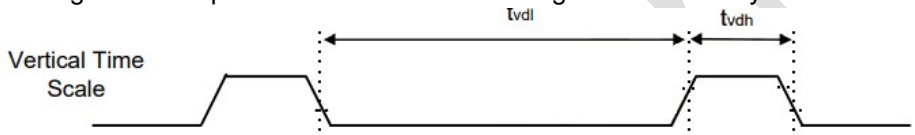
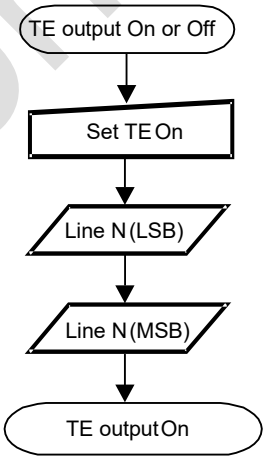
(Example)
Memory Display
 

Memory contents vs. Display Color
<table>
<tr><th></th><th>R7-R0</th><th>G7-G0</th><th>B7-B0</th></tr>
<tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Magent</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr>
<tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr>
<tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr>
<tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr>
</table>
X=don’t care</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in idle on mode.</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

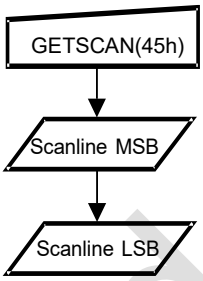
9.2.25 COLMOD: Interface Pixel Format (3Ah)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	1	0	1	0	3A
Parameter 1	**W**	X	D6	D5	D4	X	D2	D1	D0	
Description	This command is used to define the format of RGB picture data. D6~D4 : DPI Pixel format Definition, fixed @111. D2~D0 : DBI Pixel format Definition, fixed @000. If a particular interface, enter DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module undefined. Reference to: **7.3.2 RGB Data format**									
Restriction	There is no visible effect until the Frame Memory is written to.									
Flow Chart										

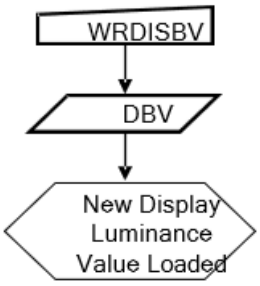
9.2.26 TESL: Set Tear Effect Scanline (44h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	0	0	1	0	0	44
Parameter 1	**W**	TELINE[15:8]								
Parameter 2	**W**	TELINE[7:0]								
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only:  **Note**: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.									
Restriction	The command has no effect when Tearing Effect output is already ON.									
Flow Chart	 									

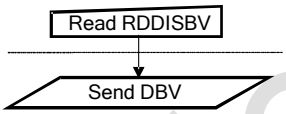
9.2.27 GETSCAN: Get the Current Scanline (45h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	0	0	1	0	1	45
Parameter 1	**W**	SLN[15:8](8'b0)								
Parameter 2	**W**	SLN[7:0](8'b0)								
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VS + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get scanline is undefined.									
Restriction	-									
Flow Chart										

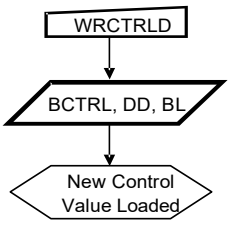
9.2.28 WRDISBV: Write Display Brightness (51h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	0	0	1	51
Parameter 1	**W**	DBV[7:0]								
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									
Flow Chart										

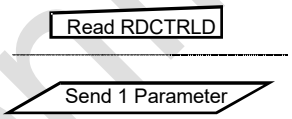
9.2.29 RDDISBV: Read Display Brightness Value (52h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	0	1	0	52
Parameter 1	**R**	DBV[7:0]								
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									
Flow Chart										

9.2.30 WRCTRLD: Write CTRL Display (53h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	0	1	1	53
Parameter 1	**W**	X	X	BCTRL	X	DD	BL	X	X	
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don’t care.									
Restriction	-									
Flow Chart										

9.2.31 RDCTRLD: Read CTRL Value Display (54h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	1	0	0	54
Parameter 1	**R**	0	0	BCTRL	0	DD	BL	0	0	
Description	This command returns ambient light and brightness control values, see chapter: BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On									
Restriction	-									
Flow Chart										

9.2.32 RDDDB: Read DDB Start (A1h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	0	1	0	0	0	0	1	A1
Parameter 1	**R**	X	X	X	X	X	X	X	X	
:	**R**	X	X	X	X	X	X	X	X	
Parameter n	**R**	X	X	X	X	X	X	X	X	

Description

This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data.

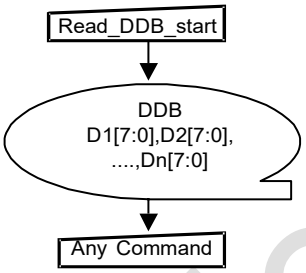
The format of returned data is as follows:
Parameter 1: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.

Parameter 2: MS (most significant) byte of Supplier ID.

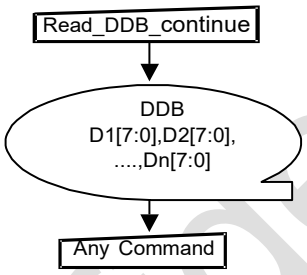
Parameter 3: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.

Parameter 4: MS (most significant) byte of Supplier Elective Data
Parameter 5: single-byte *Escape or Exit Code* (EEC). The code is interpreted as follows:
- FFh - Exit code – there is no more data in the Descriptor Block
- 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard)
- Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in *MIPI Alliance Standard for Device Descriptor Block (DDB)*.

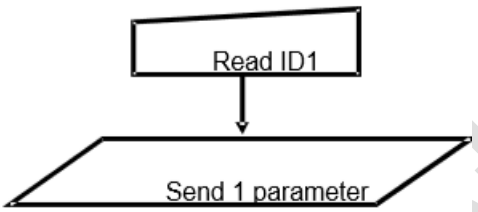
DDBs may contain many more data fields providing information about the peripheral.
In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command RDDDB: Read DDB Start (A1h) from host processor to peripheral, which includes the bus turn-around token.
The peripheral then takes control of the bus and returns the requested data. The peripheral response to RDDDB: Read DDB Start (A1h) is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command.
The response to a RDDDB: Read DDB Start (A1h) command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing

	the returned DDB data, the host processor may initiate a RDDDBCON: Read DDB Continue (A8h) command to access the next portion of the DDB. A RDDDBCON: Read DDB Continue (A8h) command begins the next read at the location following the last byte of the previous data read from the DDB. Subsequent RDDDBCON: Read DDB Continue (A8h) commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any **Read DDB xxx** command.
Restriction	-
Flow Chart	

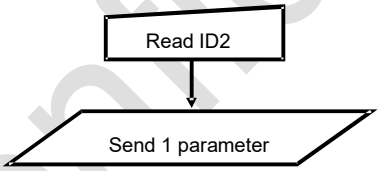
9.2.33 RDDDBCON: Read DDB Continue (A8h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	0	1	0	1	0	0	0	A8
Parameter 1	**R**	X	X	X	X	X	X	X	X	
:	**R**	X	X	X	X	X	X	X	X	
Parameter n	**R**	X	X	X	X	X	X	X	X	
Description	A RDDDB: Read DDB Start (A1h) command should be executed at least once before a RDDDBCON: Read DDB Continue (A8h) command to define the read location. Otherwise, data read with a RDDDBCON: Read DDB Continue (A8h) command is undefined.									
Restriction	-									
Flow Chart										

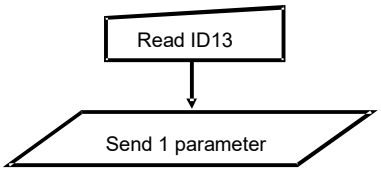
9.2.34 RDID1: Read ID1 (DAh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	1	0	1	1	0	1	0	DA
Paameter 1	**R**	module's manufacturer[7:0]								
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.									
Restriction	-									
Flow Chart										

9.2.35 RDID2: Read ID2 (DBh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DB</td></tr>
<tr><td>Parameter 1</td><td>R</td><td colspan="8">LCD module/driver version [7:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:
<table>
<tr><th>ID Byte Value V[7:0]</th><th>Version</th><th>Changes</th></tr>
<tr><td>80h</td><td></td><td></td></tr>
<tr><td>81h</td><td></td><td></td></tr>
<tr><td>82h</td><td></td><td></td></tr>
<tr><td>83h</td><td></td><td></td></tr>
<tr><td>84h</td><td></td><td></td></tr>
<tr><td>85h</td><td></td><td></td></tr>
</table>
X= Don't care</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

9.2.36 RDID3: Read ID3 (DCh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	1	0	1	1	1	0	0	DC
Parameter 1	**R**	LCD module/driver ID[7:0]								
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.									
Restriction	-									
Flow Chart										

10 Electrical Specifications

10.1 Absolute maximum ratings

Symbol	Parameter	Unit	Value	Note
VCI	Analog Supply Voltage	V	-0.3 to +6.6	Note(3) (4)
VDDI	Interface Supply Voltage	V	-0.3 to +3.6	Note(3),(4)
VDDM	High speed interface Supply Voltage	V	-0.3 to +3.6	Note(3) (5)
VSP	Positive Voltage input	V	-0.3 to +6.6	Note(6)
VSN	Negative Voltage input	V	-0.3 to -6.6	Note(7)
VGH	Power Supply Voltage	V	-0.3 to +22	Note(8)(10)
VGL	Power Supply Voltage	V	-0.3 to -16	Note(9)(10)
Top	Operating Temperature	°C	-40 to +85	Note(11)
Stg	Storage Temperature	°C	-55 to +110	Note(12)

Note:

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under DC Characteristics.
3. VDDI, VSS must be maintained.
4. To make sure VDDI ≥ VSS, VCI≥ VSSA .
5. To make sure VDDM ≥ VSSM.
6. To make sure VSP ≥ VSSA.
7. To make sure VSSA ≥ VSN
8. To make sure VGH ≥ VSSA.
9. To make sure VSSA ≥ VGL
10. VGH +|VGL| < 30V
11. For die and wafer products, specified up to +85℃.

This temperature specifications apply to the COG package.

10.2 DC Characteristics

10.2.1 RGB Interface DC electrical characteristics

(T_A=-40 ~ 85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VCI	V_{IN}	Analog Supply Voltage	2.5	-	6.6	
VDDI	V_{IN}	Interface Supply Voltage	2.5	-	3.6	
VSP	V_{IN}	Analog Supply Voltage	4.5	-	6.0	
VSN	V_{IN}	Analog Supply Voltage	2.5	-	-6.0	
VDDM	V_{IN}	High speed interface Supply Voltage	2.5	-	3.6	
Input high voltage	V_{IH}	VDDI= 2.5 ~ 3.3V VCIP= 2.5 ~ 6.0V VCI= 2.5 ~ 6.0V	0.7 x VDDI	-	VDDI	V
Input low voltage	V_{IL}		0	-	0.3 x VDDI	V
Output high voltage (SDA, GPO)	V_{OH1}	I_{OH} = -1.0 mA	0.8 x VDDI	-	VDDI	V
Output low voltage (SDA, GPO)	V_{OL1}	VDDI= 2.5 ~ 3.3V I_{OL} = 1.0 mA	0	-	0.2 x VDDI	V
Logic High level input current	I_{IH}	VS, HS	-	-	1	μA
		RESX, SCL, CSX,	-	-	1	μA
	I_{IHD}	DB[23…0], SDA	-	-	1	μA
		DB[23…0]	-	-	1	μA
Logic Low level input current	I_{IL}	VS, HS	-1	-		μA
		RESX, CSX, SCL	-1	-		μA
	I_{ILD}	DB[23…0], SDA	-1	-		μA
		DB[23…0]	-1	-		μA
Current consumption standby mode (VCIP/VCI-VSS)	$I_{ST(VDD)}$	VCI/VDDM=3.3V,	-	TBD	-	μA

Current consumption standby mode (VDDI– VSS)	$I_{ST(VDDI)}$	VDDI=3.3V T_A =25°C	-	TBD	-	μA
Current consumption during Deep-standby mode (VCIP/VCI-VSS)	$I_{DP-ST(VDD)}$	VCI/VDDM=3.3V, VDDI=3.3V T_A =25°C	-	TBD	-	μA
Current consumption during Deep-standby mode (VDDI– VSS)	$I_{DP-ST(VDDI)}$		-	TBD	-	μA

10.2.2 LVDS DC electrical characteristics

(T_A=-40 ~ 85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential input high threshold voltage	**Rx_{VTH}**	**Rx_{VCM}=1.2V**	+0.1	0.2	0.3	V
Differential input low threshold voltage	**Rx_{VTL}**		-0.3	-0.2	-0.1	V
Input voltage range (singled-end)	**Rx_{VIN}**		0.7	-	1.7	V
Differential input common mode voltage	**Rx_{VCM}**	**|VID|=0.2**	1	1.2	1.4	V
Differential input impedance	**ZID**		80	100	125	ohm
Differential input voltage	**|VID|**		0.2	-	0.6	V
Differential input leakage current	**I_{LCLVDS}**		-10	-	+10	uA
LVDS Digital Stand-by Current	**I_{STLVDS}**	**Clock & all Functions are stopped**	-	TBD	-	uA

Table 10.3: LVDS DC characteristic

Single-End Signals

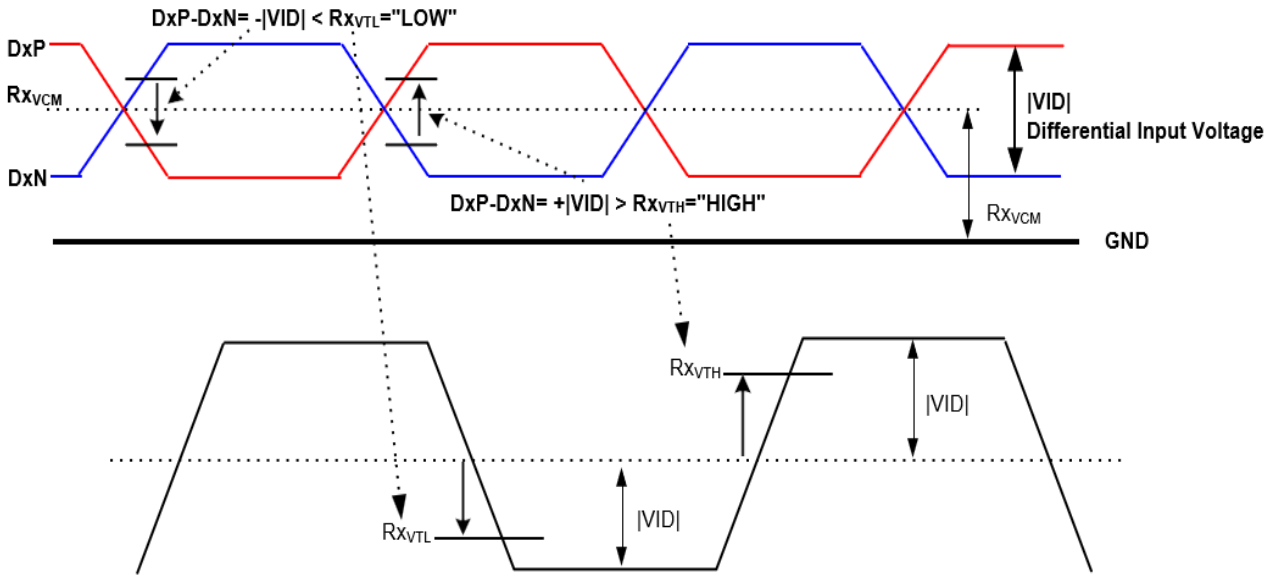


Figure 10.1: LVDS input timings

10.3 AC Characteristics

10.3.1 Reset input timings

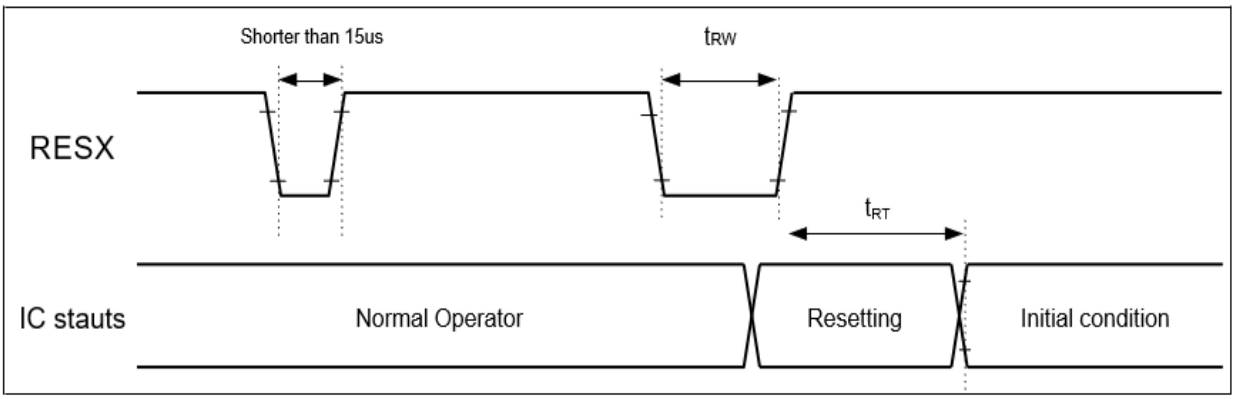


Figure 10.2: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset "L" pulse width(2)	RESX	20	-	µs
t_{RT}	Reset complete time(3)	-	-	5(5)	ms
		-	-	120(6) (7) (8)	ms

Note:

1. The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset complete time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 15 µs	Reset Rejected
Longer than 20 µs	Reset
Between 15 µs and 20 µs	Reset Start

3. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

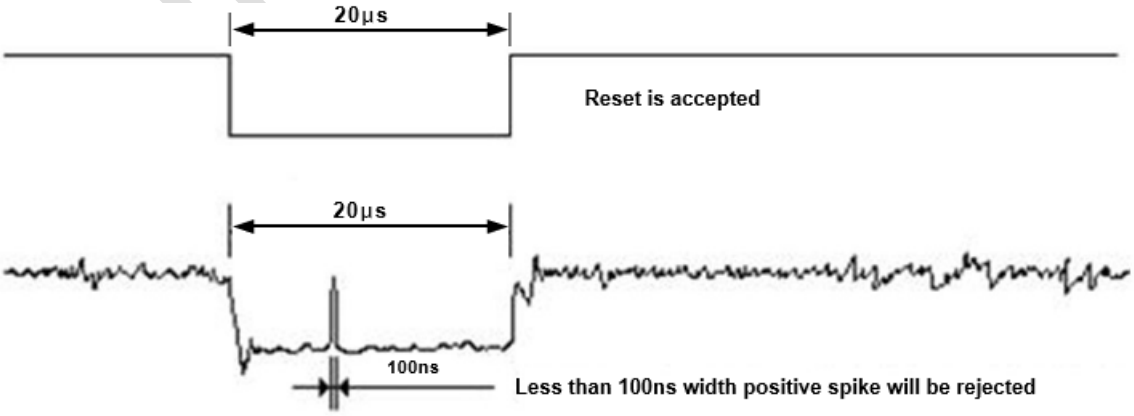


Table 10.4: Reset timings

1. When Reset is applied during Sleep In Mode.
2. When Reset is applied during Sleep Out Mode.
3. is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.
4. After Sleep Out command, it is necessary to wait 120msec then send RESX.

10.3.2 SPI electronic characteristic

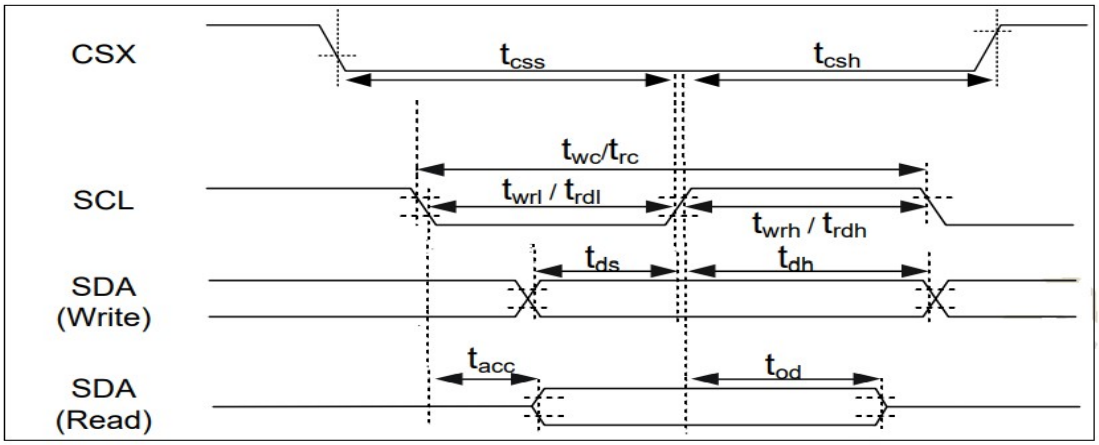


Figure 10.3: SPI interface AC characteristics

(T_A=25°C, VDDI**=3.3V, VCI=3.3V)**

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{css} t_{csh}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
SCL (Write)	t_{wc} t_{wrh} t_{wrl}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 40 40	- - -	ns	-
SCL (Read)	t_{rc} t_{rdh} t_{rdl}	Read cycle Control pulse “H” duration Control pulse “L” duration	150 60 60	- - -	ns	-
SDA (Write)	t_{ds} t_{dt}	Data setup time Data hold time	30 30	- -	ns	Note(1)
SDA (Read)	t_{acc} t_{od}	Read access time Output disable time	- 10	35 50	ns	

Note:

1. For maximum C_L=30pF, for minimum C_L=8pF.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
3. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Table 10.5: SPI interface AC characteristics

10.3.3 LVDS electronic characteristics

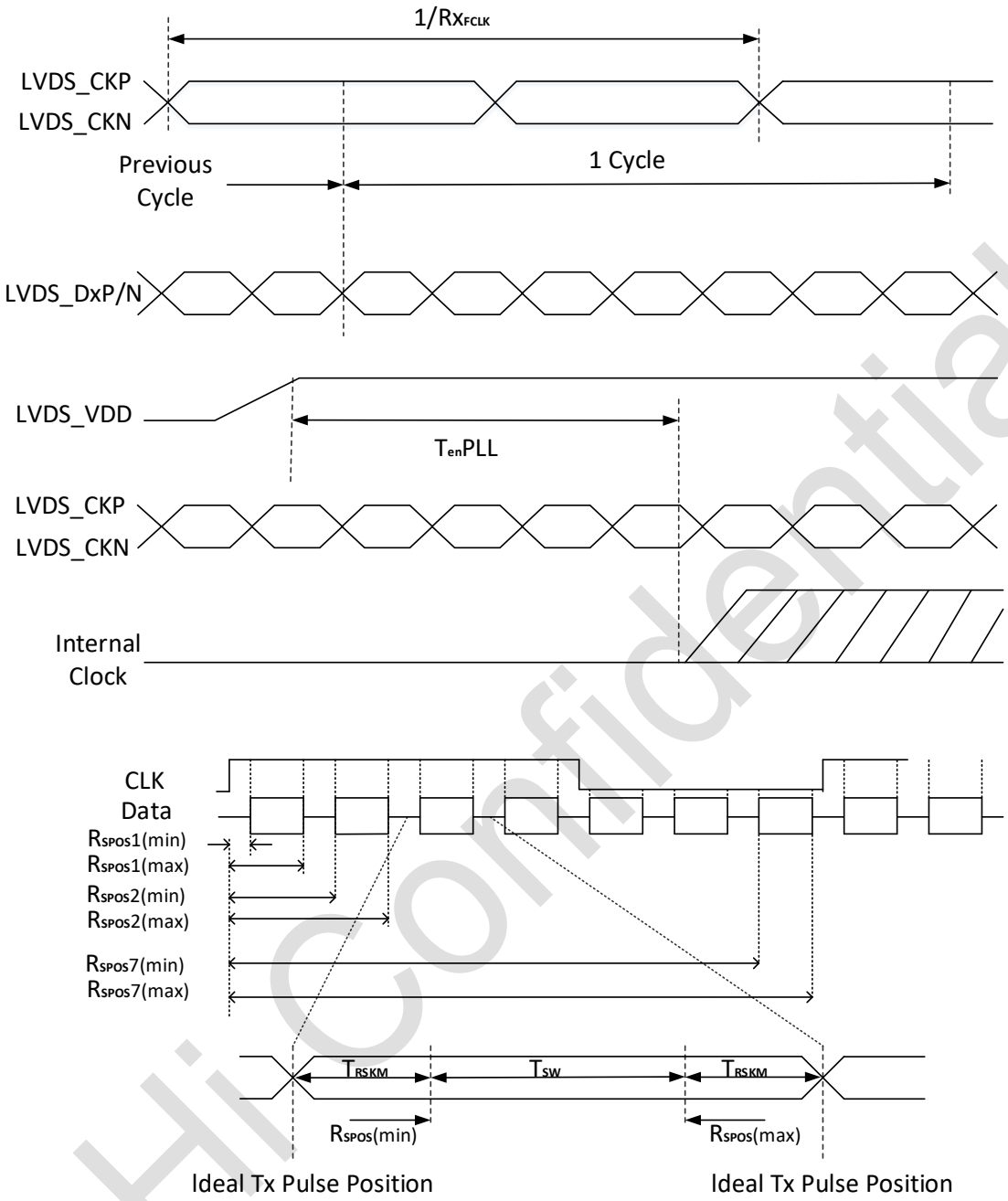


Figure 10.4: LVDS AC characteristics

TSW: Strobe width (Internal data sampling window)

Rspos : Receiver strobe position

TRSKM : Receiver strobe margin

Signal	Symbol	Min.	Typ	Max	Unit	Description
Clock frequency	Rx_{FCLK}	30		TBD	MHz	Refer to input timing table for each display resolution
Input data skew margin	T_{RSKM}	50		-	ps	|VID| = 200mV RxVCM = 1.2V RxFCLK = 81MHz
Clock high time	T_{LVCH}	-	4/(7x Rx_{FCLK})	-	ns	-
Clock low time	T_{LVCL}	-	3/(7xRx_{FCLK})	-	ns	
PLL wake-up time	T_{en}PLL	-		150	us	

Table 10.6: LVDS AC characteristics

10.3.4 DSI D-PHY electronic characteristics

The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 11.5 shows the complete set of electronic functions required for a fully featured PHY transceiver.

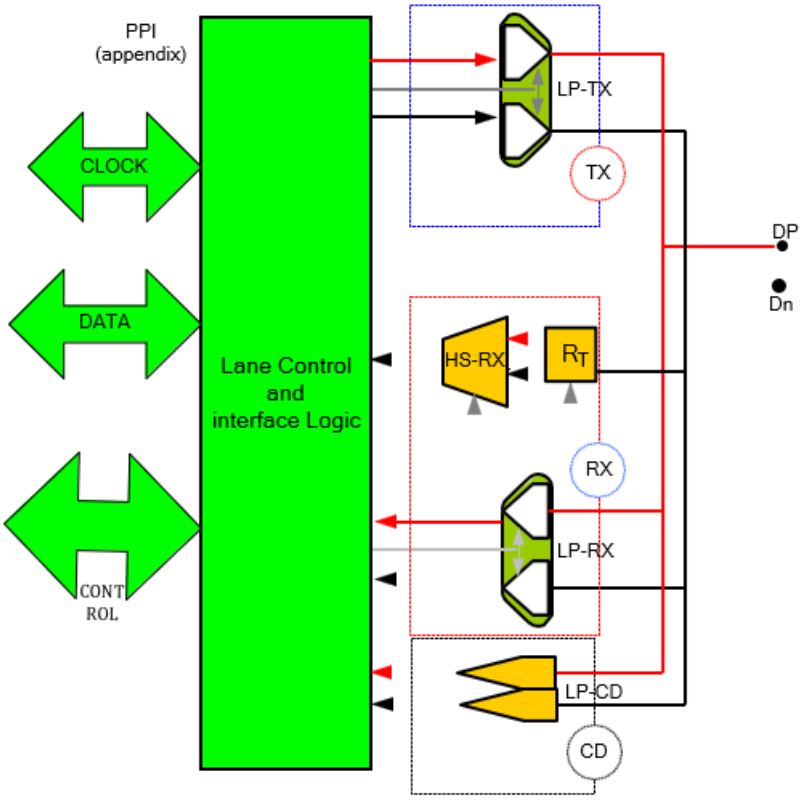


Figure 10.5: Electronic functions of a D-PHY transceiver

Figure 11.6 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speedmode during normal operation.

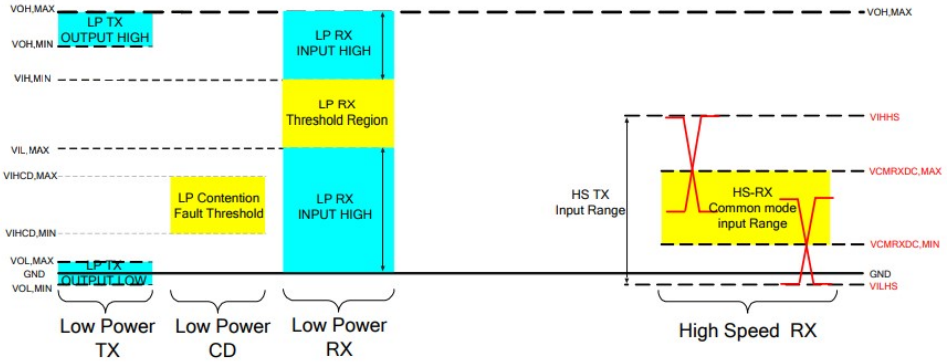


Figure 10.6: HS and LP signal levels

The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 10.7: LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30-0.075 * (VO, INST-700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note:

1. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
2. When the output voltage is between 400 mV and 930 mV.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
5. This value represents a corner point in a piecewise linear curve.
6. When the output voltage is in the range specified by VPIN(absmax).
7. When the output voltage is between 400 mV and 700 mV.
8. Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
9. When the output voltage is between 700 mV and 930 mV.

Table 10.8: LP-TX AC Specifications

The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 11.7 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.

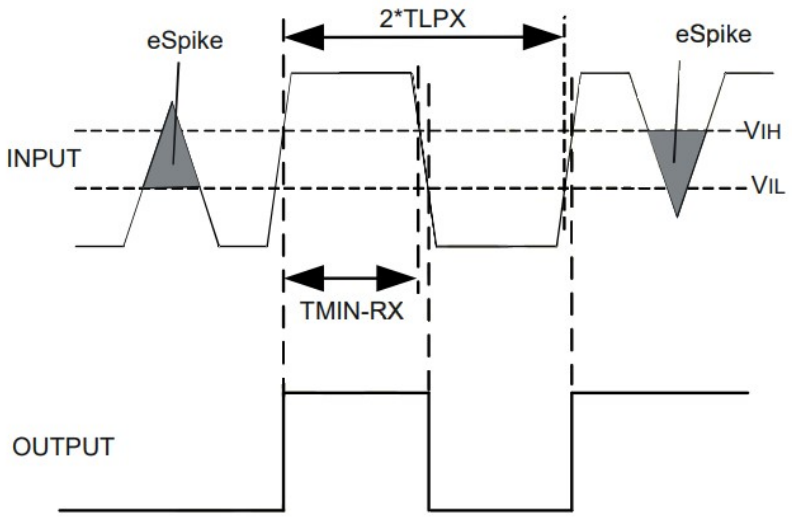


Figure 10.7: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Table 10.9: LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note:

1. Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

Table 10.10: LP-RX AC Specifications

Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.
2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 10.11: Contention Detector DC Specifications

High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 10.12: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{pp}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note:

1. ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
2. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 10.13: HS Receiver AC Specifications

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 10.8.

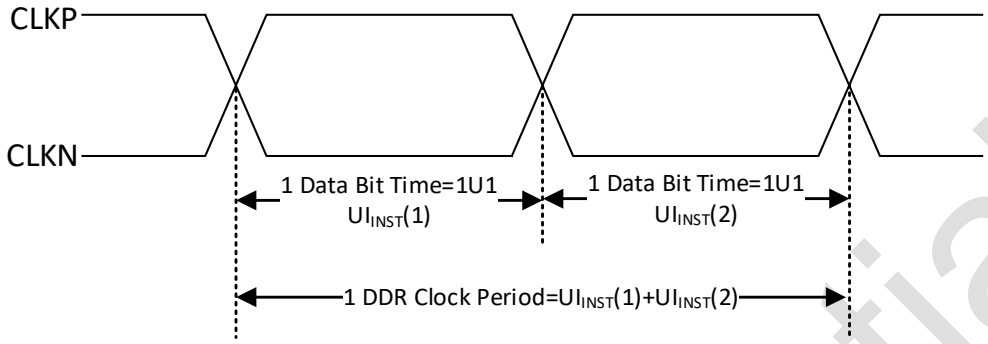


Figure 10.8: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	3.33	ns	(1), (2), (3), (4), (5)

Note:

1. This value corresponds to a minimum 300 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
3. Maximum total bit rate is 700Mbps/per lane of 2 data lanes 24-bit data format
4. Maximum total bit rate is 700Mbps/per lane of 3 data lanes 24-bit data format
5. Maximum total bit rate is 500Mbps/per lane of 4 data lanes 24-bit data format

Table 10.14: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 11.9. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

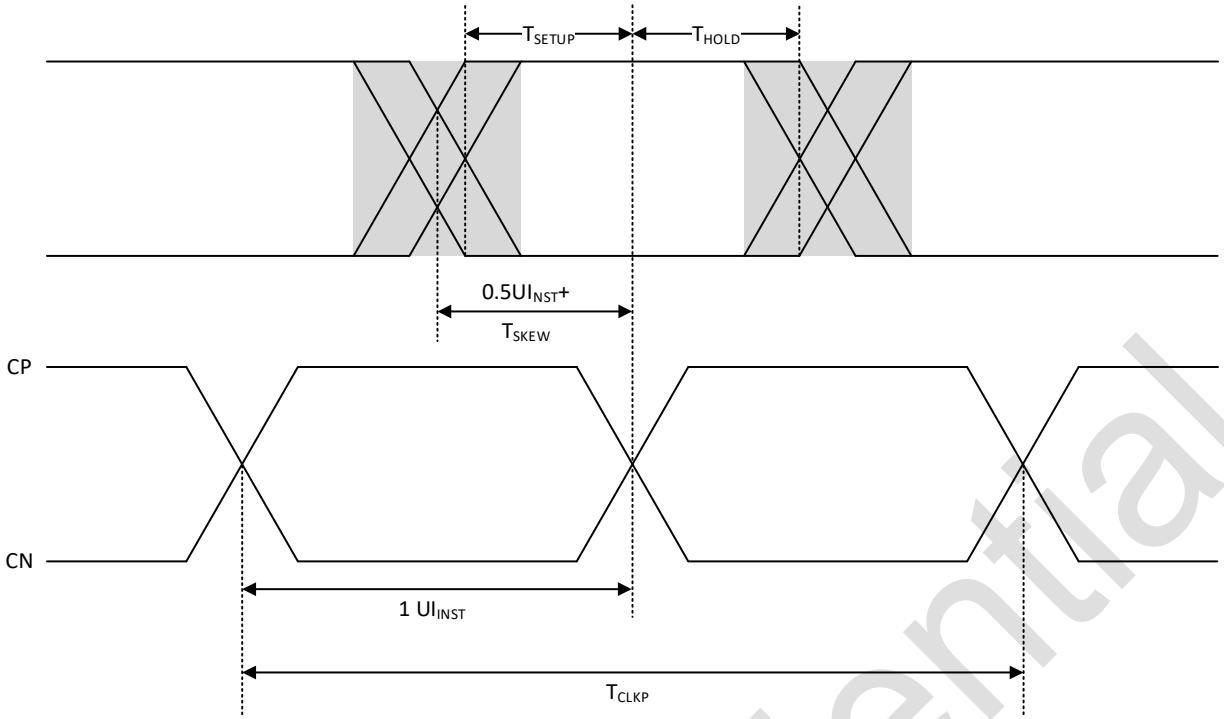


Figure 10.9: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 11.15. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 11.15 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note:

1. Total setup and hold window for receiver of 0.3*UIINST.

Table 10.15: Data to Clock Timing Specifications

Burst Mode Data Transmission

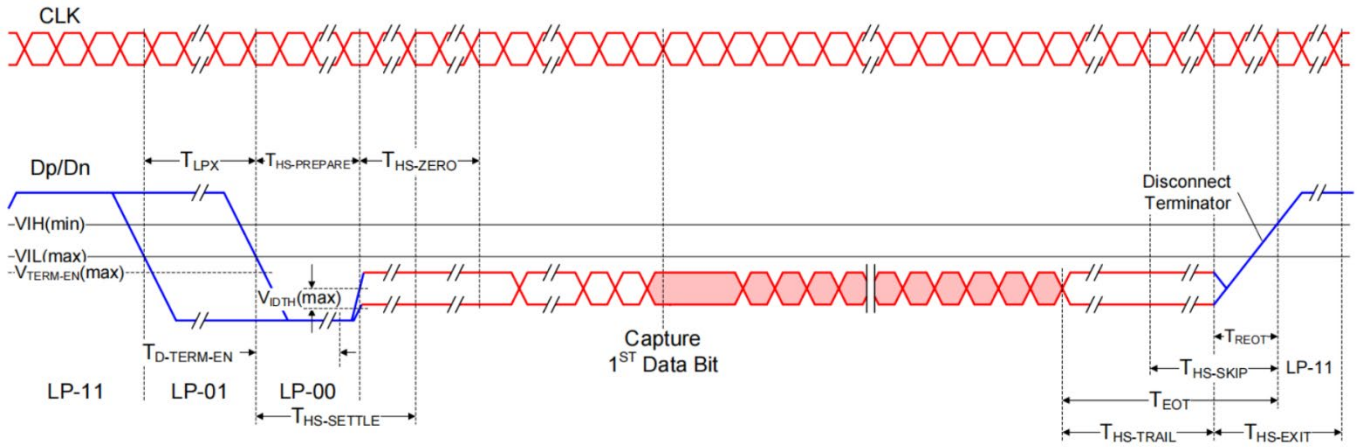


Figure 11.10: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns

$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(n*8*UI, 60+n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

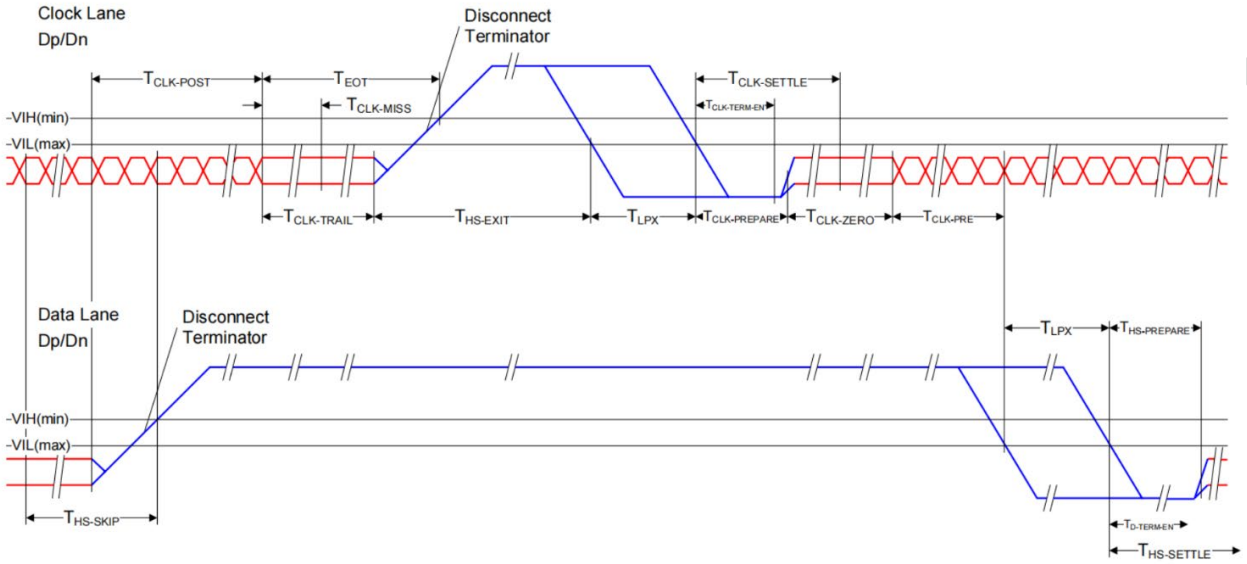
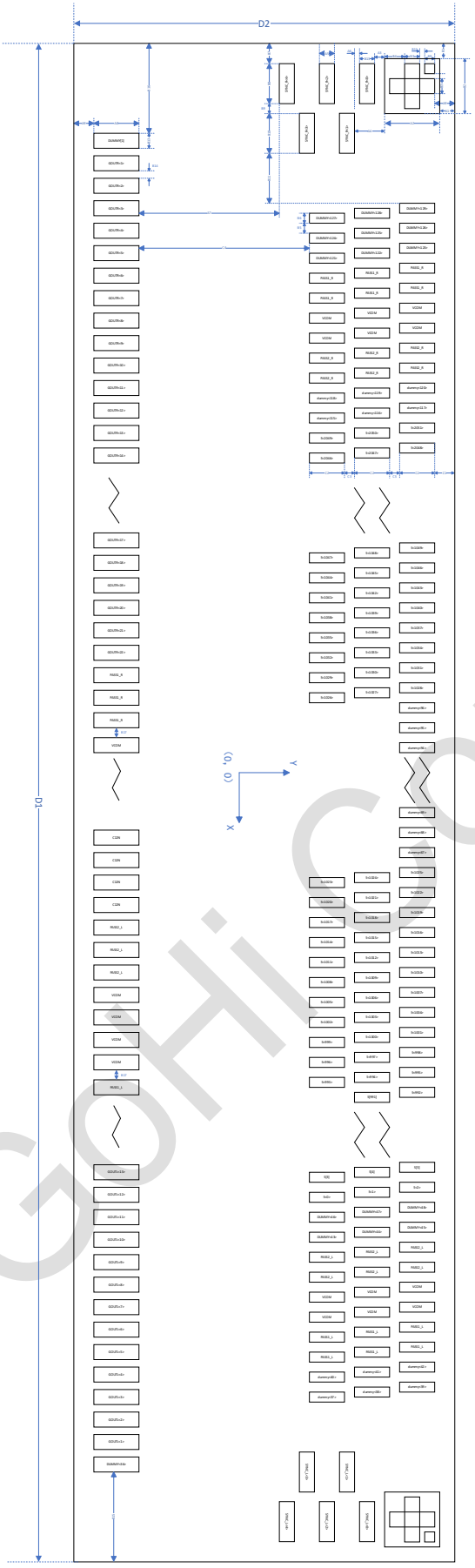


Figure 10.11: Switching the Clock Lane between Clock Transmission and Low-Power Mode

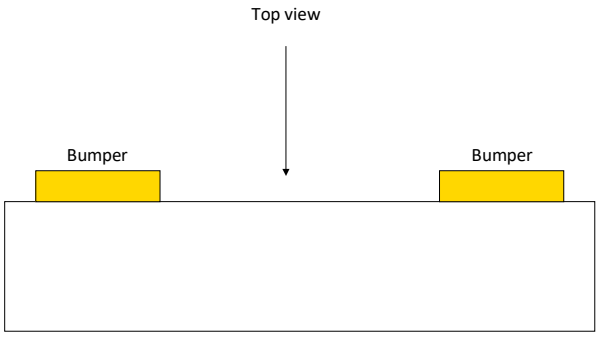
Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

11 Chip Information

11.1 Pad Assignment



Symbol	Dimension
Length (um)	27598
Width (um)	898
Thickness(um)	200(TBD)
Input Bump width (um)	30
Input Bump Numbers	606
Output Bump width (um)	16
Output Bump Numbers	2191



Symbol	Dimension
A1	39
A2	120
A3	21
A4	61
A5	30
A6	10
A7	395
A8	93
A9	40

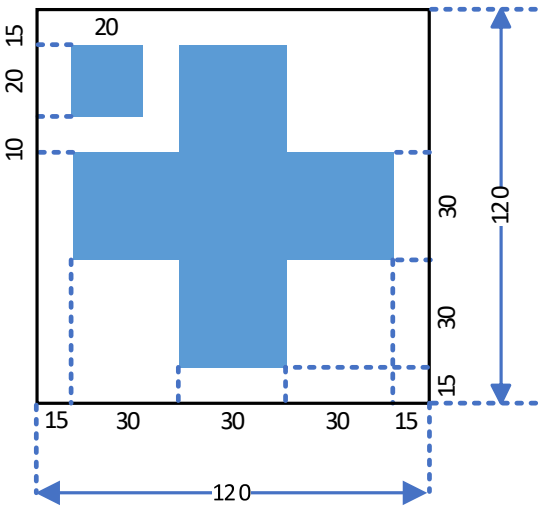
Symbol	Dimension
B1	39
B2	120
B3	30
B4	45
B5	20
B6	16
B7	49
B8	80
B9	20

Symbol	Dimension
B10	80
B11	122
B12	10
B13	30
B14	15
B15	161.5
B16	161.5
B17	25

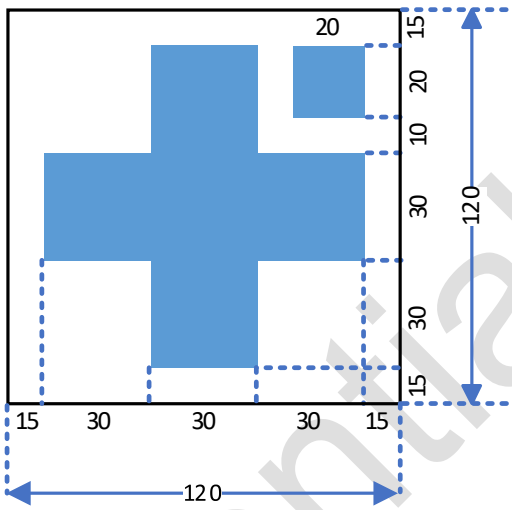
Symbol	Dimension
C1	40
C2	73
C3	17
C4	472
D1	27598
D2	898

11.2 Alignment Mark (Unit: um)

A1:Right (-13700, 350)



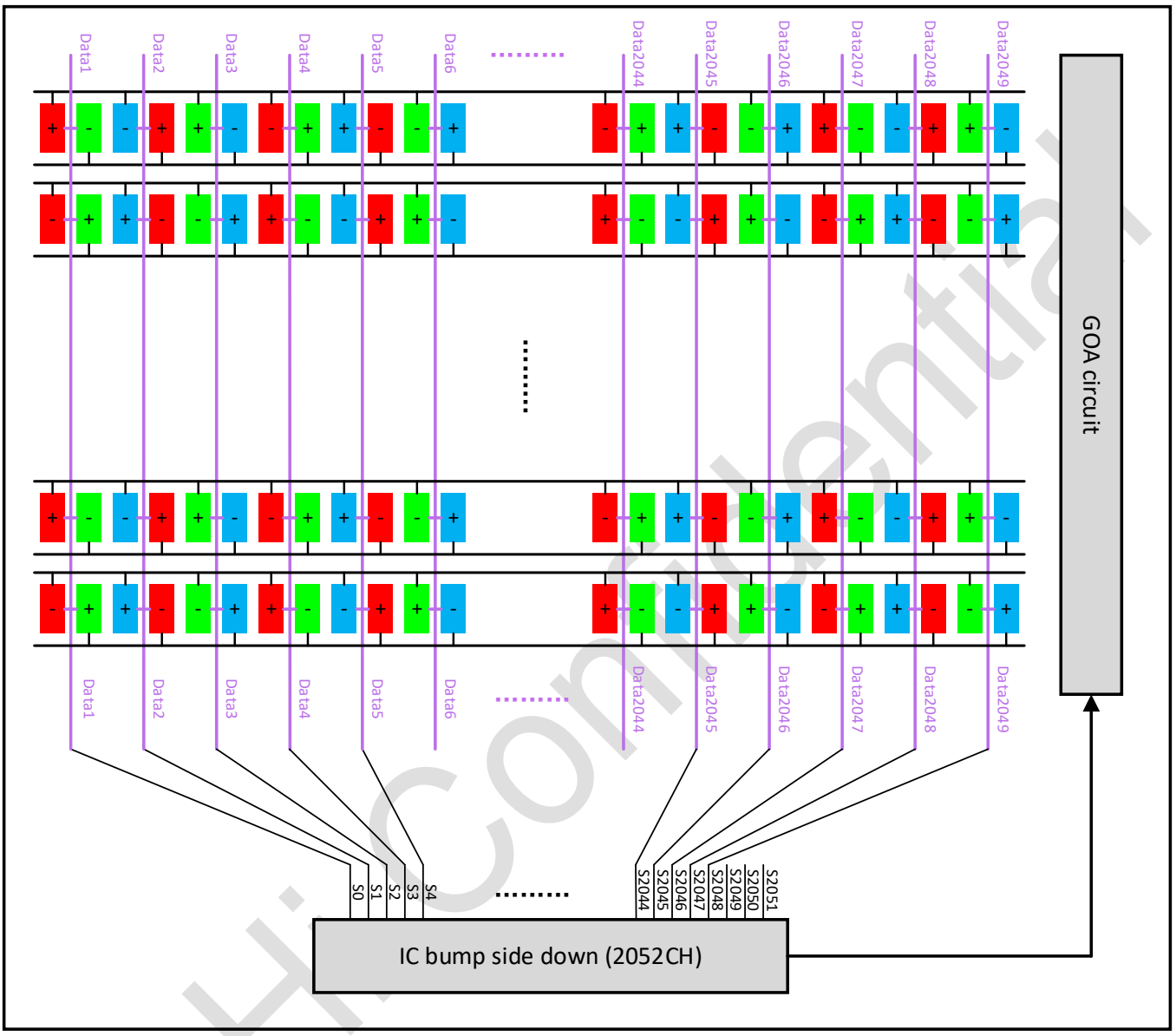
A2: Left(13700, 350)



12 Application Diagram with Panel

12.1 GIP Application_1366RGBx768 (Normal Dual Gate Driving)

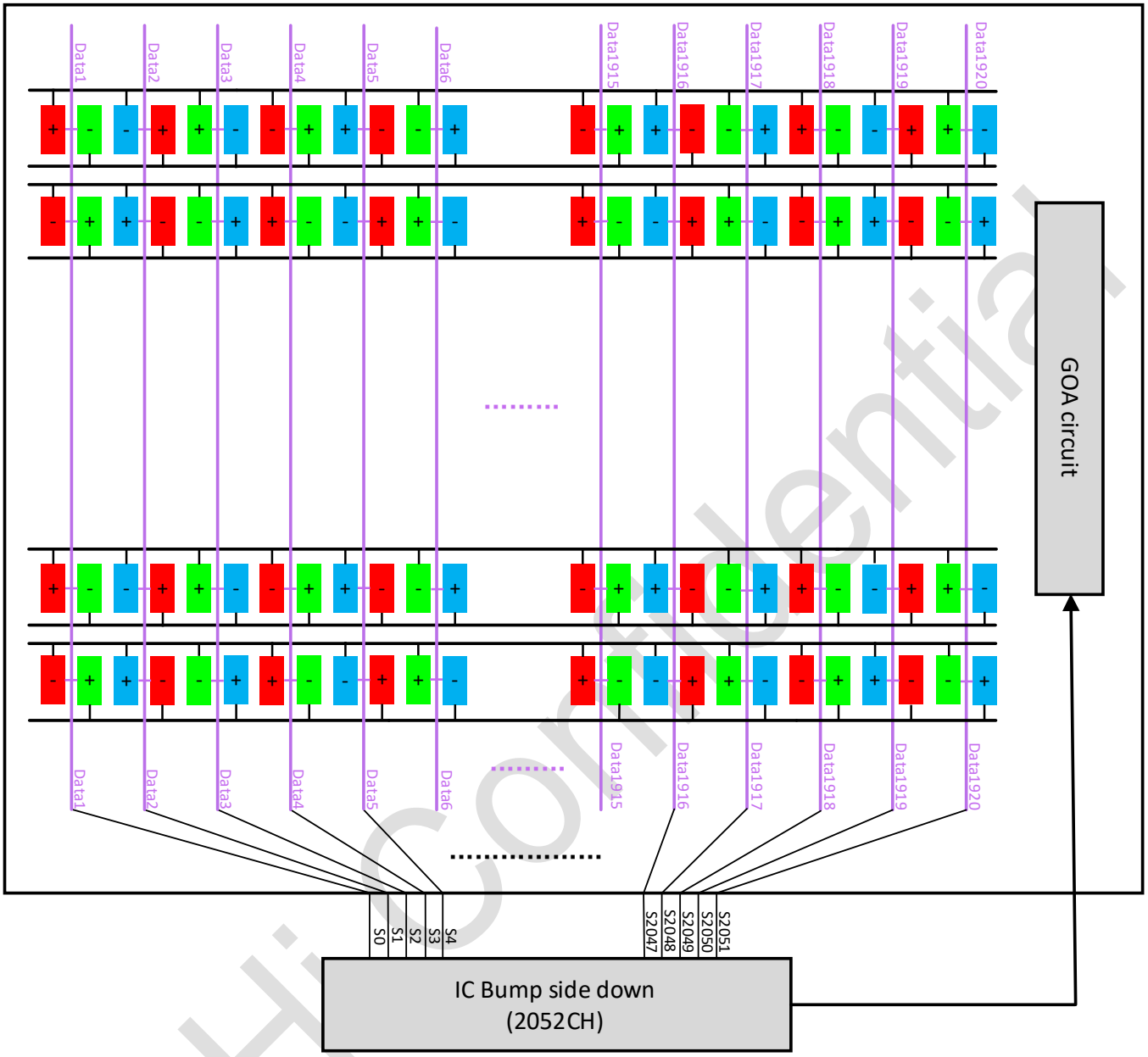
Driving method : Cas=0



Resolution	Source channel	Disable channel
1366RGBx768	S[2051:0]	-

12.2 GIP Application_1024RGBx768 (Normal Dual Gate Driving)

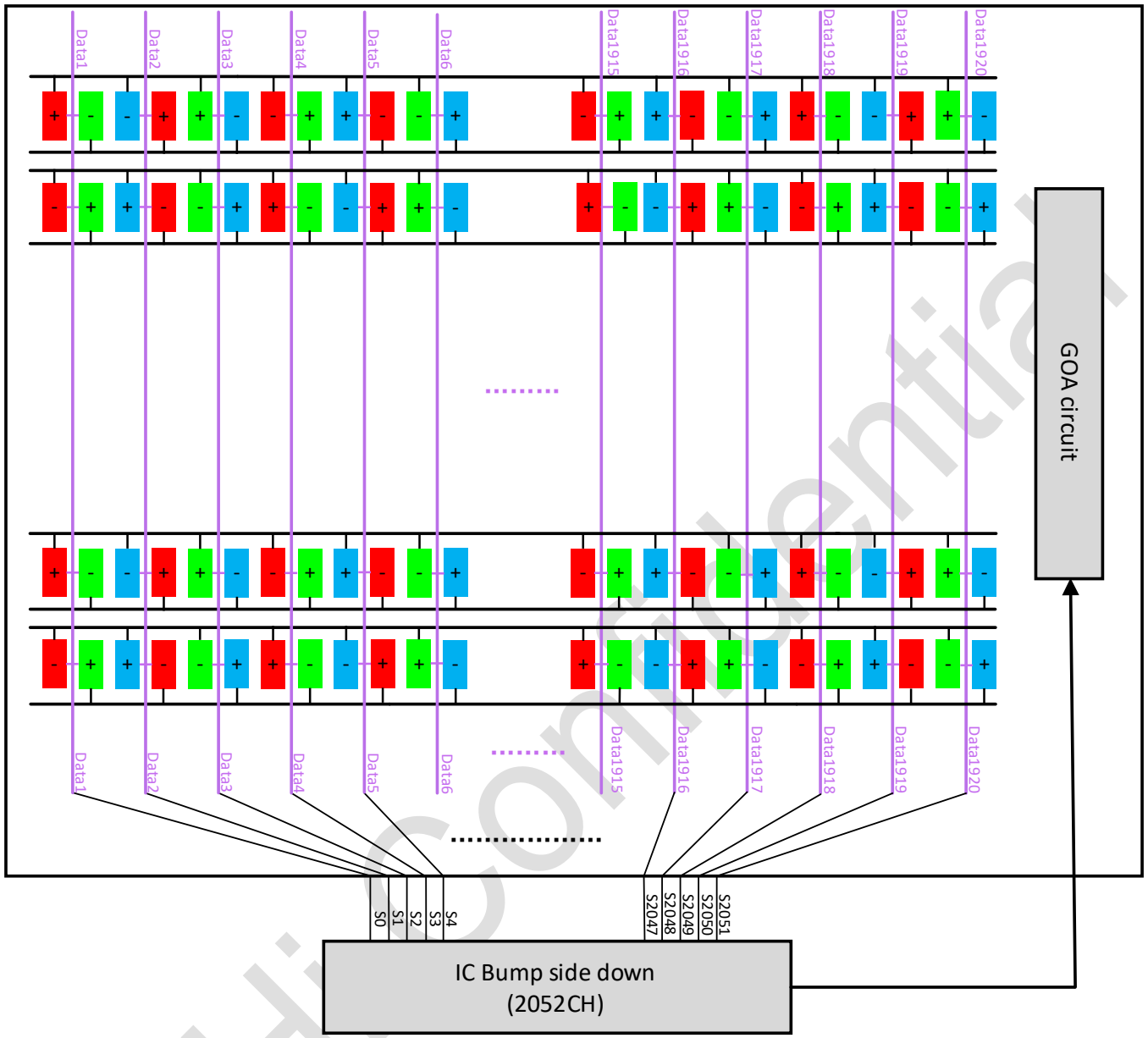
Driving method : Cas=0



Resolution	Source channel	Disable channel
1024RGBx768	S[767:0] and S[2051:1284]	S[1283:768]

12.3 GIP Application_1280RGBx800 (Normal Dual Gate Driving)

Driving method : Cas=0



Resolution	Source channel	Disable channel
1280RGBx800	S[959:0] and S[2051:1092]	S[1091:960]

12.4 Cascade Application1_1366RGBx768 (on LVDS mode)

Driving method : Cas=1 / Zigzag=0

TBD

12.5 Cascade Application2_1366RGBx768 (on LVDS mode)

Driving method : Cas=1 / Zigzag=1 / ZTYPE=0

TBD

12.6 Cascade Application3_1366RGBx768 (on LVDS mode)

Driving method : Cas=1 / Zigzag=1 / ZTYPE=1

TBD

12.7 Cascade Application4_1366RGBx768 (on LVDS mode)

Driving method : Cas=1 / Zigzag=0

TBD

12.8 Cascade Application5_1280RGBx800 (on LVDS mode)

Driving method : Cas=1 / Zigzag=1 / ZTYPE=0

TBD

12.9 Cascade Application6_1280RGBx800 (on LVDS mode)

Driving method : Cas=1 / Zigzag=1 / ZTYPE=1

TBD

12.10 Dual gate & GOA Application note

TBD

12.11 Normal Dual gate & GOA Application note

TBD

13 Ordering Information

TBD