

Product Specification

Model Name	S035HQ55HS-DC37
Description	TFT LCD Module 3.5" QVGA 320(RGB)x240 Dots
Date	2021/7/15
Version	2.0

Approved by/Date	Check by/Date	Prepared by/Date
ZHP 2021/07/15	HZX 2021/07/15	ZWF 2021/07/15

Customer Approval	
Date	



深圳市思迪科科技有限公司

SHENZHEN CDTECH ELECTRONICS

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2021/01/2	First Release.	ZWF
2.0	2021/07/15	Update the PIN interface definition	ZWF

1. General Specifications

Feature		Spec
Characteristics	Size	3.5 inch
	Resolution	320(horizontal)*240(Vertical)
	Interface	24bit-RGB
	Connect type	Connector
	Color Depth	16.7M
	Technology type	a-Si
	Pixel pitch (mm)	0.219*0.219
	Pixel Configuration	R.G.B.Stripe
	Display Mode	Normally Black
	CTP Driver IC	GT911
	Driver IC	ST7272A
	Viewing Direction	Full view
Mechanical	LCM (W x H x D) (mm)	76.90*63.90*4.89
	Active Area(mm)	70.08*52.56
	Weight (g)	TBD
	LED Numbers	6 LEDs

Note 1: Requirements on Environmental Protection: RoHs

Note 2: LCM weight tolerance: +/- 5%

2. Input/Output Terminals

No.	Symbol	Description
1-2	VBL-	Backlight LED Cathode
3-4	VBL+	Backlight LED Anode.
5	Y1(NC)	Touch panel up side (NC)
6	X1(NC)	Touch panel right side (NC)
7	NC	-
8	RESET	Reset Signal pin ("Low" is enable)
9	SPENB(NC)	Chip select(NC)
10	SPCK(NC)	Serial Clock.(NC)
11	SPDA(NC)	Serial Data(NC)
12-19	B0~B7	Data bus
20-27	G0~G7	Data bus
28-35	R0~R7	Data bus
36	HSYNC	Line Synchronous Signal
37	VSYN	Frame Synchronous Signal
38	DOTCLK	Dot-clock signal and oscillator source
39-40	NC	-
41-42	VDD	Power supply for logic operation
43	Y2(NC)	Touch panel bottom side (NC)
44	X2(NC)	Touch panel left side (NC)
45-47	NC	-
48	IF2 (NC)	Control the input data format (NC)
49	IF1 (NC)	Control the input data format (NC)
50	IF0 (NC)	Control the input data format (NC)
51	NC	-
52	DEN	Display enable signal
53-54	GND	System Ground

CTP PIN-MAP

Pin	Signal	Description
1	GND	Ground
2	VDD	Power supply
3	INT	Interrupt request to the host
4	SDA	I2C data input and output
5	SCL	I2C clock input
6	REST	Reset Pin for CTP

3. Absolute Maximum Rating

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	V _{DD}	-0.5	-	5.0	V	-
Operating Temperature	T _{OPR}	-20	-	70	°C	-
Storage Temperature	T _{STG}	-30	-	80	°C	

4. Timing characteristics

5.1 ELECTRICAL CHARACTERISTICS

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		V_{CC}	3.0	3.3	3.6	V	
		IOVCC	1.65	3.0	3.3		
Input Signal Voltage	Low Level	V_{IL}	GND	-	$0.1 \times V_{DD}$	V	
	High Level	V_{IH}	$0.8 \times V_{DD}$	-	VDD	V	
Output Signal Voltage	Low Level	V_{OL}	0	-	$0.2 \times V_{DD}$	V	
	High Level	V_{OH}	$0.8 \times V_{DD}$	-	VDD	V	

5.2 LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	-	mA	
Forward Voltage	V_F	16.2	19.2	20.4	V	
Backlight Power consumption	W_{BL}	-	0.384	-	W	
LED Lifetime		-	50000	-	Hrs	

Note 1: Each LED: $I_F = 20 \text{ mA}$, $V_F = 2.8 \sim 3.4 \text{ V}$.

Note 2: Optical performance should be evaluated at $T_a = 25^\circ \text{C}$ only.

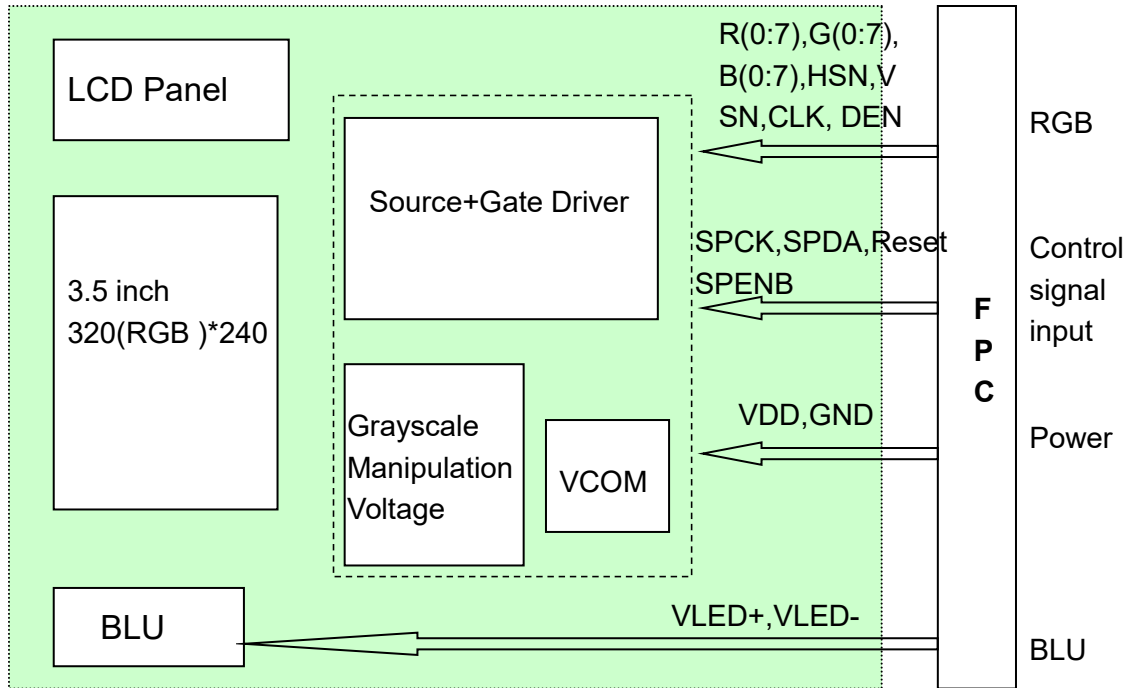
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.



CURRENT $I_F = 20 \text{ mA}$

Figure: LED connection of backlight(Constant Current)

5.3 Block Diagram



6 Interface Timing

6.1 AC Electrical Characteristics

Test Condition: (VDD=VDDP=3.3V, VDDA=5.0V, GND=GND A=GNDP=0V, TA= 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
System Operation Timing						
VDD power source slew time	T _{POr}			1000	us	From 0V to 90% VDD
RSTB active pulse width	T _{RSTB}	40			us	VDD = 3.3V
Input Output Timing						
CLKIN clock time	T _{clk}	33.3/125	-	-	ns	Please refer to timing table(p.32)
HSD to CLKIN	T _{hc}	-	-	1	CLKIN	
HSD width	T _{hwh}	1	-	-	CLKIN	
VSD width	T _{vwh}	1	-	-	Th	
HSD period time	T _h	60	63.56	67	us	
VSD setup time	T _{vst}	8	-	-	ns	
VSD hold time	T _{vhd}	10	-	-	ns	
HSD setup time	T _{hst}	8	-	-	ns	
HSD hold time	T _{hhd}	10	-	-	ns	
Data set-up time	T _{dsu}	8	-	-	ns	DIN[23:0] to CLKIN
Data hold time	T _{dhd}	10	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	T _{esd}	12	-	-	ns	DEN to CLKIN
Time that VSD to 1 st line data input	T _{vs}	2	13	127	Th	@CCIR601 / 8bit RGB HV mode Control by HDLY[6:0] setting T _{vs} = HDLY[6:0]
Time that CCIR_V to 1 st line data input	T _{vs}	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting T _{vs} = HDLY[6:0]
Time that CCIR_V to 1 st line data input	T _{vs} 17 25 33 Th					@CCIR656 PAL mode Control by HDLY[6:0] setting T _{vs} = HDLY[6:0]
Time that VSD to 1 st line data input	T _{vs}	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting T _{vs} = HDLY[6:0]
Source output stable time 1	T _{st}	-	25	30	us	96% final, CL=30pF, RL=2K
Gate output stable time	T _{gst}	-	500	1000	ns	96% final, CL=40pF
VCOMOUT output stable time	T _{cst}	-	4	8	us	96% final, CL=33nF, RL=100ohm
3-wire serial communication AC timing						
Serial clock	T _{spck}	320	-	-	ns	
SPCK pulse duty		40	50	60	%	T _{ckh} / T _{spck}
Serial data setup time	T _{isu}	120	-	-	ns	
Serial data hold time	T _{ihd}	120	-	-	ns	
Serial clock high/low	T _{ckh/l}	120	-	-	ns	
Chip select distinguish	T _{cd}	1	-	-	us	
SPENB to VSD	T _{cv}	1	-	-	us	
SPENB input setup time	T _{eck}	150	-	-	ns	
SPENB input hold time	T _{cke}	150	-	-	ns	

6.2 DC Electrical Characteristics

Recommended Operating Range

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	3.0	3.3	3.6	V	
IO Supply Voltage	VDDI	3.0	-	3.6	V	
Charge Pump Supply Voltage	PVDD	3.0	3.3	3.6	V	

DC Characteristics for Digital Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	

DC Characteristics for Analog Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-Voltage Power	VGH	13	15	16.5	V	No Load@ FR=60Hz
Negative High-Voltage Power	VGL	-7	-10	-11	V	
Output Voltage Deviation	Vod	-	±35	±45	mV	
Standby Current	Isc	-		50	uA	
Operation Current	Ioc	-	20		mA	

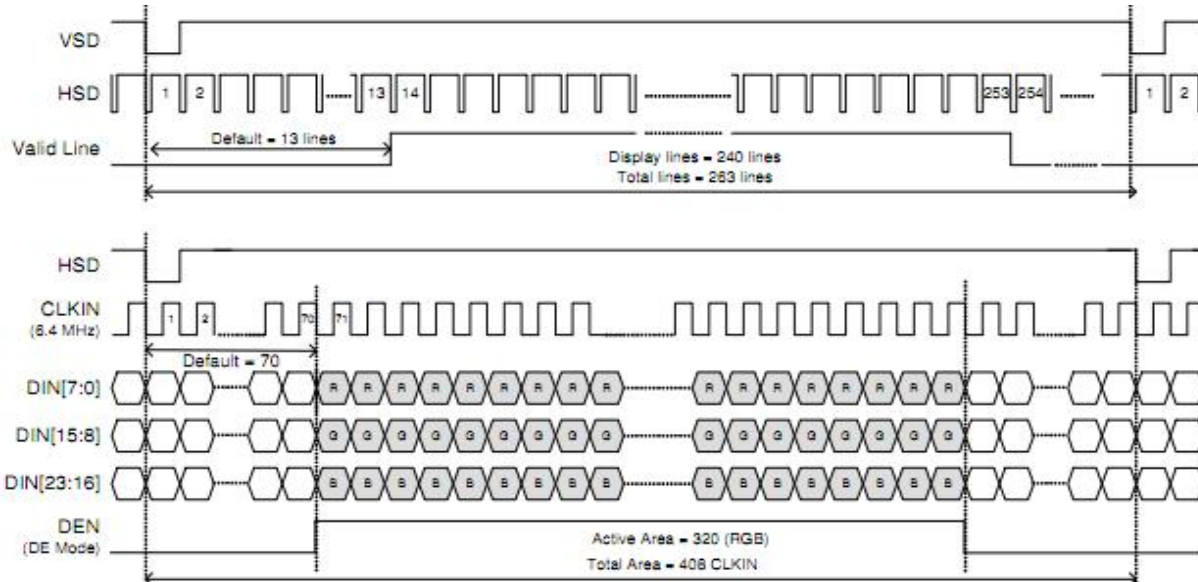
6.3 24 Bit RGB Mode

Parallel 24-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

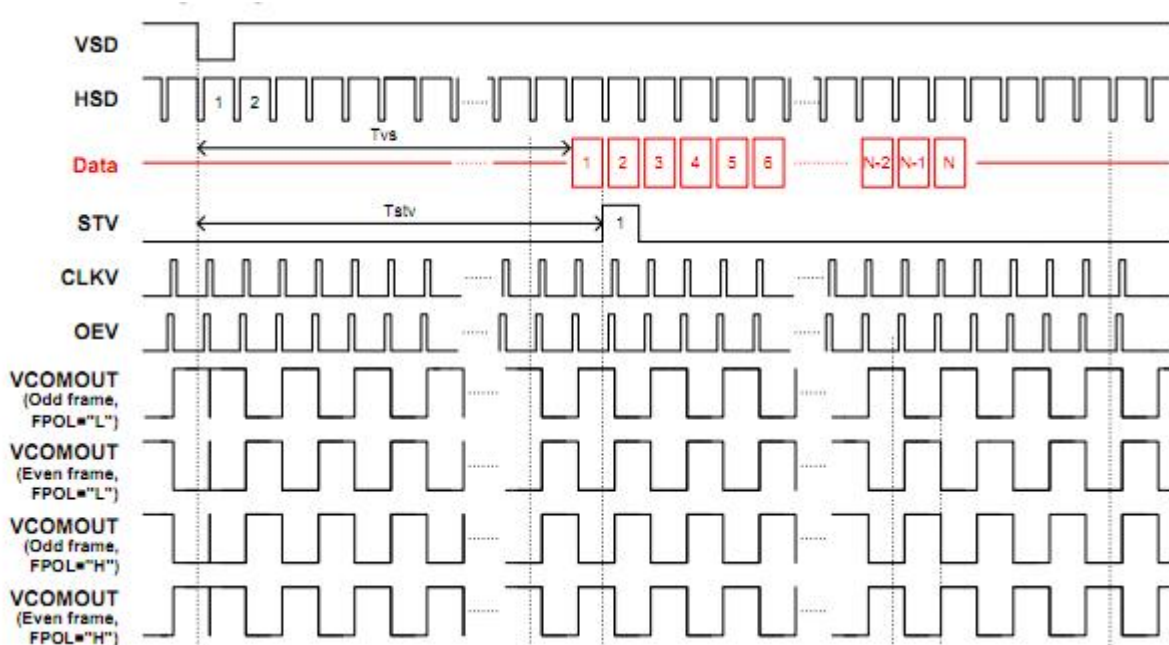
Parallel 24-bit RGB Input Timing Table						
Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK Frequency	Fclk	5	6	8	MHz	
DCLK Period	Tclk	125	167	200	ns	
HSYNC	Period Time	Th	325	371	438	DCLK
	Display Period	Thdisp		320		DCLK
	Back Porch	Thbp	3	43	43	DCLK SYNC mode back porch control by H_BLANKING[7:0] setting Thbp= H_BLANKING[7:0]
	Front Porch	Thfp	2	8	75	DCLK
	Pulse Width	Thw	2	4	43	DCLK
VSYNC	Period Time	Tv	244	260	289	HSYNC
	Display Period	Tvdisp		240		HSYNC
	Back Porch	Tvbp	2	12	12	HSYNC SYNC mode back porch control by V_BLANKING[7:0] setting Tvbp= V_BLANKING[7:0]
	Front Porch	Tvfp	2	8	37	HSYNC
	Pulse Width	Tvw	2	4	12	HSYNC

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

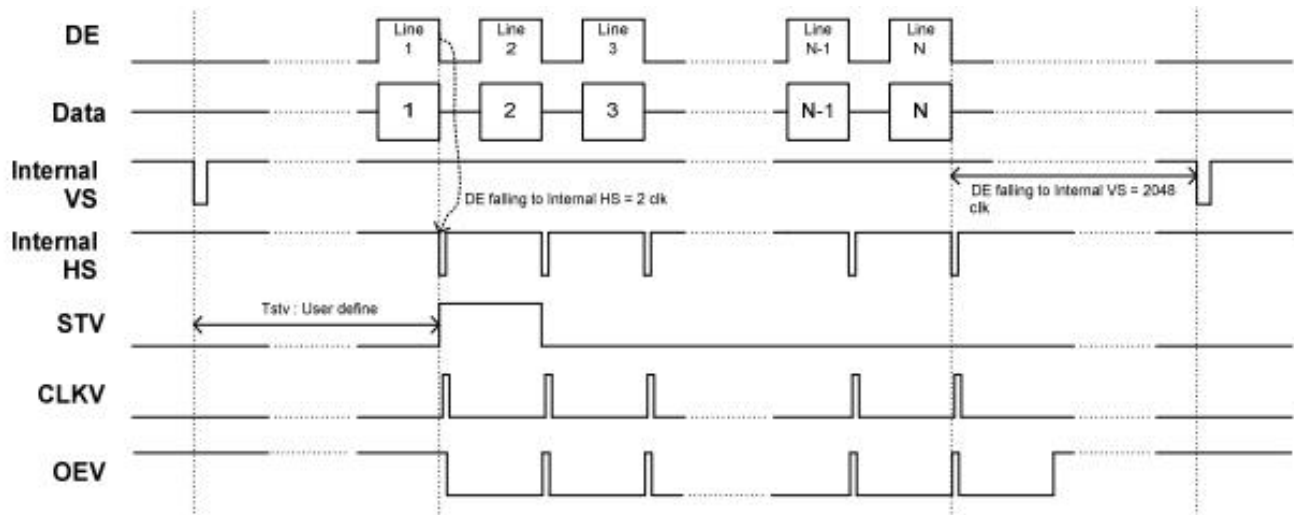
6.4 Input Data Timing



6.5 Vertical Timing Diagram (HV Mode)



6.6 Vertical Timing Diagram (DE Mode)



7 . Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	-	-	50	80	ms	FIG.1	Note4
Contrast Ratio		CR		-	600	-	-	FIG.2	Note1
Surface luminance		LV	$\theta=0^\circ$	350	400	-	cd/m2	FIG.2	Note2
Luminance uniformity		Yu	$\theta=0^\circ$	75	80	-	%	FIG.2	Note3
NTSC		-	$\theta=0^\circ$	-	50	-	%	FIG.2	Note5
Viewing angle		θ Cr>10	$\varnothing=90^\circ$	-	80	-	deg	FIG.3	Note6
			$\varnothing=270^\circ$	-	80	-	deg	FIG.3	
			$\varnothing=0^\circ$	-	80	-	deg	FIG.3	
			$\varnothing=180^\circ$	-	80	-	deg	FIG.3	
Chromaticity	Red	R _x	$\theta=0^\circ$ $\varnothing=0^\circ$ Ta=25°	TBD	TBD	TBD	-	FIG.2 CIE1931	Note5
		R _y		TBD	TBD	TBD	-		
	Green	G _x		TBD	TBD	TBD	-		
		G _y		TBD	TBD	TBD	-		
	Blue	B _x		TBD	TBD	TBD	-		
		B _y		TBD	TBD	TBD	-		
	White	W _x		0.307	0.337	0.367	-		
		W _y		0.324	0.354	0.384	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON's BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3,,Pn)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_r) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_f) is the time between photo detector output intensity changed from 10% to 90%. For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity, The x,y value is determined by screen active area center position P5. For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers’s ConoScope or DMS series Instruments or compatible.

FIG.1. The definition of response Time

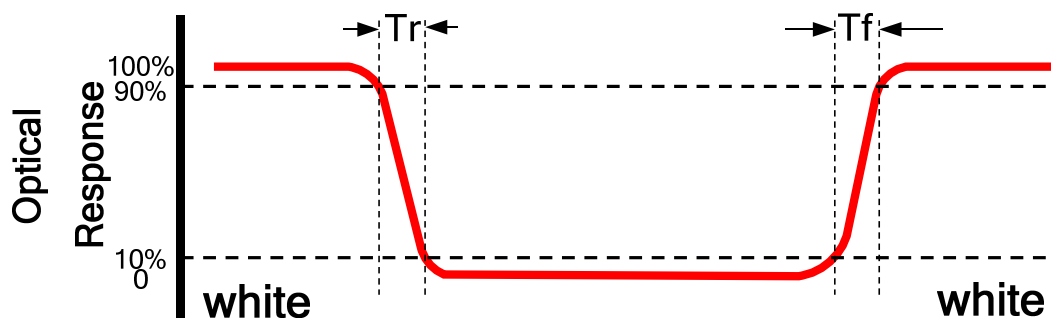


FIG.2. Measuring method for contrast ratio, surface luminance,

luminance uniformity, CIE (x,y) chromaticity

Size : S≤5”(see Figure a) A : 5 mm B : 5 mm

H,V : Active area

Light spot size $\varnothing=5\text{mm}$ (BM-5) or $\varnothing=7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure a.

measurement instrument : TOPCON’s luminance meter BM-5 or BM-7 or compatible (see Figure c).

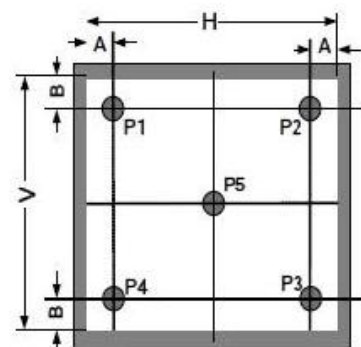


Figure a

Size : $5'' < S \leq 12.3''$ (see Figure b) H,V : Active area

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7) 50cm distance or compatible distance from the LCD surface to detector lens.

test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

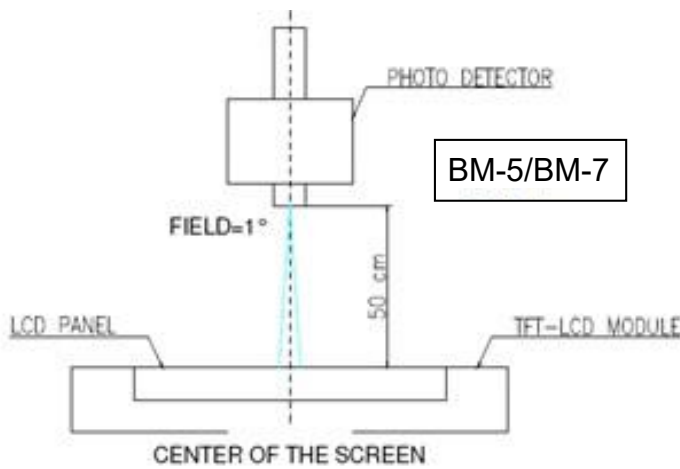
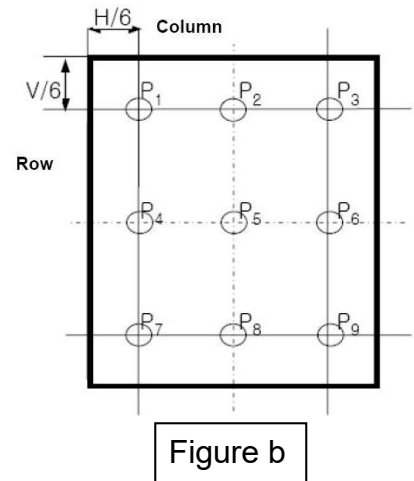
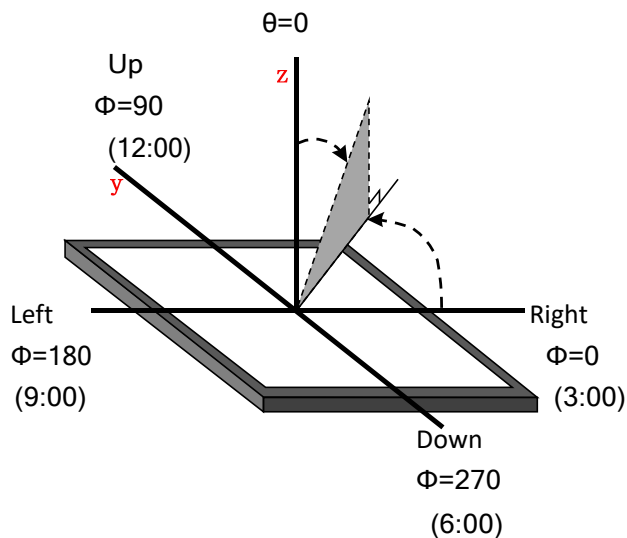


FIG.3.The definition of viewing angle



8 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	IEC60068-2-1:2007 GB2423. 2-2008
2	Low Temperature Operation	Ta= -20℃, 96hrs	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta= +80℃, 96hrs	IEC60068-2-1:2007 GB2423. 2-2008
4	Low Temperature Storage	Ta= -30℃, 96hrs	IEC60068-2-1:2007 GB2423.1-2008
5	High Temperature & Humidity Operation	Ta= +60℃, 90% RH max, 96 hours	IEC60068-2-78:2001 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 20 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14:1984, GB2423.22-2002
7	ESD	C=150pF, R=330 Ω, 5 points/panel , Air:±8KV, 5 times Contact: ±4KV, 5 times (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2:2001 GB/T17626.2-2006
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.5mm , Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (6 hours for total)	IEC60068-2-6:1982 GB/T2423.10-1995
9	Mechanical Shock (Non-operation)	Half Sine Wave 60G ,6ms,±X,±Y,±Z 3times for each direction	IEC60068-2-27:1987 GB/T2423.5—1995
10	Package Drop Test	Height: 60 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32:1990 GB/T2423.8-1995



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Notes:

1. The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

- 1).Air bubble in the LCD;
- 2).Seal leak
- 3).Non-display
- 4).missing segments
- 5).Glass crack
- 6).CR reduction >40%
- 7).IDD increase >100%
- 8).Brightness reduction >50%

9).Color coordinate tolerance >0.05

2.≤7.0 inch: The size of sample is 5pcs;

>7.0 inch: The size of sample is 2pcs;

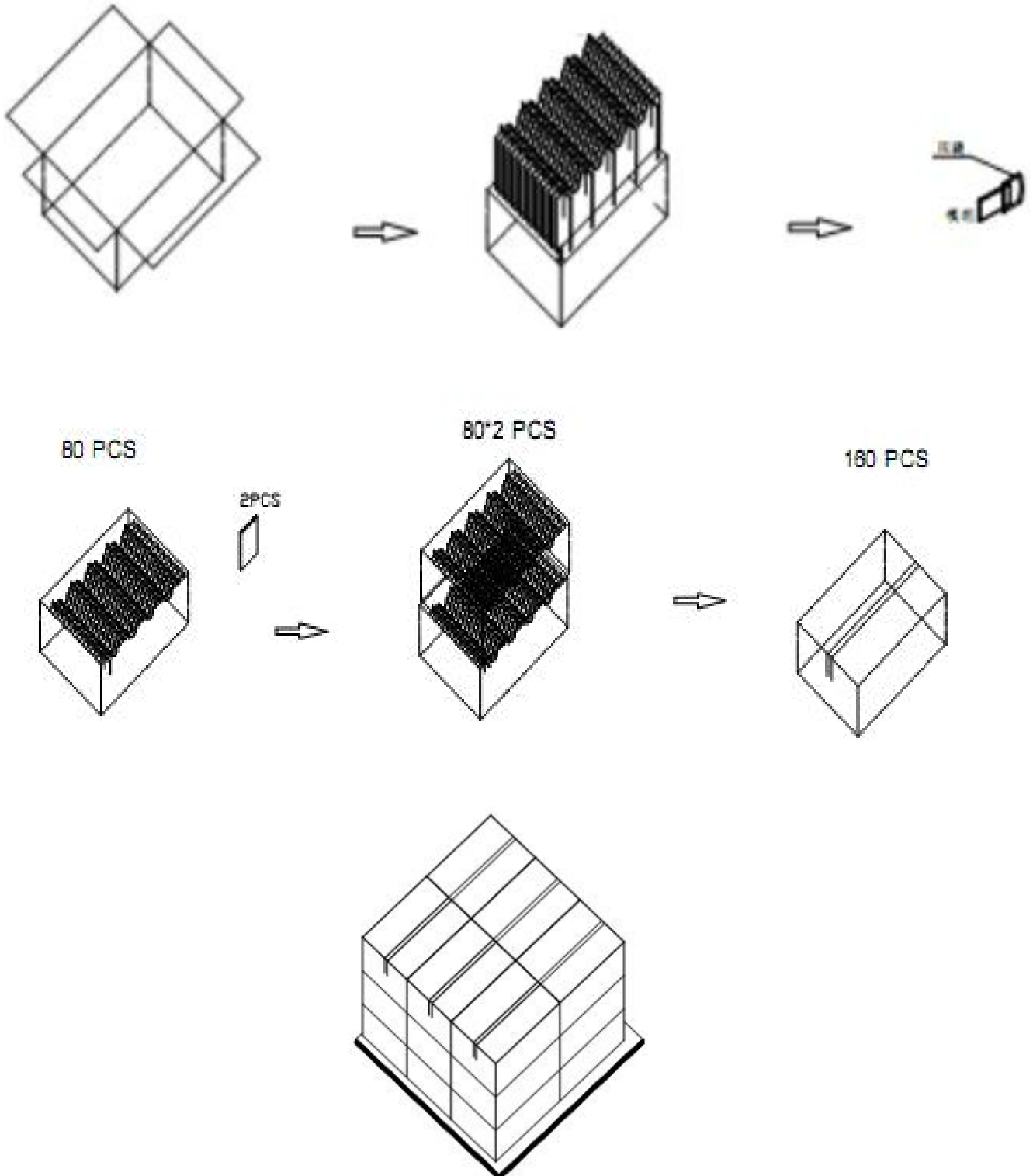
3. One test sample must complete each test item;

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.

5.In the test of High Temperature Operation and High Temperature & Humidity Operation ,the operation temperature is the surface temperature of module.

10 Packing

Packing Method



11. Precautions for Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

11.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ~ 40℃ Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.



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11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.