FL5893AC Data Sheet

8-bit 1922 channel source driver with TCON

Version 0.3
May 2024

AEC-Q100 Compliant for Automotive Applications

Hazardous Substance Free
RoHS/ REACH Compliant

Forcelead Technology Corporation

Index

1. INTRODUCTION

This chip is a source driver integrating with timing controller which contains 1922 channels of source output and several gate controller signals. In addition, those gate controller signals of this chip are able to support not only the traditional gate drivers, but also the gate-in-panel (GIP) circuit which made by amorphous Si (a-Si) process or low temperature poly-Si (LTPS) process. This chip can provide the required voltages of LCD panels with its built-in power supply circuits or external power sources. And all the functions inside it are able to be controlled by MCU with I2C and SPI. This chip can display the video signals transferred by RGB CMOS interface or LVDS interface. Furthermore, it is also embedded several fail-safe mechanisms for automotive applications. So that, this chip is possible to make a display system not only competitive but also reliable and safe.

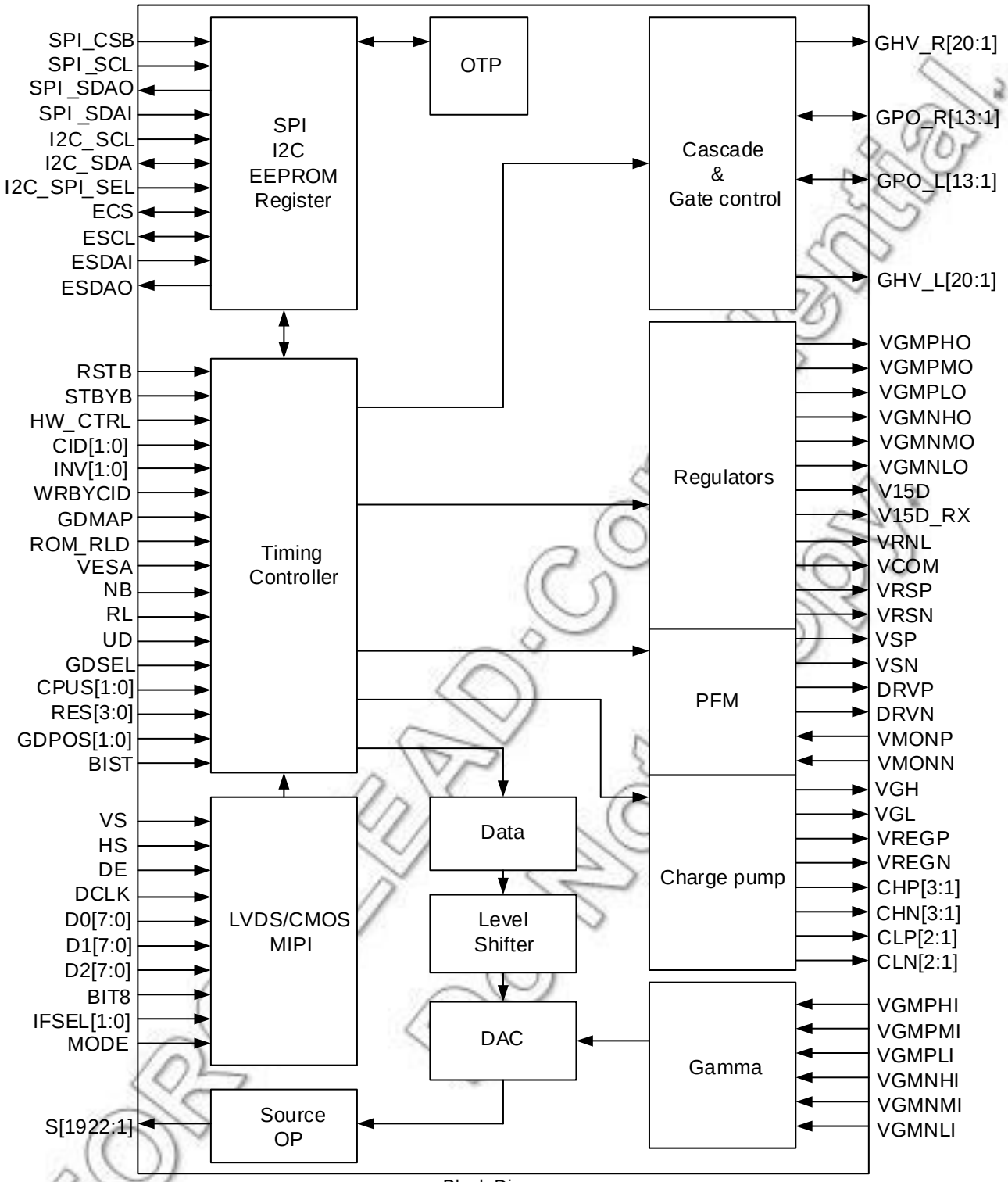
2. FEATURES

- **Support Amorphous Si (a-Si) and LTPS Type Panel Structure**
- **Support GIP Driving and External Gate Driver**
- **Maximum 4-Chip Cascade Application**
- **LCD Driver Output**
  - Source driver: 1922 channels (support multiplexer 1:3 and 2:6)
  - GIP control: 20 pins GIP control output on each side
  - Gate control: 15 side pads external gate driver output on each side
- **Programmable Panel Resolution**
- **Gray Scale**
  - RGB: 8-8-8, 6-6-6
  - LVDS: 8bit and 6bit
- **Interface**
  - Command and control: 4-wire SPI, I2C
  - Display data:
    - 18-/ 24-bit RGB CMOS
    - 1-port and 2-port LVDS (VESA & JEIDA data format)
    - MIPI DSI version 1.02
    - MIPI D-PHY version 1.00
    - MIPI 1/2/4 lane interface
- **DC-VCOM Driving Methods**
  - Dot inversion
  - Column inversion for zig-zag type panels
- **RGB Separate Gamma Setting for the Color Tracking**
- **Temperature Compensation Functions**
  - Gamma reference voltage
  - VCOM
- **Built-In Self Test (BIST) Function**
- **LVDS CRC Function**
- **Abnormal Feedback**
  - Connectivity
  - Voltage power
  - Temperature
- **Operation Voltage**
  - Input voltage:
    - Analog power supply: 3.0 ~ 3.6V
    - LVDS power supply: 3.0 ~ 3.6V
    - IO power supply: 3.0 ~ 3.6V
  - Output voltage:

- Max. gate voltage: VGH – VGL = 32V
- Max. source swing voltage: VGMNHO ~ VGMPHO = -6.2V ~ 6.2V
- VCOM voltage: -2.0V ~ 0.55V

- **Internal OTP for 5 times programming**
- **3 times OTP for VCOM setting, ID setting**
- **Low Voltage Detect (LVD)**
- **Operating Temperature Range: Ta= −40°C ~ 105°C**
- **Package Type: COG**

3. BLOCK DIAGRAM



Block Diagram

4. PIN DESCRIPTION

4.1 External Power Pins

Pin Name	Type	Description
VDDI	Power	Power supply for IO system
VDDRX	Power	Power supply for LVDS circuit
VDDP	Power	Power supply for analog circuit
VDD_PFM	Power	Power supply for PFM and charge pump circuits
VSP	Power	Power supply for source driver and power circuit
VSN	Power	Power supply for source driver and power circuit
VDD_OTP	Power	Power supply for OTP circuit
VSSI	Power	System ground for IO and digital circuit
VSSRX	Power	System ground for LVDS circuit
VSSP	Power	System ground for Internal reference circuit
VSSA	Power	System ground for analog and charge pump circuits
VSS_PFM	Power	System ground for PFM circuit

4.2 Display Interface Pins

Pin Name	Type	Description
D0[7:0], D1[7:0], D2[7:0]	I	Input pin for TTL/LVDS/MIPI display data
HS	I	Input pin for horizontal synchronization signal
VS	I	Input pin for vertical synchronization signal
DE	I	Input pin for data enable
DCLK	I	Input pin for pixel clock

4.3 Control Pins

Pin Name	Type	Description
SPI_CSB	I	Chip select signal for SPI interface **(Normally pulled high).** If I2C_SPI_SEL=H, please let these pins open.
SPI_SDAI	I	Serial data input for SPI interface **(Normally pulled low).** If I2C_SPI_SEL=H, please let these pins open.
SPI_SDAO	O	Serial data output for SPI interface
SPI_SCL	I	Clock signal for SPI interface **(Normally pulled low).** If I2C_SPI_SEL=H, please let these pins open.
I2C_SDA	I/O	Serial address and data input/output for I2C interface **(Normally pulled low for input mode).** If I2C_SPI_SEL=L, please let these pins open.
I2C_SCL	I	Clock signal for I2C interface **(Normally pulled high).** If I2C_SPI_SEL=L, please let these pins open.
I2C_SPI_SEL	I	Serial interface selection: 'H': I2C interface **'L': SPI interface (Default)**
HW_CTRL	I	Function pin control by hardware or software selection: **Output HW_CTRL function is HW_CTRL pin "XOR" register HW_CTRL_XOR bit** **(Please reference page0 R0h output HW_CTRL table description)** **'H': Hardware pin (H/W > S/W) (Default)** 'L': Software register (S/W > H/W)
IFSEL[1:0]	I	Interface select: IFSEL[1] / IFSEL[0] / Interface L / L / Parallel CMOS L / H / MIPI H / L / 1-Port LVDS **H / H / 2-Port LVDS (Default)**
BIT8	I	Data format: **'H': 8bit (Default)** 'L': 6bit

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>MODE</td><td>I</td><td>DE or SYNC mode select:
‘H’: SYNC mode
‘L’: DE mode (Default)</td></tr>
<tr><td>BIST</td><td>I</td><td>Built-in self test function:
‘H’: Enable
‘L’: Disable (Default)</td></tr>
<tr><td>INV[1:0]</td><td>I</td><td>Inversion type select:
For single gate structure, inversion type is as follows.
<table>
<tr><th>INV[1]</th><th>INV[0]</th><th>Function</th></tr>
<tr><td>L</td><td>L</td><td>1+2 dot inversion</td></tr>
<tr><td>L</td><td>H</td><td>Column inversion</td></tr>
<tr><td>H</td><td>L</td><td>4 dot inversion</td></tr>
<tr><td>H</td><td>H</td><td>Dot inversion (Default)</td></tr>
</table>
Note: Only valid in signal gate structure

For dual gate + Zig-zag structure, only Dot inversion is valid. Please refer to the section of 5.3.2.

For triple gate structure, inversion type is as follows.
<table>
<tr><th>INV[1]</th><th>INV[0]</th><th>Function</th></tr>
<tr><td>L</td><td>L</td><td>1+2 dot inversion</td></tr>
<tr><td>L</td><td>H</td><td>Column inversion</td></tr>
<tr><td>H</td><td>L</td><td>4 dot inversion</td></tr>
<tr><td>H</td><td>H</td><td>Dot inversion (Default)</td></tr>
</table>
Note: Only valid in triple gate structure</td></tr>
<tr><td>UD</td><td>I</td><td>Gate output shift vertical direction select:
‘H’: Scan Up to Down (Default)
‘L’: Scan Down to Up</td></tr>
<tr><td>RL</td><td>I</td><td>Source output shift horizontal direction select:
‘H’: S[1]->S[2]->…->S[1920] (Default)
‘L’: S[1920]->S[1919]->…->S[1]</td></tr>
<tr><td>NB</td><td>I</td><td>Panel type selection:
‘H’: Normally black (Default)
‘L’: Normally white</td></tr>
<tr><td>STBYB</td><td>I</td><td>Standby mode:
‘H’: Normal operation (Default)
‘L’: TCON, SD, power circuit and temp sensor will be turned off</td></tr>
<tr><td>RSTB</td><td>I</td><td>Reset Pin. Low active.
Initialization is executed when this pin is set to Low.</td></tr>
<tr><td>WRBYCID</td><td>I</td><td>I2C or SPI command setting for cascade structure:
‘H’: Chip WR defined by CID (Default)
‘L’: Write to all chip, read from master only</td></tr>
<tr><td>CID[1:0]</td><td>I</td><td>Chip ID setting in cascade structure:
<table>
<tr><th>CID[1]</th><th>CID[0]</th><th>Function</th></tr>
<tr><td>L</td><td>L</td><td>Master (Default)</td></tr>
<tr><td>L</td><td>H</td><td>Slave1</td></tr>
<tr><td>H</td><td>L</td><td>Slave2</td></tr>
<tr><td>H</td><td>H</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>RES[3:0]</td><td>I</td><td>Default resolution is 1920x720 (RES[3:0]=0010)
For more settings, see “Resolution and interface selection table”
Note: For arbitrary resolution, charging time and frequency should also be considered.</td></tr>
<tr><td>VESA</td><td>I</td><td>LVDS data format selection
‘H’: VESA (Default)
‘L’: JEIDA</td></tr>
<tr><td>ROM_RLD</td><td>I</td><td>OTP reload per 30 frames:
‘H’: Enable auto-reload OTP
‘L’: Disable auto-reload OTP (Default)</td></tr>
<tr><td>EXT_PWR</td><td>I</td><td>External / Internal VSP/VSN power select:
‘H’: External VSP/VSN power supply
‘L’: Internal VSP/VSN power supply (Default)</td></tr>
<tr><td>EXT_PWR2</td><td>I</td><td>External / Internal VGH/VGL power select:
‘H’: External VGH/VGL power supply
‘L’: Internal VGH/VGL power supply (Default)</td></tr>
<tr><td>GDSEL</td><td>I</td><td>GIP / GD mode select:
‘H’: Gate driver mode
‘L’: GIP mode (Default)</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>GDPOS[1:0]</td><td>I</td><td>Gate driver location setting:
<table>
<tr><th>GDPOS[1]</th><th>GDPOS[0]</th><th>Function</th></tr>
<tr><td>L</td><td>L</td><td>Left side (Default)</td></tr>
<tr><td>L</td><td>H</td><td>Right side</td></tr>
<tr><td>H</td><td>L</td><td>Interlace driving from dual side</td></tr>
<tr><td>H</td><td>H</td><td>Progressive driving the same line from dual side</td></tr>
</table></td></tr>
<tr><td>CPUS[1:0]</td><td>I</td><td>Panel module total IC quantity:
<table>
<tr><th>CPUS[1]</th><th>CPUS[0]</th><th>Function</th></tr>
<tr><td>L</td><td>L</td><td>3 (Default)</td></tr>
<tr><td>L</td><td>H</td><td>1</td></tr>
<tr><td>H</td><td>L</td><td>2</td></tr>
<tr><td>H</td><td>H</td><td>4</td></tr>
</table></td></tr>
<tr><td>ERR</td><td>O</td><td>Output pin for error detection: (Reference “Error Detection” for detail)
‘H’: No error detected (External pull-high, if need)
‘L’ : An error detected</td></tr>
<tr><td>TP_SYNC</td><td>O</td><td>Synchronization signal for touch panel</td></tr>
</table>

*Hardware default setting.

4.4 Driver Output Pins

Pin Name	Type	Description
S1~S1922	O	Source driver output pins
GHV_R[1]~GHV_R[20] GHV_L[1]~GHV_L[20]	O	GIP control output pins

4.5 PFM and Charge pump Power Pins

Pin Name	Type	Description
DRVP	O	PFM driving pin for generating VSP output. If PFM is not used, please open them.
DRVN	O	PFM driving pin for generating VSN output. If PFM is not used, please open them.
CHP1 CHP2 CHP3	I/O	Flying capacitor for generating VGH output Connecting pins on the positive side. If VGH charge pump is not used, please open them.
CHN1 CHN2 CHN3	I/O	Flying capacitor for generating VGH output Connecting pins on the negative side. If VGH charge pump is not used, please open them.
VGH	O	Power supply pin for gate driver. Connect to a capacitor for stabilization.
VREGP	O	Regulator voltage for VGH charge pump.**(Only for diode charge pump type connection)** Connecting pin for diode charge pump type. If diode charge pump type is not used, please open them.
CLP1 CLP2	I/O I/O	Flying capacitor for generating VGL output Connecting pins on the positive side. If VGL charge pump is not used, please open them.
CLN1 CLN2	I/O I/O	Flying capacitor for generating VGL output Connecting pins on the negative side. If VGL charge pump is not used, please open them.
VGL	O	Power supply pin for gate driver. Connect to a capacitor for stabilization.
VREGN	O	Regulator voltage for VGL charge pump. **(Only for diode charge pump type connection)** Connecting pin for diode charge pump type. If diode charge pump type is not used, please open them.
VMONP	I	Top terminal of feedback.
VMONN	I	Top terminal of feedback.

4.6 Internal Regulator Power Pins

Pin Name	Type	Description
V15D	O	Digital reference voltage output. Connect to a capacitor for stabilization.
V15D_RX	O	LVDS interface reference voltage output. Connect to a capacitor for stabilization.
VRNL	O	Power pin for analog circuits. Connect to a capacitor for stabilization
VRSP	O	Power pin for analog circuits. Connect to a capacitor for stabilization
VRSN	O	Power pin for analog circuits. Connect to a capacitor for stabilization

Pin Name	Type	Description
VGMPHO	O	Power output of grayscale voltage generator. Connect to a capacitor for stabilization.
VGMPMO	O	Power output of grayscale voltage generator. Connect to a capacitor for stabilization. VGMPMO= 0.5*(VGMPHO+VGMPLO)
VGMPLO	O	Power output of grayscale voltage generator. Connect to a capacitor for stabilization.
VGMNHO	O	Power output of grayscale voltage generator. Connect to a capacitor for stabilization.
VGMNMO	O	Power output of grayscale voltage generator. Connect to a capacitor for stabilization. VGMNMO= 0.5*(VGMNHO+VGMNLO)
VGMNLO	O	Power output of grayscale voltage generator. Connect to a capacitor for stabilization.
VGMPHI	I	Power pin for grayscale reference voltage. Connect to a capacitor for stabilization.
VGMPMI	I	Power pin for grayscale reference voltage. Connect to a capacitor for stabilization.
VGMPLI	I	Power pin for grayscale reference voltage. Connect to a capacitor for stabilization.
VGMNHI	I	Power pin for grayscale reference voltage. Connect to a capacitor for stabilization.
VGMNMI	I	Power pin for grayscale reference voltage. Connect to a capacitor for stabilization.
VGMNLI	I	Power pin for grayscale reference voltage. Connect to a capacitor for stabilization.
VCOM	O	Power supply for the TFT-LCD common electrode on panel side. Connect to a capacitor for stabilization.

4.7 Gate Driver Control Pins

Pin Name	Type	Description
GPO_L[13:1]	I/O	Gate driver and cascade control pins at left side
GPO_R[13:1]	I/O	Gate driver and cascade control pins at right side

4.8 Dummy and Test Pins

Pin Name	Type	Description
TEST_IN[0]	OPEN	Reserved for testing only. Leave these pins open
TEST_O[5:0]	OPEN	Reserved for testing only. Leave these pins open
TEST_I_MIPI	OPEN	Reserved for testing only. Leave these pins open
TEST_I[1:0]	OPEN	Reserved for testing only. Leave these pins open
TEST_V[2:0]	OPEN	Reserved for testing only. Leave these pins open
TEST_VR	OPEN	Reserved for testing only. Leave these pins open
TEST_VL	OPEN	Reserved for testing only. Leave these pins open
THROUGH_1	I/O	Two pad short internally for assembly test
THROUGH_2	I/O	Two pad short internally for assembly test
VCOM_R	I/O	Power supply for the TFT-LCD common electrode at panel side.
VCOM_L	I/O	Power supply for the TFT-LCD common electrode at panel side.
GDMAP	OPEN	Reserved for testing only. Leave this pin open
ECS	OPEN	Reserved for testing only. Leave this pin open
ESCL	OPEN	Reserved for testing only. Leave this pin open
ESDAI	OPEN	Reserved for testing only. Leave this pin open
ESDAO	OPEN	Reserved for testing only. Leave this pin open
ERR2	OPEN	Reserved for testing only. Leave this pin open
Dummy	OPEN	Reserved for testing only. Leave these pins open

4.9 Resolution and Interface Selection Table

RES[3:0]	Resolution	CMOS	LVDS		MIPI
			Single port	Dual port	
0000	1920 x 1200	X	X	O	O
0001	1920 x 1080	X	X	O	O
0010	1920 x 720	X	X	O	O
0011	1280 x 800	X	O	O	O
0100	1280 x 720	X	O	O	O
0101	1280 x 480	O	O	X	O
0110	1024 x 768	O	O	X	O
0111	1024 x 600	O	O	X	O
1000	1024 x 480	O	O	X	O
1001	960 x 540	O	O	X	O
1010	640 x 480	O	O	X	O
1011	600 x 1024	O	O	X	O
1100	540 x 960	O	O	X	O
1101	(Reserved)	(Reserved)			
1110	(Reserved)	(Reserved)			
1111	Programmable Resolution	O	O	O	O

○: Recommend
X: Do not recommend or not support

4.10 Output Channel Reference Table

RES[3]	RES[2]	RES[1]	RES[0]	Resolution	Dual	CID[1:0]					
						Master		Slave1		Slave2	
						Total channels	Disable channels	Total channels	Disable channels	Total channels	Disable channels
0	0	0	0	1920 x 1200	0	1920	0	1920	0	1920	0
0	0	0	1	1920 x 1080	0	1920	0	1920	0	1920	0
0	0	1	0	1920 x 720	0	1920	0	1920	0	1920	0
0	0	1	1	1280 x 800	0	1920	0	1920	0		
					1	1920	0				
0	1	0	0	1280 x 720	0	1920	0	1920	0		
					1	1920	0				
0	1	0	1	1280 x 480	0	1920	0	1920	0		
					1	1920	0				
0	1	1	0	1024 x 768	0	1536	769-1152	1536	769-1152		
					1	1536	769-1152				
0	1	1	1	1024 x 600	0	1536	769-1152	1536	769-1152		
					1	1536	769-1152				
1	0	0	0	1024 x 480	0	1536	769-1152	1536	769-1152		
					1	1536	769-1152				
1	0	0	1	960 x 540	0	1440	721-1200	1440	721-1200		
					1	1440	721-1200				
1	0	1	0	640 x 480	0	1920	0				

1	0	1	1	600 x 1024	0	1800	901-1020				
1	1	0	0	540 x 960	0	1620	817-1116				
1	1	0	1	(Reserved)							
1	1	1	0	(Reserved)							
1	1	1	1	Arbitrary Resolution	-	-		-		-	

Note: For arbitrary resolution mode, user must consult Forcelead about the output channel number of each IC.

4.11 Recommend Routing Resistance

Pad type	Pad	Resistance
Power supply	VDDI / VDD_PFM	< 5Ω
	VSSI / VSS_PFM	< 5Ω
	VDDP / VSSP	< 5Ω
	VSSA / VSS_RX	< 3Ω
	VDDRX	< 5Ω
	VSP / VSN	< 3Ω
	VDD_OTP	< 10Ω
Regulator output and reference input pins	VGMPHI / VGMPLI	< 20Ω
	VGMPMI / VGMNMI	
	VGMNHI / VGMNLI	
	VGMPHO / VGMPLO	
	VGMPMO / VGMNMO	
	VGMNHO / VGMNLO	
	V15D / V15D_RX	< 5Ω
	VCOM	< 30Ω
	VRNL	< 10Ω
	VSRP / VRSN	< 3Ω
SPI /I2C pins	SPI_CSB	< 20Ω
	SPI_SCL	
	SPI_SDAI	
	SPI_SDAO	
	I2C_SDA	
	I2C_SCL	
SPI_FLASH	ECS	< 20Ω
	ESCL	
	ESDAI	
	ESDAO	
Charge pump and PFM pins	VGH	< 10Ω
	VGL	< 10Ω
	CHP[1:3]	< 5Ω
	CHN[1:3]	
	CLP[1:2]	< 5Ω
	CLN[1:2]	
	VREGP/ VREGN	< 5Ω
	DRVP/ DRVN	< 5Ω
	VMONP/VMONN	< 50Ω

Pad type	Pad	Resistance
Input interface and output pins	D0[7:0]	< 20Ω
	D1[7:0]	
	D2[7:0]	
	HS / VS / DE / DCLK	
Input control pins	RSTB	< 50Ω
	HW_CTRL	< 150Ω
	STBYB	
	WRBYCID	
	GDMAP	
	ROM_RLD	
	EXT_PWR	
	EXT_PWR2	
	VESA	
	MODE	
	CPUS[1:0]	
	BIT8 / BIST	
	RL / UD / NB	
	GDSEL	
	FSEL[1:0]	
	INV[1:0]	
	RES[3:0]	
	GDPOS[1:0]	
	CID[1:0]	
	I2C_SPI_SEL	
Cascade pins	GPO_R[13:1]	< 100Ω
	GPO_L[13:1]	
Special Function pins	TP_SYNC	< 100Ω
	ERR	
	ERR2	
Through pins	THROUGH_[1:2]	-
	VCOM_R	-
	VCOM_L	-

5. FUNCTION DESCRIPTION

5.1 Controller Interface

5.1.1 Interface Controller Parameter

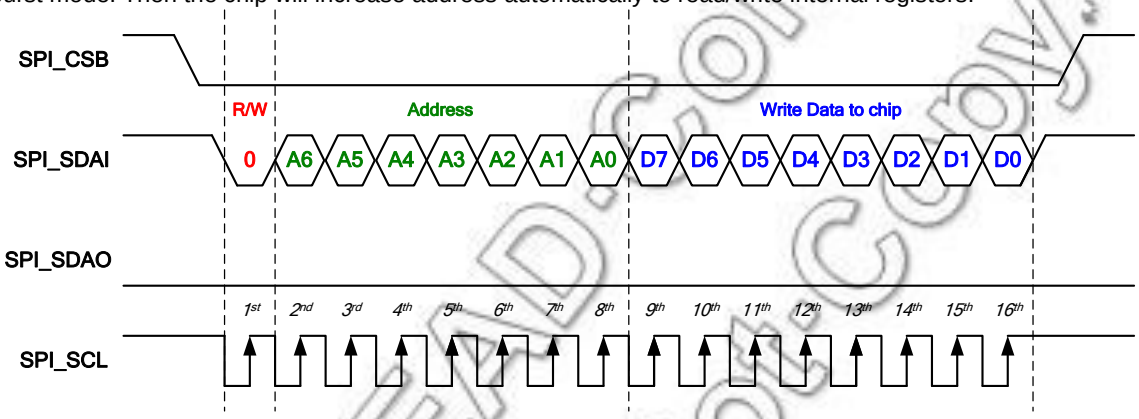
The single chip or multi chips cascade application, the parameter setting please refer to the mapping table below:

WRBYCID	CID[1:0]	R/W Bit	Function	Active Chip
H	00	"1"	Read	Master
	01			Slave1
	10			Slave2
	11			Reserved
	00	"0"	Write	Master
	01			Slave1
	10			Slave2
	11			Reserved
L	xx	"1"	Read	Master
	xx	"0"	Write	Master and Slave

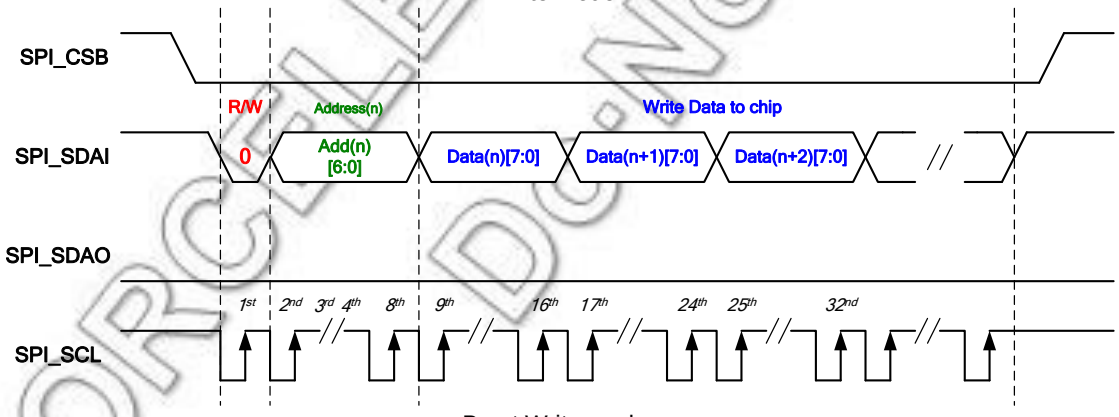
Note: When WRBYCID="L" and R/W="1" setting, read only from Master chip

5.1.2 4-Wire Serial Peripheral Interface

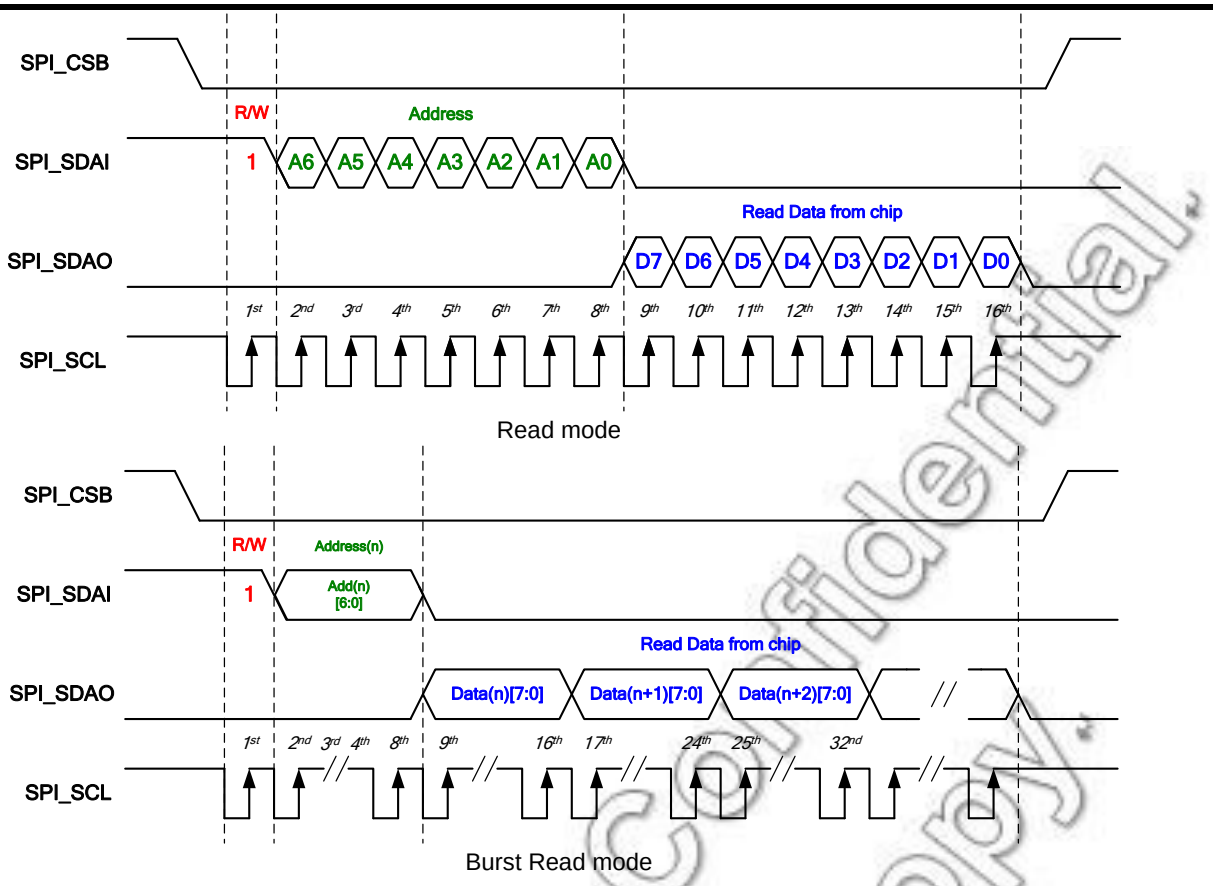
This chip supports serial peripheral interface (SPI) to set internal registers. Under write operation, R/W bit equals to "0," and the external controller sends the address and data to the chip by SPI_SDAI. Under read operation, R/W bit equals to "1," and the external controller sends the address to the chip by SPI_SDAI. Then the chip will return the data value by SPI_SDAO. The returned data should be latched at the rising edge of SPI_SCL from the external controller. This chip also supports the burst R/W mode to reduce the programming time. The external controller can just send the R/W and address once, when the chip is in the burst mode. Then the chip will increase address automatically to read/write internal registers.



Write mode



Burst Write mode



5.1.3 I2C

The I2C Compatible Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (I2C_SDA) and a Serial Clock line (I2C_SCL). Both lines must be connected with a pull-up resistor which drives I2C_SDA and I2C_SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

5.1.3.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the I2C_SDA line must remain stable during the HIGH period of the clock pulse because changes of I2C_SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig. 1.

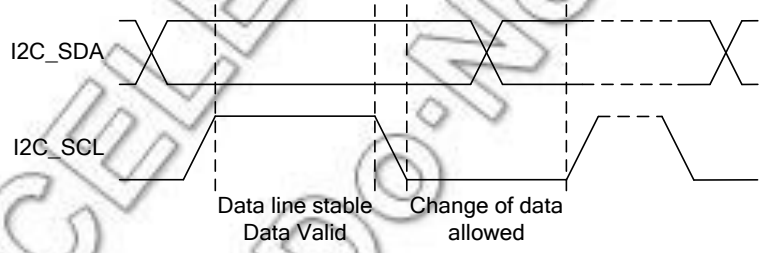


Fig. 1 Bit Transfer

5.1.3.2 START and STOP Conditions

Both I2C_SDA and I2C_SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of I2C_SDA while I2C_SCL is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of I2C_SDA while I2C_SCL is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig. 2.

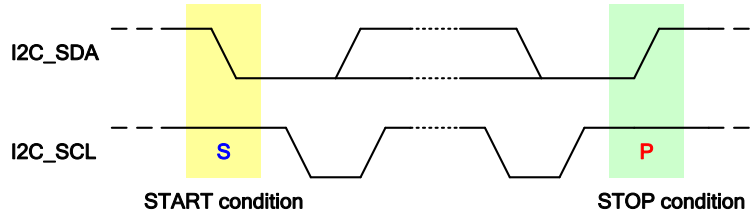


Fig. 2 Definition of START and STOP Condition

5.1.3.3 Acknowledgement

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on I2C_SDA by the transmitter when the master generates an extra acknowledge-related clock pulse. A slave receiver addressed must generate an acknowledge-bit after the reception of each byte. The device that acknowledges must pull-down the I2C_SDA line during the acknowledge-clock pulse, so that the I2C_SDA line stays LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the I2C Interface is illustrated in Fig. 3.

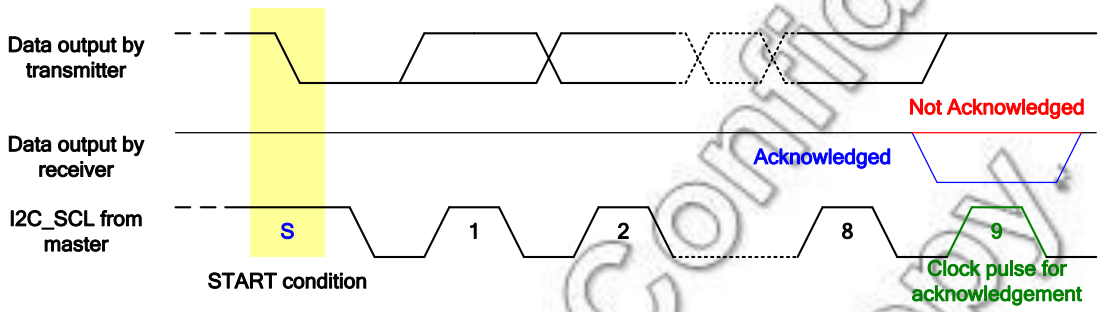
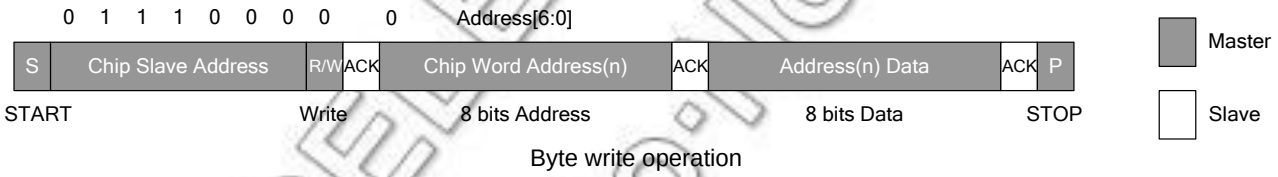


Fig. 3 Acknowledgement of I2C Interface

5.1.3.4 I2C Interface Protocol

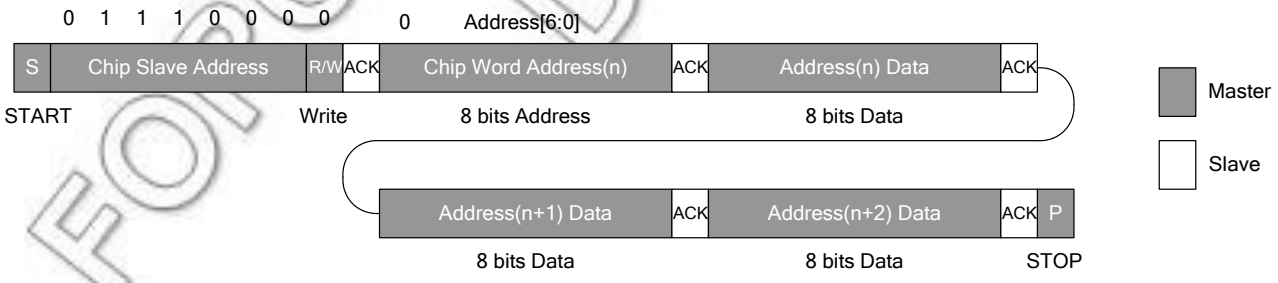
This chip supports 2-Wire Serial Interface (I2C) to set internal registers. The chip acts as a slave device, and its slave address is fixed to 0111000.

The master device sends the START signal, the 7bit slave address “0111000,” and the R/W=0 bit to inform the chip that the master device is going to do the WRITE operation, and then the chip will reply the first acknowledgement. After that, the master device sends 8-bit address to select which internal register to be set. The chip will reply the second acknowledgement if the register address is valid. The master device sends 8-bit data for the internal register value, and then the chip will reply the third acknowledgement. At last, the master device sends the STOP signal.



Byte write operation

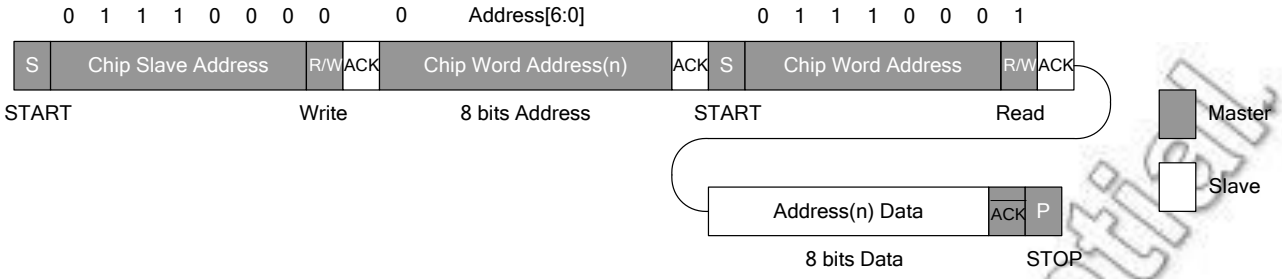
During Burst write mode, the master device can give 8bit more data value. The chip will increase address automatically to load data into internal register.



Burst write operation

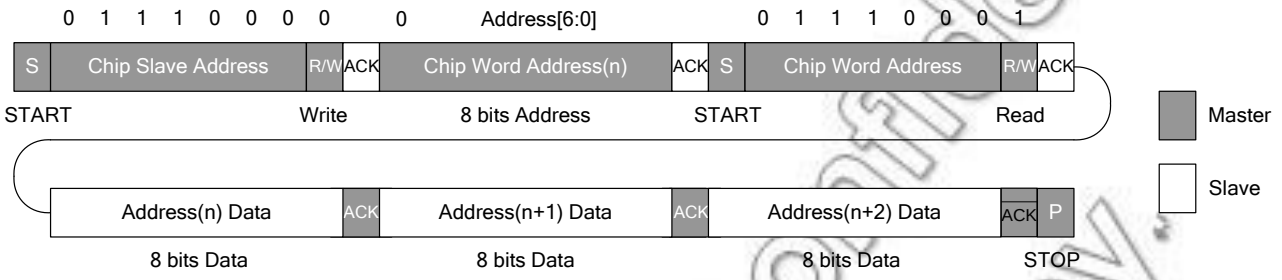
The master device sends the START signal, the 7bit slave address “0111000,” and the R/W=0 bit to inform the chip that master device is going to do the write operation, and then the chip will reply the first acknowledgement. After that, the master device sends 8-bit address to select which internal register to be read. The chip replies the second acknowledgement if the register address is valid. Instead of the STOP signal, the master device sends another START

signal, the 7bit slave address ”0111000,” and the R/W=1 bit to inform the chip that the master device is going to do the READ operation, and the chip will reply both the third acknowledgement and 8-bit data of the internal register value. Then the master device sends a not acknowledgement of read data, and the STOP signal.



Byte read operation

When the master device receives data from the chip and sends an acknowledgement, the chip will reply data until it receives a *not* acknowledgement.



Burst read operation

Note: 4.7K~8Kohm Pull-High resistance was suggested. (Only I2C_SDA signal needs).

5.2 Display Data Transmission

5.2.1 Interface and Control Settings

Interface	IFSEL[1]	IFSEL[0]	BIT8	Interface
CMOS	L	L	H	Parallel RGB888
			L	Parallel RGB666
LVDS	H	H	H	2-Port 8bit
			L	2-Port 6bit
		L	H	1-Port 8bit
			L	1-Port 6bit

5.2.1.1 CMOS & LVDS Interface Pins Connection Mapping

Pin Name	Interface							
	CMOS				LVDS			
	MLSB="L"		MLSB="H"		1-Port		2-Port	
	BIT8= "H" (8bit)	BIT8= "L" (6bit)	BIT8= "H" (8bit)	BIT8= "L" (6bit)	BIT8= "H" (8bit)	BIT8= "L" (6bit)	BIT8= "H" (8bit)	BIT8= "L" (6bit)
D2[0]	DB0	GND	DB7	GND	GND	GND	GND	GND
D2[1]	DB1	GND	DB6	GND	GND	GND	GND	GND
D2[2]	DB2	DB0	DB5	DB5	GND	GND	GND	GND
D2[3]	DB3	DB1	DB4	DB4	GND	GND	GND	GND
D2[4]	DB4	DB2	DB3	DB3	GND	GND	ED3P	VDDRX
D2[5]	DB5	DB3	DB2	DB2	GND	GND	ED3N	GND
D2[6]	DB6	DB4	DB1	DB1	GND	GND	ED2P	ED2P
D2[7]	DB7	DB5	DB0	DB0	GND	GND	ED2N	ED2N
D1[0]	DG0	GND	DG7	GND	GND	GND	ECLKP	ECLKP
D1[1]	DG1	GND	DG6	GND	GND	GND	ECLKN	ECLKN
D1[2]	DG2	DG0	DG5	DG5	GND	GND	ED1P	ED1P
D1[3]	DG3	DG1	DG4	DG4	GND	GND	ED1N	ED1N
D1[4]	DG4	DG2	DG3	DG3	GND	GND	ED0P	ED0P
D1[5]	DG5	DG3	DG2	DG2	GND	GND	ED0N	ED0N
D1[6]	DG6	DG4	DG1	DG1	D3P	VDDRX	OD3P	VDDRX
D1[7]	DG7	DG5	DG0	DG0	D3N	GND	OD3N	GND
D0[0]	DR0	GND	DR7	GND	D2P	D2P	OD2P	OD2P
D0[1]	DR1	GND	DR6	GND	D2N	D2N	OD2N	OD2N
D0[2]	DR2	DR0	DR5	DR5	CLKP	CLKP	OCLKP	OCLKP
D0[3]	DR3	DR1	DR4	DR4	CLKN	CLKN	OCLKN	OCLKN
D0[4]	DR4	DR2	DR3	DR3	D1P	D1P	OD1P	OD1P
D0[5]	DR5	DR3	DR2	DR2	D1N	D1N	OD1N	OD1N
D0[6]	DR6	DR4	DR1	DR1	D0P	D0P	OD0P	OD0P
D0[7]	DR7	DR5	DR0	DR0	D0N	D0N	OD0N	OD0N
DCLK	DCLK	DCLK	DCLK	DCLK	GND	GND	GND	GND
VS	VS	VS	VS	VS	GND	GND	GND	GND
HS	HS	HS	HS	HS	GND	GND	GND	GND
DE	DE	DE	DE	DE	GND	GND	GND	GND

5.2.1.2 MIPI Interface Pins Connection Mapping

Pin Name	MIPI IFSEL[1:0]="01"		
	r_mp_lane[1:0]="00" 4Lane	r_mp_lane[1:0]="01" 2Lane	r_mp_lane[1:0]="10" 1Lane
D2[0]	GND	GND	GND
D2[1]	GND	GND	GND
D2[2]	GND	GND	GND
D2[3]	GND	GND	GND
D2[4]	GND	GND	GND
D2[5]	GND	GND	GND
D2[6]	GND	GND	GND
D2[7]	GND	GND	GND
D1[0]	GND	GND	GND
D1[1]	GND	GND	GND
D1[2]	GND	GND	GND
D1[3]	GND	GND	GND
D1[4]	GND	GND	GND
D1[5]	GND	GND	GND
D1[6]	D3P	GND	GND
D1[7]	D3N	GND	GND
D0[0]	D2P	GND	GND
D0[1]	D2N	GND	GND
D0[2]	CLKP	CLKP	CLKP
D0[3]	CLKN	CLKN	CLKN
D0[4]	D1P	D1P	GND
D0[5]	D1N	D1N	GND
D0[6]	D0P	D0P	D0P
D0[7]	D0N	D0N	D0N
DCLK	GND	GND	GND
VS	GND	GND	GND
HS	GND	GND	GND
DE	GND	GND	GND

5.2.2 RGB Interface

5.2.2.1 Data Format

Parallel RGB888

Pin	1st Data	2nd Data	3rd Data	…	Nth Data
D00	1'R0	2'R0	3'R0	…	N'R0
D01	1'R1	2'R1	3'R1	…	N'R1
D02	1'R2	2'R2	3'R2	…	N'R2
D03	1'R3	2'R3	3'R3	…	N'R3
D04	1'R4	2'R4	3'R4	…	N'R4
D05	1'R5	2'R5	3'R5	…	N'R5
D06	1'R6	2'R6	3'R6	…	N'R6
D07	1'R7	2'R7	3'R7	…	N'R7
D10	1'G0	2'G0	3'G0	…	N'G0
D11	1'G1	2'G1	3'G1	…	N'G1
D12	1'G2	2'G2	3'G2	…	N'G2
D13	1'G3	2'G3	3'G3	…	N'G3
D14	1'G4	2'G4	3'G4	…	N'G4
D15	1'G5	2'G5	3'G5	…	N'G5
D16	1'G6	2'G6	3'G6	…	N'G6
D17	1'G7	2'G7	3'G7	…	N'G7
D20	1'B0	2'B0	3'B0	…	N'B0
D21	1'B1	2'B1	3'B1	…	N'B1
D22	1'B2	2'B2	3'B2	…	N'B2
D23	1'B3	2'B3	3'B3	…	N'B3
D24	1'B4	2'B4	3'B4	…	N'B4
D25	1'B5	2'B5	3'B5	…	N'B5
D26	1'B6	2'B6	3'B6	…	N'B6
D27	1'B7	2'B7	3'B7	…	N'B7

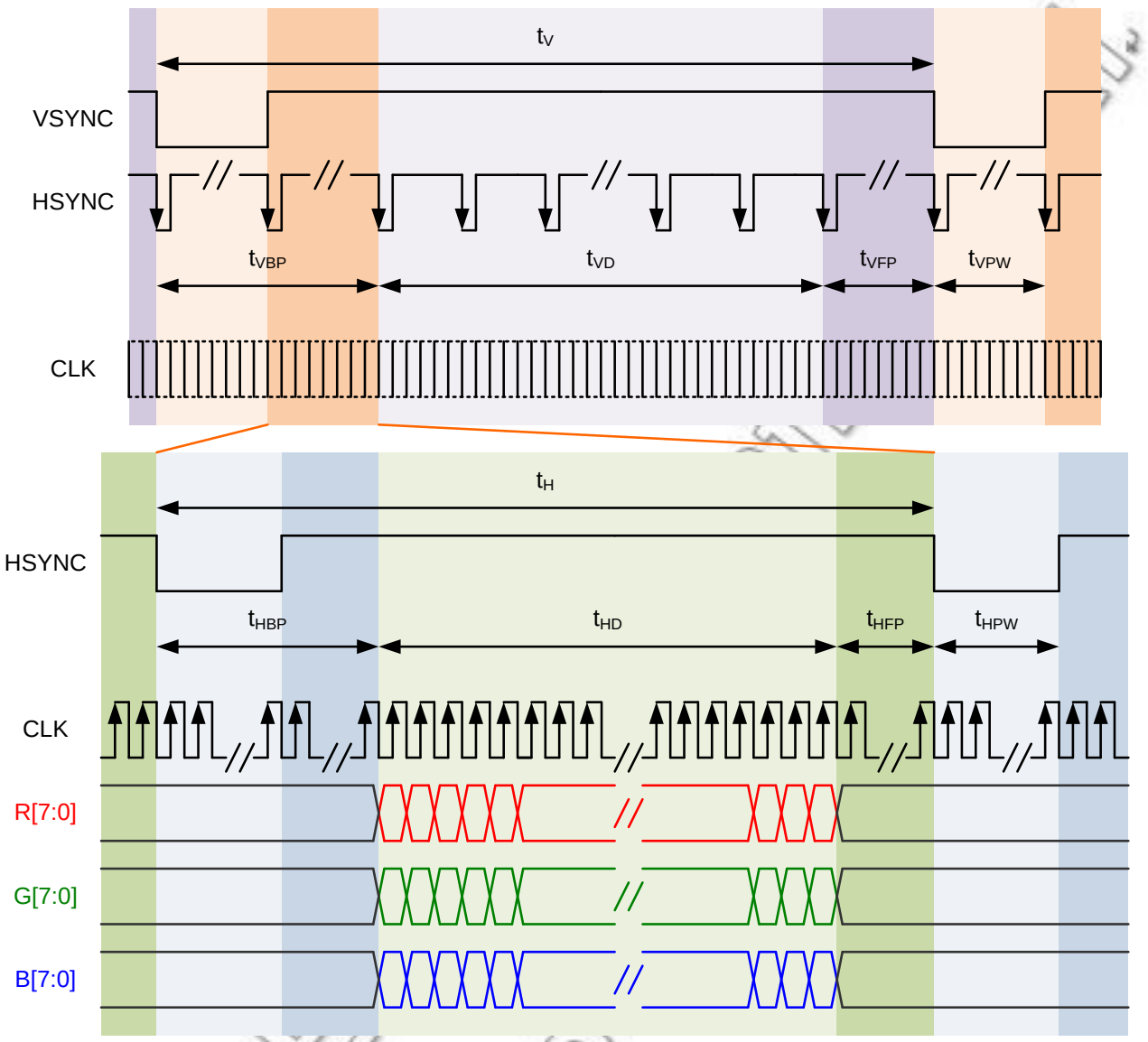
Parallel RGB666

Pin	1st Data	2nd Data	3rd Data	…	Nth Data
D00	GND	GND	GND	…	GND
D01	GND	GND	GND	…	GND
D02	1'R0	2'R0	3'R0	…	N'R0
D03	1'R1	2'R1	3'R1	…	N'R1
D04	1'R2	2'R2	3'R2	…	N'R2
D05	1'R3	2'R3	3'R3	…	N'R3
D06	1'R4	2'R4	3'R4	…	N'R4
D07	1'R5	2'R5	3'R5	…	N'R5
D10	GND	GND	GND	…	GND
D11	GND	GND	GND	…	GND
D12	1'G0	2'G0	3'G0	…	N'G0
D13	1'G1	2'G1	3'G1	…	N'G1
D14	1'G2	2'G2	3'G2	…	N'G2
D15	1'G3	2'G3	3'G3	…	N'G3
D16	1'G4	2'G4	3'G4	…	N'G4
D17	1'G5	2'G5	3'G5	…	N'G5
D20	GND	GND	GND	…	GND
D21	GND	GND	GND	…	GND
D22	1'B0	2'B0	3'B0	…	N'B0
D23	1'B1	2'B1	3'B1	…	N'B1
D24	1'B2	2'B2	3'B2	…	N'B2
D25	1'B3	2'B3	3'B3	…	N'B3
Pin	1st Data	2nd Data	3rd Data	…	Nth Data

D26	1'B4	2'B4	3'B4	···	N'B4
D27	1'B5	2'B5	3'B5	···	N'B5

5.2.2.2 SYNC Mode

Parallel RGB



1920 x 1080 (Only 2-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	66.5	67.87	75	MHz	
Horizontal blanking time	t_{HBT}	48	50	99	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	24	26	253	t_{CLK}	Include t_{HPW}
Horizontal display area	t_{HD}		960		t_{CLK}	
Horizontal front porch	t_{HFP}	24	24	255	t_{CLK}	
Horizontal period	t_H	1008	1010	1059	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	100	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	10	20	253	t_H	Include t_{VPW}
Vertical display area	t_{VD}		1080		t_H	
Vertical front porch	t_{VFP}	10	20	255	t_H	
Vertical period	t_V	1100	1120	1180	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	

Frame rate	FR	60	60	60	Hz	

1920 x 720 (2-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	44.8	46.06	49.8	MHz	
Horizontal blanking time	t_{HBT}	48	50	96	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	24	26	253	t_{CLK}	Include t_{HPW}
Horizontal display area	t_{HD}		960		tCLK	
Horizontal front porch	t_{HFP}	24	24	255	t_{CLK}	
Horizontal period	t_H	1008	1010	1056	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	66	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	10	20	253	t_H	Include t_{VPW}
Vertical display area	t_{VD}		720		tH	
Vertical front porch	t_{VFP}	10	20	255	t_H	
Vertical period	t_V	740	760	786	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

1920 x 720 (1-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	87.4	89.8	92	MHz	
Horizontal blanking time	t_{HBT}	48	50	72	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	24	26	253	t_{CLK}	Include t_{HPW}
Horizontal display area	t_{HD}		1920		tCLK	
Horizontal front porch	t_{HFP}	24	24	255	t_{CLK}	
Horizontal period	t_H	1968	1970	1992	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	50	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	10	20	253	t_H	Include t_{VPW}
Vertical display area	t_{VD}		720		tH	
Vertical front porch	t_{VFP}	10	20	255	t_H	
Vertical period	t_V	740	760	770	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

1280 x 720 (2-Port)

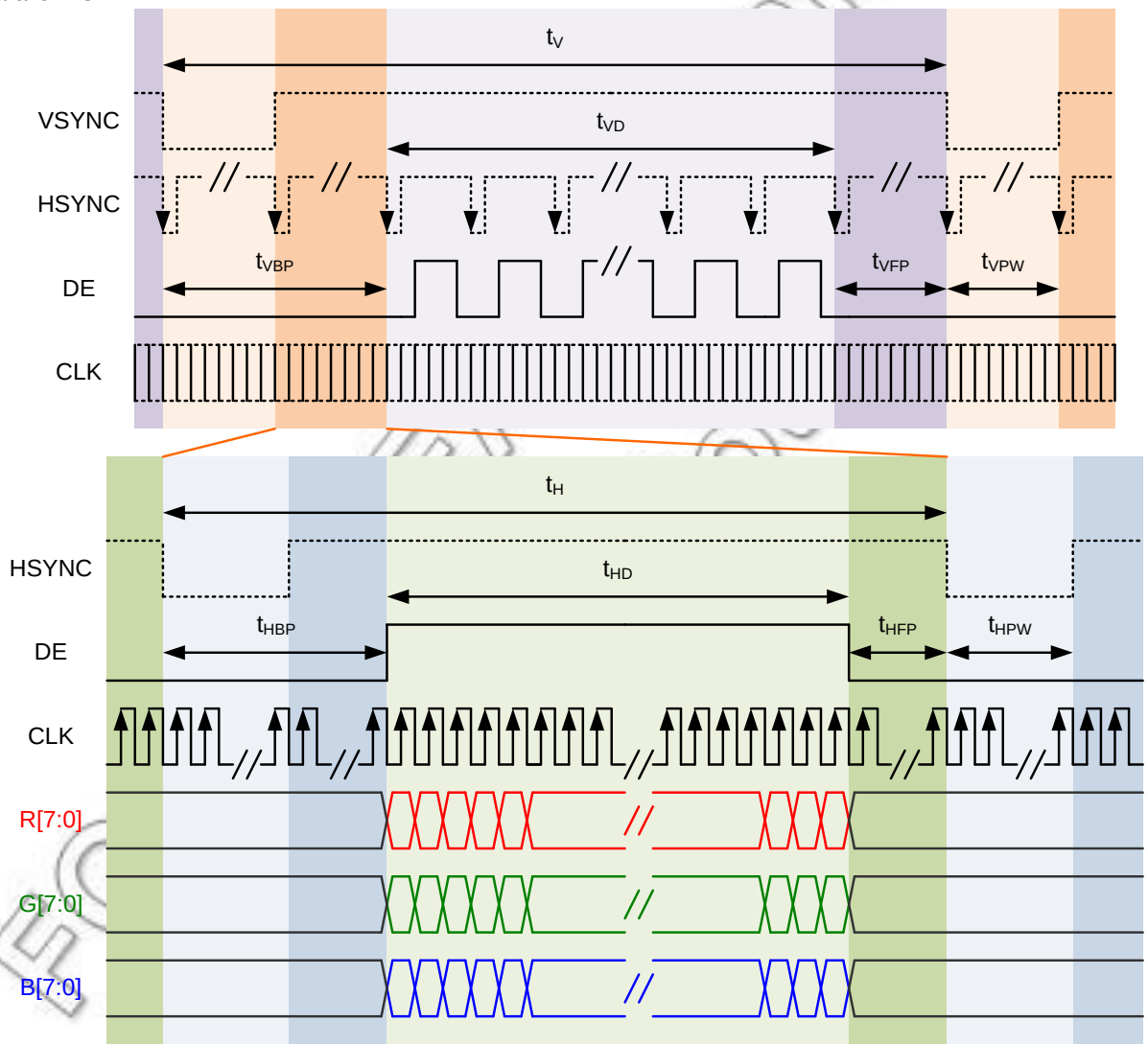
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	30.5	31.46	33.22	MHz	
Horizontal blanking time	t_{HBT}	48	50	52	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	24	26	253	t_{CLK}	Include t_{HPW}
Horizontal display area	t_{HD}		640		tCLK	
Horizontal front porch	t_{HFP}	24	24	255	t_{CLK}	
Horizontal period	t_H	688	690	692	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	80	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	10	20	253	t_H	Include t_{VPW}
Vertical display area	t_{VD}		720		tH	
Vertical front porch	t_{VFP}	10	20	255	t_H	
Vertical period	t_V	740	760	800	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

1280 x 720 (1-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	58.9	60.65	66.34	MHz	
Horizontal blanking time	t_{HBT}	48	50	102	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal back porch	t_{HBP}	24	26	253	t_{CLK}	Include t_{HPW}
Horizontal display area	t_{HD}		1280		tCLK	
Horizontal front porch	t_{HFP}	24	24	255	t_{CLK}	
Horizontal period	t_H	1328	1330	1382	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	80	t_H	t_{VBP} + t_{VFP}
Vertical back porch	t_{VBP}	10	20	253	t_H	Include t_{VPW}
Vertical display area	t_{VD}		720		tH	
Vertical front porch	t_{VFP}	10	20	255	t_H	
Vertical period	t_V	740	760	800	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

5.2.2.3 DE Mode

Parallel RGB



1920 x 1080 (Only 2-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	66.5	67.87	75	MHz	
Horizontal blanking time	t_{HBT}	48	50	99	t_{CLK}	$t_{HBP} + t_{HFP}$
Horizontal display area	t_{HD}		960		t_{CLK}	
Horizontal period	t_H	1008	1010	1059	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	100	t_H	$t_{VBP} + t_{VFP}$
Vertical display area	t_{VD}		1080		t_H	
Vertical period	t_V	1100	1120	1180	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

1920 x 720 (2-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	44.8	46.06	49.8	MHz	
Horizontal blanking time	t_{HBT}	48	50	96	t_{CLK}	$t_{HBP} + t_{HFP}$
Horizontal display area	t_{HD}		960		tCLK	
Horizontal period	t_H	1008	1010	1056	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	66	t_H	$t_{VBP} + t_{VFP}$
Vertical display area	t_{VD}		720		tH	
Vertical period	t_V	740	760	786	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

1920 x 720 (1-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	87.4	89.8	92	MHz	
Horizontal blanking time	t_{HBT}	48	50	72	t_{CLK}	$t_{HBP} + t_{HFP}$
Horizontal display area	t_{HD}		1920		tCLK	
Horizontal period	t_H	1968	1970	1992	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	50	t_H	$t_{VBP} + t_{VFP}$
Vertical display area	t_{VD}		720		tH	
Vertical period	t_V	740	760	770	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

1280 x 720 (2-Port)

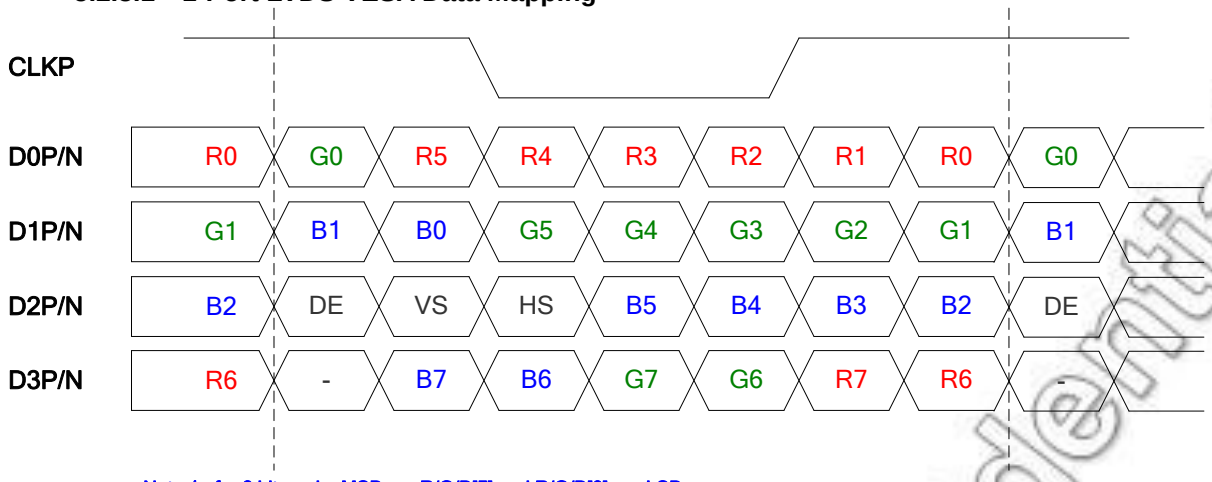
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	30.5	31.46	33.22	MHz	
Horizontal blanking time	t_{HBT}	48	50	52	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal display area	t_{HD}		640		tCLK	
Horizontal period	t_H	688	690	692	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	80	t_H	t_{VBP} + t_{VFP}
Vertical display area	t_{VD}		720		tH	
Vertical period	t_V	740	760	800	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

1280 x 720 (1-Port)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
CLK frequency	t_{CLK}	58.9	60.65	66.34	MHz	
Horizontal blanking time	t_{HBT}	48	50	102	t_{CLK}	t_{HBP} + t_{HFP}
Horizontal display area	t_{HD}		1280		tCLK	
Horizontal period	t_H	1328	1330	1382	t_{CLK}	
Horizontal pulse width	t_{HPW}	2	2	2	t_{CLK}	
Vertical blanking time	t_{VBT}	20	40	80	t_H	t_{VBP} + t_{VFP}
Vertical display area	t_{VD}		720		tH	
Vertical period	t_V	740	760	800	t_H	
Vertical pulse width	t_{VPW}	2	2	2	t_H	
Frame rate	FR	60	60	60	Hz	

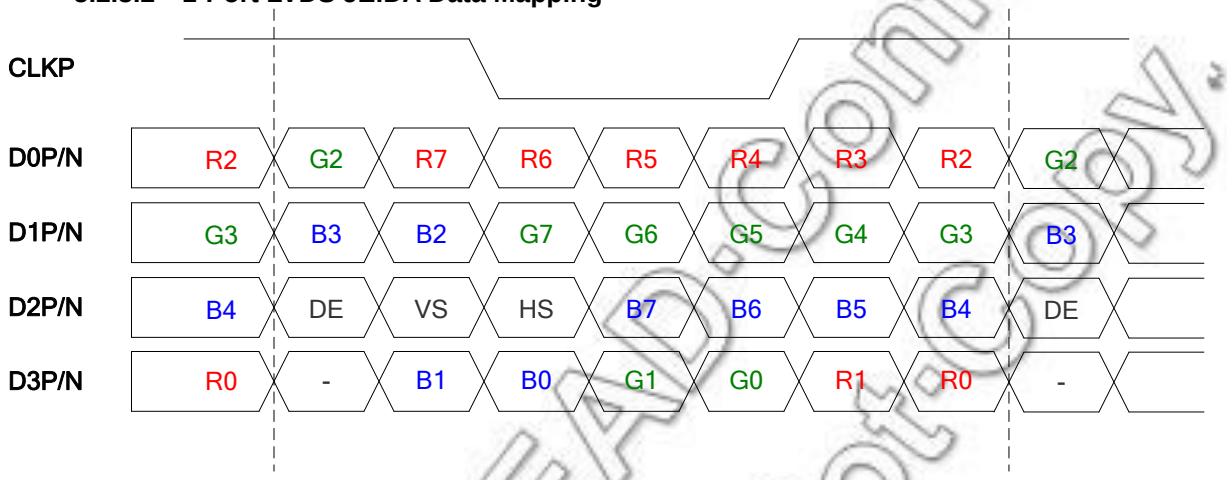
5.2.3 LVDS Interface

5.2.3.1 1-Port LVDS VESA Data Mapping



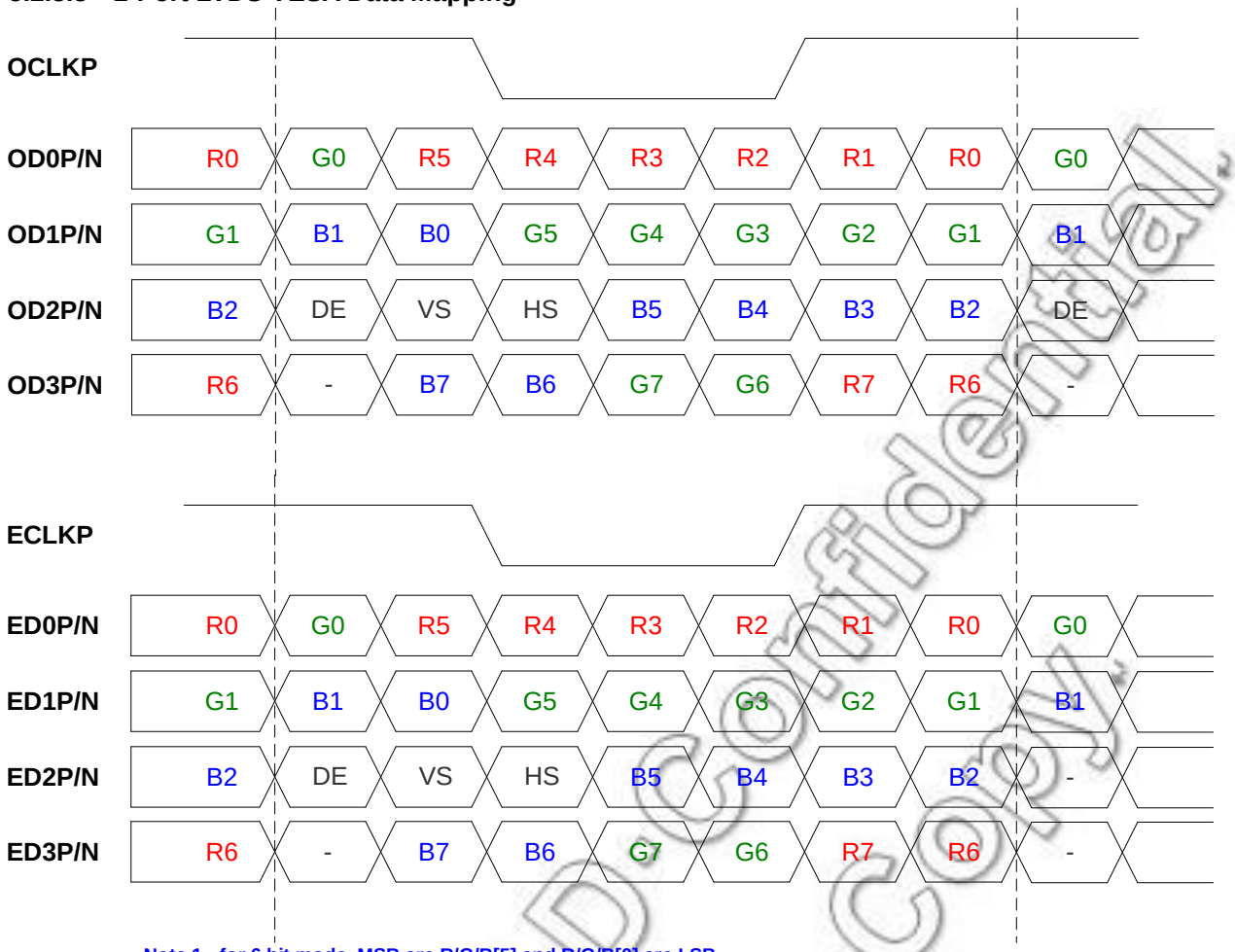
Note 1 : for 6 bit mode, MSB are R/G/B[5] and R/G/B[0] are LSB
Note 2 : for 8 bit mode, MSB are R/G/B[7] and R/G/B[0] are LSB

5.2.3.2 1-Port LVDS JEIDA Data Mapping



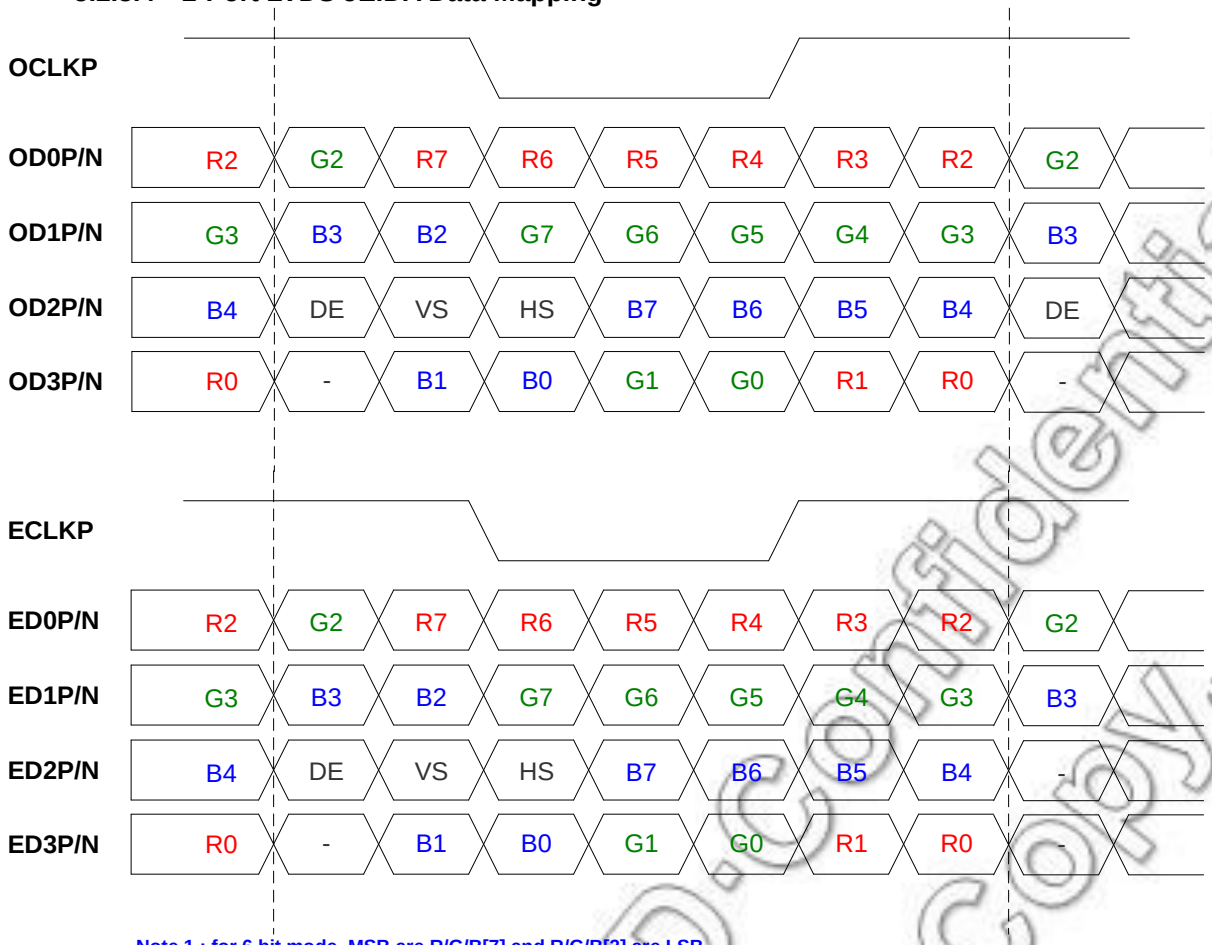
Note 1 : for 6 bit mode, MSB are R/G/B[7] and R/G/B[2] are LSB
Note 2 : for 8 bit mode, MSB are R/G/B[7] and R/G/B[0] are LSB

5.2.3.3 2-Port LVDS VESA Data Mapping



Note 1 : for 6 bit mode, MSB are R/G/B[5] and R/G/B[0] are LSB
Note 2 : for 8 bit mode, MSB are R/G/B[7] and R/G/B[0] are LSB

5.2.3.4 2-Port LVDS JEIDA Data Mapping



Note 1 : for 6 bit mode, MSB are R/G/B[7] and R/G/B[2] are LSB
Note 2 : for 8 bit mode, MSB are R/G/B[7] and R/G/B[0] are LSB

5.2.4 MIPI Function Description

5.2.4.1 MIPI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. This chip only support Video mode.

Configuration:

Lane Pair	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane /1/2/3	Unidirectional Lane ■ Forward High-Speed ■ Escape Mode (ULPS) ■ No LPDT

5.2.4.2 Display Serial Interface (DSI)

General Description

The driver IC uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode. Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the HOST to the driver IC and vice versa.

State code	Line voltage Levels		High speed	Low power	
	DP	DN		Control mode	Escape mode
HS-0	HS Low	HS High	Differential-0	Note 1	Note 1
HS-1	HS High	HS Low	Differential-1	Note 1	Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note 2

Note 1 : During high-speed transmission, the low power receivers observe LP-00 on the lines.
Note 2 :If LP-11 occurs during Escape mode, the lane returns to Stop state (Control mode LP-11)

DSI-CLK Lane

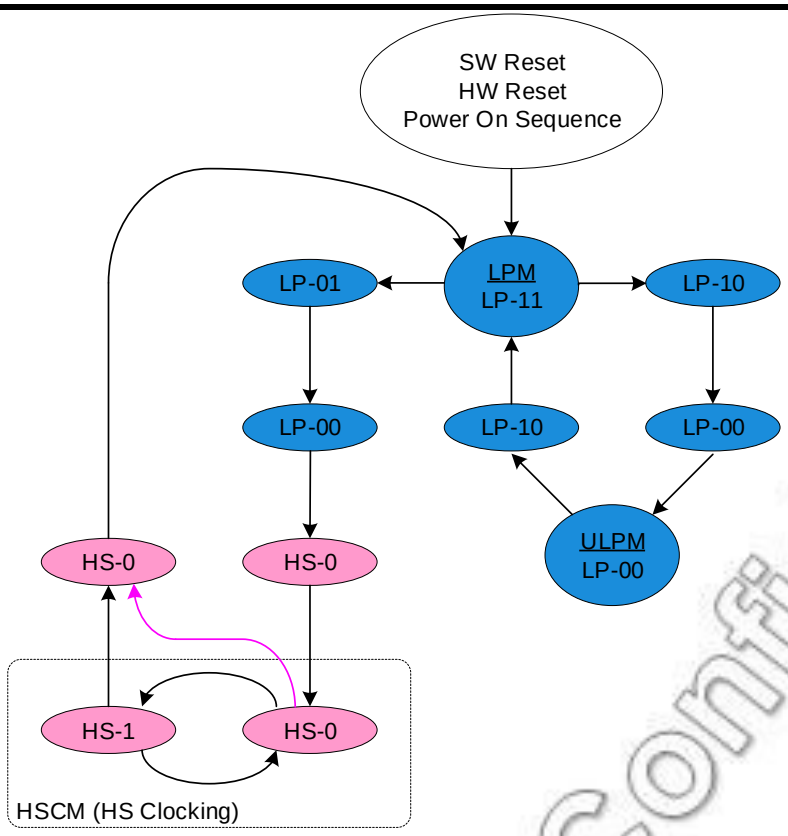
DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.



Clock Lanes Power Modes

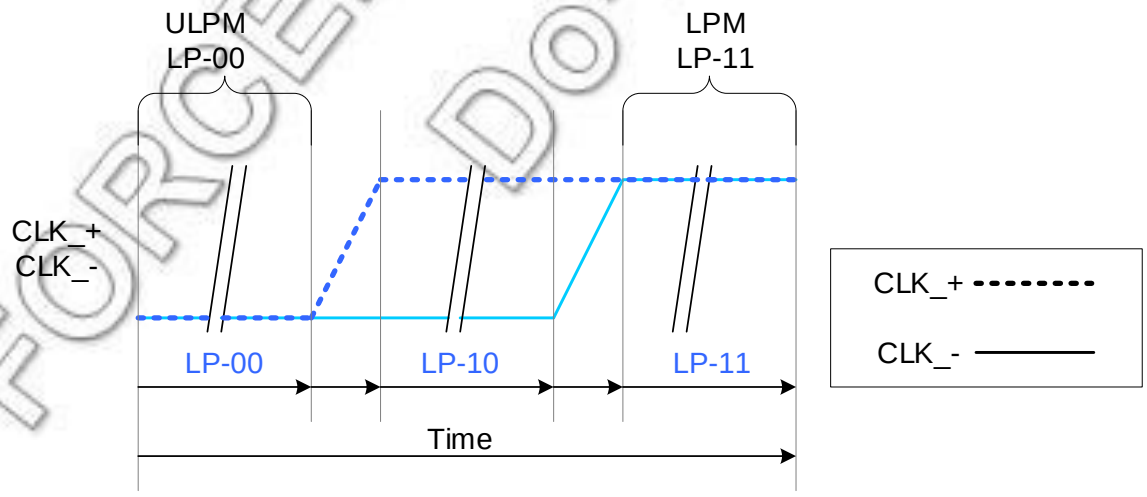
Low Power Mode

DSI-CLK+/- lanes can be driven to the Low Power Mode (LMP),when DSI-CLK lanes are entering LP-11 State Code , in three different ways:

After SW Reset, HW Reset or Power On Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM,LP-00 State Code)=>LP10=>LP-11(LPM).

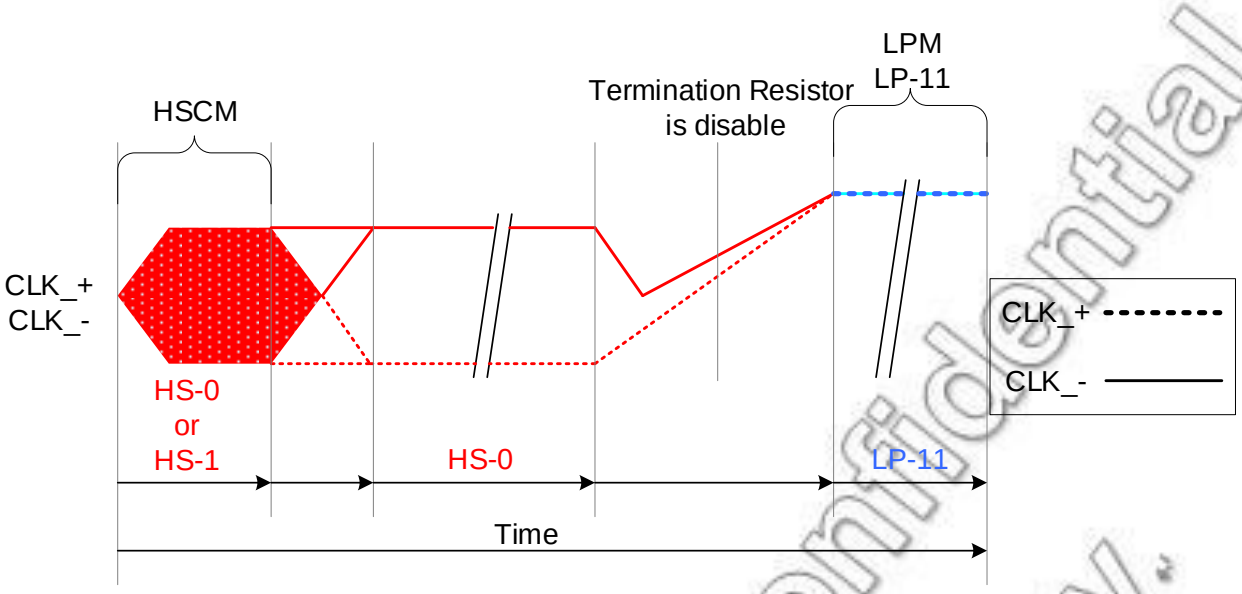
This sequence is illustrated below.



From ULPM to LPM

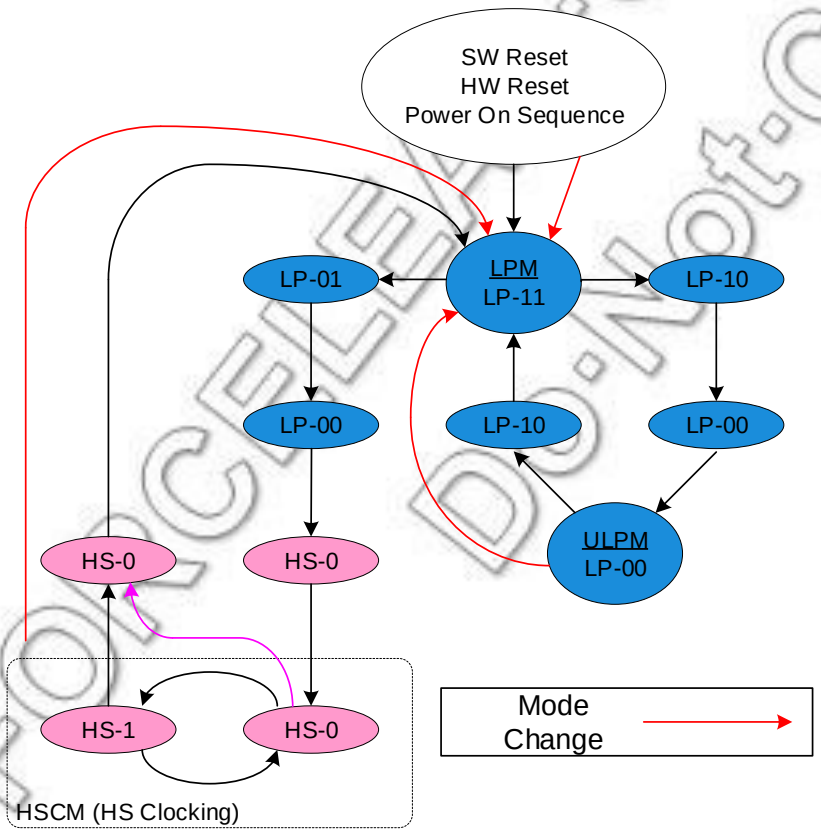
After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.



From HSCM to LPM

All three mode changes are illustrated a flow chart below.

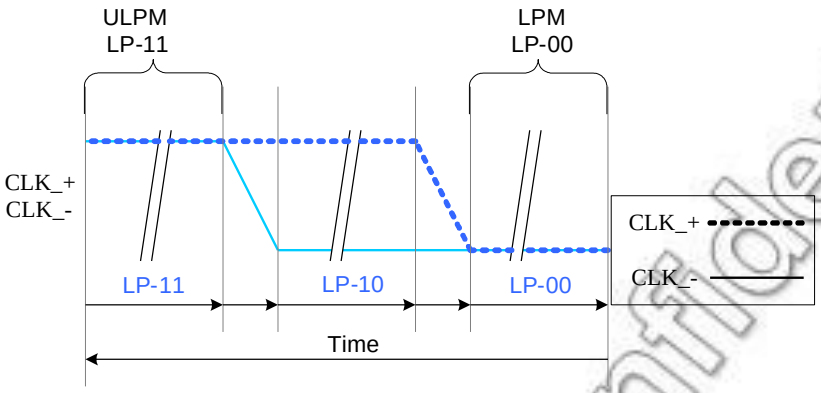


All three mode changes to LPM

Ultra Low Power Mode

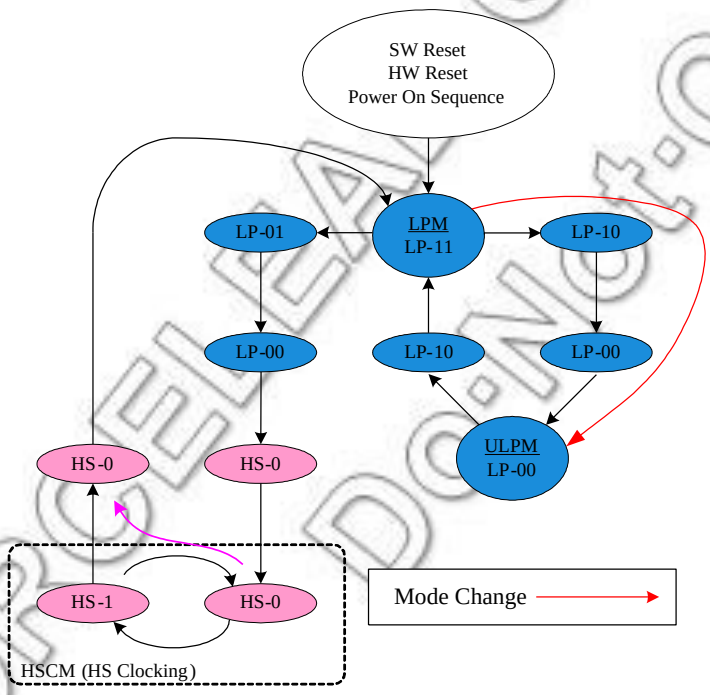
DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00(ULPM). This sequence is illustrated below.



From LPM to UPLM

The mode change is also illustrated below:



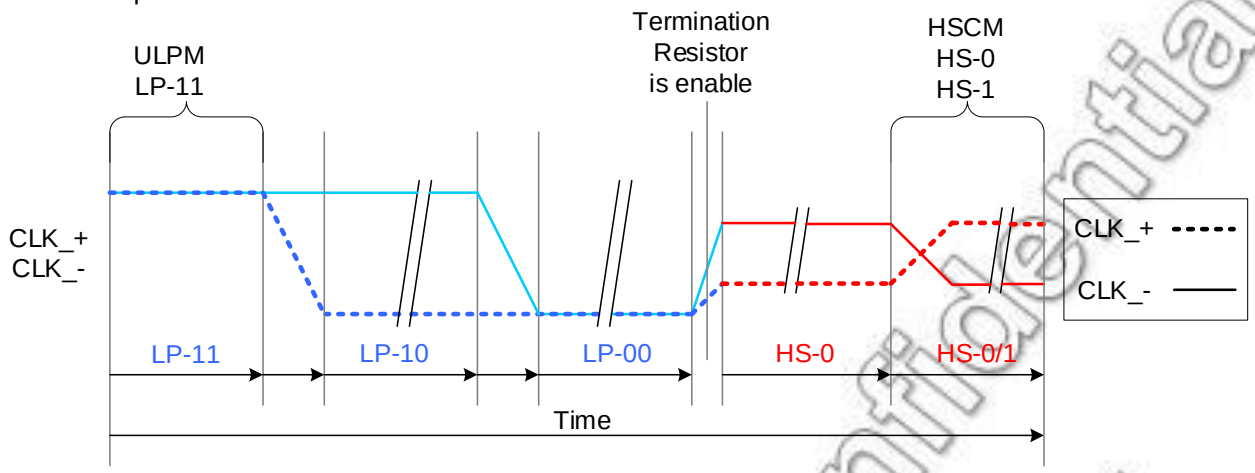
The mode change from LPM to UPLM

High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

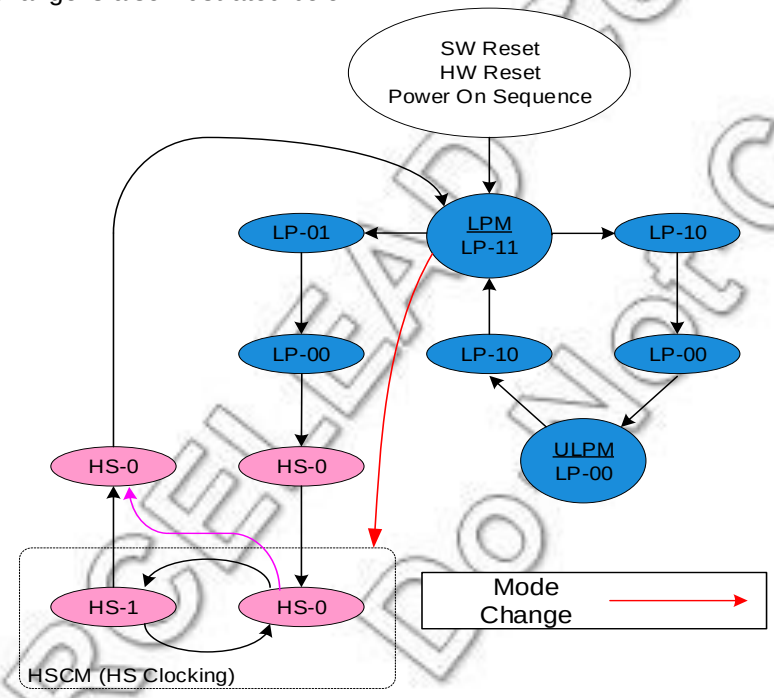
The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.



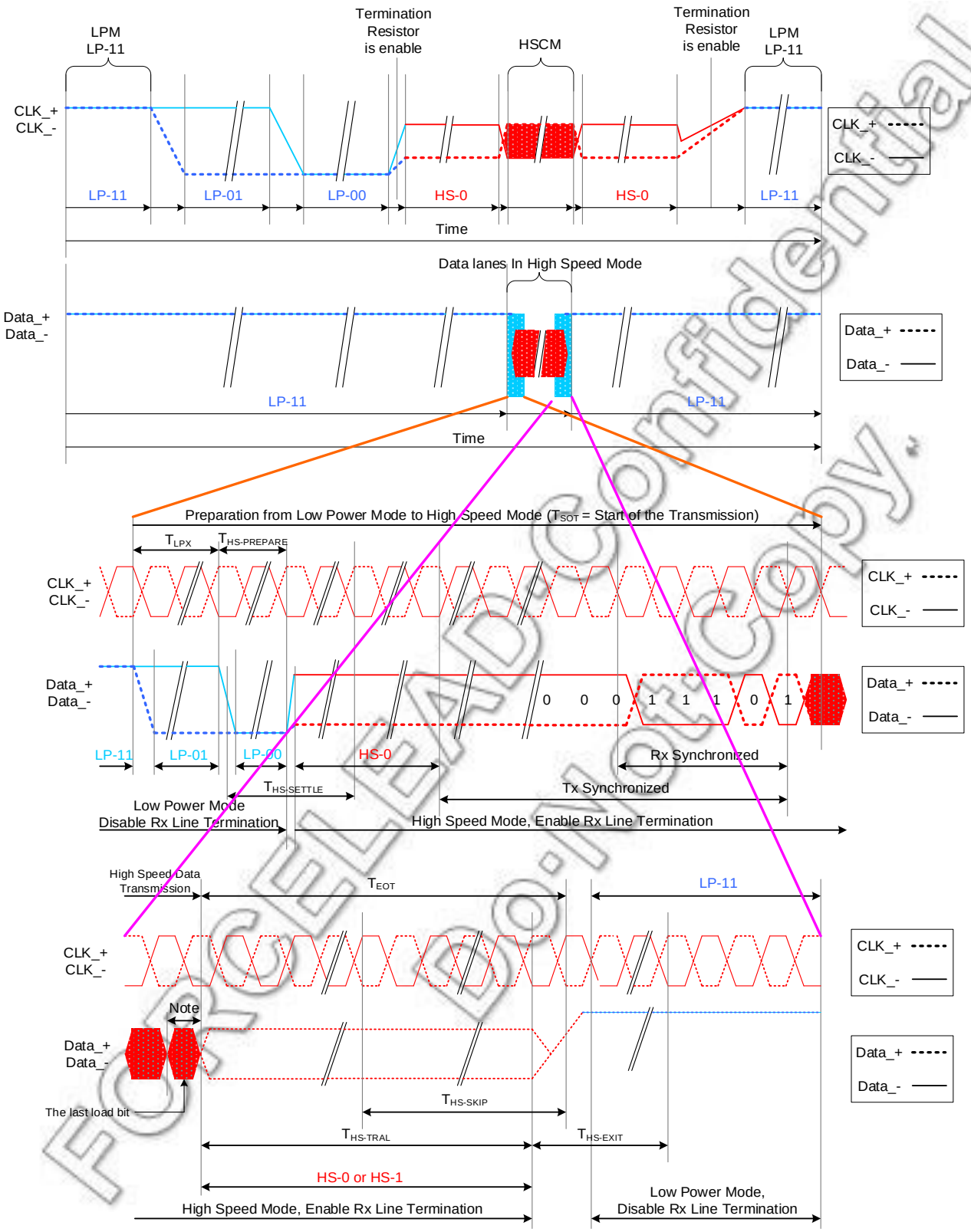
From LPM to HSCM

The mode change is also illustrated below:



Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.



High Speed Clock Burst

DSI-DATA Lane

Escape Mode

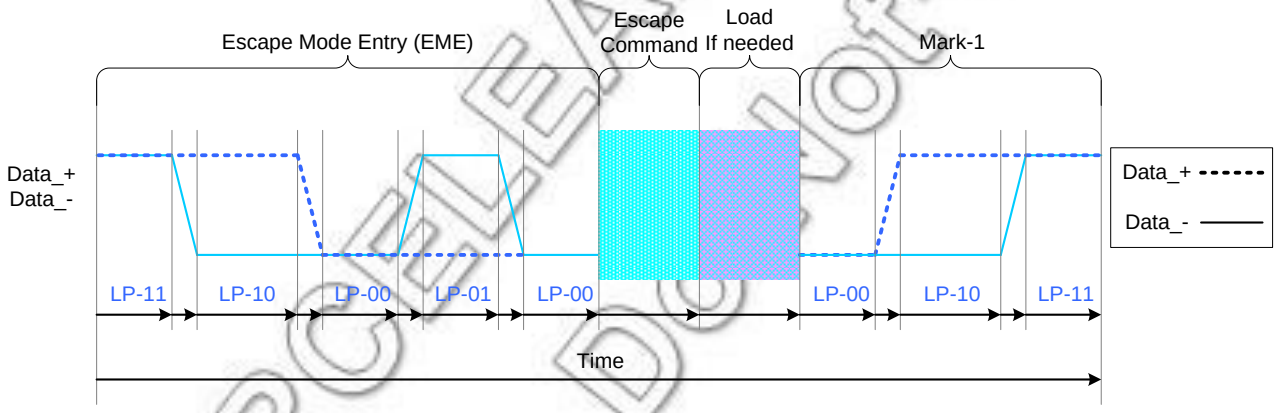
Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is reset the display module
- Indicate “Tearing Effect” (TEE), which is used for a TE trigger event from the display module to the MCU
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command(EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it. Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001 b
Ultra-Low Power Mode	Mode	0001 1110 b
Undefined-1, Note	Mode	1001 1111 b
Undefined-2, Note	Mode	1101 1110 b
Remote Application Reset	Trigge	0110 0010 b
Tearing Effect	Triggerr	0101 1101 b
Acknowledge	Trigger	0010 0001 b
Uknown-5, Note	Trigger	1010 0000 b

Note: This Escape command support has not been implemented on the display module.

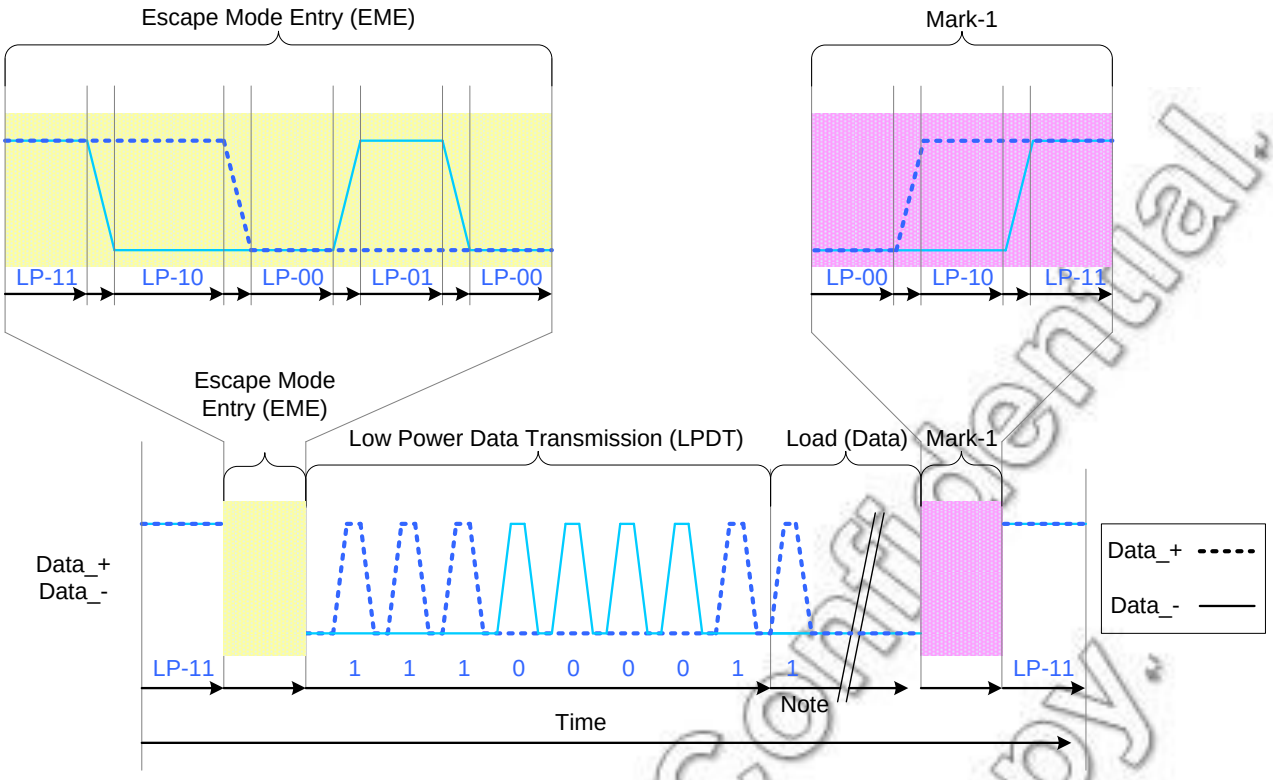
Low-Power Data Transmission(LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

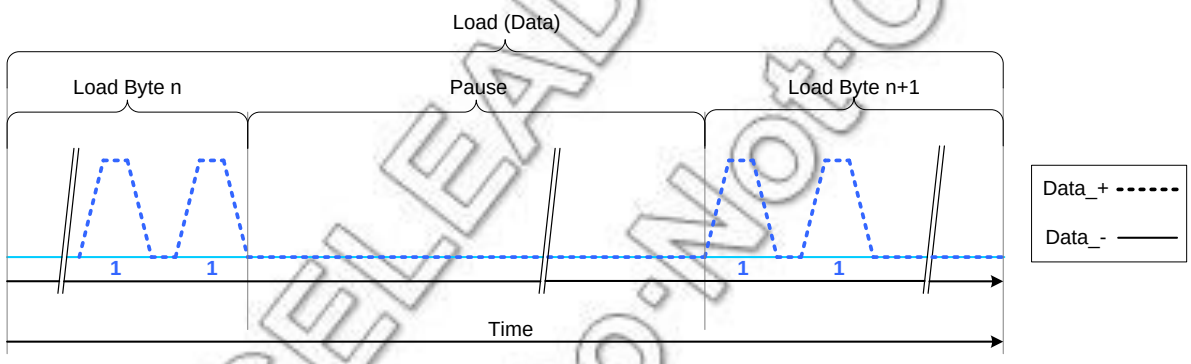
- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data): One or more bytes (8 bits) Data lanes are in pause mode when data lanes are stopped (Bothe lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note : Load (Data) is presenting that the first bit is logical "1" in this Exsample

Low-Power Data Transmission (LPDT)



Pause (Example)

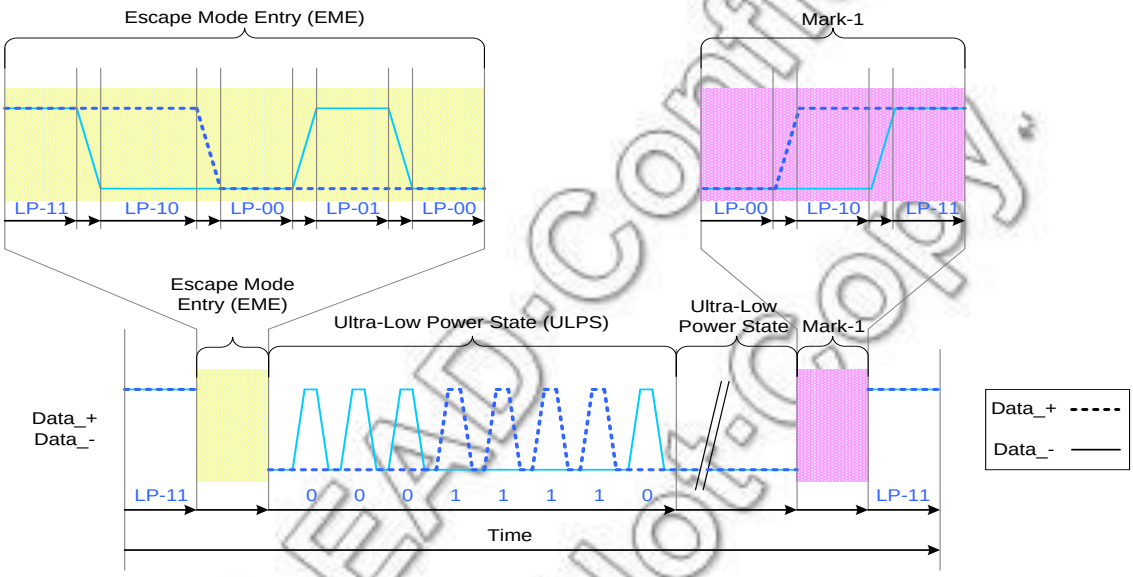
Ultra-Low Power State(ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Ultra-Low Power State (ULPS)

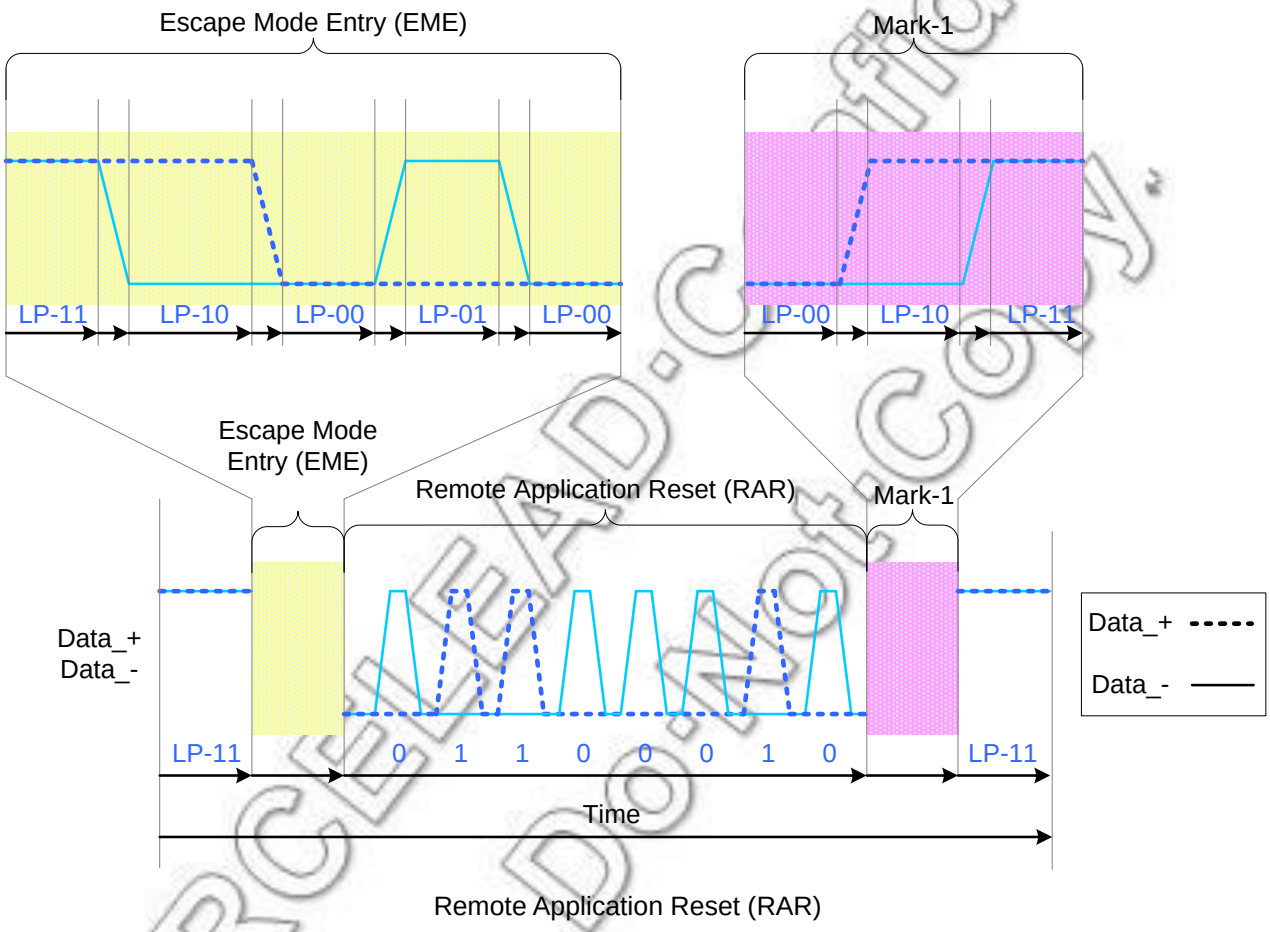
Remote Application Reset(RAP)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



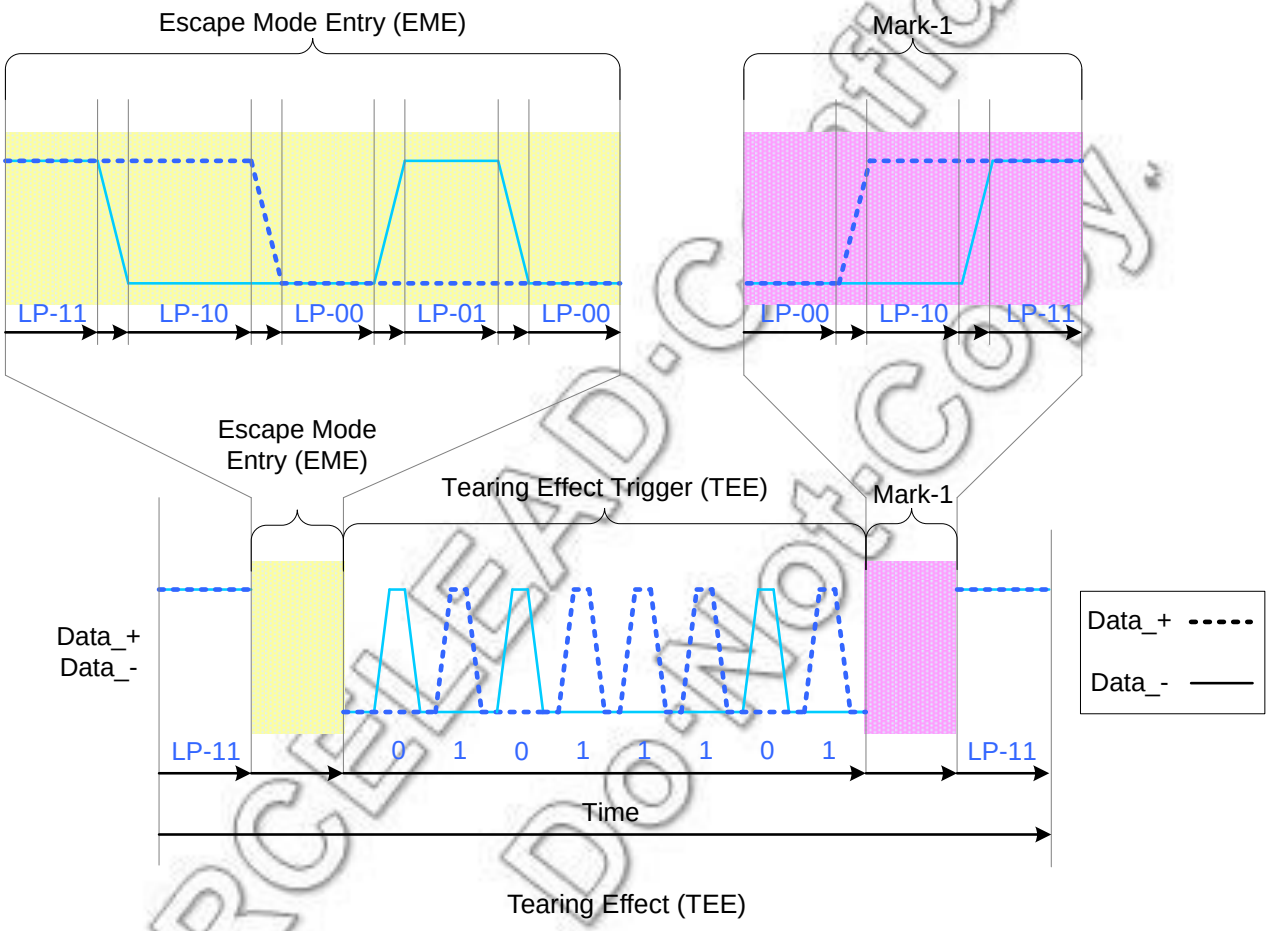
Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note: Tearing Effect (TEE) cannot be used in MIPI Video Mode

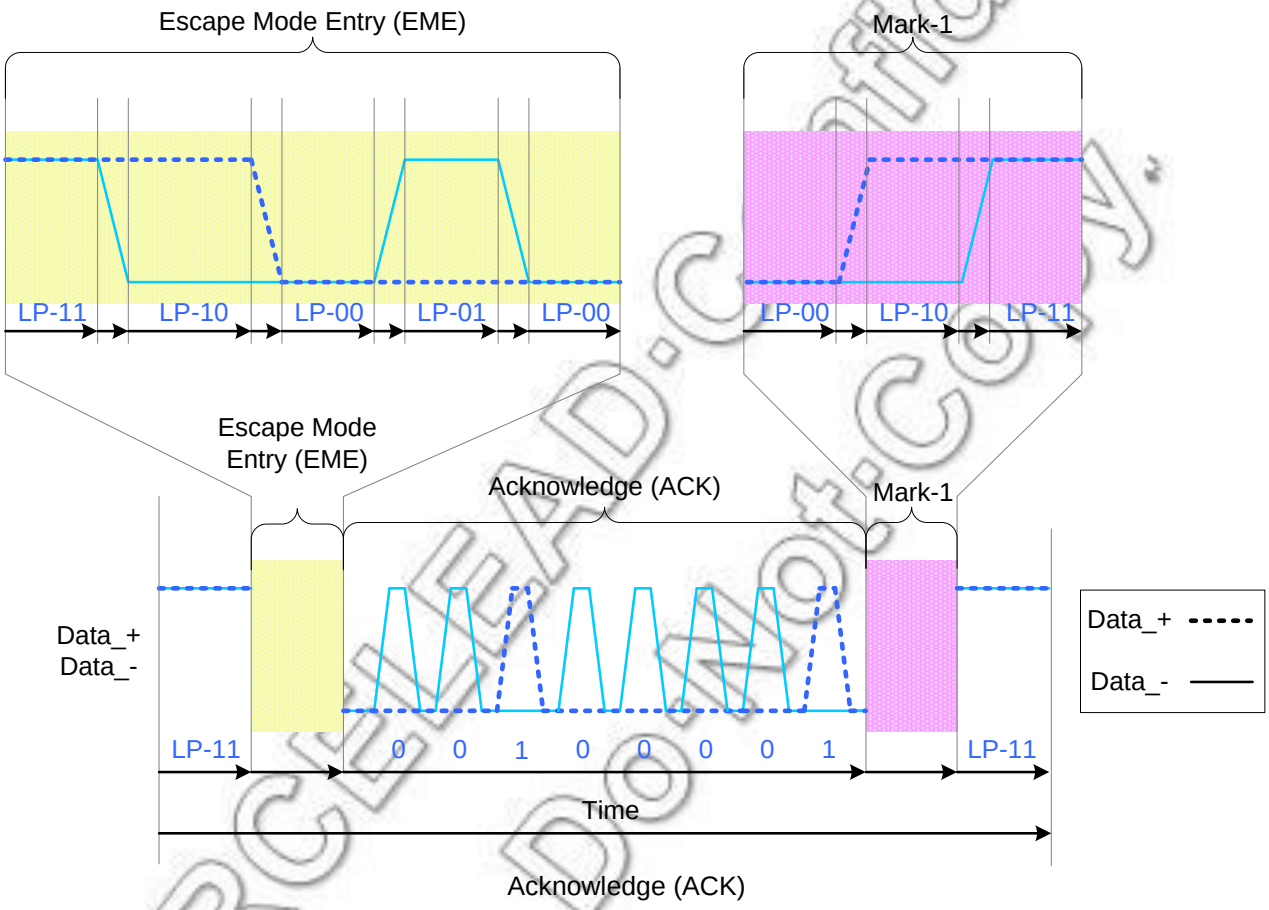
Acknowledge(ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



High Speed Data Transmission (HSDP)

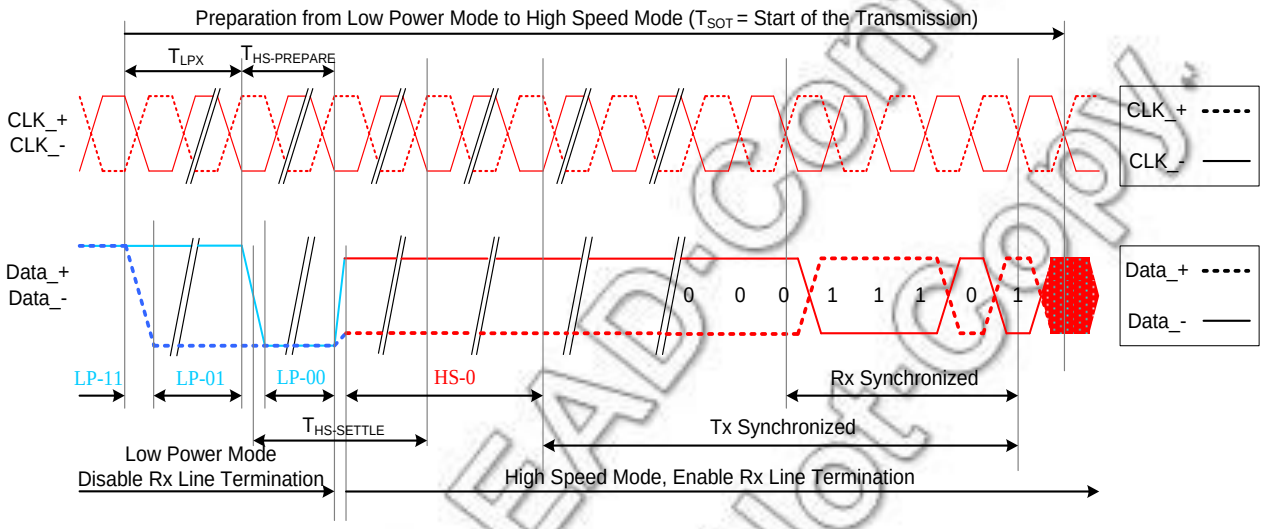
- **Entering High-Speed Data Transmission (T_{SOT} of HSDT)**

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes of the display module are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below



Entering High-Speed Data transmission (TSOT of HSDT)

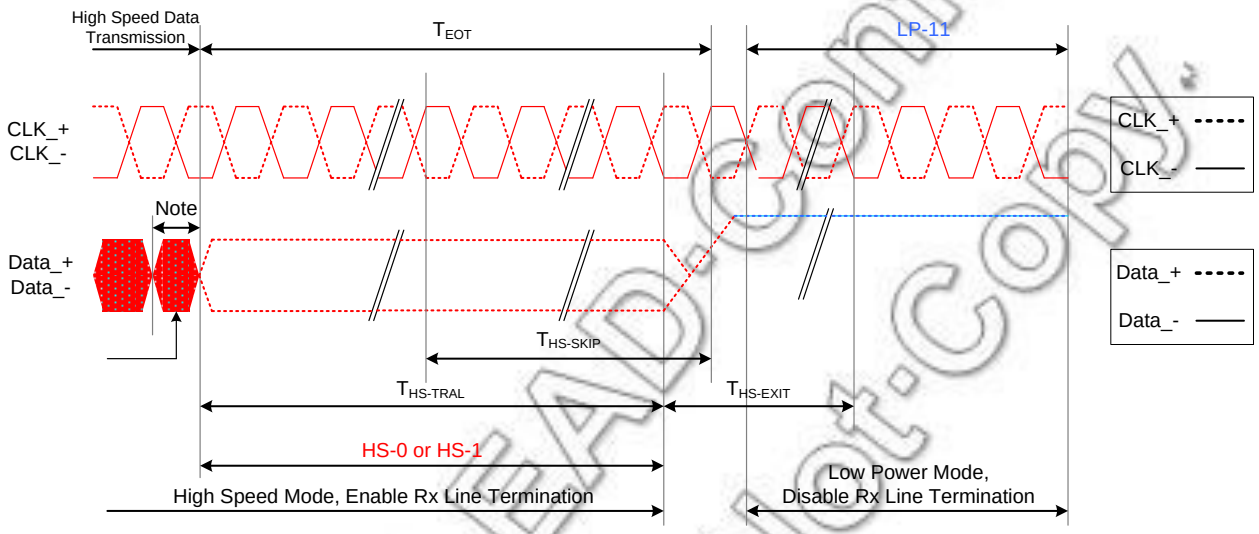
- **Leaving High-Speed Data Transmission (TSOT of HSDT)**

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode.

Data lanes of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

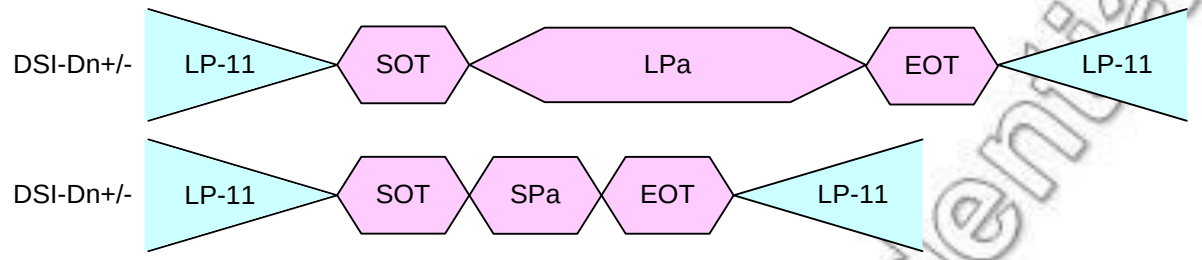


Leaving High-Speed data Transmission (TEOT of HSDT)

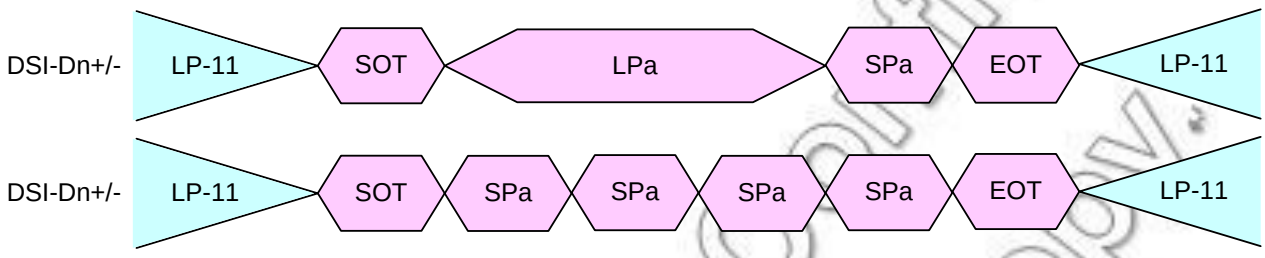
- **Burst of the High-Speed Data Transmission(HSDT)**

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets.

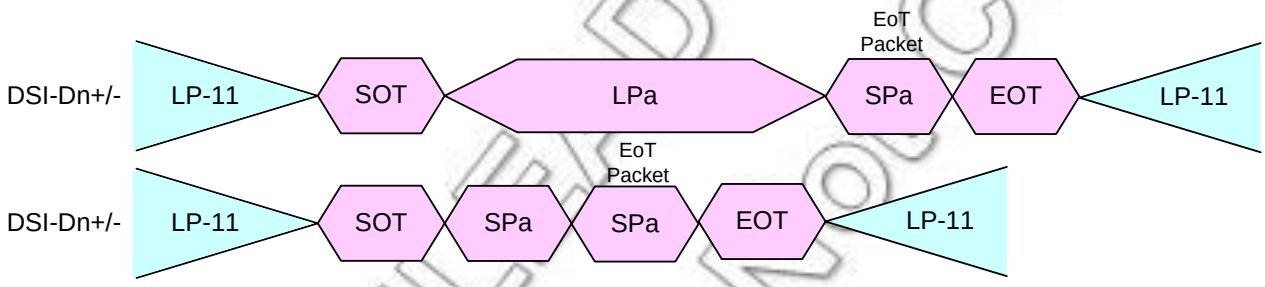
These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.



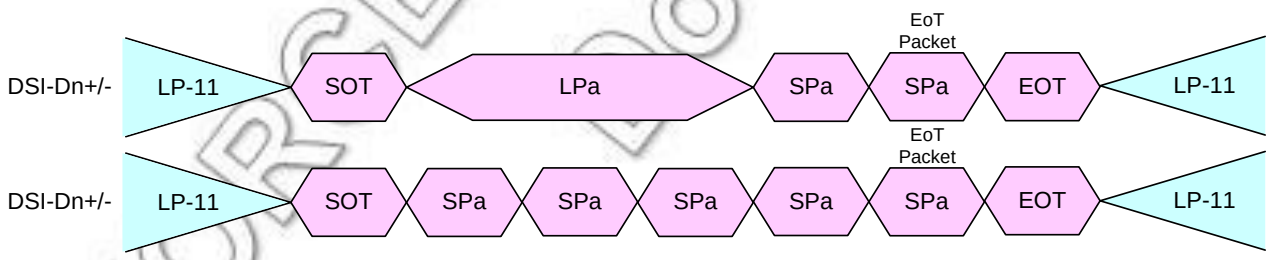
Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission



Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are'1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

- **Bus Turnaround(BTA)**

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

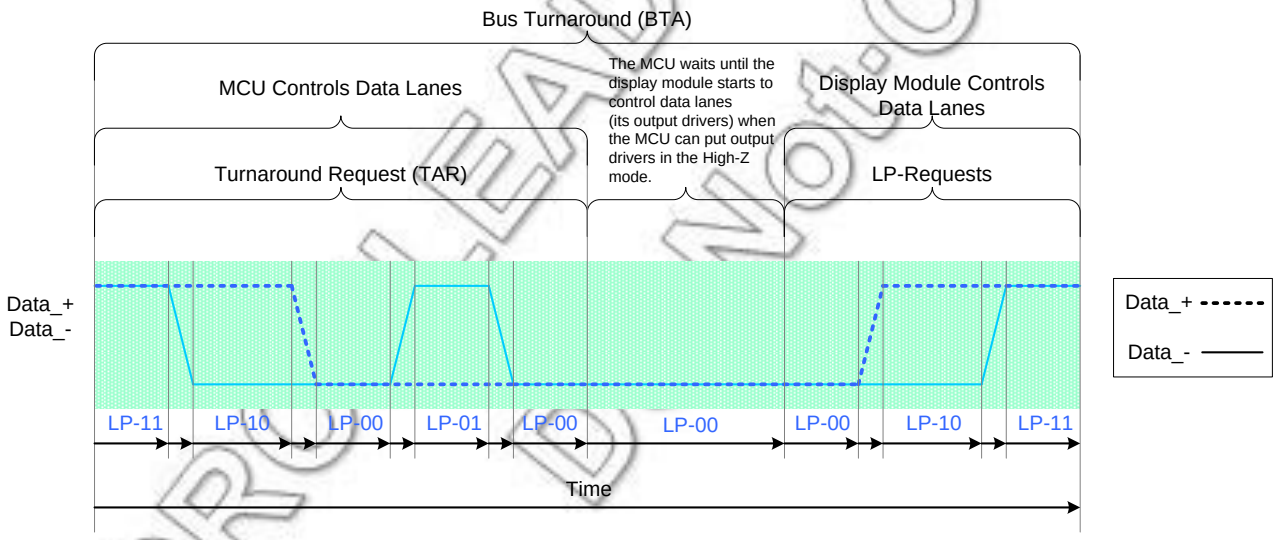
• Start (MCU):LP-11

• Turnaround Request (MCU): LP-11 _ LP-10 _ LP-00 _ LP-10 _ LP-00

• The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)

• The display module changes to the stop mode: LP-00 _ LP-10 _ LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.



Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU.

5.2.4.3 DCS Packet Level Communication

Short Packet (SPA) and Long Packet (LPA) Structure

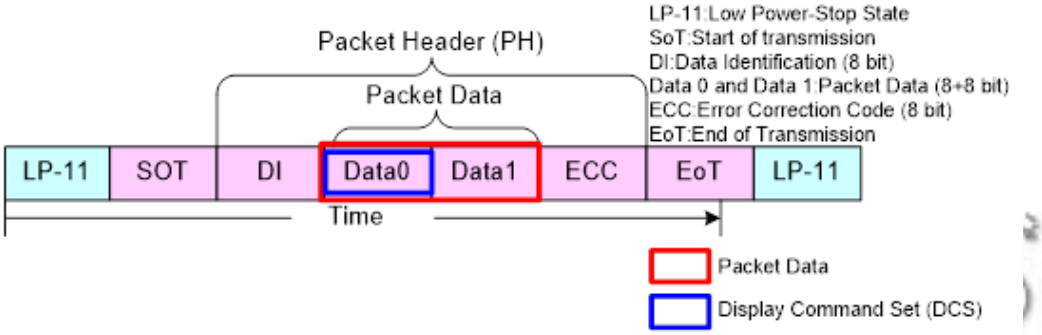
Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

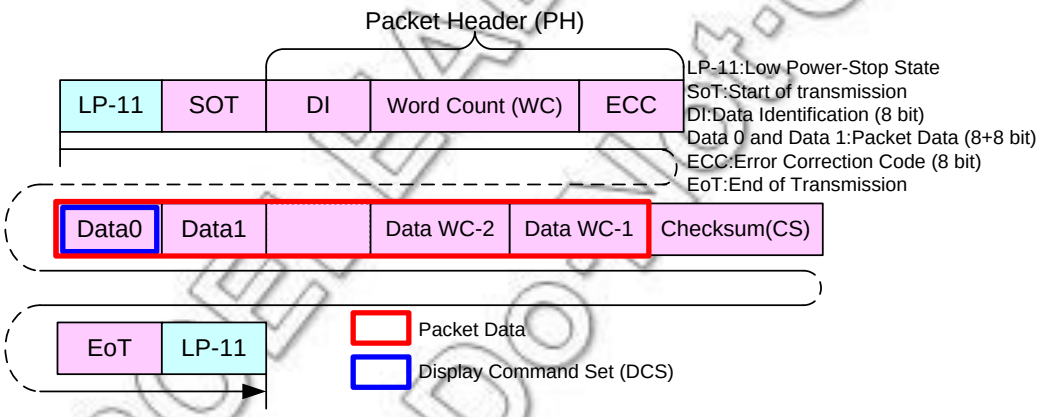
- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

Short Packet (Spa) Structure:



Long Packet (Spa) Structure:



Note:
Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.
** LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11*
** LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11*
** LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11*

- **Display Command Set (DCS)**

Display Command Set (DCS) is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa).

- **Data Identification(DI)**

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

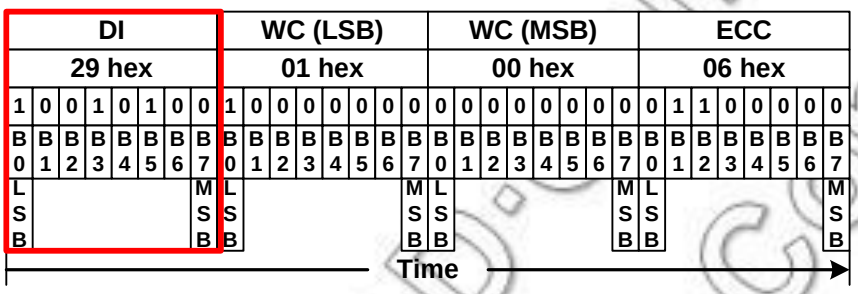
• Virtual Channel (VC), 2 bits, DI[7...6]

• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Data Identification (DI) Structure



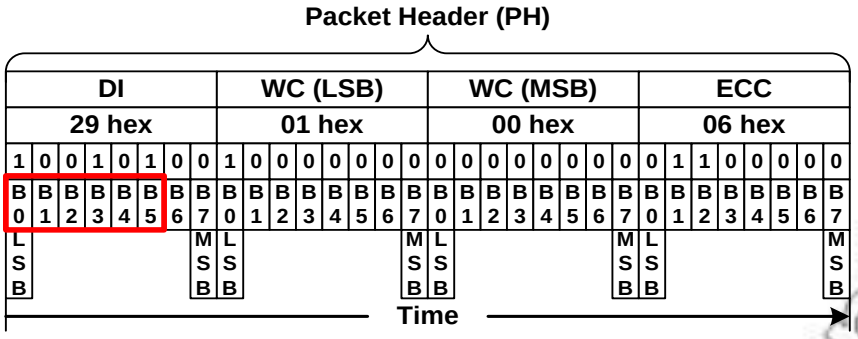
Data Identification (DI) on the Packet Header(PH)

- **Virtual Channel (VC)**

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the HOST. The FL11280 supports Virtual Channel only when VC = 00.

- **Data Type(DT)**

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.
Bits of the Data Type (DT) are illustrated for reference purposes below.



Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type	Data Type	Description	Packet
01h	00 0001	Sync Event, V Sync Start.	Short
11h	01 0001	Sync Event, V Sync End.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
31h	11 0001	Sync Event, H Sync End.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write. (LP only)	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB,5-6-5 Format.	Long
2Eh	10 1110	Loosely Packed Pixel Stream,18-bit RGB,6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long
X0h and xFh, unspecified	xx 0000 xx 1111	Do not use All unspecified codes are reserved	

Data Type (DT) from MCU to the Display Module (or Other Devices)

From the Display Module (or Other Devices) to the MCU									
Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER
1Ah	0	1	1	0	1	0	Generic Read Long Response	Short	GENRR-L
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2_S

Data Type (DT) from the Display Module (or Other Devices) to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

- **Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)**

“Generic Write, 2 Parameter” (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module.

- **Generic Write Long (GENW-L) , Data Type = 10 1001 (29h)**

“Generic Write Long” (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 101001b), from the MCU to the display module.

- **Generic Read , 1 Parameter (GENR1-S) , Data Type = 01 0100 (14h)**

“Generic Read, 1 Parameter (GENR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT,01 0100b), from the MCU to the display module.

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module.

- **Display Command Set (DCS) Write, No Parameter (DCSWN-S) , Data Type = 00 0101 (05h)**

“Display Command Set (DCS) Write, No Parameter” is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module.

- **Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) , Data Type = 01 0101 (15h)**

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module.

- **Display Command Set (DCS) Read, No Parameter (DCSRN-S), Data Type = 00 0110 (06h)**

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module.

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module.

- **Null Packet, No Data (NP-L) , Data Type = 00 1001 (09h)**

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b),from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending.

- **End of Transmission Packet (EoTP), Data Type = 00 1000 (08h)**

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 001000b), from the MCU to the display module. The purpose of this command is terminated the high speed mode (HPDT) properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MCU can decide if it want to use the "End of Transmission Packet" (EoTP) or not. The ST7701S has the capability to support both: i.e. If MCU applies the EoTP, it shall report the "DSI Protocol Violation" error when the EoTP is not detected in the high speed (HS). This error reporting can be enable/disable by bit DIS_EoTP_HS of command B100h (page 0).

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Marked-1" (=leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

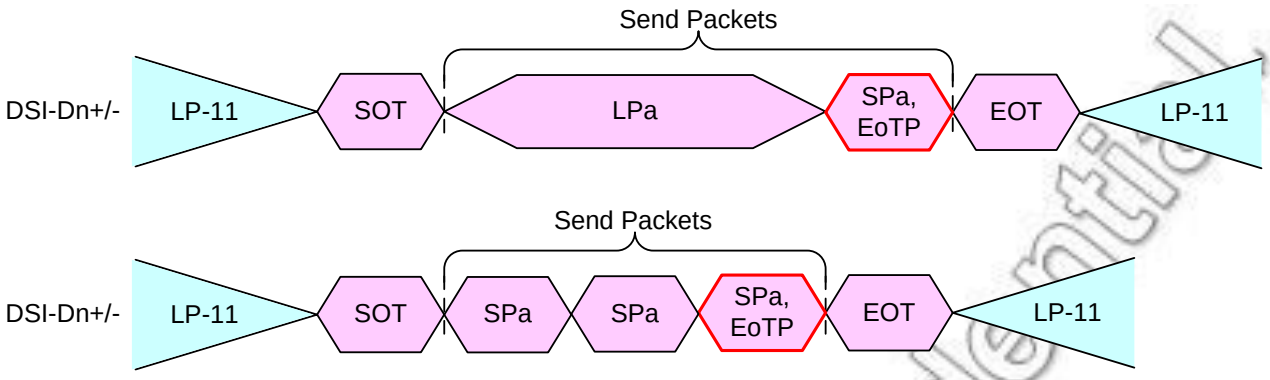
The display module is not allowed to send "End of Transmission Packet" (EoTP) to MCU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Direction	Display Module (DM) in High Speed Data Transmission (HPDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU=>Display Driver	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Driver=>MCU	HS Mode is not available (EoTP is not available)	EoTP can not be sent by the Display Driver

Receiving and Transmitting EoTP during LPDT

Some use case of the “End of Transmission Packet” (EoTP) are illustrated only for reference purpose below.



End of Transmission Packet (EoTP)-Example

- **Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)**

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

• Data Type = 00 0001 (01h) V Sync Start • Data Type = 01 0001 (11h) V Sync End

• Data Type = 10 0001 (21h) H Sync Start • Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

- **Color Mode On Command, and, Data Type = 01 0010 (12h)**

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

- **Color Mode Off Command, Data Type = 00 0010 (02h)**

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

- **Shutdown Peripheral Command, Data Type = 10 0010 (22h)**

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

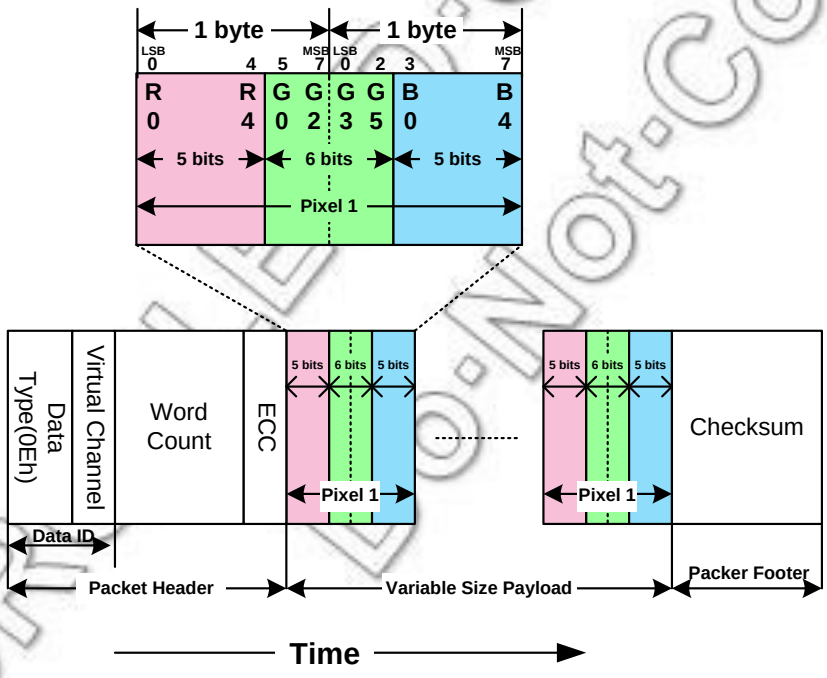
- **Turn On Peripheral Command, Data Type = 11 0010 (32h)**

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

- **Blanking Packet (Long), Data Type = 01 1001 (19h)**

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

- Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)



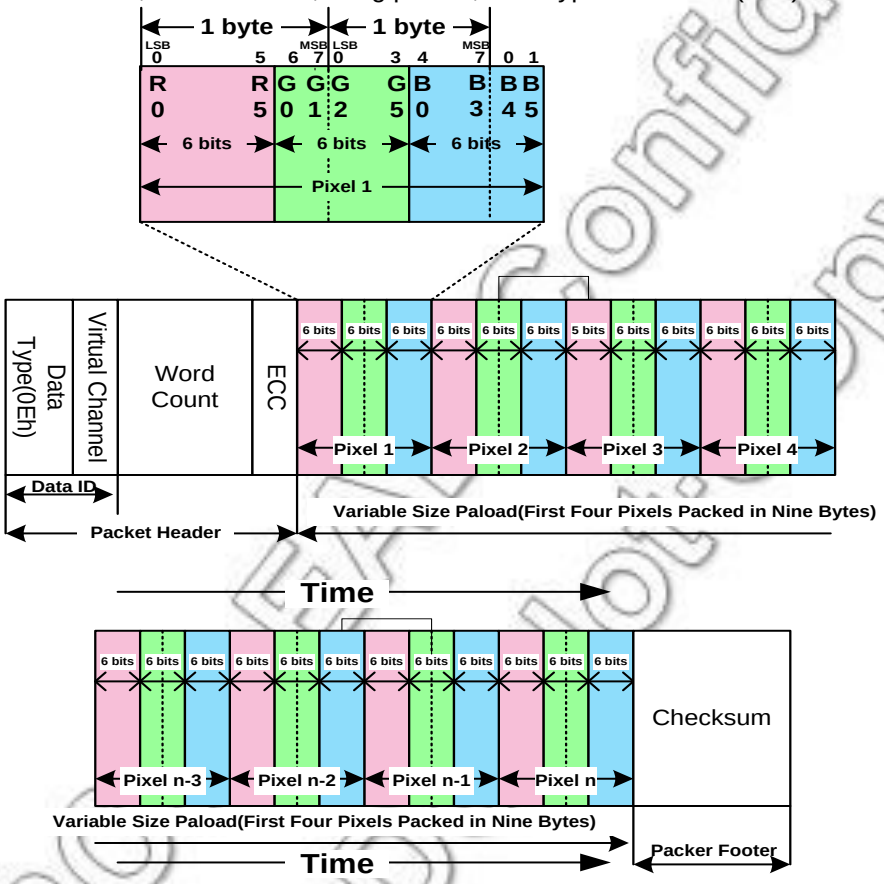
16-bit per Pixel-RGB Color Format, Long packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

- Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)



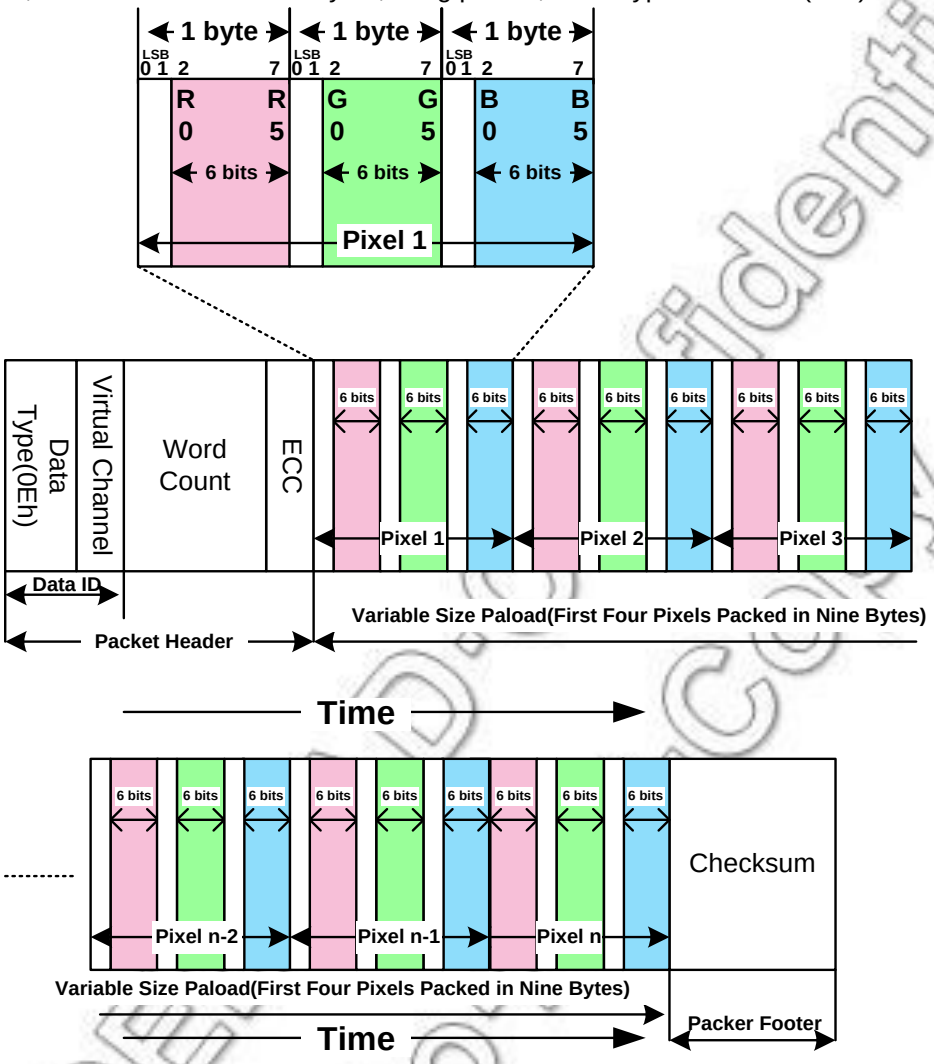
18-bit per Pixel-RGB Color Format, Long pack

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial

bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device

- Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)



18-bit per Pixel (Loosely Packed)-RGB Color Format, Long pack

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

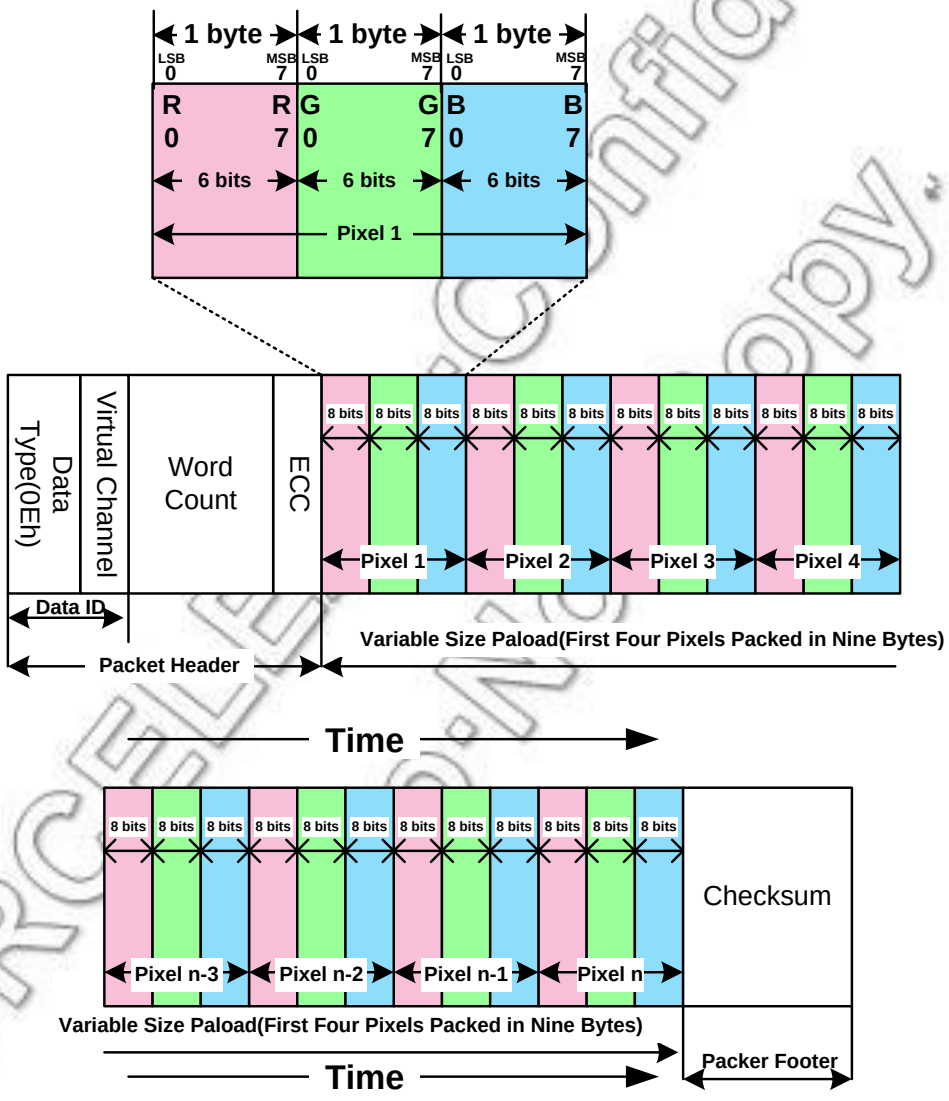
This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

- **Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)**

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.



24-bit per Pixel -RGB Color Format, Long packet

Packet From the Display Module To the MCU

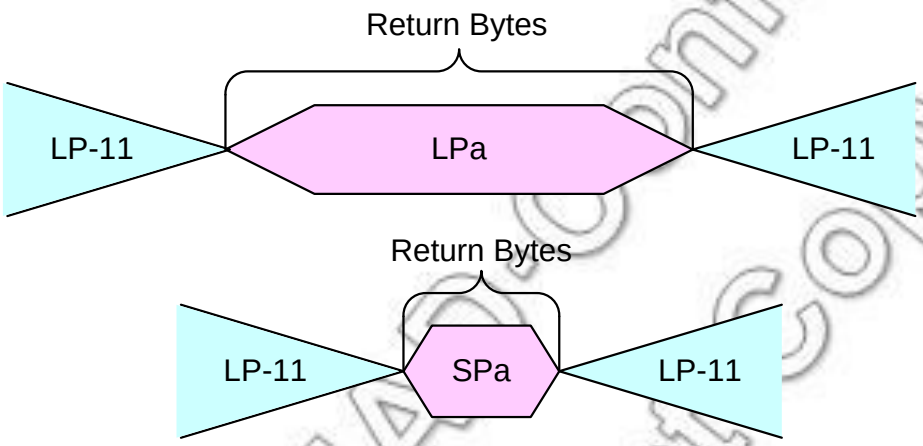
- **Used Packet Types**

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) Read, No Parameter", (DCSRN-S)) or an Acknowledge with Error Report .The used packet type is defined on Data Type (DT).

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.

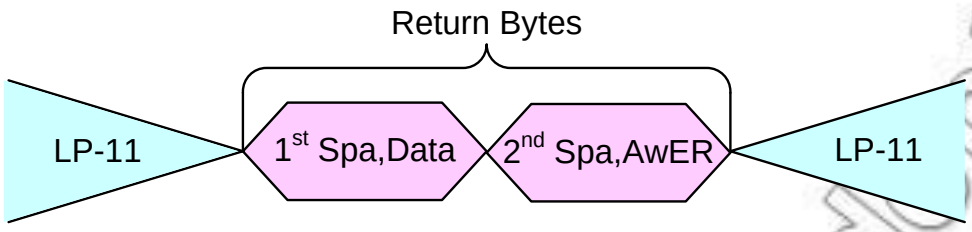


Return Bytes on Signal Packet

From the Display Module (or Other Devices) to the MCU									
Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER
1Ah	0	1	1	0	1	0	Generic Read Long Response	Short	GENRR-L
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2_S

Data Type for Display Module-sourced Packets

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” where has been detected and corrected a single bit error by the EEC (See bit 8 on Table” Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”). This return packets are illustrated for reference purpose below.



Exception When Return Bytes on Several Packet

AwER=Acknowledge with Error Report

- **Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)**

“Acknowledge with Error Report” (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

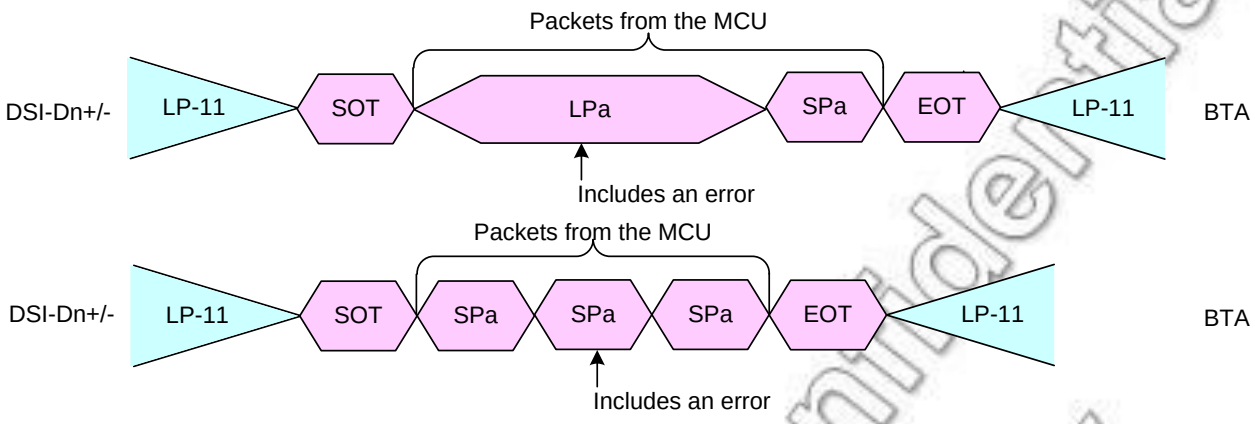
The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to ‘1’,as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

Acknowledge with Error Report (AwER) for Response

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA).Some examples are illustrated below for reference purpose.



Error Packet

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)”commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.

- **Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)**

“Generic Read Long Response” (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. “Generic Read Long Response” (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

- **DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)**

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. “DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

- **DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)**

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

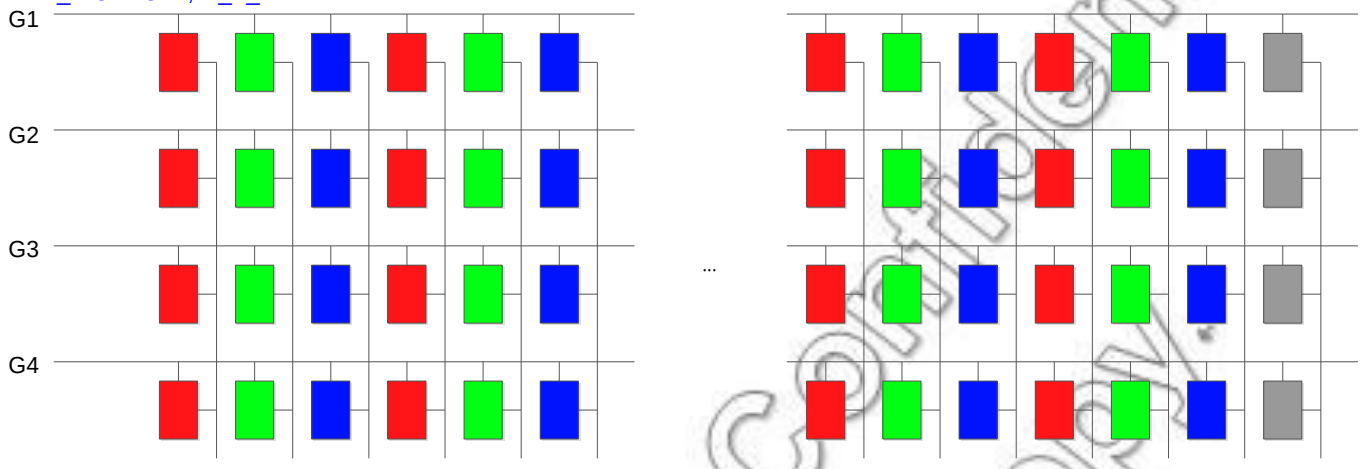
5.3 Panel Application

5.3.1 Single Gate Panel Configuration

Gate Driver Mode = **Single Gate**	Sub-pixel Direction	Sub-pixel Arrangement
(Reg.) STRIPE_EN=H, SG_TYPE[1:0]=LH LTPS_EN=L, H_INV=L, DZS[1 :0]=LL	Stripe	**(1) Normal Arrangement**
		(2) Zig-Zag Arrangement

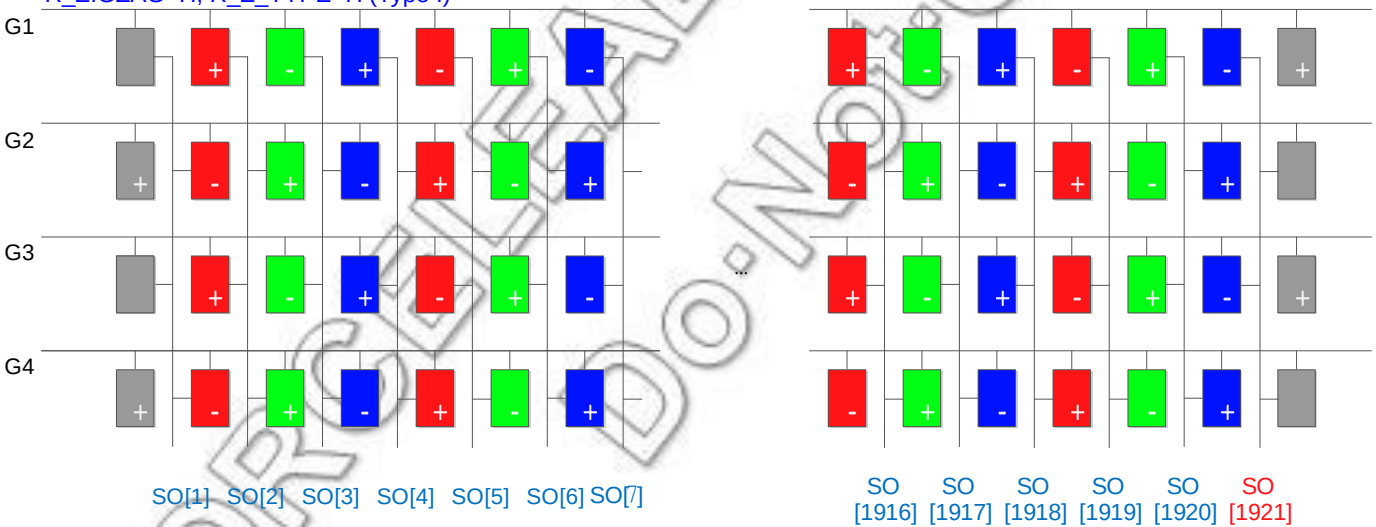
(1). Normal Arrangement

R_ZIGZAG=L, R_Z_TYPE=X



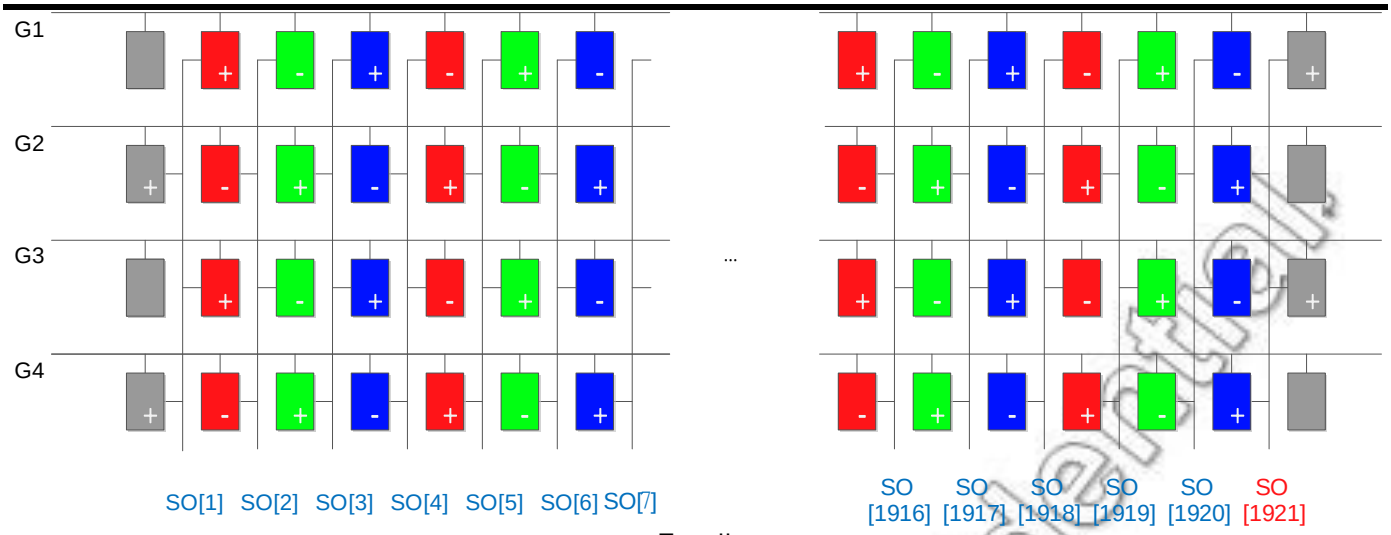
(2). Zig-Zag Arrangement

R_ZIGZAG=H, R_Z_TYPE=H (Type I)



Type I

R_ZIGZAG=H, R_Z_TYPE=L (Type II)



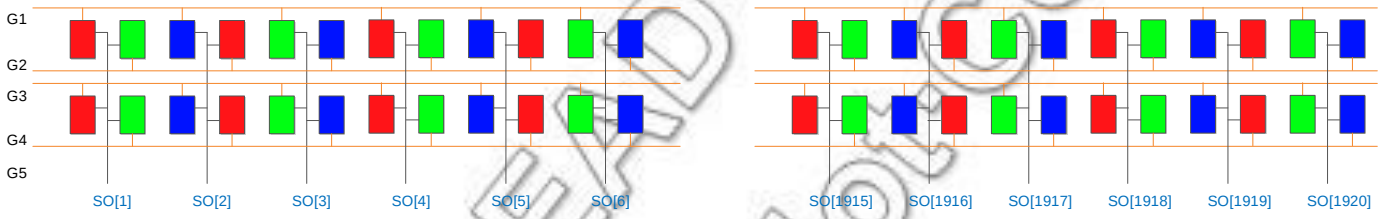
Type II

5.3.2 Dual Gate Panel Configuration

Gate Driver Mode = **Dual Gate**	Sub-pixel Direction	Sub-pixel Arrangement
(Reg.) STRIPE_EN=H, SG_TYPE[1:0]=HL LTPS_EN=L,	Stripe	**(1) Normal Arrangement**
		(2) Zig-Zag Arrangement

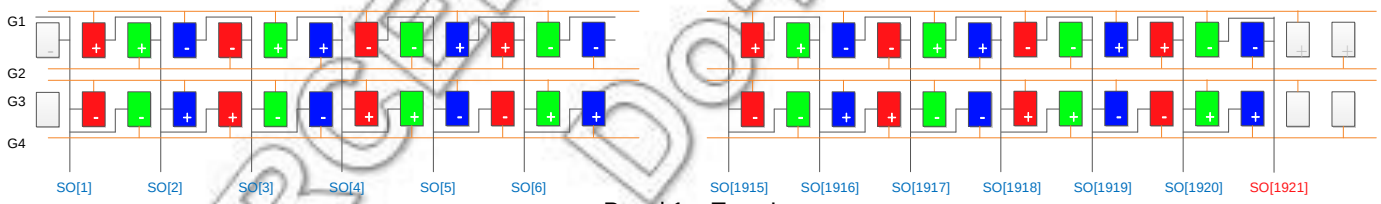
(1). Normal Arrangement

R_ZIGZAG=L, R_Z_TYPE=X, R_H_INV=L, R_DZS[1:0]=LL



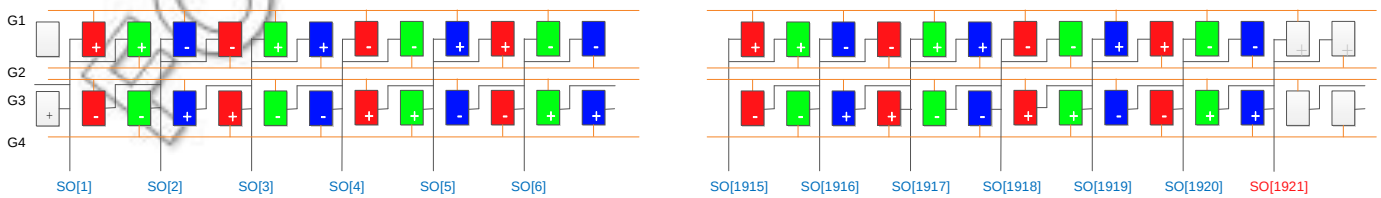
(2). Zig-Zag Arrangement

R_ZIGZAG=H, R_Z_TYPE=H, R_H_INV=H, R_DZS[1:0]=HH (Panel 1 – Type I)



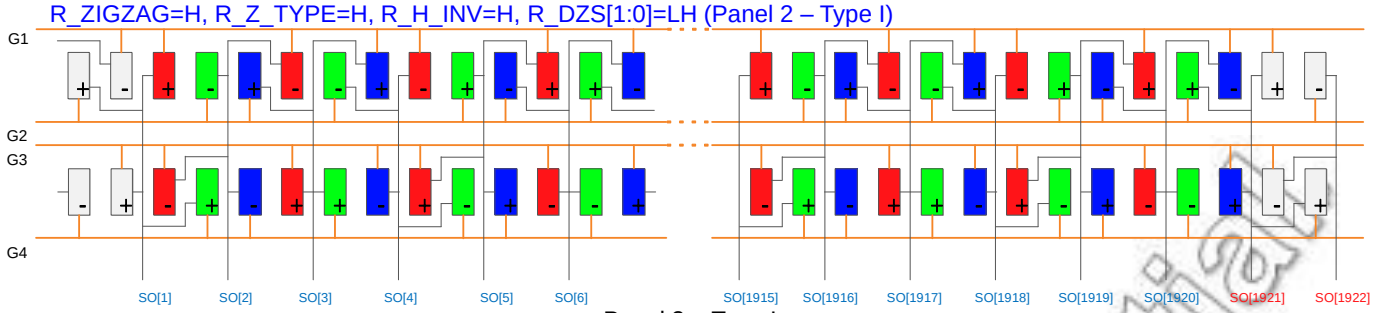
Panel 1 – Type I

R_ZIGZAG=H, R_Z_TYPE=L, R_H_INV=H, R_DZS[1:0]=HH (Panel 1 – Type II)



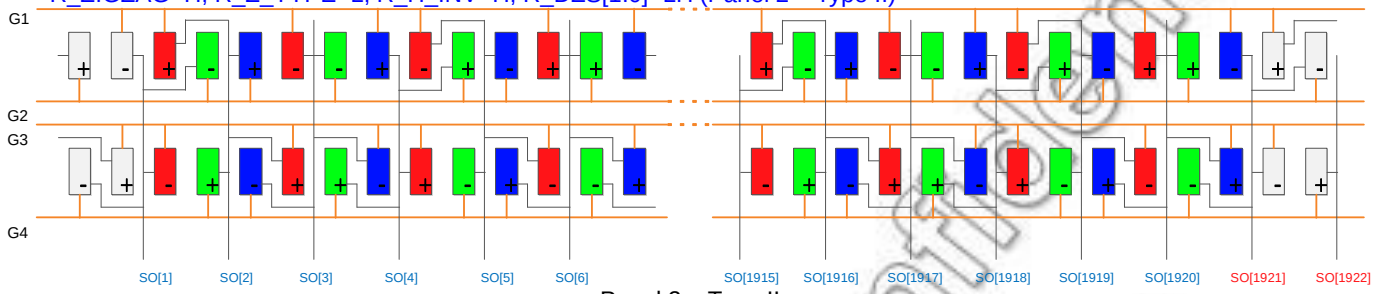
Panel 1 – Type II

R_ZIGZAG=H, R_Z_TYPE=H, R_H_INV=H, R_DZS[1:0]=LH (Panel 2 – Type I)



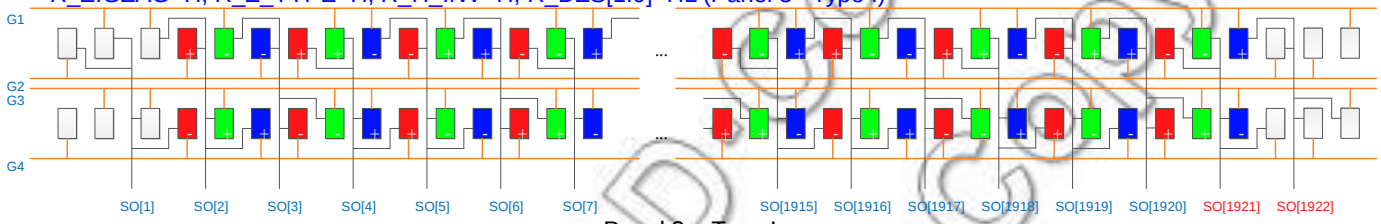
Panel 2 – Type I

R_ZIGZAG=H, R_Z_TYPE=L, R_H_INV=H, R_DZS[1:0]=LH (Panel 2 – Type II)



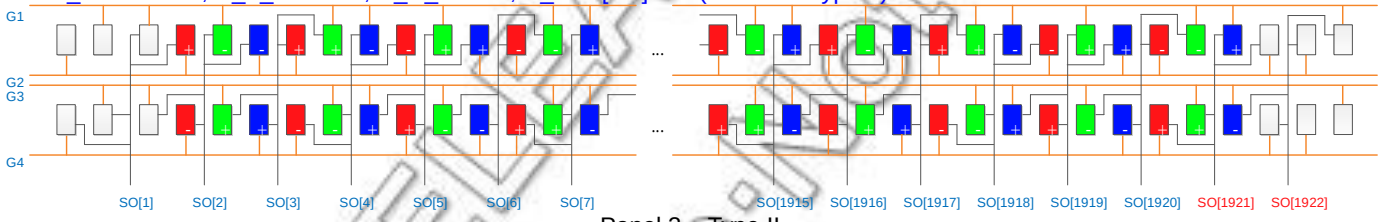
Panel 2 – Type II

R_ZIGZAG=H, R_Z_TYPE=H, R_H_INV=H, R_DZS[1:0]=HL (Panel 3– Type I)



Panel 3 – Type I

R_ZIGZAG=H, R_Z_TYPE=L, R_H_INV=H, R_DZS[1:0]=HL (Panel 3– Type II)



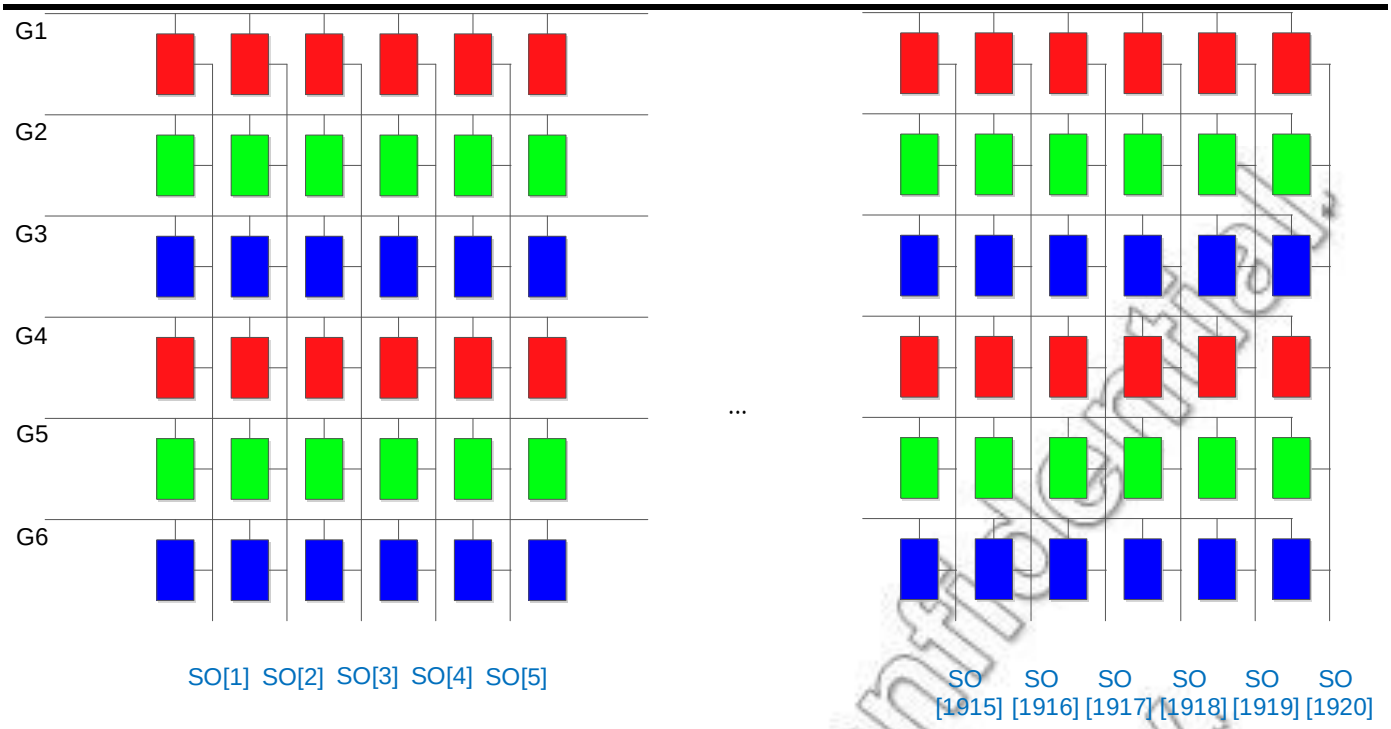
Panel 3 – Type II

5.3.3 Triple Gate Panel Configuration

Gate Driver Mode = **Dual Gate**	Sub-pixel Direction	Sub-pixel Arrangement
(Reg.) STRIPE_EN=L, SG_TYPE[1:0]=HH LTPS_EN=L, DZS[1 :0]=LL	Lateral	**(1) Normal Arrangement**
		(2) Zig-Zag Arrangement

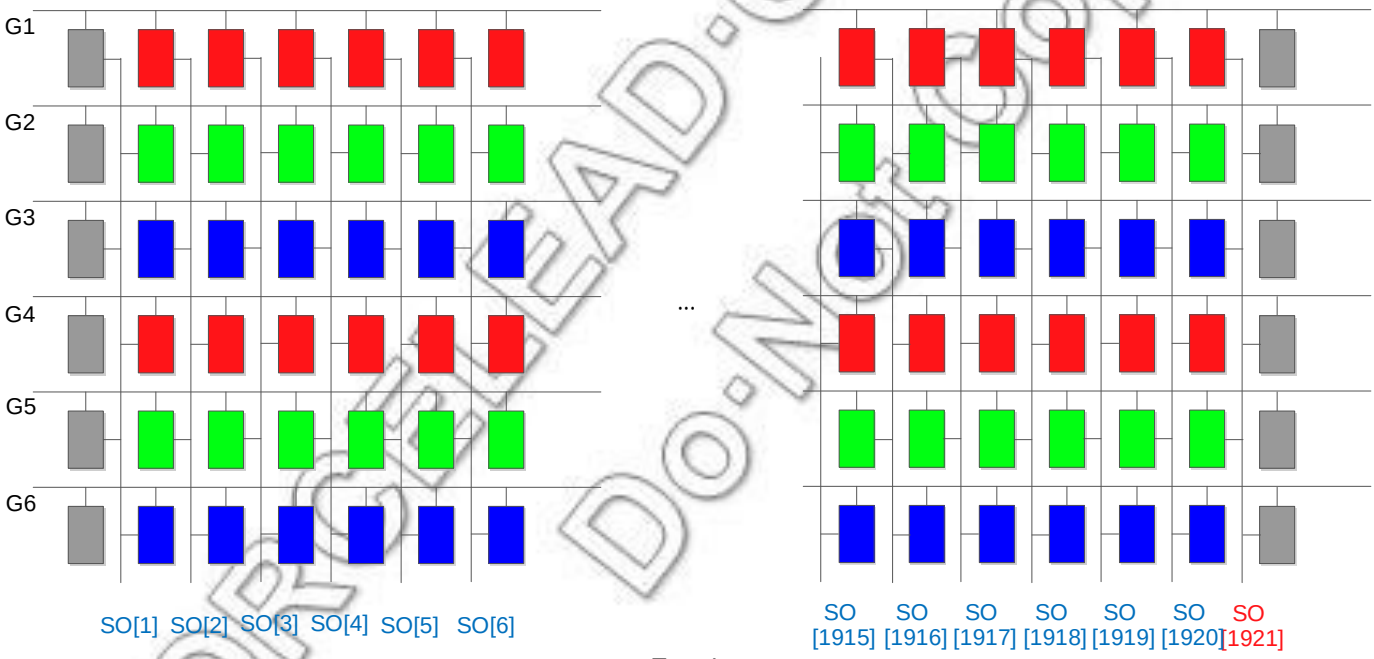
(1). Normal Arrangement

R_ZIGZAG=L, R_Z_TYPE=X, R_H_INV=H or L (L for Inversion type= + + +, - - -)



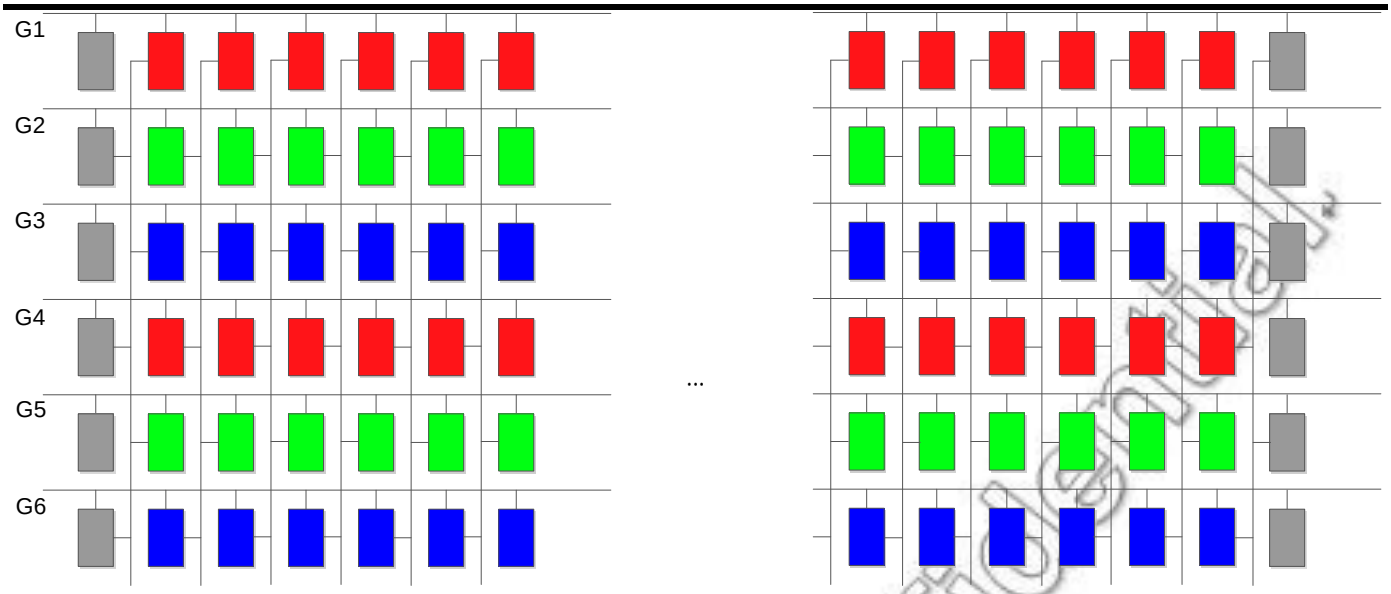
(2). Zig-Zag Arrangement

R_ZIGZAG=H, R_Z_TYPE=H, R_H_INV=H or L (L for Inversion type= + + +, - - -)



Type I

R_ZIGZAG=H, R_Z_TYPE=L, R_H_INV=H or L (L for Inversion type= + + +, - - -)



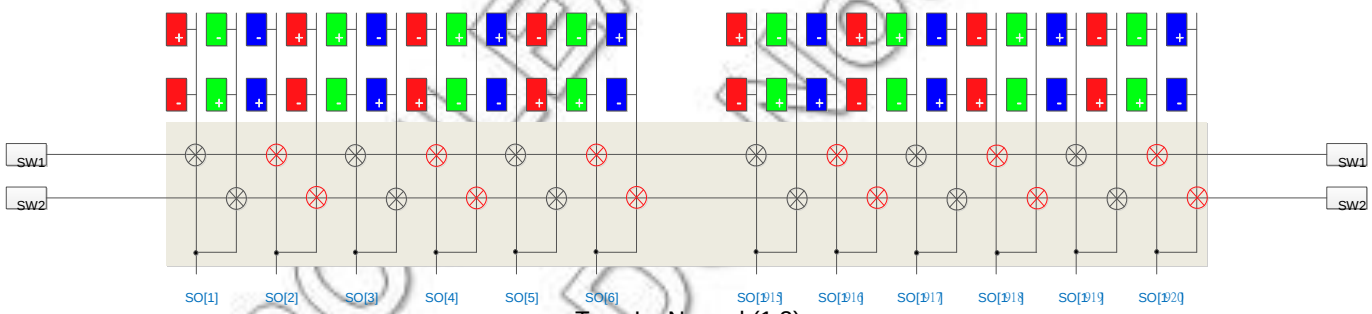
Type II

5.3.4 LTPS GIP 2 MUX Panel Configuration

LTPS GIP Panel Mode = **2 Mux**	Sub-pixel Direction	Sub-pixel Arrangement
(Reg.) STRIPE_EN=H, SG_TYPE[1:0]=HL LTPS_EN=H, DZS[1 :0]=LL	Stripe	**(1) Normal Arrangement**
		(2) Zig-Zag Arrangement

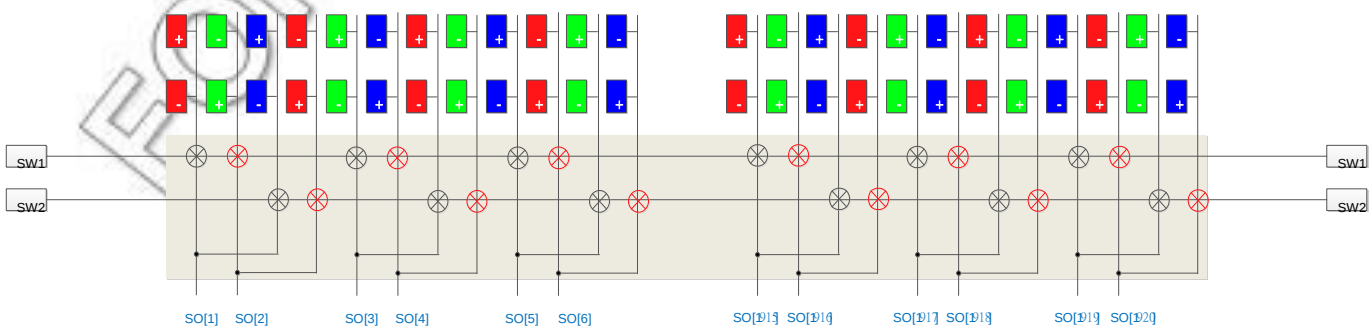
(1). Normal Arrangement

R_ZIGZAG=L, R_Z_TYPE=X, R_LTPS_SW=L, R_H_INV=L



Type I – Normal (1:2)

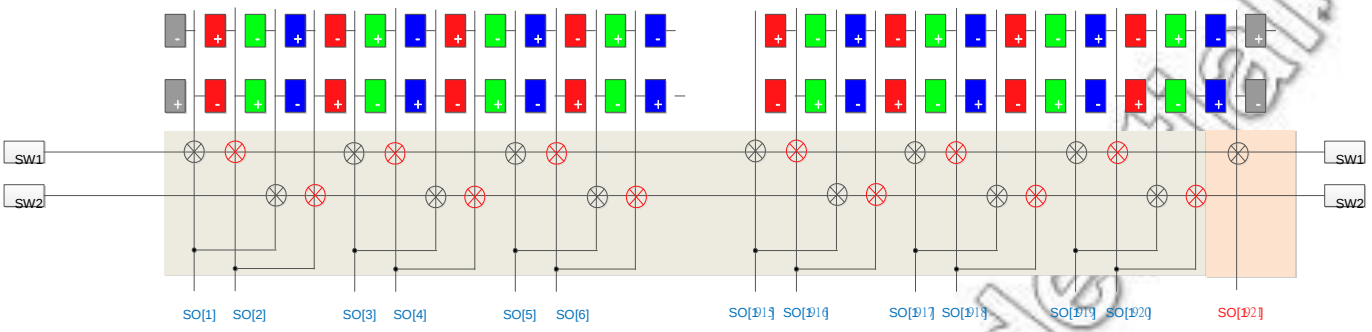
R_ZIGZAG=L, R_Z_TYPE=X, R_LTPS_SW=H, R_H_INV=H



Type II – Swap (2:4)

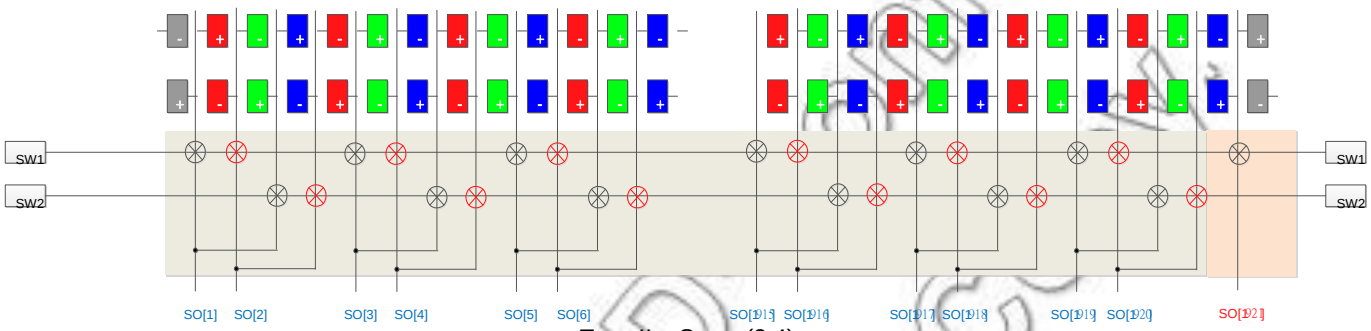
(2). Zig-Zag Arrangement

R_ZIGZAG=H, R_Z_TYPE=H, R_LTPS_SW=H, R_H_INV=H



Type I – Swap (2:4)

R_ZIGZAG=H, R_Z_TYPE=L R_LTPS_SW=H, R_H_INV=H



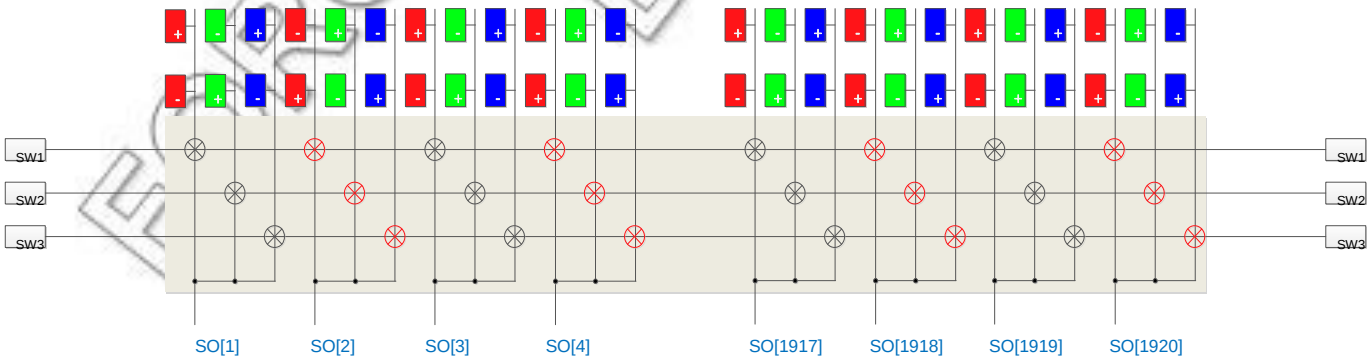
Type II – Swap (2:4)

5.3.5 LTPS GIP 3 MUX Panel Configuration

LTPS GIP Panel Mode = 3 **Mux**	Sub-pixel Direction	Sub-pixel Arrangement
(Reg.) STRIPE_EN=H, SG_TYPE[1:0]=HH LTPS_EN=H, H_INV=L, DZS[1 :0]=LL	Stripe	**(1) Normal Arrangement**
		(2) Zig-Zag Arrangement

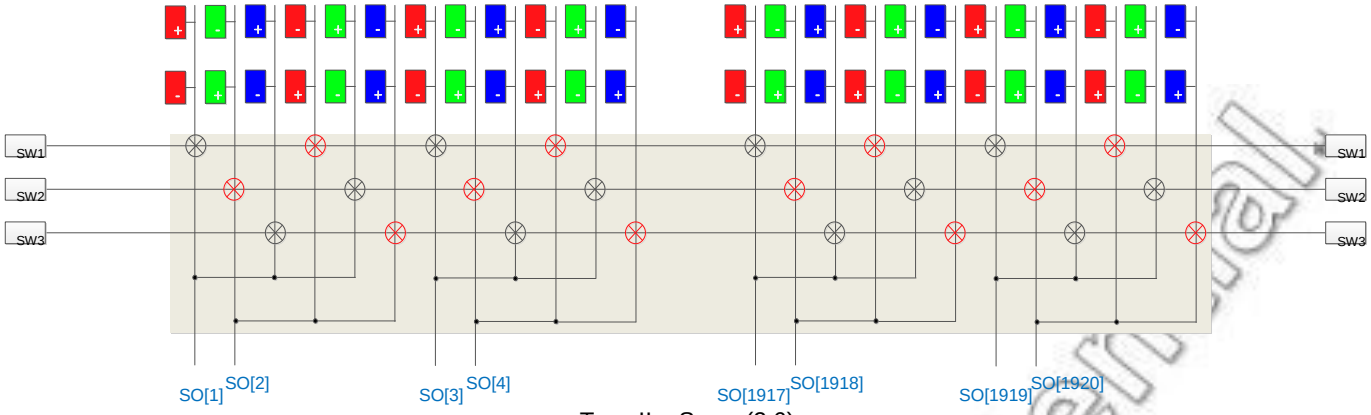
(1). Normal Arrangement

R_ZIGZAG=L, R_Z_TYPE=X, R_LTPS_SW=L



Type I – Normal (1:3)

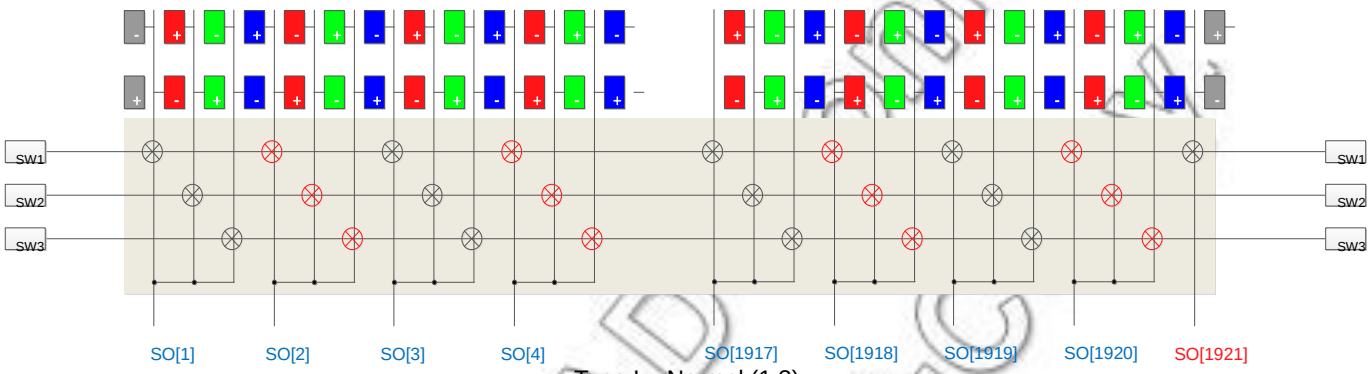
R_ZIGZAG=L, R_Z_TYPE=X, R_LTPS_SW=H



Type II – Swap (2:6)

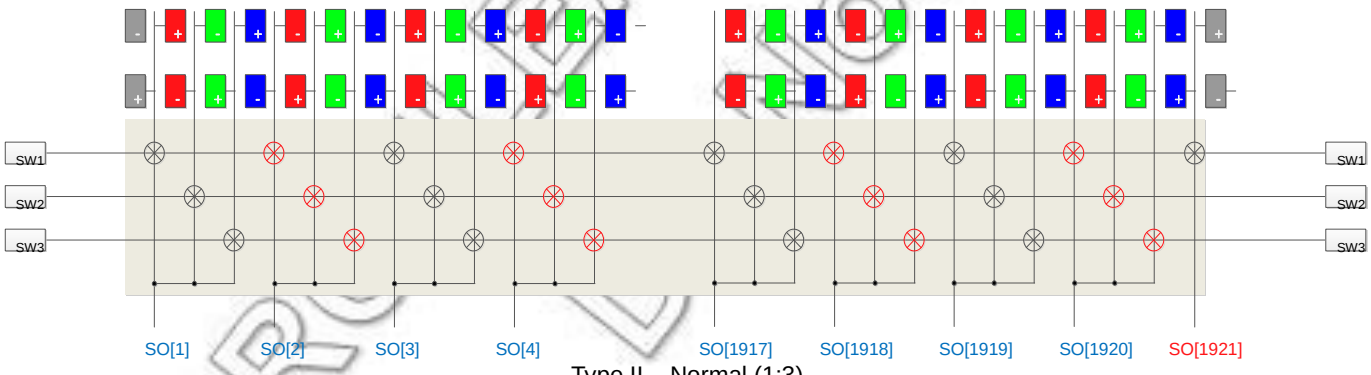
(2). Zig-Zag Arrangement

R_ZIGZAG=H, R_Z_TYPE=H, R_LTPS_SW=L



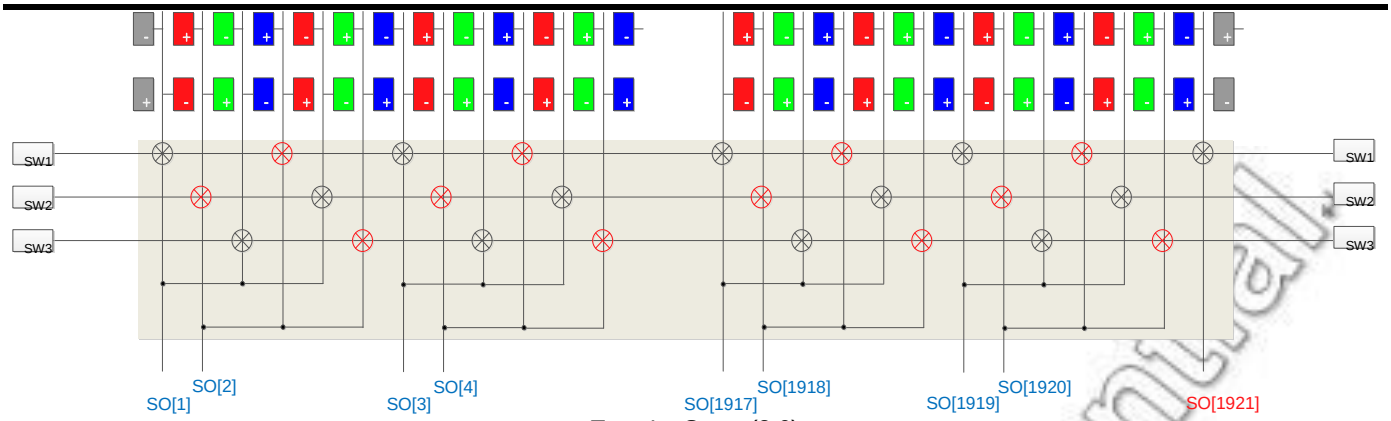
Type I – Normal (1:3)

R_ZIGZAG=H, R_Z_TYPE=L, R_LTPS_SW=L



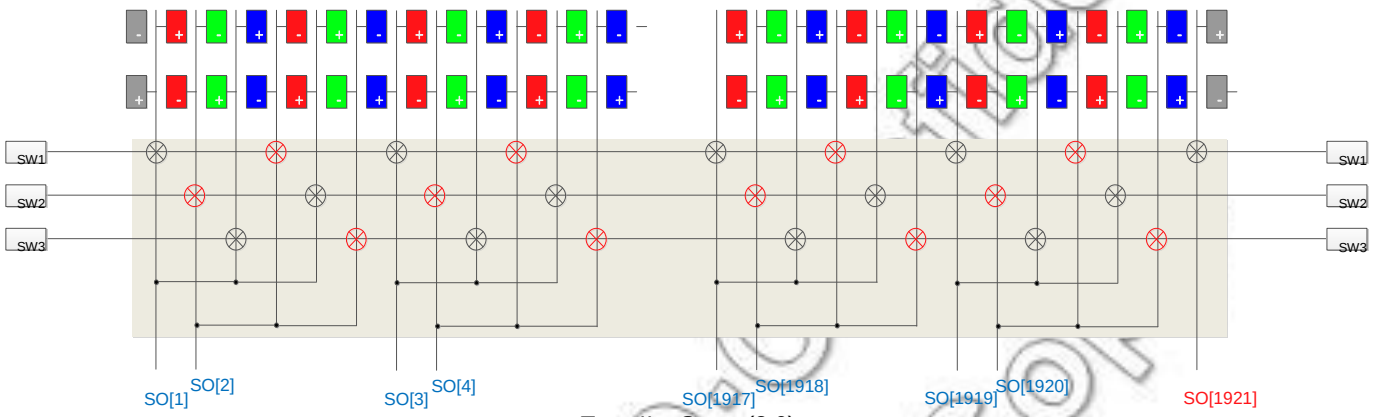
Type II – Normal (1:3)

R_ZIGZAG=H, R_Z_TYPE=H, R_LTPS_SW=H



Type I – Swap (2:6)

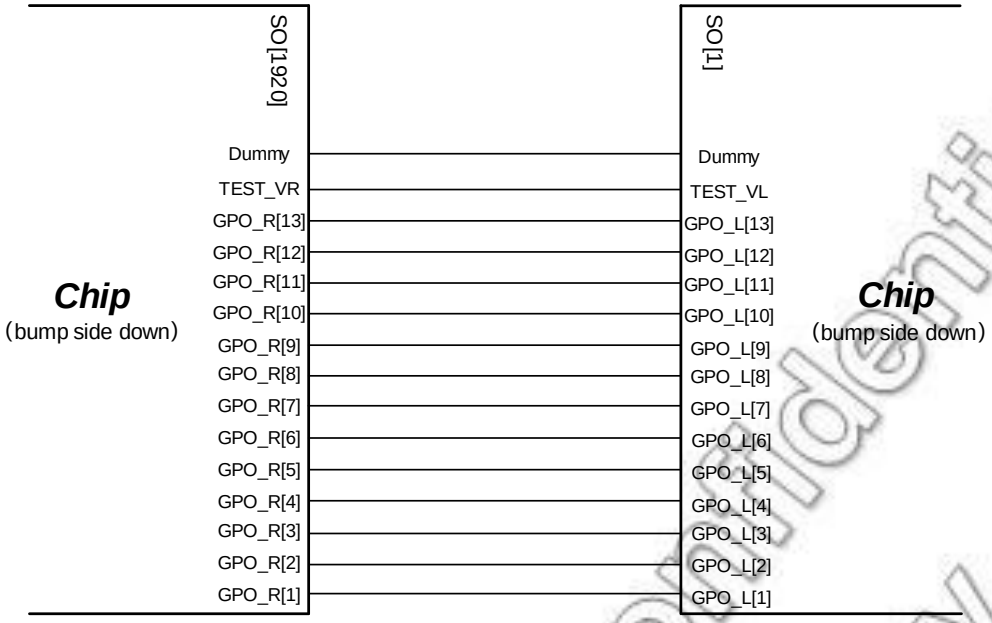
R_ZIGZAG=H, R_Z_TYPE=L, R_LTPS_SW=H



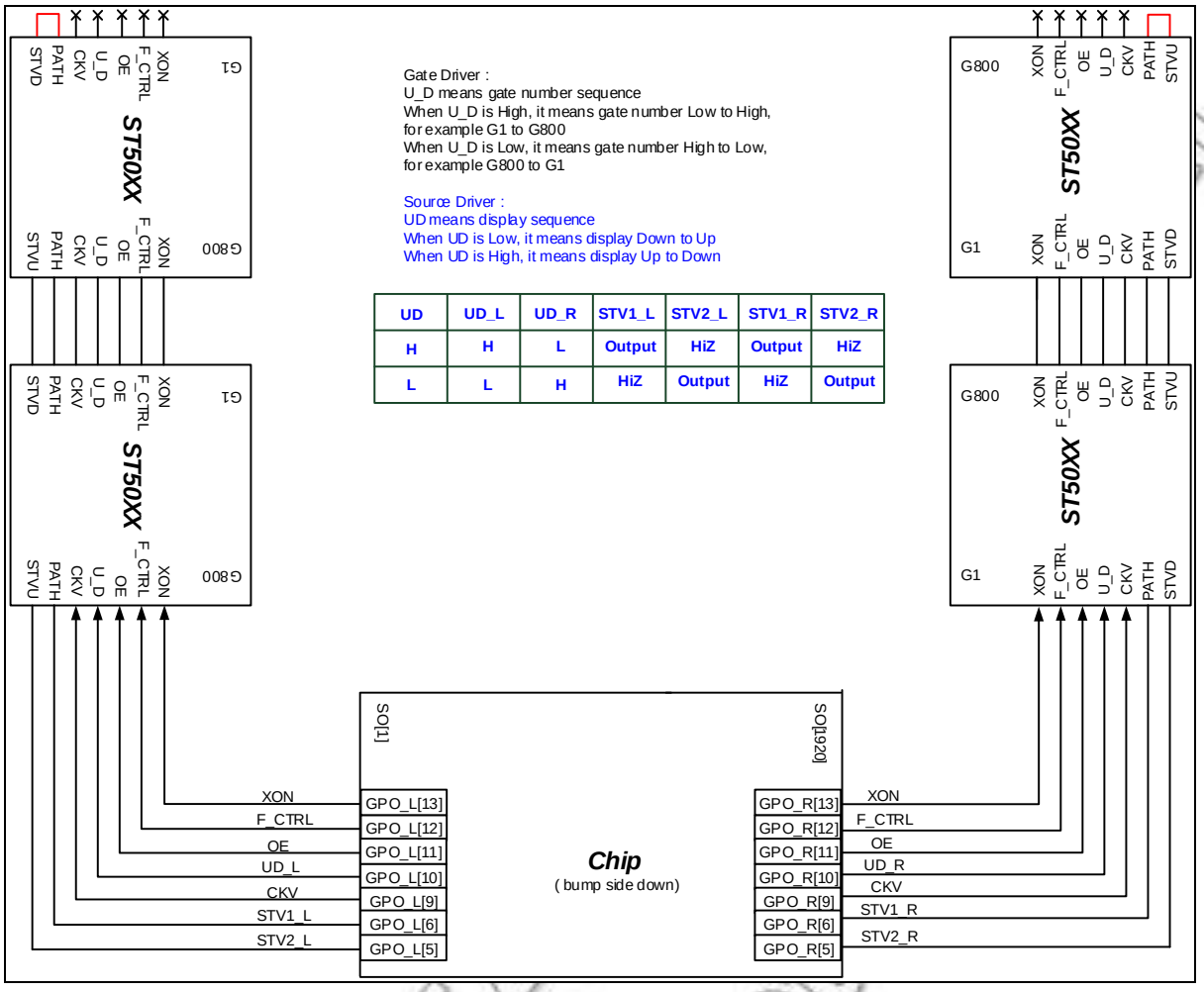
Type II – Swap (2:6)

5.4 Cascade GIP Driving and Gate Driver Driving Connection

5.4.1 Driving with GIP Timing



5.4.2 Driving with External Gate Driver



UD	UD_L	UD_R	STV1_L	STV2_L	STV1_R	STV2_R
H	H	L	Output	HiZ	Output	HiZ
L	L	H	HiZ	Output	HiZ	Output

5.5 Arbitrary Resolution Setting

This chip can be programmed to support arbitrary resolutions, and its input timing supports SYNC or DE mode.

There are some constraints of the utilization of channels. This chip disabled output channels are symmetric from chip center to left and right side. And there are N+2 channels in dual gate + Zig-Zag application, so it would be set to 1922 channels.

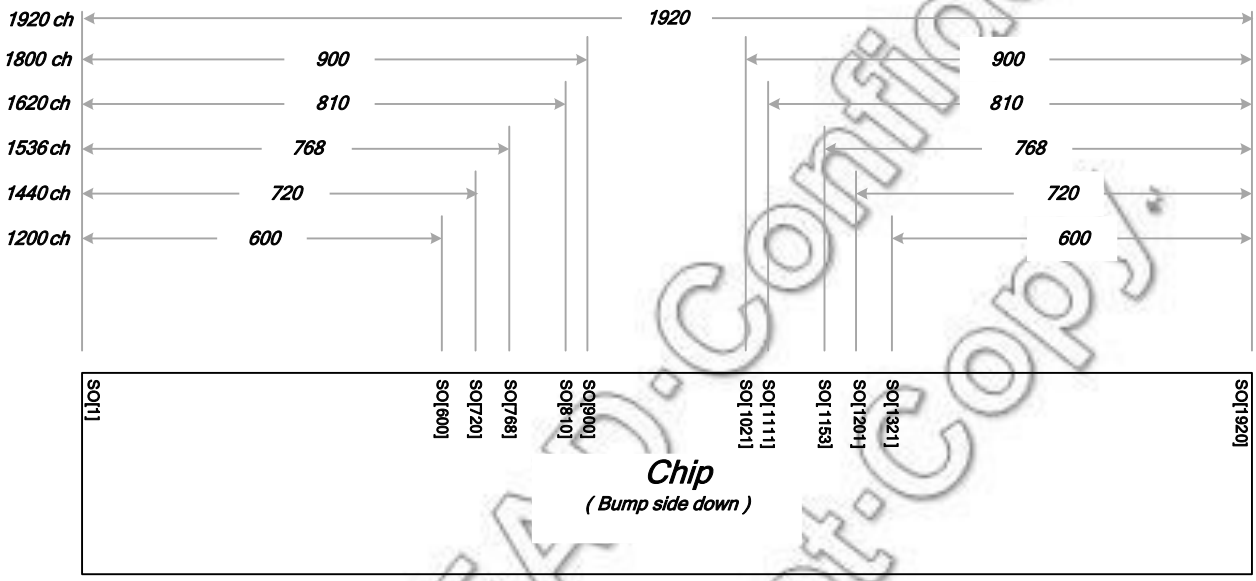
In the case of single gate applications, there are some limitations as below:

(1) Maximum pixel clock rate is 100Mhz.

(2) 172(RGB) ≤ HDISP ≤ 2560(RGB), VDISP ≤ 4000

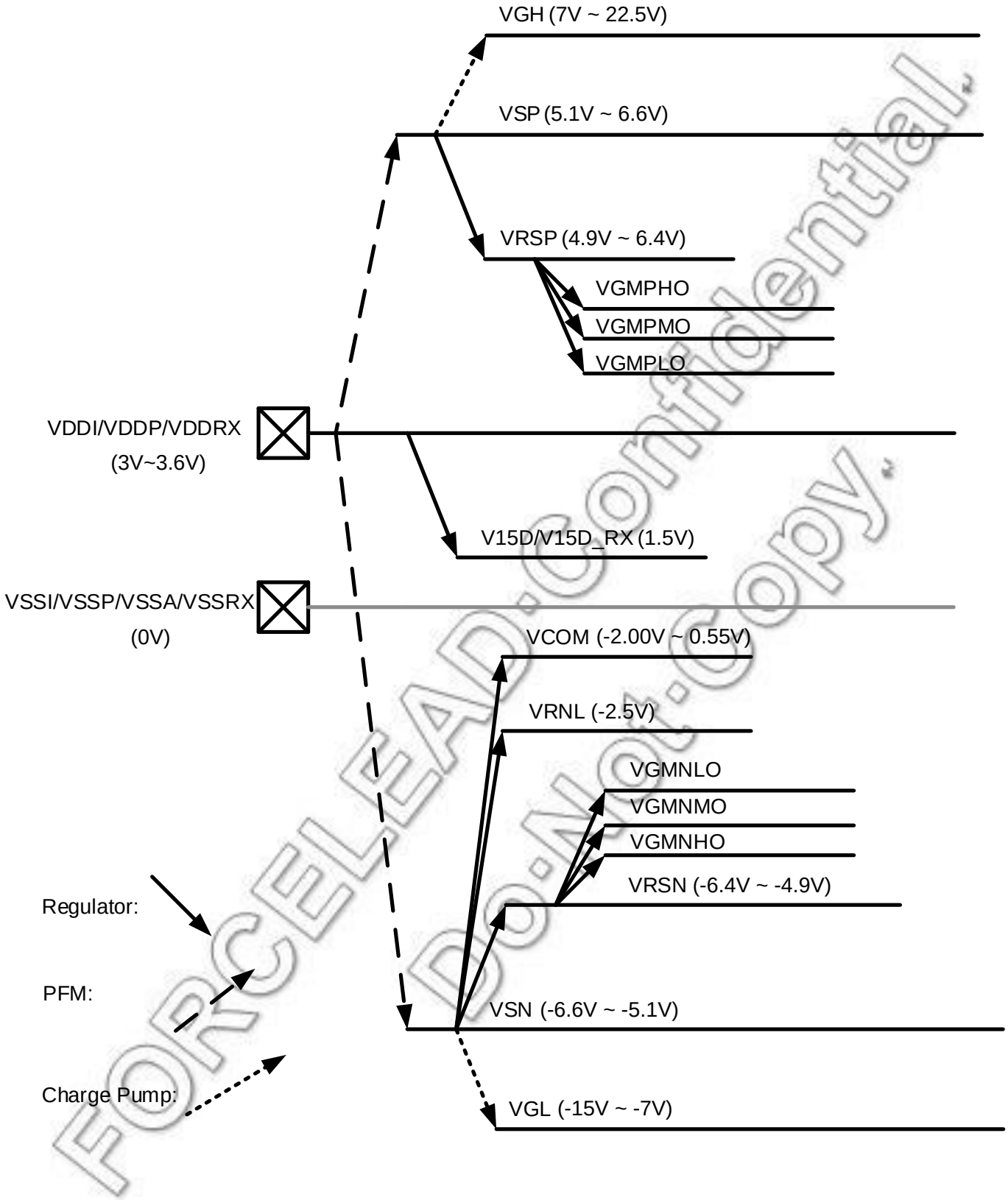
(3) HDISP must set as multiple of 4

(4) VDISP must set as multiple of 2

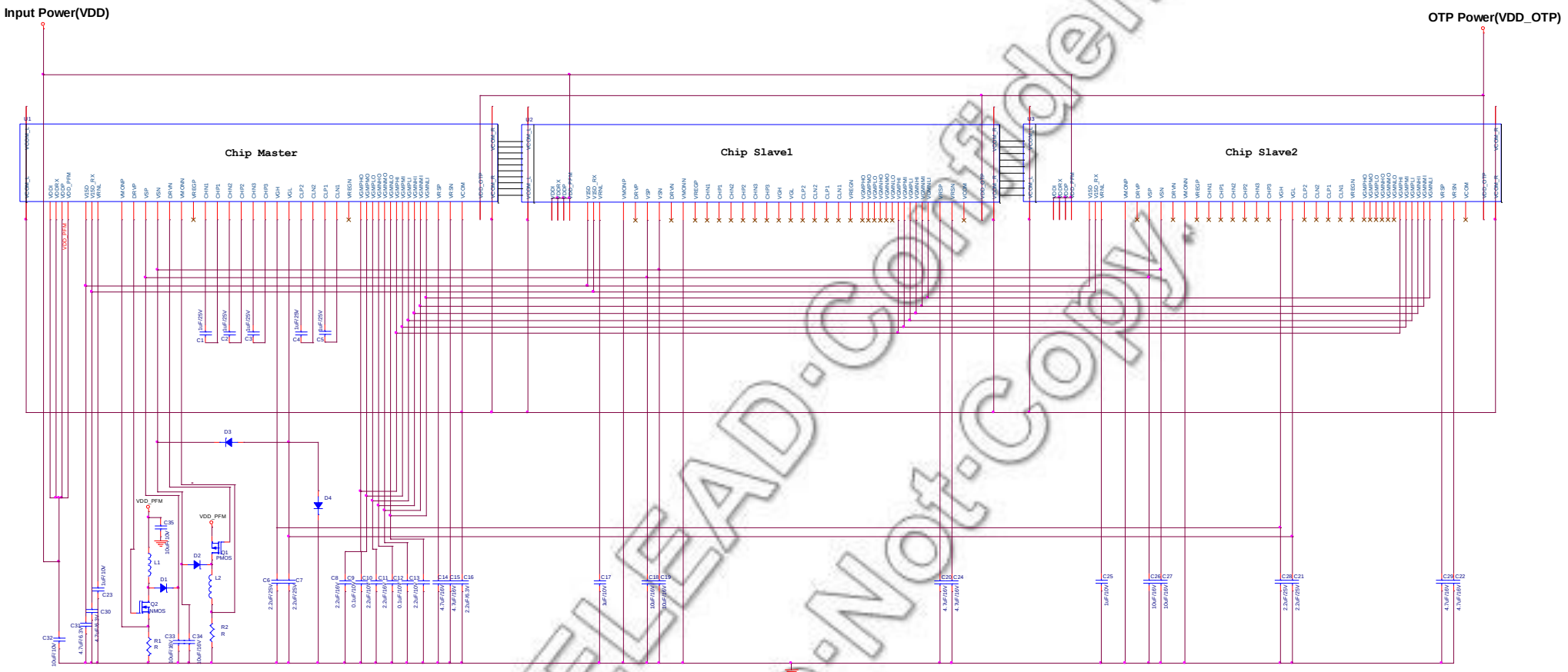


5.6 Power System

5.6.1 Power Tree



5.6.2 External Connections of Internal Power Mode



5.6.3 Internal Power Mode Requirement of External Components

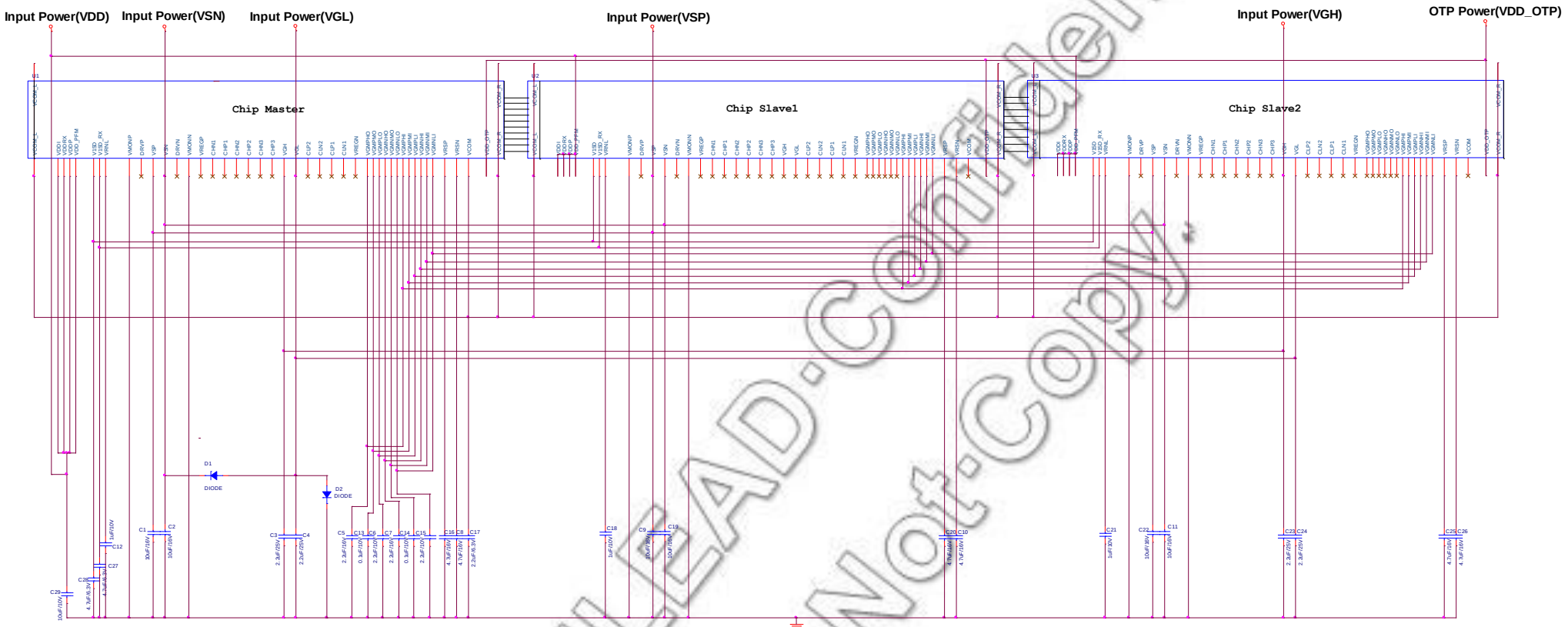
Item	Capacitance (uF)	Rated voltage (V)	Remarks
C9, C12	0.1	10	X7R
C17, C23, C25	1.0	10	X7R
C1, C2, C3, C4, C5	1.0	25	X7R
C16	2.2	6.3	X7R
C10, C13	2.2	10	X7R
C8, C11	2.2	16	X7R
C6, C7, C21, C28	2.2	25	X7R
C30, C31	4.7	6.3	X7R
C14, C15, C20, C22, C24, C29	4.7	16	X7R
C32, C35	10	10	X7R
C18, C19, C26, C27,C33, C34	10	16	X7R
Item	**VF**	**VR**	**Remarks**
D1, D2	VF＜0.6V/200mA	>25V	-
D3, D4	VF＜0.6V/200mA	>25V	-
Item	**Inductance**	**Current**	**Remarks**
L1, L2	4.7uH	I> 2A	
Item	Type	**Rated voltage (V)**	**Remarks**
Q1	PMOS	VDS< -20V	I> 2A
Q2	NMOS	VDS> 20V	I> 2A
Item	Resistance (Ohm)	**Rated watt (W)**	**Remarks**
R1, R2	0.1	1/10	0603

5.6.3.1 IC Connections Capacitance table

Item	Capacitance (uF)	Rated voltage (V)	Remarks
VDDI, VDDP, VDDRX, VDD_PFM	10	10	X7R
V15D, V15D_RX	4.7	6.3	X7R
VRNL	1.0	10	X7R
VSP, VSN	10	16	X7R
VCOM	2.2	6.3	X7R
VGMPLO, VGMNLO	2.2	10	X7R
VGMPMO, VGMNMO	0.1	10	X7R
VGMPHO, VGMNHO	2.2	16	X7R
VRSP, VRSN	4.7	16	X7R
CHP1, CHP2, CHP3 CHN1, CHN2, CHN3 CLP1, CLP2 CLN1, CLN2	1.0	25	X7R
VGH, VGL	2.2	25	X7R

Note：All the component values list on the table above are only for reference.
The values may need to be adjusted by different panel loading.

5.6.4 External Connections of External Power Mode



5.6.5 External Power Mode Requirement of External Components

Item	Capacitance (uF)	Rated voltage (V)	Remarks
C13, C14	0.1	10	X7R
C12, C18, C21	1.0	10	X7R
C17	2.2	6.3	X7R
C6, C15	2.2	10	X7R
C5, C7	2.2	16	X7R
C3, C4	2.2	25	X7R
C27, C28	4.7	6.3	X7R
C8, C10, C16, C20 C25, C26	4.7	16	X7R
C29	10.0	10	X7R
C1, C2, C9, C11, C19, C22	10.0	16	X7R
Item	**VF**	**VR**	**Remarks**
D1,D2	VF＜0.6V/200mA	>25V	

Note：All the component values list on the table above are only for reference.
The values may need to be adjusted by different panel loading.

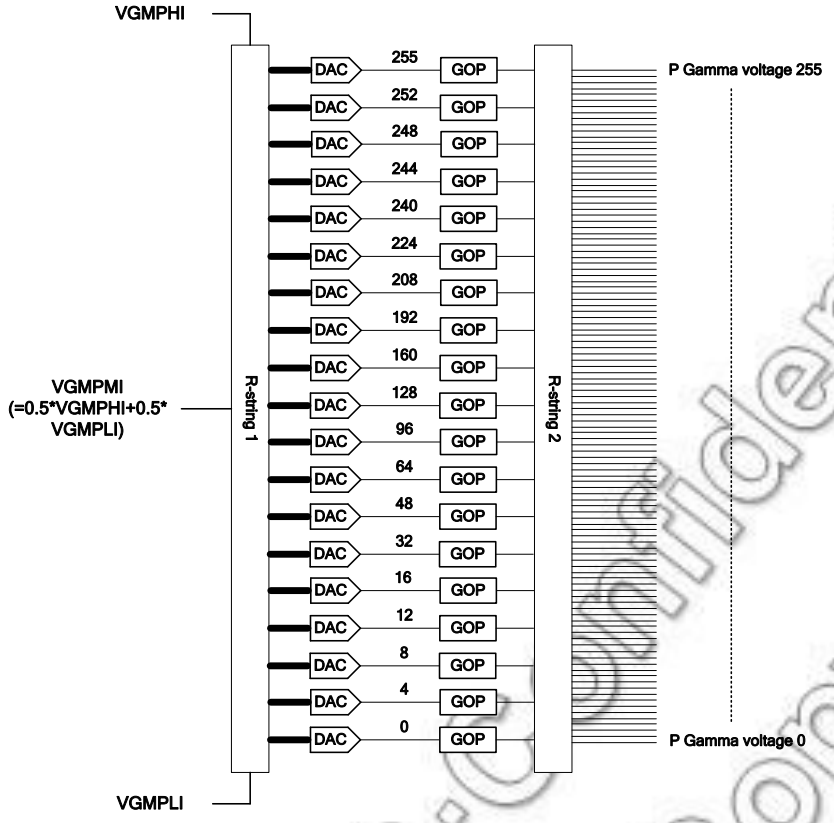
5.6.5.1 IC Connections Capacitance table

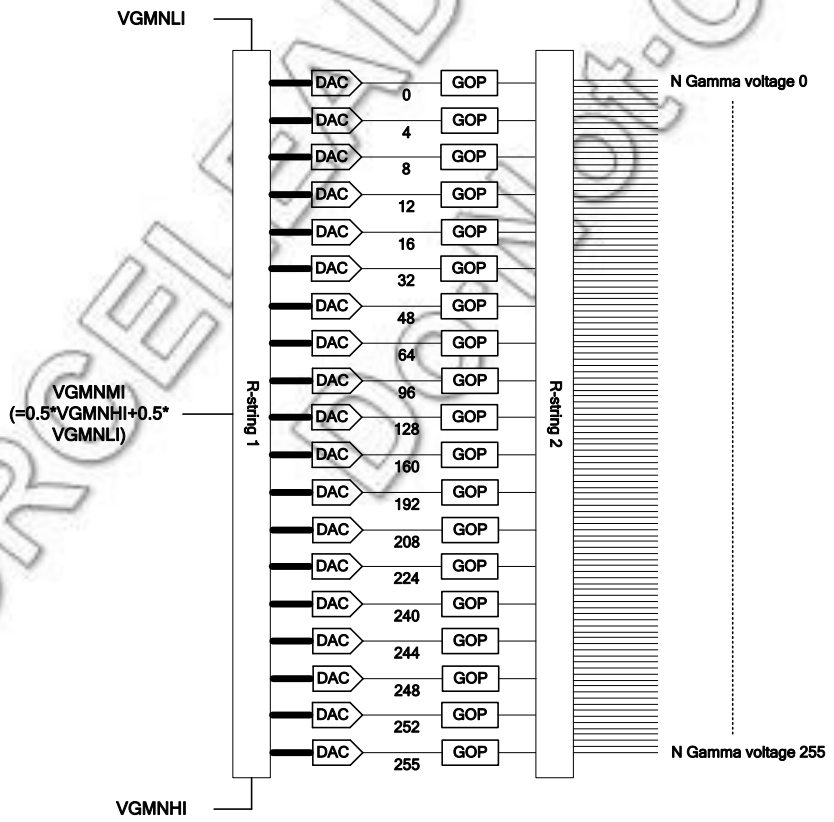
Item	Capacitance (uF)	Rated voltage (V)	Remarks
VDDI, VDDP, VDDRX, VDD_PFM	10	10	X7R
V15D, V15D_RX	4.7	6.3	X7R
VRNL	1.0	10	X7R
VSP, VSN	10	16	X7R
VCOM	2.2	6.3	X7R
VGMPLO, VGMNLO	2.2	10	X7R
VGMPMO, VGMNMO	0.1	10	X7R
VGMPHO, VGMNHO	2.2	16	X7R
VRSP, VRSN	4.7	16	X7R
CHP1, CHP2, CHP3 CHN1, CHN2, CHN3 CLP1, CLP2 CLN1, CLN2	1.0	25	X7R
VGH, VGL	2.2	25	X7R

Note：All the component values list on the table above are only for reference.
The values may need to be adjusted by different panel loading.

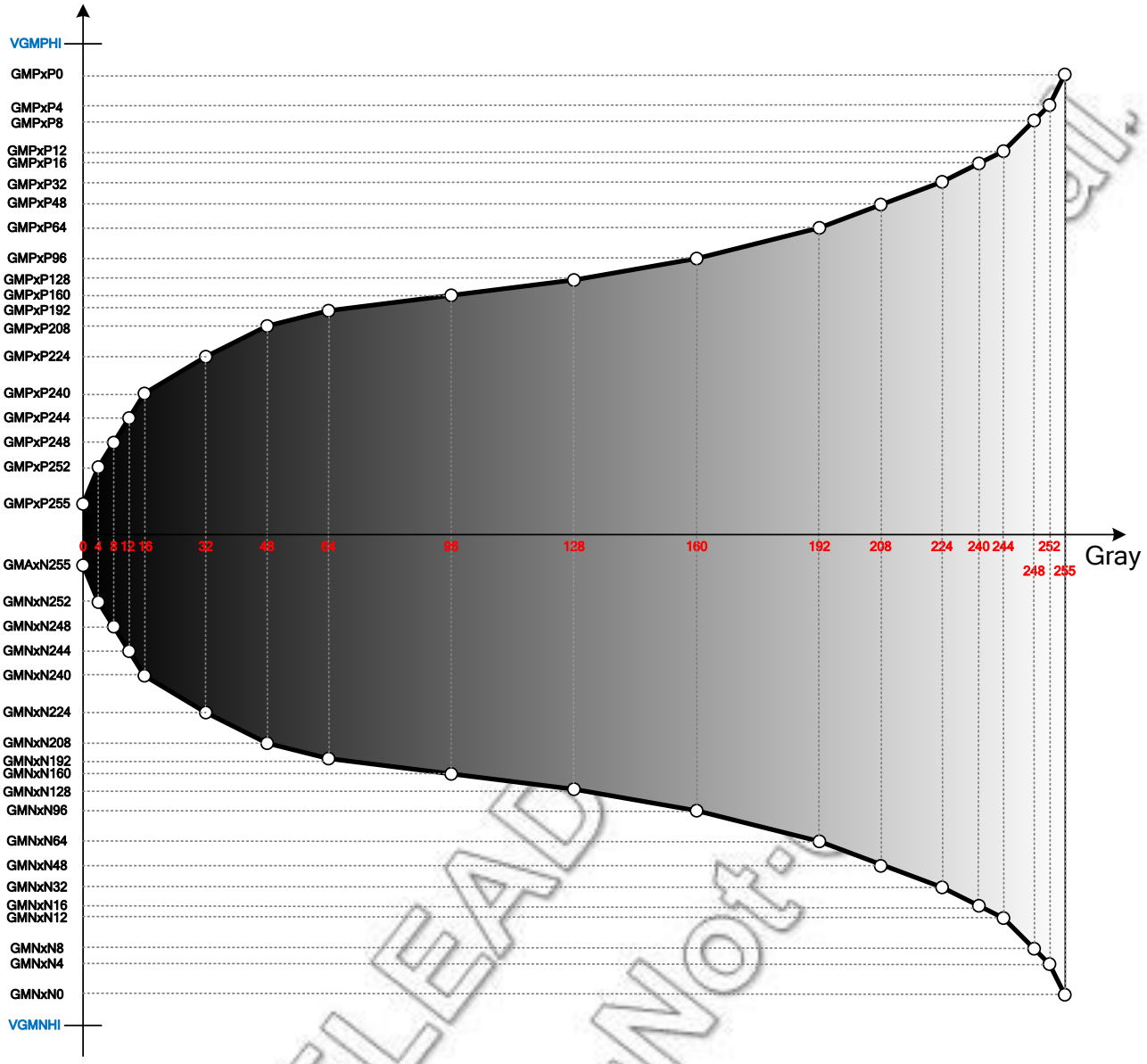
5.7 Gamma Circuit

There are 19 independently adjustable nodes for each of the positive and negative gamma curve respectively.

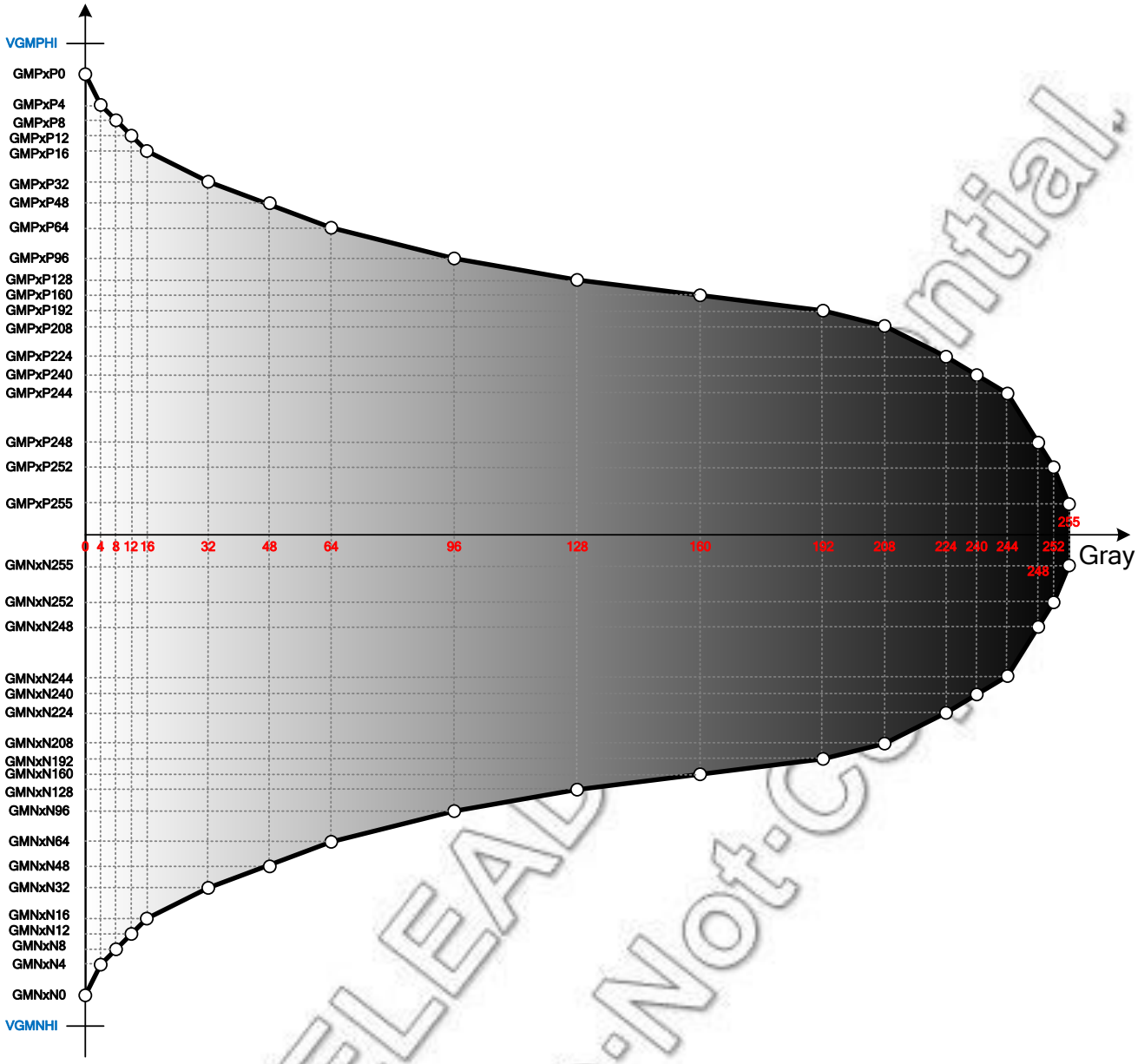




5.7.1 Gamma Voltage Curves for Normal Black Modules



5.7.2 Gamma Voltages Curve for Normal White Modules



5.7.3 Gamma Voltage Formula for Normally Black Modules

8Bit Gray Code	Positive Gamma Voltage (x = R or G or B)	Negative Gamma Voltage (x = R or G or B)
255	GMAx0	GMAx0
254	(GMAx0-GMAx4) / 4 × 3 + GMAx4	(GMAx0-GMAx4) / 4 × 3 + GMAx4
253	(GMAx0-GMAx4) / 4 × 2 + GMAx4	(GMAx0-GMAx4) / 4 × 2 + GMAx4
252	(GMAx0-GMAx4) / 4 × 1 + GMAx4	(GMAx0-GMAx4) / 4 × 1 + GMAx4
251	GMAx4	GMAx4
250	(GMAx4-GMAx8) / 4 × 3 + GMAx8	(GMAx4-GMAx8) / 4 × 3 + GMAx8
249	(GMAx4-GMAx8) / 4 × 2 + GMAx8	(GMAx4-GMAx8) / 4 × 2 + GMAx8
248	(GMAx4-GMAx8) / 4 × 1 + GMAx8	(GMAx4-GMAx8) / 4 × 1 + GMAx8
247	GMAx8	GMAx8
246	(GMAx8-GMAx12) / 4 × 3 + GMAx12	(GMAx8-GMAx12) / 4 × 3 + GMAx12
245	(GMAx8-GMAx12) / 4 × 2 + GMAx12	(GMAx8-GMAx12) / 4 × 2 + GMAx12
244	(GMAx8-GMAx12) / 4 × 1 + GMAx12	(GMAx8-GMAx12) / 4 × 1 + GMAx12
243	GMAx12	GMAx12
242	(GMAPx12-GMAx16) / 4 × 3 + GMAx16	(GMAx12-GMAx16) / 4 × 3 + GMAx16
241	(GMAPx12-GMAx16) / 4 × 2 + GMAx16	(GMAx12-GMAx16) / 4 × 2 + GMAx16
240	(GMAPx12-GMAx16) / 4 × 1 + GMAx16	(GMAx12-GMAx16) / 4 × 1 + GMAx16
239	GMAx16	GMAx16
238	(GMAx16-GMAx32) / 16 × 15 + GMAx32	(GMAx16-GMAx32) / 16 × 15 + GMAx32
237	(GMAx16-GMAx32) / 16 × 14 + GMAx32	(GMAx16-GMAx32) / 16 × 14 + GMAx32
236	(GMAx16-GMAx32) / 16 × 13 + GMAx32	(GMAx16-GMAx32) / 16 × 13 + GMAx32
235	(GMAx16-GMAx32) / 16 × 12 + GMAx32	(GMAx16-GMAx32) / 16 × 12 + GMAx32
234	(GMAx16-GMAx32) / 16 × 11 + GMAx32	(GMAx16-GMAx32) / 16 × 11 + GMAx32
233	(GMAx16-GMAx32) / 16 × 10 + GMAx32	(GMAx16-GMAx32) / 16 × 10 + GMAx32
232	(GMAx16-GMAx32) / 16 × 9 + GMAx32	(GMAx16-GMAx32) / 16 × 9 + GMAx32
231	(GMAx16-GMAx32) / 16 × 8 + GMAx32	(GMAx16-GMAx32) / 16 × 8 + GMAx32
230	(GMAx16-GMAx32) / 16 × 7 + GMAx32	(GMAx16-GMAx32) / 16 × 7 + GMAx32
229	(GMAx16-GMAx32) / 16 × 6 + GMAx32	(GMAx16-GMAx32) / 16 × 6 + GMAx32
228	(GMAx16-GMAx32) / 16 × 5 + GMAx32	(GMAx16-GMAx32) / 16 × 5 + GMAx32
227	(GMAx16-GMAx32) / 16 × 4 + GMAx32	(GMAx16-GMAx32) / 16 × 4 + GMAx32
226	(GMAx16-GMAx32) / 16 × 3 + GMAx32	(GMAx16-GMAx32) / 16 × 3 + GMAx32
225	(GMAx16-GMAx32) / 16 × 2 + GMAx32	(GMAx16-GMAx32) / 16 × 2 + GMAx32
224	(GMAx16-GMAx32) / 16 × 1 + GMAx32	(GMAx16-GMAx32) / 16 × 1 + GMAx32
223	GMAx32	GMAx32
222	(GMAx32-GMAx48) / 16 × 15 + GMAPx48	(GMAx32-GMAx48) / 16 × 15 + GMAx48
221	(GMAx32-GMAx48) / 16 × 14 + GMAPx48	(GMAx32-GMAx48) / 16 × 14 + GMAx48
220	(GMAx32-GMAx48) / 16 × 13 + GMAPx48	(GMAx32-GMAx48) / 16 × 13 + GMAx48
219	(GMAx32-GMAx48) / 16 × 12 + GMAPx48	(GMAx32-GMAx48) / 16 × 12 + GMAx48
218	(GMAx32-GMAx48) / 16 × 11 + GMAPx48	(GMAx32-GMAx48) / 16 × 11 + GMAx48

217	(GMAx32-GMAx48)	/ 16 × 10 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	10	+	GMAx48
216	(GMAx32-GMAx48)	/ 16 × 9 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	9	+	GMAx48
215	(GMAx32-GMAx48)	/ 16 × 8 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	8	+	GMAx48
214	(GMAx32-GMAx48)	/ 16 × 7 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	7	+	GMAx48
213	(GMAx32-GMAx48)	/ 16 × 6 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	6	+	GMAx48
212	(GMAx32-GMAx48)	/ 16 × 5 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	5	+	GMAx48
211	(GMAx32-GMAx48)	/ 16 × 4 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	4	+	GMAx48
210	(GMAx32-GMAx48)	/ 16 × 3 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	3	+	GMAx48
209	(GMAx32-GMAx48)	/ 16 × 2 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	2	+	GMAx48
208	(GMAx32-GMAx48)	/ 16 × 1 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	1	+	GMAx48
207	GMAx48			GMAx48				
206	(GMAx48-GMAx64)	/ 16 × 15 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	15	+	GMAx64
205	(GMAx48-GMAx64)	/ 16 × 14 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	14	+	GMAx64
204	(GMAx48-GMAx64)	/ 16 × 13 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	13	+	GMAx64
203	(GMAx48-GMAx64)	/ 16 × 12 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	12	+	GMAx64
202	(GMAx48-GMAx64)	/ 16 × 11 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	11	+	GMAx64
201	(GMAx48-GMAx64)	/ 16 × 10 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	10	+	GMAx64
200	(GMAx48-GMAx64)	/ 16 × 9 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	9	+	GMAx64
199	(GMAx48-GMAx64)	/ 16 × 8 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	8	+	GMAx64
198	(GMAx48-GMAx64)	/ 16 × 7 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	7	+	GMAx64
197	(GMAx48-GMAx64)	/ 16 × 6 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	6	+	GMAx64
196	(GMAx48-GMAx64)	/ 16 × 5 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	5	+	GMAx64
195	(GMAx48-GMAx64)	/ 16 × 4 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	4	+	GMAx64
194	(GMAx48-GMAx64)	/ 16 × 3 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	3	+	GMAx64
193	(GMAx48-GMAx64)	/ 16 × 2 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	2	+	GMAx64
192	(GMAx48-GMAx64)	/ 16 × 1 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	1	+	GMAx64
191	GMAx64			GMAx64				
190	(GMAx64-GMAx96)	/ 32 × 31 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	31	+	GMAx96
189	(GMAx64-GMAx96)	/ 32 × 30 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	30	+	GMAx96
188	(GMAx64-GMAx96)	/ 32 × 29 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	29	+	GMAx96
187	(GMAx64-GMAx96)	/ 32 × 28 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	28	+	GMAx96
186	(GMAx64-GMAx96)	/ 32 × 27 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	27	+	GMAx96
185	(GMAx64-GMAx96)	/ 32 × 26 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	26	+	GMAx96
184	(GMAx64-GMAx96)	/ 32 × 25 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	25	+	GMAx96
183	(GMAx64-GMAx96)	/ 32 × 24 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	24	+	GMAx96
182	(GMAx64-GMAx96)	/ 32 × 23 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	23	+	GMAx96
181	(GMAx64-GMAx96)	/ 32 × 22 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	22	+	GMAx96
180	(GMAx64-GMAx96)	/ 32 × 21 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	21	+	GMAx96
179	(GMAx64-GMAx96)	/ 32 × 20 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	20	+	GMAx96
178	(GMAx64-GMAx96)	/ 32 × 19 +	GMAx96	(GMAx64-GMAx96)	/ 32 ×	19	+	GMAx96

177	(GMAx64-GMAx96)	/ 32 ×	18	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	18	+	GMAx96
176	(GMAx64-GMAx96)	/ 32 ×	17	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	17	+	GMAx96
175	(GMAx64-GMAx96)	/ 32 ×	16	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	16	+	GMAx96
174	(GMAx64-GMAx96)	/ 32 ×	15	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	15	+	GMAx96
173	(GMAx64-GMAx96)	/ 32 ×	14	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	14	+	GMAx96
172	(GMAx64-GMAx96)	/ 32 ×	13	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	13	+	GMAx96
171	(GMAx64-GMAx96)	/ 32 ×	12	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	12	+	GMAx96
170	(GMAx64-GMAx96)	/ 32 ×	11	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	11	+	GMAx96
169	(GMAx64-GMAx96)	/ 32 ×	10	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	10	+	GMAx96
168	(GMAx64-GMAx96)	/ 32 ×	9	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	9	+	GMAx96
167	(GMAx64-GMAx96)	/ 32 ×	8	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	8	+	GMAx96
166	(GMAx64-GMAx96)	/ 32 ×	7	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	7	+	GMAx96
165	(GMAx64-GMAx96)	/ 32 ×	6	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	6	+	GMAx96
164	(GMAx64-GMAx96)	/ 32 ×	5	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	5	+	GMAx96
163	(GMAx64-GMAx96)	/ 32 ×	4	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	4	+	GMAx96
162	(GMAx64-GMAx96)	/ 32 ×	3	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	3	+	GMAx96
161	(GMAx64-GMAx96)	/ 32 ×	2	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	2	+	GMAx96
160	(GMAx64-GMAx96)	/ 32 ×	1	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	1	+	GMAx96
159	GMAx96					GMAx96				
158	(GMAx96-GMAx128)	/ 32 ×	31	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	31	+	GMAx128
157	(GMAx96-GMAx128)	/ 32 ×	30	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	30	+	GMAx128
156	(GMAx96-GMAx128)	/ 32 ×	29	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	29	+	GMAx128
155	(GMAx96-GMAx128)	/ 32 ×	28	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	28	+	GMAx128
154	(GMAx96-GMAx128)	/ 32 ×	27	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	27	+	GMAx128
153	(GMAx96-GMAx128)	/ 32 ×	26	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	26	+	GMAx128
152	(GMAx96-GMAx128)	/ 32 ×	25	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	25	+	GMAx128
151	(GMAx96-GMAx128)	/ 32 ×	24	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	24	+	GMAx128
150	(GMAx96-GMAx128)	/ 32 ×	23	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	23	+	GMAx128
149	(GMAx96-GMAx128)	/ 32 ×	22	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	22	+	GMAx128
148	(GMAx96-GMAx128)	/ 32 ×	21	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	21	+	GMAx128
147	(GMAx96-GMAx128)	/ 32 ×	20	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	20	+	GMAx128
146	(GMAx96-GMAx128)	/ 32 ×	19	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	19	+	GMAx128
145	(GMAx96-GMAx128)	/ 32 ×	18	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	18	+	GMAx128
144	(GMAx96-GMAx128)	/ 32 ×	17	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	17	+	GMAx128
143	(GMAx96-GMAx128)	/ 32 ×	16	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	16	+	GMAx128
142	(GMAx96-GMAx128)	/ 32 ×	15	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	15	+	GMAx128
141	(GMAx96-GMAx128)	/ 32 ×	14	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	14	+	GMAx128
140	(GMAx96-GMAx128)	/ 32 ×	13	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	13	+	GMAx128
139	(GMAx96-GMAx128)	/ 32 ×	12	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	12	+	GMAx128
138	(GMAx96-GMAx128)	/ 32 ×	11	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	11	+	GMAx128

137	(GMAx96-GMAx128)	/ 32 ×	10	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	10	+	GMAx128
136	(GMAx96-GMAx128)	/ 32 ×	9	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	9	+	GMAx128
135	(GMAx96-GMAx128)	/ 32 ×	8	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	8	+	GMAx128
134	(GMAx96-GMAx128)	/ 32 ×	7	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	7	+	GMAx128
133	(GMAx96-GMAx128)	/ 32 ×	6	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	6	+	GMAx128
132	(GMAx96-GMAx128)	/ 32 ×	5	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	5	+	GMAx128
131	(GMAx96-GMAx128)	/ 32 ×	4	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	4	+	GMAx128
130	(GMAx96-GMAx128)	/ 32 ×	3	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	3	+	GMAx128
129	(GMAx96-GMAx128)	/ 32 ×	2	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	2	+	GMAx128
128	(GMAx96-GMAx128)	/ 32 ×	1	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	1	+	GMAx128
127	GMAx128					GMAx128				
126	(GMAx128-GMAx160)	/ 32 ×	31	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	31	+	GMAx160
125	(GMAx128-GMAx160)	/ 32 ×	30	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	30	+	GMAx160
124	(GMAx128-GMAx160)	/ 32 ×	29	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	29	+	GMAx160
123	(GMAx128-GMAx160)	/ 32 ×	28	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	28	+	GMAx160
122	(GMAx128-GMAx160)	/ 32 ×	27	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	27	+	GMAx160
121	(GMAx128-GMAx160)	/ 32 ×	26	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	26	+	GMAx160
120	(GMAx128-GMAx160)	/ 32 ×	25	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	25	+	GMAx160
119	(GMAx128-GMAx160)	/ 32 ×	24	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	24	+	GMAx160
118	(GMAx128-GMAx160)	/ 32 ×	23	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	23	+	GMAx160
117	(GMAx128-GMAx160)	/ 32 ×	22	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	22	+	GMAx160
116	(GMAx128-GMAx160)	/ 32 ×	21	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	21	+	GMAx160
115	(GMAx128-GMAx160)	/ 32 ×	20	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	20	+	GMAx160
114	(GMAx128-GMAx160)	/ 32 ×	19	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	19	+	GMAx160
113	(GMAx128-GMAx160)	/ 32 ×	18	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	18	+	GMAx160
112	(GMAx128-GMAx160)	/ 32 ×	17	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	17	+	GMAx160
111	(GMAx128-GMAx160)	/ 32 ×	16	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	16	+	GMAx160
110	(GMAx128-GMAx160)	/ 32 ×	15	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	15	+	GMAx160
109	(GMAx128-GMAx160)	/ 32 ×	14	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	14	+	GMAx160
108	(GMAx128-GMAx160)	/ 32 ×	13	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	13	+	GMAx160
107	(GMAx128-GMAx160)	/ 32 ×	12	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	12	+	GMAx160
106	(GMAx128-GMAx160)	/ 32 ×	11	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	11	+	GMAx160
105	(GMAx128-GMAx160)	/ 32 ×	10	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	10	+	GMAx160
104	(GMAx128-GMAx160)	/ 32 ×	9	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	9	+	GMAx160
103	(GMAx128-GMAx160)	/ 32 ×	8	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	8	+	GMAx160
102	(GMAx128-GMAx160)	/ 32 ×	7	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	7	+	GMAx160
101	(GMAx128-GMAx160)	/ 32 ×	6	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	6	+	GMAx160
100	(GMAx128-GMAx160)	/ 32 ×	5	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	5	+	GMAx160
99	(GMAx128-GMAx160)	/ 32 ×	4	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	4	+	GMAx160
98	(GMAx128-GMAx160)	/ 32 ×	3	+	GMAx160	(GMAx128-GMAx160)	/ 32 ×	3	+	GMAx160

97	(GMAx128-GMAx160) / 32 × 2 + GMAx160	(GMAx128-GMAx160) / 32 × 2 + GMAx160
96	(GMAx128-GMAx160) / 32 × 1 + GMAx160	(GMAx128-GMAx160) / 32 × 1 + GMAx160
95	GMAx160	GMAx160
94	(GMAx160-GMAx192) / 32 × 31 + GMAx192	(GMAx160-GMAx192) / 32 × 31 + GMAx192
93	(GMAx160-GMAx192) / 32 × 30 + GMAx192	(GMAx160-GMAx192) / 32 × 30 + GMAx192
92	(GMAx160-GMAx192) / 32 × 29 + GMAx192	(GMAx160-GMAx192) / 32 × 29 + GMAx192
91	(GMAx160-GMAx192) / 32 × 28 + GMAx192	(GMAx160-GMAx192) / 32 × 28 + GMAx192
90	(GMAx160-GMAx192) / 32 × 27 + GMAx192	(GMAx160-GMAx192) / 32 × 27 + GMAx192
89	(GMAx160-GMAx192) / 32 × 26 + GMAx192	(GMAx160-GMAx192) / 32 × 26 + GMAx192
88	(GMAx160-GMAx192) / 32 × 25 + GMAx192	(GMAx160-GMAx192) / 32 × 25 + GMAx192
87	(GMAx160-GMAx192) / 32 × 24 + GMAx192	(GMAx160-GMAx192) / 32 × 24 + GMAx192
86	(GMAx160-GMAx192) / 32 × 23 + GMAx192	(GMAx160-GMAx192) / 32 × 23 + GMAx192
85	(GMAx160-GMAx192) / 32 × 22 + GMAx192	(GMAx160-GMAx192) / 32 × 22 + GMAx192
84	(GMAx160-GMAx192) / 32 × 21 + GMAx192	(GMAx160-GMAx192) / 32 × 21 + GMAx192
83	(GMAx160-GMAx192) / 32 × 20 + GMAx192	(GMAx160-GMAx192) / 32 × 20 + GMAx192
82	(GMAx160-GMAx192) / 32 × 19 + GMAx192	(GMAx160-GMAx192) / 32 × 19 + GMAx192
81	(GMAx160-GMAx192) / 32 × 18 + GMAx192	(GMAx160-GMAx192) / 32 × 18 + GMAx192
80	(GMAx160-GMAx192) / 32 × 17 + GMAx192	(GMAx160-GMAx192) / 32 × 17 + GMAx192
79	(GMAx160-GMAx192) / 32 × 16 + GMAx192	(GMAx160-GMAx192) / 32 × 16 + GMAx192
78	(GMAx160-GMAx192) / 32 × 15 + GMAx192	(GMAx160-GMAx192) / 32 × 15 + GMAx192
77	(GMAx160-GMAx192) / 32 × 14 + GMAx192	(GMAx160-GMAx192) / 32 × 14 + GMAx192
76	(GMAx160-GMAx192) / 32 × 13 + GMAx192	(GMAx160-GMAx192) / 32 × 13 + GMAx192
75	(GMAx160-GMAx192) / 32 × 12 + GMAx192	(GMAx160-GMAx192) / 32 × 12 + GMAx192
74	(GMAx160-GMAx192) / 32 × 11 + GMAx192	(GMAx160-GMAx192) / 32 × 11 + GMAx192
73	(GMAx160-GMAx192) / 32 × 10 + GMAx192	(GMAx160-GMAx192) / 32 × 10 + GMAx192
72	(GMAx160-GMAx192) / 32 × 9 + GMAx192	(GMAx160-GMAx192) / 32 × 9 + GMAx192
71	(GMAx160-GMAx192) / 32 × 8 + GMAx192	(GMAx160-GMAx192) / 32 × 8 + GMAx192
70	(GMAx160-GMAx192) / 32 × 7 + GMAx192	(GMAx160-GMAx192) / 32 × 7 + GMAx192
69	(GMAx160-GMAx192) / 32 × 6 + GMAx192	(GMAx160-GMAx192) / 32 × 6 + GMAx192
68	(GMAx160-GMAx192) / 32 × 5 + GMAx192	(GMAx160-GMAx192) / 32 × 5 + GMAx192
67	(GMAx160-GMAx192) / 32 × 4 + GMAx192	(GMAx160-GMAx192) / 32 × 4 + GMAx192
66	(GMAx160-GMAx192) / 32 × 3 + GMAx192	(GMAx160-GMAx192) / 32 × 3 + GMAx192
65	(GMAx160-GMAx192) / 32 × 2 + GMAx192	(GMAx160-GMAx192) / 32 × 2 + GMAx192
64	(GMAx160-GMAx192) / 32 × 1 + GMAx192	(GMAx160-GMAx192) / 32 × 1 + GMAx192
63	GMAx192	GMAx192
62	(GMAx192-GMAx208) / 16 × 15 + GMAx208	(GMAx192-GMAx208) / 16 × 15 + GMAx208
61	(GMAx192-GMAx208) / 16 × 14 + GMAx208	(GMAx192-GMAx208) / 16 × 14 + GMAx208
60	(GMAx192-GMAx208) / 16 × 13 + GMAx208	(GMAx192-GMAx208) / 16 × 13 + GMAx208
59	(GMAx192-GMAx208) / 16 × 12 + GMAx208	(GMAx192-GMAx208) / 16 × 12 + GMAx208
58	(GMAx192-GMAx208) / 16 × 11 + GMAx208	(GMAx192-GMAx208) / 16 × 11 + GMAx208

57	(GMAx192-GMAx208) / 16 × 10 + GMAx208	(GMAx192-GMAx208) / 16 × 10 + GMAx208
56	(GMAx192-GMAx208) / 16 × 9 + GMAx208	(GMAx192-GMAx208) / 16 × 9 + GMAx208
55	(GMAx192-GMAx208) / 16 × 8 + GMAx208	(GMAx192-GMAx208) / 16 × 8 + GMAx208
54	(GMAx192-GMAx208) / 16 × 7 + GMAx208	(GMAx192-GMAx208) / 16 × 7 + GMAx208
53	(GMAx192-GMAx208) / 16 × 6 + GMAx208	(GMAx192-GMAx208) / 16 × 6 + GMAx208
52	(GMAx192-GMAx208) / 16 × 5 + GMAx208	(GMAx192-GMAx208) / 16 × 5 + GMAx208
51	(GMAx192-GMAx208) / 16 × 4 + GMAx208	(GMAx192-GMAx208) / 16 × 4 + GMAx208
50	(GMAx192-GMAx208) / 16 × 3 + GMAx208	(GMAx192-GMAx208) / 16 × 3 + GMAx208
49	(GMAx192-GMAx208) / 16 × 2 + GMAx208	(GMAx192-GMAx208) / 16 × 2 + GMAx208
48	(GMAx192-GMAx208) / 16 × 1 + GMAx208	(GMAx192-GMAx208) / 16 × 1 + GMAx208
47	GMAx208	GMAx208
46	(GMAx208-GMAx224) / 16 × 15 + GMAx224	(GMAx208-GMAx224) / 16 × 15 + GMAx224
45	(GMAx208-GMAx224) / 16 × 14 + GMAx224	(GMAx208-GMAx224) / 16 × 14 + GMAx224
44	(GMAx208-GMAx224) / 16 × 13 + GMAx224	(GMAx208-GMAx224) / 16 × 13 + GMAx224
43	(GMAx208-GMAx224) / 16 × 12 + GMAx224	(GMAx208-GMAx224) / 16 × 12 + GMAx224
42	(GMAx208-GMAx224) / 16 × 11 + GMAx224	(GMAx208-GMAx224) / 16 × 11 + GMAx224
41	(GMAx208-GMAx224) / 16 × 10 + GMAx224	(GMAx208-GMAx224) / 16 × 10 + GMAx224
40	(GMAx208-GMAx224) / 16 × 9 + GMAx224	(GMAx208-GMAx224) / 16 × 9 + GMAx224
39	(GMAx208-GMAx224) / 16 × 8 + GMAx224	(GMAx208-GMAx224) / 16 × 8 + GMAx224
38	(GMAx208-GMAx224) / 16 × 7 + GMAx224	(GMAx208-GMAx224) / 16 × 7 + GMAx224
37	(GMAx208-GMAx224) / 16 × 6 + GMAx224	(GMAx208-GMAx224) / 16 × 6 + GMAx224
36	(GMAx208-GMAx224) / 16 × 5 + GMAx224	(GMAx208-GMAx224) / 16 × 5 + GMAx224
35	(GMAx208-GMAx224) / 16 × 4 + GMAx224	(GMAx208-GMAx224) / 16 × 4 + GMAx224
34	(GMAx208-GMAx224) / 16 × 3 + GMAx224	(GMAx208-GMAx224) / 16 × 3 + GMAx224
33	(GMAx208-GMAx224) / 16 × 2 + GMAx224	(GMAx208-GMAx224) / 16 × 2 + GMAx224
32	(GMAx208-GMAx224) / 16 × 1 + GMAx224	(GMAx208-GMAx224) / 16 × 1 + GMAx224
31	GMAx224	GMAx224
30	(GMAx224-GMAx240) / 16 × 15 + GMAx240	(GMAx224-GMAx240) / 16 × 15 + GMAx240
29	(GMAx224-GMAx240) / 16 × 14 + GMAx240	(GMAx224-GMAx240) / 16 × 14 + GMAx240
28	(GMAx224-GMAx240) / 16 × 13 + GMAx240	(GMAx224-GMAx240) / 16 × 13 + GMAx240
27	(GMAx224-GMAx240) / 16 × 12 + GMAx240	(GMAx224-GMAx240) / 16 × 12 + GMAx240
26	(GMAx224-GMAx240) / 16 × 11 + GMAx240	(GMAx224-GMAx240) / 16 × 11 + GMAx240
25	(GMAx224-GMAx240) / 16 × 10 + GMAx240	(GMAx224-GMAx240) / 16 × 10 + GMAx240
24	(GMAx224-GMAx240) / 16 × 9 + GMAx240	(GMAx224-GMAx240) / 16 × 9 + GMAx240
23	(GMAx224-GMAx240) / 16 × 8 + GMAx240	(GMAx224-GMAx240) / 16 × 8 + GMAx240
22	(GMAx224-GMAx240) / 16 × 7 + GMAx240	(GMAx224-GMAx240) / 16 × 7 + GMAx240
21	(GMAx224-GMAx240) / 16 × 6 + GMAx240	(GMAx224-GMAx240) / 16 × 6 + GMAx240
20	(GMAx224-GMAx240) / 16 × 5 + GMAx240	(GMAx224-GMAx240) / 16 × 5 + GMAx240
19	(GMAx224-GMAx240) / 16 × 4 + GMAx240	(GMAx224-GMAx240) / 16 × 4 + GMAx240
18	(GMAx224-GMAx240) / 16 × 3 + GMAx240	(GMAx224-GMAx240) / 16 × 3 + GMAx240

17	(GMAx224-GMAx240) / 16 × 2 + GMAx240	(GMAx224-GMAx240) / 16 × 2 + GMAx240
16	(GMAx224-GMAx240) / 16 × 1 + GMAx240	(GMAx224-GMAx240) / 16 × 1 + GMAx240
15	GMAx240	GMAx240
14	(GMAx240-GMAx244) / 4 × 3 + GMAx244	(GMAx240-GMAx244) / 4 × 3 + GMAx244
13	(GMAx240-GMAx244) / 4 × 2 + GMAx244	(GMAx240-GMAx244) / 4 × 2 + GMAx244
12	(GMAx240-GMAx244) / 4 × 1 + GMAx244	(GMAx240-GMAx244) / 4 × 1 + GMAx244
11	GMAx244	GMAx244
10	(GMAx244-GMAx248) / 4 × 3 + GMAx248	(GMAx244-GMAx248) / 4 × 3 + GMAx248
9	(GMAx244-GMAx248) / 4 × 2 + GMAx248	(GMAx244-GMAx248) / 4 × 2 + GMAx248
8	(GMAx244-GMAx248) / 4 × 1 + GMAx248	(GMAx244-GMAx248) / 4 × 1 + GMAx248
7	GMAx248	GMAx248
6	(GMAx248-GMAx252) / 4 × 3 + GMAx252	(GMAx248-GMAx252) / 4 × 3 + GMAx252
5	(GMAx248-GMAx252) / 4 × 2 + GMAx252	(GMAx248-GMAx252) / 4 × 2 + GMAx252
4	(GMAx248-GMAx252) / 4 × 1 + GMAx252	(GMAx248-GMAx252) / 4 × 1 + GMAx252
3	GMAx252	GMAx252
2	(GMAx252-GMAx255) / 3 × 2 + GMAx255	(GMAx252-GMAx255) / 3 × 2 + GMAx255
1	(GMAx252-GMAx255) / 3 × 1 + GMAx255	(GMAx252-GMAx255) / 3 × 1 + GMAx255
0	GMAx255	GMAx255

5.7.4 Gamma Voltage Formula for Normally White Modules

8Bit Gray Code	Positive Gamma Voltage (x = R or G or B)	Negative Gamma Voltage (x = R or G or B)
0	GMAx0	GMAx0
1	(GMAx0-GMAx4) / 4 × 3 + GMAx4	(GMAx0-GMAx4) / 4 × 3 + GMAx4
2	(GMAx0-GMAx4) / 4 × 2 + GMAx4	(GMAx0-GMAx4) / 4 × 2 + GMAx4
3	(GMAx0-GMAx4) / 4 × 1 + GMAx4	(GMAx0-GMAx4) / 4 × 1 + GMAx4
4	GMAx4	GMAx4
5	(GMAx4-GMAx8) / 4 × 3 + GMAx8	(GMAx4-GMAx8) / 4 × 3 + GMAx8
6	(GMAx4-GMAx8) / 4 × 2 + GMAx8	(GMAx4-GMAx8) / 4 × 2 + GMAx8
7	(GMAx4-GMAx8) / 4 × 1 + GMAx8	(GMAx4-GMAx8) / 4 × 1 + GMAx8
8	GMAx8	GMAx8
9	(GMAx8-GMAx12) / 4 × 3 + GMAx12	(GMAx8-GMAx12) / 4 × 3 + GMAx12
10	(GMAx8-GMAx12) / 4 × 2 + GMAx12	(GMAx8-GMAx12) / 4 × 2 + GMAx12
11	(GMAx8-GMAx12) / 4 × 1 + GMAx12	(GMAx8-GMAx12) / 4 × 1 + GMAx12
12	GMAx12	GMAx12
13	(GMAPx12-GMAx16) / 4 × 3 + GMAx16	(GMAx12-GMAx16) / 4 × 3 + GMAx16
14	(GMAPx12-GMAx16) / 4 × 2 + GMAx16	(GMAx12-GMAx16) / 4 × 2 + GMAx16
15	(GMAPx12-GMAx16) / 4 × 1 + GMAx16	(GMAx12-GMAx16) / 4 × 1 + GMAx16
16	GMAx16	GMAx16
17	(GMAx16-GMAx32) / 16 × 15 + GMAx32	(GMAx16-GMAx32) / 16 × 15 + GMAx32
18	(GMAx16-GMAx32) / 16 × 14 + GMAx32	(GMAx16-GMAx32) / 16 × 14 + GMAx32

19	(GMAx16-GMAx32)	/ 16 × 13 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	13	+	GMAx32
20	(GMAx16-GMAx32)	/ 16 × 12 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	12	+	GMAx32
21	(GMAx16-GMAx32)	/ 16 × 11 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	11	+	GMAx32
22	(GMAx16-GMAx32)	/ 16 × 10 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	10	+	GMAx32
23	(GMAx16-GMAx32)	/ 16 × 9 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	9	+	GMAx32
24	(GMAx16-GMAx32)	/ 16 × 8 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	8	+	GMAx32
25	(GMAx16-GMAx32)	/ 16 × 7 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	7	+	GMAx32
26	(GMAx16-GMAx32)	/ 16 × 6 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	6	+	GMAx32
27	(GMAx16-GMAx32)	/ 16 × 5 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	5	+	GMAx32
28	(GMAx16-GMAx32)	/ 16 × 4 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	4	+	GMAx32
29	(GMAx16-GMAx32)	/ 16 × 3 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	3	+	GMAx32
30	(GMAx16-GMAx32)	/ 16 × 2 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	2	+	GMAx32
31	(GMAx16-GMAx32)	/ 16 × 1 +	GMAx32	(GMAx16-GMAx32)	/ 16 ×	1	+	GMAx32
32	GMAx32			GMAx32				
33	(GMAx32-GMAx48)	/ 16 × 15 +	GMAPx48	(GMAx32-GMAx48)	/ 16 ×	15	+	GMAx48
34	(GMAx32-GMAx48)	/ 16 × 14 +	GMAPx48	(GMAx32-GMAx48)	/ 16 ×	14	+	GMAx48
35	(GMAx32-GMAx48)	/ 16 × 13 +	GMAPx48	(GMAx32-GMAx48)	/ 16 ×	13	+	GMAx48
36	(GMAx32-GMAx48)	/ 16 × 12 +	GMAPx48	(GMAx32-GMAx48)	/ 16 ×	12	+	GMAx48
37	(GMAx32-GMAx48)	/ 16 × 11 +	GMAPx48	(GMAx32-GMAx48)	/ 16 ×	11	+	GMAx48
38	(GMAx32-GMAx48)	/ 16 × 10 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	10	+	GMAx48
39	(GMAx32-GMAx48)	/ 16 × 9 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	9	+	GMAx48
40	(GMAx32-GMAx48)	/ 16 × 8 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	8	+	GMAx48
41	(GMAx32-GMAx48)	/ 16 × 7 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	7	+	GMAx48
42	(GMAx32-GMAx48)	/ 16 × 6 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	6	+	GMAx48
43	(GMAx32-GMAx48)	/ 16 × 5 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	5	+	GMAx48
44	(GMAx32-GMAx48)	/ 16 × 4 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	4	+	GMAx48
45	(GMAx32-GMAx48)	/ 16 × 3 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	3	+	GMAx48
46	(GMAx32-GMAx48)	/ 16 × 2 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	2	+	GMAx48
47	(GMAx32-GMAx48)	/ 16 × 1 +	GMAx48	(GMAx32-GMAx48)	/ 16 ×	1	+	GMAx48
48	GMAx48			GMAx48				
49	(GMAx48-GMAx64)	/ 16 × 15 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	15	+	GMAx64
50	(GMAx48-GMAx64)	/ 16 × 14 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	14	+	GMAx64
51	(GMAx48-GMAx64)	/ 16 × 13 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	13	+	GMAx64
52	(GMAx48-GMAx64)	/ 16 × 12 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	12	+	GMAx64
53	(GMAx48-GMAx64)	/ 16 × 11 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	11	+	GMAx64
54	(GMAx48-GMAx64)	/ 16 × 10 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	10	+	GMAx64
55	(GMAx48-GMAx64)	/ 16 × 9 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	9	+	GMAx64
56	(GMAx48-GMAx64)	/ 16 × 8 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	8	+	GMAx64
57	(GMAx48-GMAx64)	/ 16 × 7 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	7	+	GMAx64
58	(GMAx48-GMAx64)	/ 16 × 6 +	GMAx64	(GMAx48-GMAx64)	/ 16 ×	6	+	GMAx64

59	(GMAx48-GMAx64)	/ 16 ×	5	+	GMAx64	(GMAx48-GMAx64)	/ 16 ×	5	+ GMAx64
60	(GMAx48-GMAx64)	/ 16 ×	4	+	GMAx64	(GMAx48-GMAx64)	/ 16 ×	4	+ GMAx64
61	(GMAx48-GMAx64)	/ 16 ×	3	+	GMAx64	(GMAx48-GMAx64)	/ 16 ×	3	+ GMAx64
62	(GMAx48-GMAx64)	/ 16 ×	2	+	GMAx64	(GMAx48-GMAx64)	/ 16 ×	2	+ GMAx64
63	(GMAx48-GMAx64)	/ 16 ×	1	+	GMAx64	(GMAx48-GMAx64)	/ 16 ×	1	+ GMAx64
64	GMAx64					GMAx64			
65	(GMAx64-GMAx96)	/ 32 ×	31	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	31	+ GMAx96
66	(GMAx64-GMAx96)	/ 32 ×	30	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	30	+ GMAx96
67	(GMAx64-GMAx96)	/ 32 ×	29	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	29	+ GMAx96
68	(GMAx64-GMAx96)	/ 32 ×	28	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	28	+ GMAx96
69	(GMAx64-GMAx96)	/ 32 ×	27	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	27	+ GMAx96
70	(GMAx64-GMAx96)	/ 32 ×	26	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	26	+ GMAx96
71	(GMAx64-GMAx96)	/ 32 ×	25	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	25	+ GMAx96
72	(GMAx64-GMAx96)	/ 32 ×	24	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	24	+ GMAx96
73	(GMAx64-GMAx96)	/ 32 ×	23	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	23	+ GMAx96
74	(GMAx64-GMAx96)	/ 32 ×	22	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	22	+ GMAx96
75	(GMAx64-GMAx96)	/ 32 ×	21	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	21	+ GMAx96
76	(GMAx64-GMAx96)	/ 32 ×	20	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	20	+ GMAx96
77	(GMAx64-GMAx96)	/ 32 ×	19	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	19	+ GMAx96
78	(GMAx64-GMAx96)	/ 32 ×	18	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	18	+ GMAx96
79	(GMAx64-GMAx96)	/ 32 ×	17	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	17	+ GMAx96
80	(GMAx64-GMAx96)	/ 32 ×	16	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	16	+ GMAx96
81	(GMAx64-GMAx96)	/ 32 ×	15	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	15	+ GMAx96
82	(GMAx64-GMAx96)	/ 32 ×	14	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	14	+ GMAx96
83	(GMAx64-GMAx96)	/ 32 ×	13	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	13	+ GMAx96
84	(GMAx64-GMAx96)	/ 32 ×	12	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	12	+ GMAx96
85	(GMAx64-GMAx96)	/ 32 ×	11	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	11	+ GMAx96
86	(GMAx64-GMAx96)	/ 32 ×	10	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	10	+ GMAx96
87	(GMAx64-GMAx96)	/ 32 ×	9	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	9	+ GMAx96
88	(GMAx64-GMAx96)	/ 32 ×	8	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	8	+ GMAx96
89	(GMAx64-GMAx96)	/ 32 ×	7	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	7	+ GMAx96
90	(GMAx64-GMAx96)	/ 32 ×	6	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	6	+ GMAx96
91	(GMAx64-GMAx96)	/ 32 ×	5	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	5	+ GMAx96
92	(GMAx64-GMAx96)	/ 32 ×	4	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	4	+ GMAx96
93	(GMAx64-GMAx96)	/ 32 ×	3	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	3	+ GMAx96
94	(GMAx64-GMAx96)	/ 32 ×	2	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	2	+ GMAx96
95	(GMAx64-GMAx96)	/ 32 ×	1	+	GMAx96	(GMAx64-GMAx96)	/ 32 ×	1	+ GMAx96
96	GMAx96					GMAx96			
97	(GMAx96-GMAx128)	/ 32 ×	31	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	31	+ GMAx128
98	(GMAx96-GMAx128)	/ 32 ×	30	+	GMAx128	(GMAx96-GMAx128)	/ 32 ×	30	+ GMAx128

99	(GMAx96-GMAx128)	/ 32 × 29 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	29	+	GMAx128
100	(GMAx96-GMAx128)	/ 32 × 28 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	28	+	GMAx128
101	(GMAx96-GMAx128)	/ 32 × 27 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	27	+	GMAx128
102	(GMAx96-GMAx128)	/ 32 × 26 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	26	+	GMAx128
103	(GMAx96-GMAx128)	/ 32 × 25 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	25	+	GMAx128
104	(GMAx96-GMAx128)	/ 32 × 24 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	24	+	GMAx128
105	(GMAx96-GMAx128)	/ 32 × 23 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	23	+	GMAx128
106	(GMAx96-GMAx128)	/ 32 × 22 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	22	+	GMAx128
107	(GMAx96-GMAx128)	/ 32 × 21 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	21	+	GMAx128
108	(GMAx96-GMAx128)	/ 32 × 20 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	20	+	GMAx128
109	(GMAx96-GMAx128)	/ 32 × 19 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	19	+	GMAx128
110	(GMAx96-GMAx128)	/ 32 × 18 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	18	+	GMAx128
111	(GMAx96-GMAx128)	/ 32 × 17 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	17	+	GMAx128
112	(GMAx96-GMAx128)	/ 32 × 16 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	16	+	GMAx128
113	(GMAx96-GMAx128)	/ 32 × 15 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	15	+	GMAx128
114	(GMAx96-GMAx128)	/ 32 × 14 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	14	+	GMAx128
115	(GMAx96-GMAx128)	/ 32 × 13 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	13	+	GMAx128
116	(GMAx96-GMAx128)	/ 32 × 12 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	12	+	GMAx128
117	(GMAx96-GMAx128)	/ 32 × 11 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	11	+	GMAx128
118	(GMAx96-GMAx128)	/ 32 × 10 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	10	+	GMAx128
119	(GMAx96-GMAx128)	/ 32 × 9 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	9	+	GMAx128
120	(GMAx96-GMAx128)	/ 32 × 8 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	8	+	GMAx128
121	(GMAx96-GMAx128)	/ 32 × 7 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	7	+	GMAx128
122	(GMAx96-GMAx128)	/ 32 × 6 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	6	+	GMAx128
123	(GMAx96-GMAx128)	/ 32 × 5 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	5	+	GMAx128
124	(GMAx96-GMAx128)	/ 32 × 4 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	4	+	GMAx128
125	(GMAx96-GMAx128)	/ 32 × 3 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	3	+	GMAx128
126	(GMAx96-GMAx128)	/ 32 × 2 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	2	+	GMAx128
127	(GMAx96-GMAx128)	/ 32 × 1 +	GMAx128	(GMAx96-GMAx128)	/ 32 ×	1	+	GMAx128
128	GMAx128			GMAx128				
129	(GMAx128-GMAx160)	/ 32 × 31 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	31	+	GMAx160
130	(GMAx128-GMAx160)	/ 32 × 30 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	30	+	GMAx160
131	(GMAx128-GMAx160)	/ 32 × 29 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	29	+	GMAx160
132	(GMAx128-GMAx160)	/ 32 × 28 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	28	+	GMAx160
133	(GMAx128-GMAx160)	/ 32 × 27 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	27	+	GMAx160
134	(GMAx128-GMAx160)	/ 32 × 26 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	26	+	GMAx160
135	(GMAx128-GMAx160)	/ 32 × 25 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	25	+	GMAx160
136	(GMAx128-GMAx160)	/ 32 × 24 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	24	+	GMAx160
137	(GMAx128-GMAx160)	/ 32 × 23 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	23	+	GMAx160
138	(GMAx128-GMAx160)	/ 32 × 22 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	22	+	GMAx160

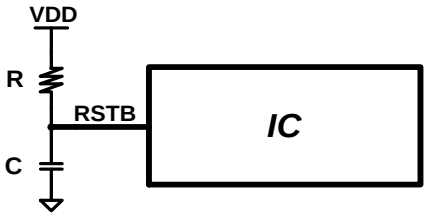
139	(GMAx128-GMAx160)	/ 32 × 21 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	21	+	GMAx160
140	(GMAx128-GMAx160)	/ 32 × 20 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	20	+	GMAx160
141	(GMAx128-GMAx160)	/ 32 × 19 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	19	+	GMAx160
142	(GMAx128-GMAx160)	/ 32 × 18 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	18	+	GMAx160
143	(GMAx128-GMAx160)	/ 32 × 17 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	17	+	GMAx160
144	(GMAx128-GMAx160)	/ 32 × 16 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	16	+	GMAx160
145	(GMAx128-GMAx160)	/ 32 × 15 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	15	+	GMAx160
146	(GMAx128-GMAx160)	/ 32 × 14 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	14	+	GMAx160
147	(GMAx128-GMAx160)	/ 32 × 13 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	13	+	GMAx160
148	(GMAx128-GMAx160)	/ 32 × 12 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	12	+	GMAx160
149	(GMAx128-GMAx160)	/ 32 × 11 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	11	+	GMAx160
150	(GMAx128-GMAx160)	/ 32 × 10 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	10	+	GMAx160
151	(GMAx128-GMAx160)	/ 32 × 9 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	9	+	GMAx160
152	(GMAx128-GMAx160)	/ 32 × 8 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	8	+	GMAx160
153	(GMAx128-GMAx160)	/ 32 × 7 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	7	+	GMAx160
154	(GMAx128-GMAx160)	/ 32 × 6 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	6	+	GMAx160
155	(GMAx128-GMAx160)	/ 32 × 5 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	5	+	GMAx160
156	(GMAx128-GMAx160)	/ 32 × 4 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	4	+	GMAx160
157	(GMAx128-GMAx160)	/ 32 × 3 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	3	+	GMAx160
158	(GMAx128-GMAx160)	/ 32 × 2 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	2	+	GMAx160
159	(GMAx128-GMAx160)	/ 32 × 1 +	GMAx160	(GMAx128-GMAx160)	/ 32 ×	1	+	GMAx160
160	GMAx160			GMAx160				
161	(GMAx160-GMAx192)	/ 32 × 31 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	31	+	GMAx192
162	(GMAx160-GMAx192)	/ 32 × 30 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	30	+	GMAx192
163	(GMAx160-GMAx192)	/ 32 × 29 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	29	+	GMAx192
164	(GMAx160-GMAx192)	/ 32 × 28 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	28	+	GMAx192
165	(GMAx160-GMAx192)	/ 32 × 27 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	27	+	GMAx192
166	(GMAx160-GMAx192)	/ 32 × 26 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	26	+	GMAx192
167	(GMAx160-GMAx192)	/ 32 × 25 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	25	+	GMAx192
168	(GMAx160-GMAx192)	/ 32 × 24 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	24	+	GMAx192
169	(GMAx160-GMAx192)	/ 32 × 23 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	23	+	GMAx192
170	(GMAx160-GMAx192)	/ 32 × 22 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	22	+	GMAx192
171	(GMAx160-GMAx192)	/ 32 × 21 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	21	+	GMAx192
172	(GMAx160-GMAx192)	/ 32 × 20 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	20	+	GMAx192
173	(GMAx160-GMAx192)	/ 32 × 19 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	19	+	GMAx192
174	(GMAx160-GMAx192)	/ 32 × 18 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	18	+	GMAx192
175	(GMAx160-GMAx192)	/ 32 × 17 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	17	+	GMAx192
176	(GMAx160-GMAx192)	/ 32 × 16 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	16	+	GMAx192
177	(GMAx160-GMAx192)	/ 32 × 15 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	15	+	GMAx192
178	(GMAx160-GMAx192)	/ 32 × 14 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	14	+	GMAx192

179	(GMAx160-GMAx192)	/ 32 × 13 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	13	+	GMAx192
180	(GMAx160-GMAx192)	/ 32 × 12 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	12	+	GMAx192
181	(GMAx160-GMAx192)	/ 32 × 11 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	11	+	GMAx192
182	(GMAx160-GMAx192)	/ 32 × 10 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	10	+	GMAx192
183	(GMAx160-GMAx192)	/ 32 × 9 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	9	+	GMAx192
184	(GMAx160-GMAx192)	/ 32 × 8 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	8	+	GMAx192
185	(GMAx160-GMAx192)	/ 32 × 7 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	7	+	GMAx192
186	(GMAx160-GMAx192)	/ 32 × 6 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	6	+	GMAx192
187	(GMAx160-GMAx192)	/ 32 × 5 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	5	+	GMAx192
188	(GMAx160-GMAx192)	/ 32 × 4 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	4	+	GMAx192
189	(GMAx160-GMAx192)	/ 32 × 3 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	3	+	GMAx192
190	(GMAx160-GMAx192)	/ 32 × 2 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	2	+	GMAx192
191	(GMAx160-GMAx192)	/ 32 × 1 +	GMAx192	(GMAx160-GMAx192)	/ 32 ×	1	+	GMAx192
192	GMAx192			GMAx192				
193	(GMAx192-GMAx208)	/ 16 × 15 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	15	+	GMAx208
194	(GMAx192-GMAx208)	/ 16 × 14 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	14	+	GMAx208
195	(GMAx192-GMAx208)	/ 16 × 13 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	13	+	GMAx208
196	(GMAx192-GMAx208)	/ 16 × 12 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	12	+	GMAx208
197	(GMAx192-GMAx208)	/ 16 × 11 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	11	+	GMAx208
198	(GMAx192-GMAx208)	/ 16 × 10 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	10	+	GMAx208
199	(GMAx192-GMAx208)	/ 16 × 9 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	9	+	GMAx208
200	(GMAx192-GMAx208)	/ 16 × 8 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	8	+	GMAx208
201	(GMAx192-GMAx208)	/ 16 × 7 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	7	+	GMAx208
202	(GMAx192-GMAx208)	/ 16 × 6 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	6	+	GMAx208
203	(GMAx192-GMAx208)	/ 16 × 5 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	5	+	GMAx208
204	(GMAx192-GMAx208)	/ 16 × 4 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	4	+	GMAx208
205	(GMAx192-GMAx208)	/ 16 × 3 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	3	+	GMAx208
206	(GMAx192-GMAx208)	/ 16 × 2 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	2	+	GMAx208
207	(GMAx192-GMAx208)	/ 16 × 1 +	GMAx208	(GMAx192-GMAx208)	/ 16 ×	1	+	GMAx208
208	GMAx208			GMAx208				
209	(GMAx208-GMAx224)	/ 16 × 15 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	15	+	GMAx224
210	(GMAx208-GMAx224)	/ 16 × 14 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	14	+	GMAx224
211	(GMAx208-GMAx224)	/ 16 × 13 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	13	+	GMAx224
212	(GMAx208-GMAx224)	/ 16 × 12 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	12	+	GMAx224
213	(GMAx208-GMAx224)	/ 16 × 11 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	11	+	GMAx224
214	(GMAx208-GMAx224)	/ 16 × 10 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	10	+	GMAx224
215	(GMAx208-GMAx224)	/ 16 × 9 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	9	+	GMAx224
216	(GMAx208-GMAx224)	/ 16 × 8 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	8	+	GMAx224
217	(GMAx208-GMAx224)	/ 16 × 7 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	7	+	GMAx224
218	(GMAx208-GMAx224)	/ 16 × 6 +	GMAx224	(GMAx208-GMAx224)	/ 16 ×	6	+	GMAx224

219	(GMAx208-GMAx224) / 16 × 5 + GMAx224	(GMAx208-GMAx224) / 16 × 5 + GMAx224
220	(GMAx208-GMAx224) / 16 × 4 + GMAx224	(GMAx208-GMAx224) / 16 × 4 + GMAx224
221	(GMAx208-GMAx224) / 16 × 3 + GMAx224	(GMAx208-GMAx224) / 16 × 3 + GMAx224
222	(GMAx208-GMAx224) / 16 × 2 + GMAx224	(GMAx208-GMAx224) / 16 × 2 + GMAx224
223	(GMAx208-GMAx224) / 16 × 1 + GMAx224	(GMAx208-GMAx224) / 16 × 1 + GMAx224
224	GMAx224	GMAx224
225	(GMAx224-GMAx240) / 16 × 15 + GMAx240	(GMAx224-GMAx240) / 16 × 15 + GMAx240
226	(GMAx224-GMAx240) / 16 × 14 + GMAx240	(GMAx224-GMAx240) / 16 × 14 + GMAx240
227	(GMAx224-GMAx240) / 16 × 13 + GMAx240	(GMAx224-GMAx240) / 16 × 13 + GMAx240
228	(GMAx224-GMAx240) / 16 × 12 + GMAx240	(GMAx224-GMAx240) / 16 × 12 + GMAx240
229	(GMAx224-GMAx240) / 16 × 11 + GMAx240	(GMAx224-GMAx240) / 16 × 11 + GMAx240
230	(GMAx224-GMAx240) / 16 × 10 + GMAx240	(GMAx224-GMAx240) / 16 × 10 + GMAx240
231	(GMAx224-GMAx240) / 16 × 9 + GMAx240	(GMAx224-GMAx240) / 16 × 9 + GMAx240
232	(GMAx224-GMAx240) / 16 × 8 + GMAx240	(GMAx224-GMAx240) / 16 × 8 + GMAx240
233	(GMAx224-GMAx240) / 16 × 7 + GMAx240	(GMAx224-GMAx240) / 16 × 7 + GMAx240
234	(GMAx224-GMAx240) / 16 × 6 + GMAx240	(GMAx224-GMAx240) / 16 × 6 + GMAx240
235	(GMAx224-GMAx240) / 16 × 5 + GMAx240	(GMAx224-GMAx240) / 16 × 5 + GMAx240
236	(GMAx224-GMAx240) / 16 × 4 + GMAx240	(GMAx224-GMAx240) / 16 × 4 + GMAx240
237	(GMAx224-GMAx240) / 16 × 3 + GMAx240	(GMAx224-GMAx240) / 16 × 3 + GMAx240
238	(GMAx224-GMAx240) / 16 × 2 + GMAx240	(GMAx224-GMAx240) / 16 × 2 + GMAx240
239	(GMAx224-GMAx240) / 16 × 1 + GMAx240	(GMAx224-GMAx240) / 16 × 1 + GMAx240
240	GMAx240	GMAx240
241	(GMAx240-GMAx244) / 4 × 3 + GMAx244	(GMAx240-GMAx244) / 4 × 3 + GMAx244
242	(GMAx240-GMAx244) / 4 × 2 + GMAx244	(GMAx240-GMAx244) / 4 × 2 + GMAx244
243	(GMAx240-GMAx244) / 4 × 1 + GMAx244	(GMAx240-GMAx244) / 4 × 1 + GMAx244
244	GMAx244	GMAx244
245	(GMAx244-GMAx248) / 4 × 3 + GMAx248	(GMAx244-GMAx248) / 4 × 3 + GMAx248
246	(GMAx244-GMAx248) / 4 × 2 + GMAx248	(GMAx244-GMAx248) / 4 × 2 + GMAx248
247	(GMAx244-GMAx248) / 4 × 1 + GMAx248	(GMAx244-GMAx248) / 4 × 1 + GMAx248
248	GMAx248	GMAx248
249	(GMAx248-GMAx252) / 4 × 3 + GMAx252	(GMAx248-GMAx252) / 4 × 3 + GMAx252
250	(GMAx248-GMAx252) / 4 × 2 + GMAx252	(GMAx248-GMAx252) / 4 × 2 + GMAx252
251	(GMAx248-GMAx252) / 4 × 1 + GMAx252	(GMAx248-GMAx252) / 4 × 1 + GMAx252
252	GMAx252	GMAx252
253	(GMAx252-GMAx255) / 3 × 2 + GMAx255	(GMAx252-GMAx255) / 3 × 2 + GMAx255
254	(GMAx252-GMAx255) / 3 × 1 + GMAx255	(GMAx252-GMAx255) / 3 × 1 + GMAx255
255	GMAx255	GMAx255

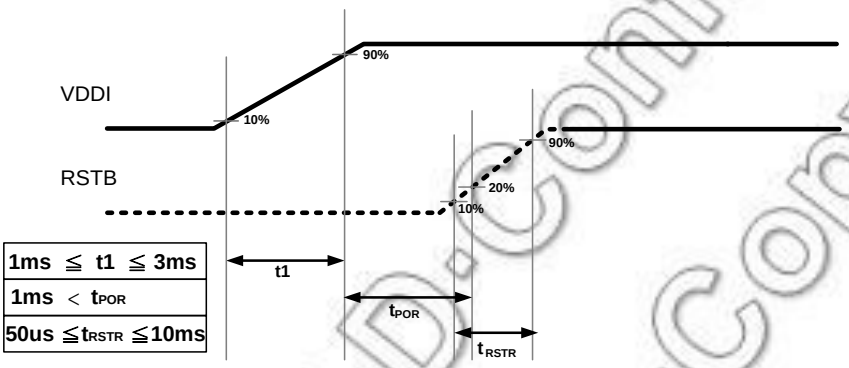
5.8 Reset

Setting RSTB pin to “L” (hardware reset) can initialize internal function. Generally, VDDI is not stable at the time that the system power is just turned ON. The hardware reset is required to initialize internal registers after VDDI is stable. Initialized by RSTB pin is essential before operating. There are two suggestions for the hardware reset connection. One is RSTB controlled by MCU. The other is connecting an external RC circuit with RSTB pin, and the recommended RC circuit is 47 KΩ ~ 200KΩ + 0.47uF. (For 1ms ≤ t1 ≤3ms)

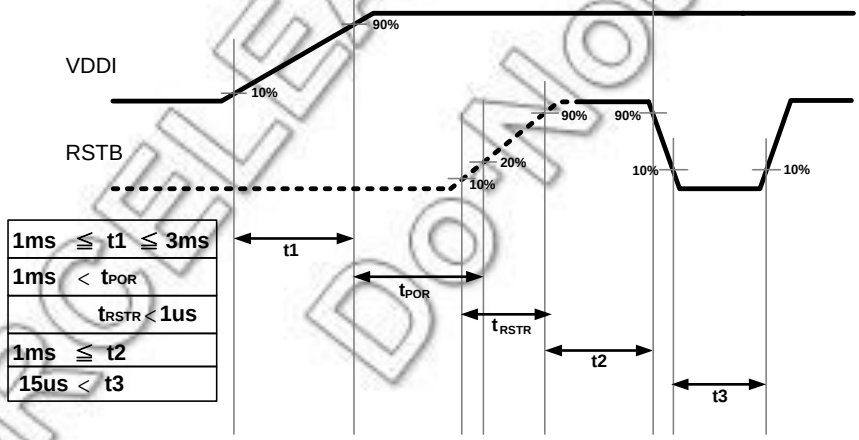


Recommend power on reset timing is shown as below.

* For RSTB pin +RC:

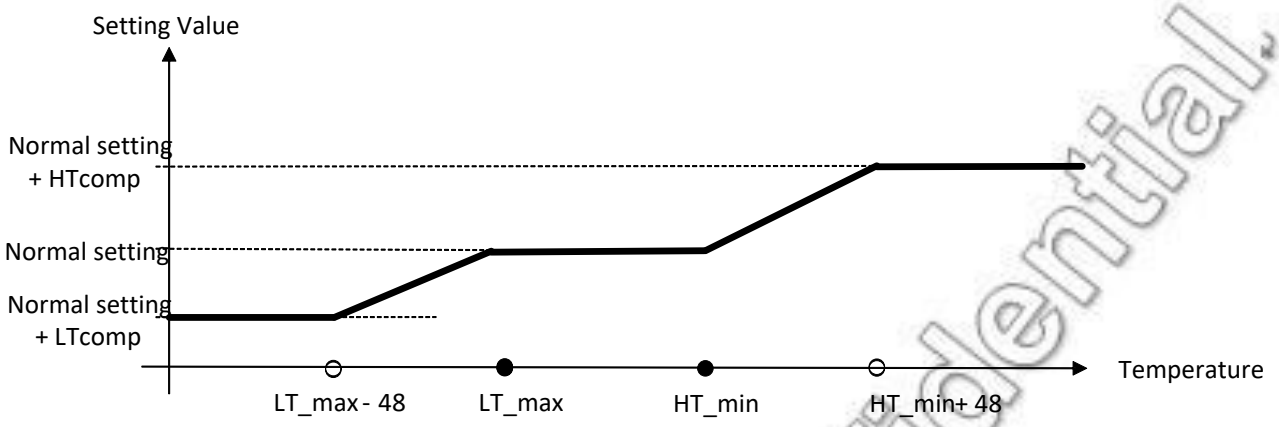


* For RSTB pin controlled by external MCU:



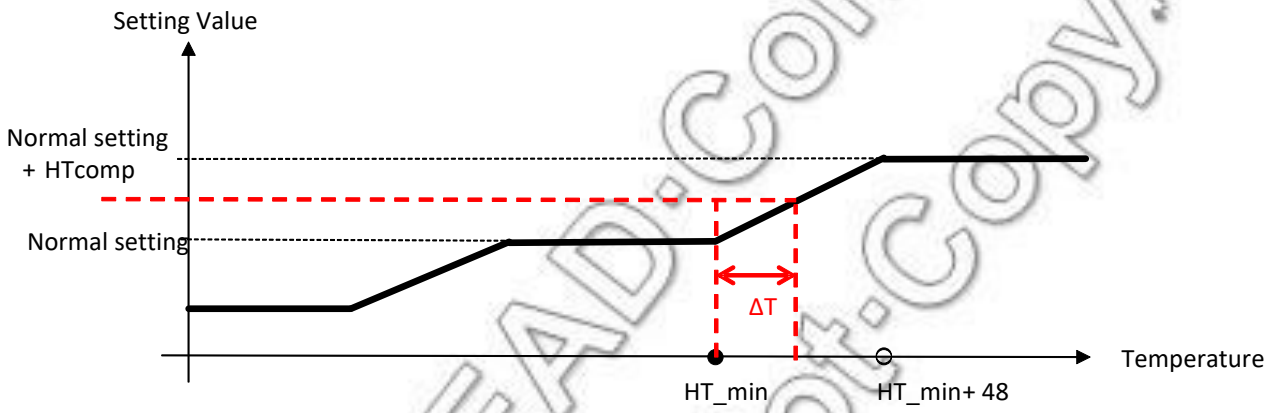
5.9 Temperature Compensation Function

Set “HT_min” and “LT_max” to define the minimum temperature of high temperature region and the maximum temperature of low temperature region. This chip changes the setting values of VCOM / VGMPHO /VGMNHO / VGH / VGL according to “HTcomp” or “LTcomp” when current temperature is in high or low temperature region.



The setting values change linearly as the temperature varies. For example, if the temperature is greater than “HT_min” by ΔT, then the new setting is as below:

Setting Value = Normal setting + (ΔT/48) * HTcomp

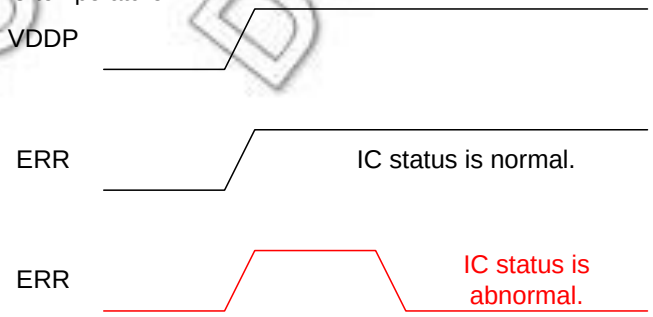


When the setting is changed, it begins to update the setting +1 or -1 every 64 frames until it reaches to new setting.

5.10 Function Safety

5.10.1 Error Feedback

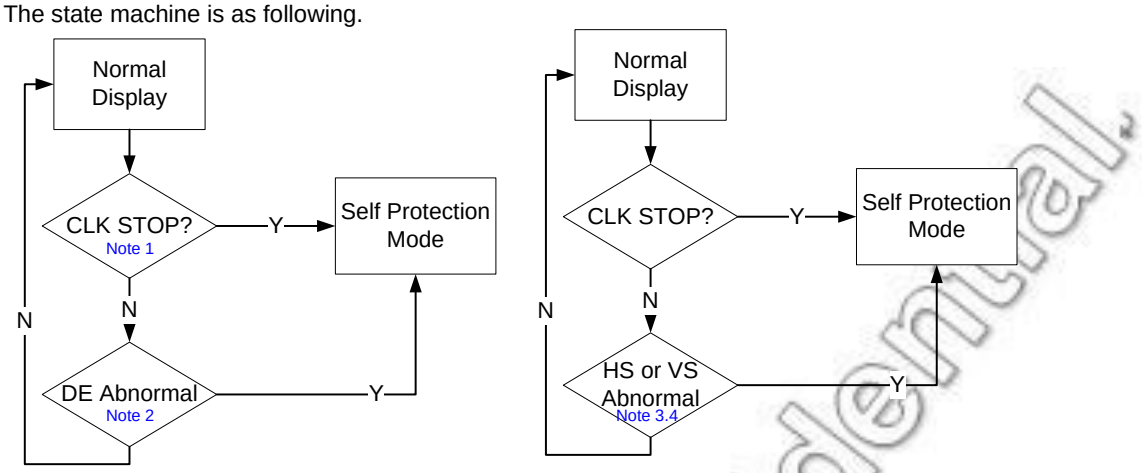
In order to satisfy the automotive safety requirement, this chip supports function detection and status feedback about not only data connectivity but also internal power and IC temperature. The ERR pin can indicate the IC operational status spontaneously. If the ERR pin keeps ‘H’ during power-on period, the IC can work well with good connectivity, proper internal power setting, and reasonable IC temperature.



Once ERR pin goes ‘L’, please read the IC status in register Page0, R29h. It can help assist system to find out or solve the problem.

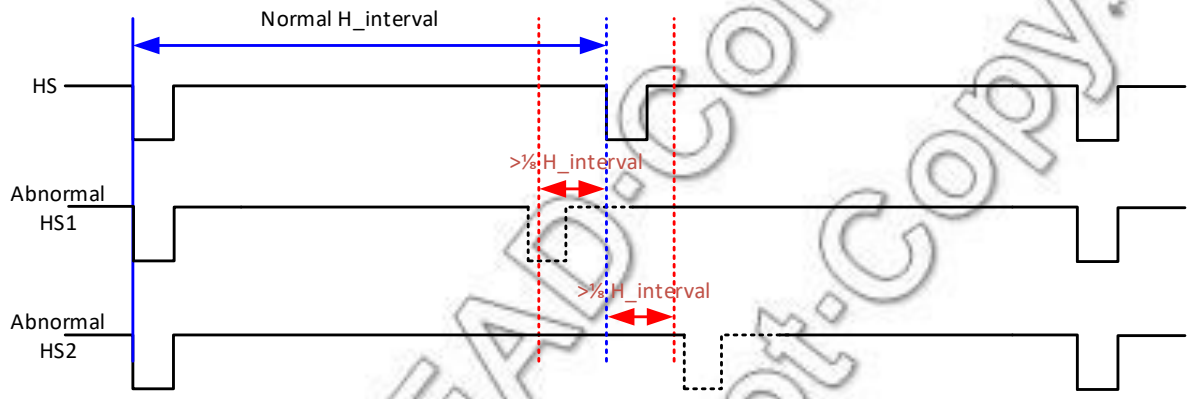
5.10.2 Fail Safe

This chip can detect DE, VS, HS, and CLK. If any of these signals is abnormal, it will enter self-protection mode and display black pattern. The state machine is as following.

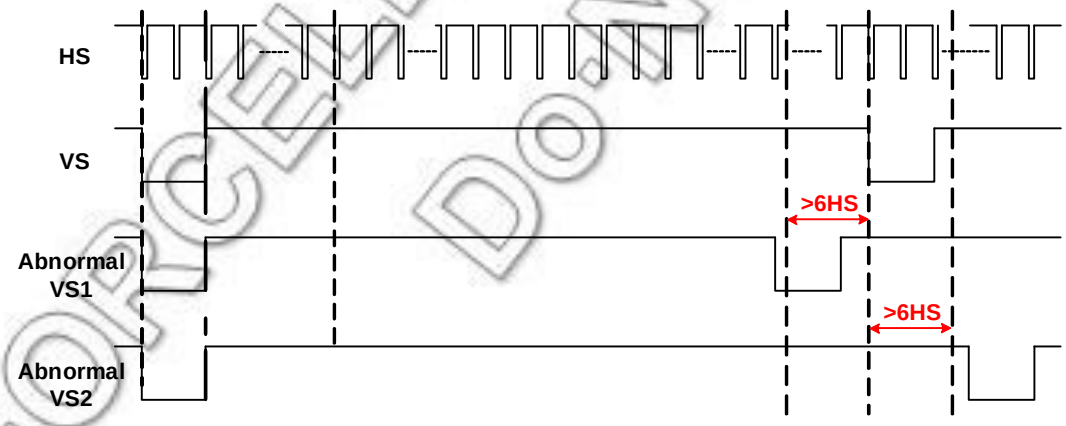


Note:

1. DCLK does not toggle over 20us, this chip will enter self-protection mode and display black pattern.
2. "DE abnormal" includes mismatch of DE high pulse width and H resolution, and mismatch of DE high pulse number and V resolution.
3. HS abnormal stands for HS interval being over the limitation as shown below (HFP tolerance= ±⅛ H_interval).

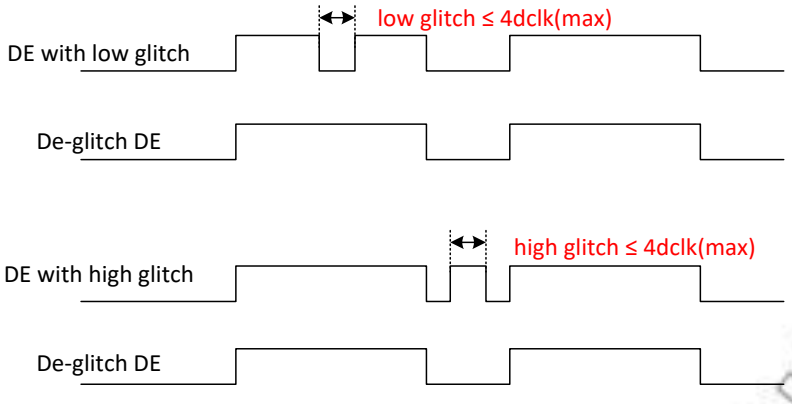


4. VS abnormal stands for VS interval being over the limitation as shown below (VFP tolerance= ±6*HS).



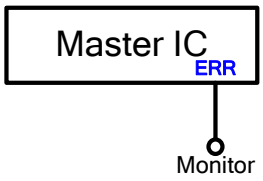
5.10.3 De-glitch

This chip supports de-glitch function in order to prevent the input signal such as VS, HS, or DE from the interference with glitch. The pulse width of glitch would be ignored by setting DEG_EN and DEGS[1:0].



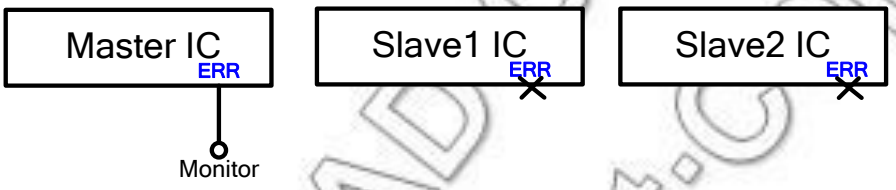
5.10.4 ERR Pin Connection

5.10.4.1 Single Chip Application

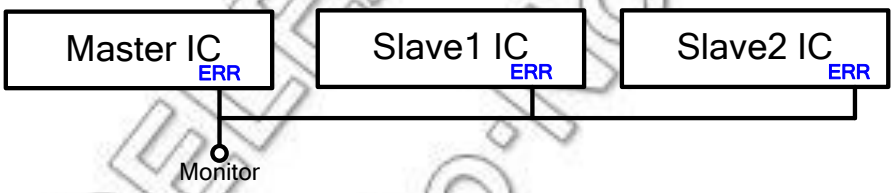


5.10.4.2 Cascade Application

Connection1:



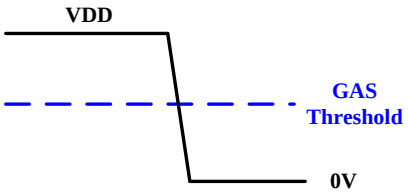
Connection2:



5.11 GAS Function

When the power voltage of VDD (3.3V) abnormal power off, that will cause the image still keeps on the LCD panel for a long time or next time power on quickly, LCD panel will be flicker display. GAS (Gate All Select) function can let the image disappears quickly and resolved flicker display.

This chip has VDD abnormal power off detection and send GIP signals to panel gate circuit by register setting. When GAS function is operating, it can discharge residual electricity in LCD panel.



6. REGISTER COMMAND

6.1 Register Command List

6.1.1 Page Section

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
00h	Page[3]	Page[2]	Page[1]	Page[0]	WALL	Reserved	AID[1:0]		F8h

6.1.2 Page 0

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	GDPOS[1:0]		MODE	RL	UD	GDSEL	HW_CTRL_XOR	BIST	00h
02h	EXT_PWR	Reserved	INV[1:0]		EXT_PWR2	ROM_RLD	IFSEL[1:0]		00h
03h	VESA	P_ON	P_OFF	MISS_DET_ON	NB	DEG_EN	DEGS[1:0]		70h
04h	DE_POL	VS_POL	HS_POL	CK_POL	MLSB	DISPON	BGR	BIT8	10h
05h	VACT[11:8]				RES[3:0]				20h
06h	VACT[7:1]							Reserved	D0h
07h	HACT[11:10]		Reserved	WRBYCID	VBP[8]	VFP[8]	HBP[8]	HFP[8]	40h
08h	HACT[9:2]								E0h
09h	VBP[7:0]								14h
0Ah	VFP[7:0]								14h
0Bh	HBP[7:0]								14h
0Ch	HFP[7:0]								14h
0Dh	ID1[7:0]								00h
0Eh	ID2[7:0]								00h
0Fh	Reserved	Reserved	Reserved	Reserved	Reserved	CPUS[1:0]		CPUS_XOR	00h
10h	BCK_DIV_PON[1:0]		BIST_PCYC[1:0]		BIST_PAT[3:0]				4Eh
11h	BIST_W[7:0]								FFh
12h	MSK_RX_ERR	MSK_RLD_ERR	MSK_VDD_LV	VSP_LV_ACT	VSN_LV_ACT	VGL_LV_ACT	VGH_LV_ACT	MSK_STV_ERR	00h
13h	MSK_DE_ERR	MSK_HS_ERR	MSK_VS_ERR	MSK_CK_ERR	MSK_MG_ERR	VSPN_ACT	VGHL_ACT	MSK_HT	00h
14h	MSK_LT	Reserved	PON_SKIP	FAST_PON[1:0]		STS_HOLD[2:0]			40h
15h	ERR_NORM_SEL[1:0]		ERR_ABN_SEL[1:0]		ERR_DETOFF	ERR_DETOFF_SEL	ERR_INITIAL	SEL_NEW_ERR	46h
16h	Reserved	Reserved	Reserved	Reserved	ADD_BHBLK[3:0]				80h
17h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
18h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	80h
19h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
1Ah	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	80h
1Bh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
1Ch	TP_EN	TP_SYNCV	TP_BLKEN	TP_INV	TP_ABENB	TP_OUT_SEL[2:0]			24h
1Dh	TPDLY[7:0]								09h
1Eh	TPHLD[7:0]								18h
1Fh	Reserved	Reserved	Reserved	SD_DET_EN	BVBLK_P1	TPDLY[10:8]			00h
20h	BCK_DIV[1:0]		2X_BHBLK	BIST_XTALK_W	BIST_VBLK[3:0]				47h

21h	VGMPHO_2ND_TRIM[2:0]			VGMNHO_2ND_TRIM[2:0]			V15D_RX_2ND_TRIM[1:0]		00h
22h	VGH_2ND_TRIM[1:0]		VGL_2ND_TRIM[1:0]		Reserved	VRSP_2ND_TRIM[2:0]			00h
23h	VRSN_2ND_TRIM[2:0]			TS_2ND_TRIM[4:0]					00h
24h~25h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
26h	RSTB								6Ch
27h	STBYB								A7h
28h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
29h	LT_ST	HT_ST	Reserved	STV_ST	DE_ST	VS_ST	HS_ST	CLK_ST	R/O
2Ah	TS_ENV[7:0]								R/O
2Bh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	R/O
2Ch	RLD_ST	LVDS_ST	Reserved	MERGE_ST	Reserved	Reserved	Reserved	Reserved	R/O
2Dh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	R/O
2Eh	Reserved	Reserved	Reserved	Reserved	VSP_LVB	VSN_LVB	VGL_LVB	VGH_LVB	R/O
2Fh	VGH_OVD	VGL_OVD	STB_ST	Reserved	Reserved	Reserved	Reserved	Reserved	R/O
30h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	R/O
31h	VGL_OK	VGH_OK	VSN_DEB_OK	VSP_DEB_OK	VSP_DEB_OCP	VSN_DEB_OCP	VSP_DEB_OVP	VSN_DEB_OVP	R/O
32h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	R/O
33h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	R/O
34h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	R/O
35h~3Dh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
3Eh	RGBCRC_GOLD_ALL[15:8]								00h
3Fh	RGBCRC_GOLD_ALL[7:0]								00h
40h	RGBCRC_EN_ALL[1:0]		RGBCRC_INI	RGBCRC_MODE_SEL_ALL	RGBCRC_ERR_CNT[1:0]		RGBCRC_SWAP[1:0]		20h
41h	RGBCRC_LSB	RGBCRC_MODE_SEL_1	RGBCRC_EN1[1:0]		RGBCRC_HST1[11:8]				00h
42h	RGBCRC_HST1[7:0]								00h
43h	Reserved	Reserved	Reserved	Reserved	RGBCRC_VST1[11:8]				00h
44h	RGBCRC_VST1[7:0]								00h
45h	Reserved	Reserved	Reserved	Reserved	RGBCRC_HEND1[11:8]				00h
46h	RGBCRC_HEND1[7:0]								00h
47h	Reserved	Reserved	Reserved	Reserved	RGBCRC_VEND1[11:8]				00h
48h	RGBCRC_VEND1[7:0]								00h
49h	RGBCRC_GOLD1[15:8]								00h
4Ah	RGBCRC_GOLD1[7:0]								00h
4Bh	Reserved	RGBCRC_MODE_SEL_2	RGBCRC_EN2[1:0]		RGBCRC_HST2[11:8]				00h
4Ch	RGBCRC_HST2[7:0]								00h
4Dh	Reserved	Reserved	Reserved	Reserved	RGBCRC_VST2[11:8]				00h
4Eh	RGBCRC_VST2[7:0]								00h
4Fh	Reserved	Reserved	Reserved	Reserved	RGBCRC_HEND2[11:8]				00h
50h	RGBCRC_HEND2[7:0]								00h
51h	Reserved	Reserved	Reserved	Reserved	RGBCRC_VEND2[11:8]				00h

52h	RGBCRC_VEND2[7:0]								00h
53h	RGBCRC_GOLD2[15:8]								00h
54h	RGBCRC_GOLD2[7:0]								00h
55h	Reserved	RGBCRC_MODE_SEL_3	RGBCRC_EN3[1:0]		RGBCRC_HST3[11:8]				00h
56h	RGBCRC_HST3[7:0]								00h
57h	Reserved	Reserved	Reserved	Reserved	RGBCRC_VST3[11:8]				00h
58h	RGBCRC_VST3[7:0]								00h
59h	Reserved	Reserved	Reserved	Reserved	RGBCRC_HEND3[11:8]				00h
5Ah	RGBCRC_HEND3[7:0]								00h
5Bh	Reserved	Reserved	Reserved	Reserved	RGBCRC_VEND3[11:8]				00h
5Ch	RGBCRC_VEND3[7:0]								00h
5Dh	RGBCRC_GOLD3[15:8]								00h
5Eh	RGBCRC_GOLD3[7:0]								00h
5Fh	Reserved	RGBCRC_MODE_SEL_4	RGBCRC_EN4[1:0]		RGBCRC_HST4[11:8]				00h
60h	RGBCRC_HST4[7:0]								00h
61h	Reserved	Reserved	Reserved	Reserved	RGBCRC_VST4[11:8]				00h
62h	RGBCRC_VST4[7:0]								00h
63h	Reserved	Reserved	Reserved	Reserved	RGBCRC_HEND4[11:8]				00h
64h	RGBCRC_HEND4[7:0]								00h
65h	Reserved	Reserved	Reserved	Reserved	RGBCRC_VEND4[11:8]				00h
66h	RGBCRC_VEND4[7:0]								00h
67h	RGBCRC_GOLD4[15:8]								00h
68h	RGBCRC_GOLD4[7:0]								00h
69h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
6Ah	CRC_NOW_RO_1[15:8]								R/O
6Bh	CRC_NOW_RO_1[7:0]								R/O
6Ch	CRC_NOW_RO_2[15:8]								R/O
6Dh	CRC_NOW_RO_2[7:0]								R/O
6Eh	CRC_NOW_RO_3[15:8]								R/O
6Fh	CRC_NOW_RO_3[7:0]								R/O
70h	CRC_NOW_RO_4[15:8]								R/O
71h	CRC_NOW_RO_4[7:0]								R/O
72h	CRC_ERR_FCNT_1[7:0]								R/O
73h	CRC_ERR_FCNT_2[7:0]								R/O
74h	CRC_ERR_FCNT_3[7:0]								R/O
75h	CRC_ERR_FCNT_4[7:0]								R/O
76h	CRC_NOW_RO_ALL[15:8]								R/O
77h	CRC_NOW_RO_ALL[7:0]								R/O
78h	CRC_ERR_FCNT_ALL[7:0]								R/O

Note：Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

6.1.3 Page 2

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	Reserved	R_GMA_BYP	x	x	x	x	GMAR0[9:8]		00h
02h	GMAR0[7:0]								71h
03h	x	x	x	x	x	x	GMAR4[9:8]		00h
04h	GMAR4[7:0]								74h
05h	x	x	x	x	x	x	GMAR8[9:8]		00h
06h	GMAR8[7:0]								7Fh
07h	x	x	x	x	x	x	GMAR12[9:8]		00h
08h	GMAR12[7:0]								97h
09h	x	x	x	x	x	x	GMAR16[9:8]		00h
0Ah	GMAR16[7:0]								BDh
0Bh	x	x	x	x	x	x	GMAR32[9:8]		01h
0Ch	GMAR32[7:0]								0Ch
0Dh	x	x	x	x	x	x	GMAR48[9:8]		01h
0Eh	GMAR48[7:0]								45h
0Fh	x	x	x	x	x	x	GMAR64[9:8]		01h
10h	GMAR64[7:0]								71h
11h	x	x	x	x	x	x	GMAR96[9:8]		01h
12h	GMAR96[7:0]								B0h
13h	x	x	x	x	x	x	GMAR128[9:8]		01h
14h	GMAR128[7:0]								E7h
15h	x	x	x	x	x	x	GMAR160[9:8]		02h
16h	GMAR160[7:0]								1Eh
17h	x	x	x	x	x	x	GMAR192[9:8]		02h
18h	GMAR192[7:0]								60h
19h	x	x	x	x	x	x	GMAR208[9:8]		02h
1Ah	GMAR208[7:0]								8Bh
1Bh	x	x	x	x	x	x	GMAR224[9:8]		02h
1Ch	GMAR224[7:0]								C0h
1Dh	x	x	x	x	x	x	GMAR240[9:8]		03h
1Eh	GMAR240[7:0]								0Ch
1Fh	x	x	x	x	x	x	GMAR244[9:8]		03h
20h	GMAR244[7:0]								27h
21h	x	x	x	x	x	x	GMAR248[9:8]		03h
22h	GMAR248[7:0]								46h
23h	x	x	x	x	x	x	GMAR252[9:8]		03h
24h	GMAR252[7:0]								71h
25h	x	x	x	x	x	x	GMAR255[9:8]		03h
26h	GMAR255[7:0]								B4h

Note：Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

6.1.4 Page 3

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	Reserved	x	x	x	x	x	GMAG0[9:8]		00h
02h	GMAG0[7:0]								71h
03h	x	x	x	x	x	x	GMAG4[9:8]		00h
04h	GMAG4[7:0]								74h
05h	x	x	x	x	x	x	GMAG8[9:8]		00h
06h	GMAG8[7:0]								7Fh
07h	x	x	x	x	x	x	GMAG12[9:8]		00h
08h	GMAG12[7:0]								97h
09h	x	x	x	x	x	x	GMAG16[9:8]		00h
0Ah	GMAG16[7:0]								BDh
0Bh	x	x	x	x	x	x	GMAG32[9:8]		01h
0Ch	GMAG32[7:0]								0Ch
0Dh	x	x	x	x	x	x	GMAG48[9:8]		01h
0Eh	GMAG48[7:0]								45h
0Fh	x	x	x	x	x	x	GMAG64[9:8]		01h
10h	GMAG64[7:0]								71h
11h	x	x	x	x	x	x	GMAG96[9:8]		01h
12h	GMAG96[7:0]								B0h
13h	x	x	x	x	x	x	GMAG128[9:8]		01h
14h	GMAG128[7:0]								E7h
15h	x	x	x	x	x	x	GMAG160[9:8]		02h
16h	GMAG160[7:0]								1Eh
17h	x	x	x	x	x	x	GMAG192[9:8]		02h
18h	GMAG192[7:0]								60h
19h	x	x	x	x	x	x	GMAG208[9:8]		02h
1Ah	GMAG208[7:0]								8Bh
1Bh	x	x	x	x	x	x	GMAG224[9:8]		02h
1Ch	GMAG224[7:0]								C0h
1Dh	x	x	x	x	x	x	GMAG240[9:8]		03h
1Eh	GMAG240[7:0]								0Ch
1Fh	x	x	x	x	x	x	GMAG244[9:8]		03h
20h	GMAG244[7:0]								27h
21h	x	x	x	x	x	x	GMAG248[9:8]		03h
22h	GMAG248[7:0]								46h
23h	x	x	x	x	x	x	GMAG252[9:8]		03h
24h	GMAG252[7:0]								71h

25h	x	x	x	x	x	x	GMAG255[9:8]	03h
26h	GMAG255[7:0]							B4h

Note：Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

6.1.5 Page 4

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	Reserved	x	x	x	x	x	GMAB0[9:8]		00h
02h	GMAB0[7:0]								71h
03h	x	x	x	x	x	x	GMAB4[9:8]		00h
04h	GMAB4[7:0]								74h
05h	x	x	x	x	x	x	GMAB8[9:8]		00h
06h	GMAB8[7:0]								7Fh
07h	x	x	x	x	x	x	GMAB12[9:8]		00h
08h	GMAB12[7:0]								97h
09h	x	x	x	x	x	x	GMAB16[9:8]		00h
0Ah	GMAB16[7:0]								BDh
0Bh	x	x	x	x	x	x	GMAB32[9:8]		01h
0Ch	GMAB32[7:0]								0Ch
0Dh	x	x	x	x	x	x	GMAB48[9:8]		01h
0Eh	GMAB48[7:0]								45h
0Fh	x	x	x	x	x	x	GMAB64[9:8]		01h
10h	GMAB64[7:0]								71h
11h	x	x	x	x	x	x	GMAB96[9:8]		01h
12h	GMAB96[7:0]								B0h
13h	x	x	x	x	x	x	GMAB128[9:8]		01h
14h	GMAB128[7:0]								E7h
15h	x	x	x	x	x	x	GMAB160[9:8]		02h
16h	GMAB160[7:0]								1Eh
17h	x	x	x	x	x	x	GMAB192[9:8]		02h
18h	GMAB192[7:0]								60h
19h	x	x	x	x	x	x	GMAB208[9:8]		02h
1Ah	GMAB208[7:0]								8Bh
1Bh	x	x	x	x	x	x	GMAB224[9:8]		02h
1Ch	GMAB224[7:0]								C0h
1Dh	x	x	x	x	x	x	GMAB240[9:8]		03h
1Eh	GMAB240[7:0]								0Ch
1Fh	x	x	x	x	x	x	GMAB244[9:8]		03h
20h	GMAB244[7:0]								27h
21h	x	x	x	x	x	x	GMAB248[9:8]		03h
22h	GMAB248[7:0]								46h

23h	x	x	x	x	x	x	GMAB252[9:8]	03h
24h	GMAB252[7:0]							71h
25h	x	x	x	x	x	x	GMAB255[9:8]	03h
26h	GMAB255[7:0]							B4h

Note：Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

6.1.6 Page 5

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
02h	GOUTL02_SEL[1:0]		GOUTL01_SEL[5:0]						FFh
03h	GOUTL03_SEL[3:0]				GOUTL02_SEL[5:2]				FFh
04h	GOUTL03_SEL[5:4]		GOUTL04_SEL[5:0]						FFh
05h	GOUTL06_SEL[1:0]		GOUTL05_SEL[5:0]						FFh
06h	GOUTL07_SEL[3:0]				GOUTL06_SEL[5:2]				FFh
07h	GOUTL07_SEL[5:4]		GOUTL08_SEL[5:0]						FFh
08h	GOUTL10_SEL[1:0]		GOUTL09_SEL[5:0]						FFh
09h	GOUTL11_SEL[3:0]				GOUTL10_SEL[5:2]				FFh
0Ah	GOUTL11_SEL[5:4]		GOUTL12_SEL[5:0]						FFh
0Bh	GOUTL14_SEL[1:0]		GOUTL13_SEL[5:0]						FFh
0Ch	GOUTL15_SEL[3:0]				GOUTL14_SEL[5:2]				FFh
0Dh	GOUTL15_SEL[5:4]		GOUTL16_SEL[5:0]						FFh
0Eh	GOUTL18_SEL[1:0]		GOUTL17_SEL[5:0]						FFh
0Fh	GOUTL19_SEL[3:0]				GOUTL18_SEL[5:2]				FFh
10h	GOUTL19_SEL[5:4]		GOUTL20_SEL[5:0]						FFh
11h	GIP_SR_L[1:0]		GIP_CSH_SEL_L[1:0]		GIP_CSL_SEL_L[1:0]		GIP_CS_EN_L[1:0]		68h
12h	GIP_CS_EN_L[9:2]								00h
13h	Reserved	Reserved	Reserved	Reserved	VSP_SEL[3:0]				0Ah
14h	Reserved	Reserved	Reserved	Reserved	VSN_SEL[3:0]				0Ah
15h	Reserved	Reserved	Reserved	VGH_SEL[4:0]					0Ah
16h	Reserved	Reserved	Reserved	Reserved	VGL_SEL[3:0]				0Ah
17h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
18h	Reserved	Reserved	VCOM_EN_ID[1:0]		Reserved	VCOM_DRV[2:0]			03h
19h	Reserved	Reserved	Reserved	TS_EN	TS_HYS_FRM[1:0]		TS_HYS[1:0]		05h
1Ah	Reserved	HTWARN_MIN[6:0]							69h
1Bh	LTWARN_MAX[7:0]								D8h
1Ch	Reserved	HT_MIN[6:0]							3Ch
1Dh	LT_MAX[7:0]								00h
1Eh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1Eh
1Fh	Reserved	Reserved	VCOM_HYS_FRM[1:0]		VCOM_FRM[3:0]				10h
20h	VCOM_OFFS[7:0]								00h

21h	Reserved	HTVCOM_EN	HTVCOM[5:0]						00h
22h	Reserved	LTVCOM_EN	LTVCOM[5:0]						00h
23h	VGM_HT_EN	VGM_LT_EN	Reserved	VGMPHO_HT[4:0]					00h
24h	VGMPLO_HT[4]	VGMNLO_HT[4]	Reserved	VGMNHO_HT[4:0]					00h
25h	VGMPLO_HT[3:0]				VGMNLO_HT[3:0]				00h
26h	VGHL_HT_EN	VGHL_LT_EN	Reserved	VGMPHO_LT[4:0]					00h
27h	VGMPLO_LT[4]	VGMNLO_LT[4]	Reserved	VGMNHO_LT[4:0]					00h
28h	VGMPLO_LT[3:0]				VGMNLO_LT[3:0]				00h
29h	Reserved	Reserved	Reserved	HT_VGH_SEL[4:0]					0Ah
2Ah	Reserved	Reserved	Reserved	LT_VGH_SEL[4:0]					0Ah
2Bh	HT_VGL_SEL[3:0]				LT_VGL_SEL[3:0]				AAh
2Ch	Reserved	Reserved	Reserved	Reserved	VGM_HYS_FRM[1:0]		Reserved	Reserved	01h
2Dh	Reserved	VREF_VSP_OCP_SEL[2:0]			Reserved	VREF_VSN_OCP_SEL[2:0]			22h
2Eh	VREF_VSP_ON_THR[1:0]		VREF_VSN_ON_THR[1:0]		Reserved	Reserved	Reserved	Reserved	00h
2Fh	OTP_VCOM_TIMES[7:0]								R/O
30h	1ST_VCOM_SEL[7:0]								5Fh
31h	2ND_VCOM_SEL[7:0]								00h
32h	3RD_VCOM_SEL[7:0]								00h

Note：Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

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Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OTP_PWR_RDY_TO_WR	OTP_AUTO_WRITE	00h
02h	OTP_PWR_RDY_FLAG	Reserved	Reserved	Reserved	AUTO_WR_EN_FLAG	Reserved	Reserved	MARGIN_READY_OK	00h
03h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OTP_READ	00h
04h	OTP_RD_DATA[7:0]								00h
05h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RDADDR[8]	00h
06h	RDADDR[7:0]								FFh
07h	SINGLE_WRITE[7:0]								00h
08h	PROG_NUM_COUNT[7:0]								00h
0Dh	OTP_PASSWORD1								55h
0Eh	OTP_PASSWORD2								AAh
0Fh	OTP_NOT_RLD								55h
10h	SOFT-WARE RELOAD SETTING[7:0]								00h
11h	OTP_SINGLE_WR_DIN[7:0]								00h

Note：Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

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Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	PFM_VSP_DUTY[3]	Reserved	PFM_VSP_TOFF_DUTY[1:0]		PFM_VSN_DUTY[3]	Reserved	PFM_VSN_TOFF_DUTY[1:0]		00h
02h	GOUTR02_SER[1:0]		GOUTR01_SER[5:0]						FFh

03h	GOUTR03_SER[3:0]				GOUTR02_SER[5:2]				FFh
04h	GOUTR03_SER[5:4]		GOUTR04_SER[5:0]						FFh
05h	GOUTR06_SER[1:0]		GOUTR05_SER[5:0]						FFh
06h	GOUTR07_SER[3:0]				GOUTR06_SER[5:2]				FFh
07h	GOUTR07_SER[5:4]		GOUTR08_SER[5:0]						FFh
08h	GOUTR10_SER[1:0]		GOUTR09_SER[5:0]						FFh
09h	GOUTR11_SER[3:0]				GOUTR10_SER[5:2]				FFh
0Ah	GOUTR11_SER[5:4]		GOUTR12_SER[5:0]						FFh
0Bh	GOUTR14_SER[1:0]		GOUTR13_SER[5:0]						FFh
0Ch	GOUTR15_SER[3:0]				GOUTR14_SER[5:2]				FFh
0Dh	GOUTR15_SER[5:4]		GOUTR16_SER[5:0]						FFh
0Eh	GOUTR18_SER[1:0]		GOUTR17_SER[5:0]						FFh
0Fh	GOUTR19_SER[3:0]				GOUTR18_SER[5:2]				FFh
10h	GOUTR19_SER[5:4]		GOUTR20_SER[5:0]						FFh
11h	GIP_SR_R[1:0]		GIP_CSH_SEL_R[1:0]		GIP_CSL_SEL_R[1:0]		GIP_CS_EN_R[1:0]		68h
12h	GIP_CS_EN_R[9:2]								00h
13h	VRSP_SEL[3:0]				VRSN_SEL[3:0]				DDh
14h	PFM_VSP_DUTY_CTL_EN	PFM_VSP_TOFF_EN	VSP_CMPR_SEL	HPFM_EN	PFM_VSN_DUTY_CTL_EN	PFM_VSN_TOFF_EN	VSN_CMPR_SEL	PFM_DIVF	00h
15h	VGMPHO_SEL[3:0]				VGMNHO_SEL[3:0]				DDh
16h	VGMPLO_SEL[3:0]				VGMNLO_SEL[3:0]				11h
17h	PFM_VSP_DUTY[2:0]			PFM_VSP_FREQ[2:0]			PFM_VSP_CYC[1:0]		ADh
18h	PFM_VSP_OCP_EN	PFM_OVP_EN	PFM_DRVP_Buf[1:0]		PFM_VSP_EN	PFM_VSN_EN	PFM_DRVN_Buf[1:0]		EEh
19h	PFM_VSN_DUTY2:0]			PFM_VSN_FREQ[2:0]			PFM_VSN_CYC[1:0]		ADh
1Ah	LVD_VSP_EN	LVD_VSP_SET[2:0]			GAS_VDD_EN	GAS_VDD_SET[2:0]			4Ch
1Bh	LVD_VSN_EN	LVD_VSN_SET[2:0]			LVD_VGL_EN	LVD_VGL_SET[2:1]		Reserved	43h
1Ch	VDD_LV_SEL[1:0]		GAS_SCALE[1:0]		LVD_VGH_EN	LVD_VGH_SET[2:0]			04h
1Dh	Reserved	Reserved	VSN_DEB_FREQ[1:0]		Reserved	VSN_DEB_EN	Reserved	Reserved	10h
1Eh	PFM_VSN_OCP_EN	PFM_OCP_DEB[2:0]			PFM_SEQ_EN	PFM_OVP_DEB[2:0]			B3h
1Fh	Reserved	Reserved	PFM_VSP_PD_EN	PFM_VSN_PD_EN	OCP_PROT_EN	PFM_OK_DEB[2:0]			33h
20h	Reserved	Reserved	PFM_VSN_DEB_SEL[1:0]		Reserved	Reserved	PFM_VSN_HYS_SEL[1:0]		00h
21h	VSP_ADD_NUM[3:0]				VSP_SUB_NUM[3:0]				00h
22h	VSN_ADD_NUM[3:0]				VSN_SUB_NUM[3:0]				00h
23h	Reserved	PFM_VSP_2ND_TRIM[2:0]			Reserved	PFM_VSP_VOF_SEL[2:0]			03h
24h	Reserved	PFM_VSN_2ND_TRIM[2:0]			Reserved	PFM_VSN_VOF_SEL[2:0]			03h
25h	CP_VGH_RATIO_SEL[1:0]		CP_VGH_MODE_SEL[1:0]		Reserved	CP_VGH_CLK[2:0]			74h
26h	CP_VGL_RATIO_SEL	CP_VGL_MODE_SEL	Reserved	Reserved	Reserved	CP_VGL_CLK[2:0]			C4h
27h	CP_VGH_OVD	CP_VGL_OVD	CP_OVD_DEB[2:0]			CP_OK_DEB[2:0]			D2h
28h	CP_VGH_OVD_SEL[1:0]		CP_VGL_OVD_SEL[1:0]		CP_VGH_SR[1:0]		CP_VGL_SR[1:0]		0Fh
29h	CP_CLK_DLY[1:0]		CP_EN_TO_PD_DLY[2:0]			Reserved	Reserved	Reserved	84h

Note：Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

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Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	D3_SKEW_A_ID0[1:0]		D2_SKEW_A_ID0[1:0]		D1_SKEW_A_ID0[1:0]		D0_SKEW_A_ID0[1:0]		00h
02h	CK_SKEW_A_ID0[1:0]		D3_SKEW_B_ID0[1:0]		D2_SKEW_B_ID0[1:0]		D1_SKEW_B_ID0[1:0]		00h
03h	D0_SKEW_B_ID0[1:0]		CK_SKEW_B_ID0[1:0]		D3_SKEW_A_ID1[1:0]		D2_SKEW_A_ID1[1:0]		00h
04h	D1_SKEW_A_ID1[1:0]		D0_SKEW_A_ID1[1:0]		CK_SKEW_A_ID1[1:0]		D3_SKEW_B_ID1[1:0]		00h
05h	D2_SKEW_B_ID1[1:0]		D1_SKEW_B_ID1[1:0]		D0_SKEW_B_ID1[1:0]		CK_SKEW_B_ID1[1:0]		00h
06h	D3_SKEW_A_ID2[1:0]		D2_SKEW_A_ID2[1:0]		D1_SKEW_A_ID2[1:0]		D0_SKEW_A_ID2[1:0]		00h
07h	CK_SKEW_A_ID2[1:0]		D3_SKEW_B_ID2[1:0]		D2_SKEW_B_ID2[1:0]		D1_SKEW_B_ID2[1:0]		00h
08h	D0_SKEW_B_ID2[1:0]		CK_SKEW_B_ID2[1:0]		DLL_IF_ID3	DLL_IF_ID2	DLL_IF_ID1	DLL_IF_ID0	00h
09h	TR_ID3[1:0]		TR_ID2[1:0]		TR_ID1[1:0]		TR_ID0[1:0]		FFh
0Ah	Reserved	Reserved	Reserved	Reserved	D3_SKEW_A_ID3[1:0]		D2_SKEW_A_ID3[1:0]		00h
0Bh	D1_SKEW_A_ID3[1:0]		D0_SKEW_A_ID3[1:0]		CK_SKEW_A_ID3[1:0]		D3_SKEW_B_ID3[1:0]		00h
0Ch	D2_SKEW_B_ID3[1:0]		D1_SKEW_B_ID3[1:0]		D0_SKEW_B_ID3[1:0]		CK_SKEW_B_ID3[1:0]		00h
0Dh	Reserved	EN_LVDS_MX	DIO_SR[1:0]		TR_EN	LVDS_CKPOL	EN_LVDS_MX_VB	RX_DATSWAP	18h
20h	Reserved	MP_LANE[1:0]		MP_EoTP	Reserved	Reserved	Reserved	Reserved	03h

Note：Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

6.1.10 PageA

Address (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
01h	x	GMAP_A0[6:0]							00h
02h	x	GMAP_A2[6:0]							02h
03h	x	GMAP_A4[6:0]							04h
04h	x	GMAP_A8[6:0]							08h
05h	x	GMAP_A16[6:0]							10h
06h	x	GMAP_A24[6:0]							18h
07h	x	GMAP_A32[6:0]							00h
08h	x	GMAP_A48[6:0]							10h
09h	x	GMAP_A80[6:0]							10h
0Ah	x	GMAP_A128[6:0]							40h
0Bh	x	GMAP_A176[6:0]							70h
0Ch	x	GMAP_A208[6:0]							70h
0Dh	x	GMAP_A224[6:0]							70h
0Eh	x	GMAP_A232[6:0]							68h
0Fh	x	GMAP_A240[6:0]							70h
10h	x	GMAP_A248[6:0]							78h
11h	x	GMAP_A252[6:0]							7Ch
12h	x	GMAP_A254[6:0]							7Eh
13h	x	GMAP_A255[6:0]							7Fh
14h	x	GMAN_A0[6:0]							00h

15h	x	GMAN_A2[6:0]	02h
16h	x	GMAN_A4[6:0]	04h
17h	x	GMAN_A8[6:0]	08h
18h	x	GMAN_A16[6:0]	10h
19h	x	GMAN_A24[6:0]	18h
1Ah	x	GMAN_A32[6:0]	00h
1Bh	x	GMAN_A48[6:0]	10h
1Ch	x	GMAN_A80[6:0]	10h
1Dh	x	GMAN_A128[6:0]	40h
1Eh	x	GMAN_A176[6:0]	70h
1Fh	x	GMAN_A208[6:0]	70h
20h	x	GMAN_A224[6:0]	70h
21h	x	GMAN_A232[6:0]	68h
22h	x	GMAN_A240[6:0]	70h
23h	x	GMAN_A248[6:0]	78h
24h	x	GMAN_A252[6:0]	7Ch
25h	x	GMAN_A254[6:0]	7Eh
26h	x	GMAN_A255[6:0]	7Fh

6.2 Register Command Description

6.2.1 Page Selection

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	00h	Page[3]	Page[2]	Page[1]	Page[0]	WALL	Reserved	AID[1:0]	
Default		1	1	1	1	1	0	0	0

Description

Page[3:0]: Command page selection.

Page[3:0]	Function
0000	Page 0
0001	Page 1
0010	Page 2
…	…
1111	Page F (Default)

WALL: Write command setting for cascade structure.

WALL	Function
0	By CID setting
1	All Chip (Default)

AID[1:0]: Active chip ID.
When WALL=1, SPI/I2C writes all ICs.
When WALL=0, SPI/I2C Write/Read depends on CID[1:0]= AID[1:0].

AID[1]	AID[0]	Function
0	0	Master (Default)
0	1	Slave1
1	0	Slave2
1	1	Reserved

6.2.2 Page 0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	GDPOS[1:0]		MODE	RL	UD	GDSEL	HW_CTRL_XOR	BIST
Default		0	0	0	0	0	0	0	0

Description

GDPOS[1:0]: Gate driver location setting. (when HW_CTRL output is software)

GDPOS[1]	GDPOS[1] PIN	Output GDPOS[1]
0	0	0 (Default)
0	1	1
1	0	1
1	1	0
GDPOS[0]	GDPOS[0] PIN	Output GDPOS[0]
0	0	0
0	1	1
1	0	1
1	1	0

MODE: DE or SYNC mode. (when HW_CTRL output is software)

MODE	MODE PIN	Output MODE
0	0	0
0	1	1
1	0	1
1	1	0

RL: Source driver Left/Right scan sequence. (when HW_CTRL output is software)

RL	RL PIN	Output RL
0	0	0
0	**1**	**1**
1	0	1
1	1	0

UD: Gate UP or Down scan selection. (when HW_CTRL output is software)

UD	UD PIN	Output UD
0	0	0
0	**1**	**1**
1	0	1
1	1	0

GDSEL: GIP or Gate driver mode selection. (when HW_CTRL output is software)

GDSEL	GDSEL PIN	Output GDSEL
0	**0**	**0**
0	1	1
1	0	1
1	1	0

HW_CTRL_XOR: XOR with hardware pin HW_CTRL.

HW_CTRL_XOR	HW_CTRL PIN	Output HW_CTRL
0	0	Software
0	**1**	**Hardware**
1	0	Hardware
1	1	Software

BIST: BIST mode. (when HW_CTRL output is software)

BIST	BIST PIN	Output BIST
0	**0**	**0**
0	1	1
1	0	1
1	1	0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	02h	EXT_PWR	Reserved	INV[1:0]		EXT_PWR2	ROM_RLD	IFSEL[1:0]	
Default		0	0	0	0	0	0	0	0

Description

EXT_PWR: VSP/VSN power mode selection. (when HW_CTRL output is software)

EXT_PWR	EXT_PWR PIN	Output EXT_PWR
0	**0**	**0**
0	1	1
1	0	1
1	1	0

INV[1:0]: Inversion type. (when HW_CTRL output is software)

INV[1]	INV[1] PIN	Output INV[1]
0	0	0
0	**1**	**1**
1	0	1
1	1	0

INV[0]	INV[0] PIN	Output INV[0]
0	0	0
0	**1**	**1**
1	0	1
1	1	0

Note: Only valid in signal gate structure

EXT_PWR2: VGH/VGL power mode selection. (when HW_CTRL output is software)

EXT_PWR2	EXT_PWR2 PIN	Output EXT_PWR2
0	**0**	**0**
0	1	1
1	0	1
1	1	0

ROM_RLD: OTP reload. (when HW_CTRL output is software)

ROM_RLD	ROM_RLD PIN	Output ROM_RLD
0	**0**	**0**
0	1	1
1	0	1
1	1	0

IFSEL[1:0]: Interface selection. (when HW_CTRL output is software)

IFSEL[1]	IFSEL[1] PIN	Output IFSEL[1]
0	0	0
0	**1**	**1 (Default)**
1	0	1
1	1	0
IFSEL[0]	IFSEL[0] PIN	Output IFSEL[0]
0	0	0
0	**1**	**1**
1	0	1
1	1	0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	03h	VESA	P_ON	P_OFF	MISS_DET	NB	DEG_EN	DEGS[1:0]	
Default		0	1	1	1	0	0	0	0

Description

VESA: LVDS data format selection. (when HW_CTRL output is software)

VESA	VESA PIN	Data format
0	0	JEIDA
0	**1**	**VESA**
1	0	VESA
1	1	JEIDA

P_ON: Power on pattern.

P_ON	Power on pattern
0	White
1	Black **(Default)**

P_OFF: Power off pattern.

P_OFF	Power off pattern
0	White
1	**Black (Default)**

MISS_DET: Missing signal detection mode. Please refer to the section of 5.10.3

MISS_DET	Missing signal detection
0	Disable
1	**Enable (Default)**

NB: Panel type selection. (when HW_CTRL output is software)

NB	NB PIN	Output NB
0	0	0
0	**1**	**1**
1	0	1
1	1	0

DEG_EN: De-noise control. Please refer to the section of 5.10.3

DEG_EN	De-noise control
0	**Disable (Default)**
1	Enable

DEGS[1:0]: De-noise selection. Please refer to the section of 5.10.3

DEGS[1:0]	De-noise selection
0h	**1CLK (Default)**
1h	2CLK
2h	3CLK
3h	4CLK

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	04h	DE_POL	VS_POL	HS_POL	CK_POL	MLSB	DISPON	BGR	BIT8
Default		0	0	0	1	0	0	0	0

Description

DE_POL: DE input signal polarity inverse control.

DE_POL	DE polarity
0	**Normal (Default)**
1	Inverse

VS_POL: VS input signal polarity inverse control.

VS_POL	VS polarity
0	**Normal (Default)**
1	Inverse

HS_POL: HS input signal polarity inverse control.

HS_POL	HS polarity
0	**Normal (Default)**
1	Inverse

CK_POL: Clock polarity. (only for TTL interface)

CLK_POL	CLK polarity

0	latch data at clock falling edge
1	**latch data at clock rising edge (Default)**

MLSB: MSB to LSB sequence reverse control (only for TTL interface)

MLSB	MSB to LSB sequence
0	**Normal (Default)**
1	Inverse

DISPON: Display pattern control.

DISPON	Function
0	**Normal display (Default)**
1	Black pattern

BGR: Input data RGB to BGR mapping control.

BGR	Mapping
0	**RGB (Default)**
1	BGR

BIT8: Data format. (when HW_CTRL output is software)

BIT8	BIT8 PIN	Output BIT8
0	0	0
0	**1**	**1**
1	0	1
1	1	0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	05h	VACT[11:8]				RES[3:0]			
Default		0	0	1	0	0	0	0	0

Description

VACT[11:8]: Vertical display area setting. (MSB)
Note: VACT must be even setting.

RES[4:0]: Resolution selection. (when HW_CTRL output is software)

RES[3]	RES[3] PIN	Output RES[3]
0	**0**	**0**
0	1	1
1	0	1
1	1	0
RES[2]	RES[2] PIN	Output RES[2]
0	**0**	**0**
0	1	1
1	0	1
1	1	0
RES[1]	RES[1] PIN	Output RES[1]
0	0	0
0	**1**	**1**
1	0	1
1	1	0
RES[0]	RES[0] PIN	Output RES[0]
0	**0**	**0**
0	1	1
1	0	1

	1	1	0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	06h	VACT[7:1]							Reserved
Default		1	1	0	1	0	0	0	0
Description		**VACT[7:1]:** Vertical display area setting. (LSB) Note: VACT must be even setting.							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	07h	HACT[11:10]		Reserved	WRBYCID	VBP[8]	VFP[8]	HBP[8]	HFP[8]
Default		0	1	0	0	0	0	0	0
Description		**HACT[11:8]:** Horizontal display area setting. (MSB) Note: HACT min support 172xRGB. **WRBYCID:** Distinction chip ID identification by I2C or SPI. (when HW_CTRL output is software)							

WRBYCID	WRBYCID PIN	Output WRBYCID
0	0	0
0	1	1
1	**0**	**1**
1	1	0

VBP[8]: Vertical back porch setting. (MSB) (include Vsync width)

VFP[8]: Vertical front porch setting. (MSB)

HBP[8]: Horizontal back porch setting. (MSB) (include Vsync width)

HFP[8]: Horizontal front porch setting. (MSB)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	08h	HACT[9:2]							
Default		1	1	1	0	0	0	0	0
Description		**HACT[9:2]:** Horizontal display area setting. (LSB) Note: HACT min support 172xRGB.							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	09h	VBP[7:0]							
Default		0	0	0	1	0	1	0	0
Description		**VBP[7:0]:** Vertical back porch setting. (LSB) (include Vsync width)							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ah	VFP[7:0]							
Default		0	0	0	1	0	1	0	0
Description		**VFP[7:0]:** Vertical front porch setting (MSB)							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Bh	HBP[7:0]							
Default		0	0	0	1	0	1	0	0
Description		**HBP[7:0]:** Horizontal back porch setting. (LSB) (include Hsync width)							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ch	HFP[7:0]							
Default		0	0	0	1	0	1	0	0
Description		**HFP[7:0]:** Horizontal front porch setting. (LSB)							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Dh	ID1[7:0]							
Default		0	0	0	0	0	0	0	0
Description		**ID1[7:0]:** User ID1.							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Eh	ID2[7:0]							
Default		0	0	0	0	0	0	0	0
Description		**ID2[7:0]:**User ID2.							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Fh	Reserved	Reserved	Reserved	Reserved	Reserved	CPUS[1:0]		CPUS_XOR
Default		0	0	0	0	0	0	0	0

Description

CPUS[1:0]: Panel module total IC quantity selection.

CPUS[1]	CPUS[1] PIN	Output CPUS[1]
0	**0**	**0**
0	1	1
1	0	1
1	1	0
CPUS[0]	CPUS[0] PIN	Output CPUS[0]
0	**0**	**0**
0	1	1
1	0	1
1	1	0

CPUS_XOR: CPUS[1:0] setting function control selection.

CPUS_XOR	Fucntion
0	**Hardware**
1	Software

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0

R/W	10h	BCK_DIV_PON[1:0]		BIST_PCYC[1:0]		BIST_PAT[3:0]			
Default		0	1	0	0	1	1	1	0

Description

BCK_DIV_PON[1:0]: Power on BIST clock selection

BCK_DIV_PON[1:0]	Function
0h	100Mhz
1h	**50MHz (Default)**
2h	25MHz
3h	12.5MHz

BIST_PCYC[1:0]: Set the time of each BIST pattern showing up when BIST pattern is in auto running cycle.

BIST_PCYC[1:0]	Function
0h	**128 frames (Default)**
1h	64 frames
2h	256 frames
3h	(Reserved)

BIST_PAT[3:0]: BIST pattern selection. Please refer to “BIST PATTERN TABLE” for details.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	11h	BIST_W[7:0]							
Default		1	1	1	1	1	1	1	1

Description

BIST_W[7:0]: Set grey level 0~255 of BIST White, Red, Green and Blue Pattern.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	12h	MSK_RX_ERR	MSK_RLD_ERR	MSK_VDD_LV	VSP_LV_ACT	VSN_LV_ACT	VGL_LV_ACT	VGH_LV_ACT	MSK_STV_ERR
Default		0	0	0	0	0	0	0	0

Description

MSK_RX_ERR: Mask Rx error.

MSK_RLD_ERR: Mask the MTP reload error.

MSK_VDD_LV: Mask VDD LVD (Low Voltage Detect) NG.

VSP_LV_ACT: Enable the behavior of VSP LVD (Low Voltage Detect) NG.

VSN_LV_ACT: Enable the behavior of VSN LVD (Low Voltage Detect) NG.

VGL_LV_ACT: Enable the behavior of VGL LVD (Low Voltage Detect) NG.

VGH_LV_ACT: Enable the behavior of VGH LVD (Low Voltage Detect) NG.

MSK_STV_ERR: Mask STV signal error.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	13h	MSK_DE_ERR	MSK_HS_ERR	MSK_VS_ERR	MSK_CK_ERR	MSK_MG_ERR	VSPN_ACT	VGHL_ACT	MSK_HT
Default		0	0	0	0	0	0	0	0

Description	**MSK_DE_ERR:** Mask DE signal error. **MSK_HS_ERR:** Mask HS signal error. **MSK_VS_ERR:** Mask VS signal error. **MSK_CK_ERR:** Mask CLOCK stop error. **MSK_MG_ERR:** Mask LVDS 2 port merged error. **VSPN_ACT:** When LVD_VSP_EN=1 / LVD_VSN_EN=1 (REG.) VSP_LV_ACT / VSN_LV_ACT=0 & VSPN_ACT=X (REG.), IC reports error only. VSP_LV_ACT / VSN_LV_ACT=1 & VSPN_ACT=0 (REG.), IC reports error and displays black pattern. VSP_LV_ACT / VSN_LV_ACT=1 & VSPN_ACT=1 (REG.), IC reports error and does GAS. **MSK_HT:** Mask high temperature warring alarm.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	14h	MSK_LT	Reserved	PON_SKIP	FAST_PON[1:0]		STS_HOLD[2:0]		
Default		0	1	0	0	0	0	0	0

Description

MSK_LT: Mask low temperature warring alarm.

PON_SKIP: SKIP the power-on pattern.

FAST_PON[1:0]: Speed up the power-on sequence by ratios.

FAST_PON[1:0]	Function
0h	**1X Normal (Default)**
1h	2X
2h	4X
3h	Reserved

STS_HOLD[2:0]: Set the hold time of error status.

STS_HOLD[2:0]	Function
0h	**100ms (Default)**
1h	200ms
2h	400ms
3h	800ms
Others	Keeps holding

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	15h	ERR_NORM_SEL[1:0]		ERR_ABN_SEL[1:0]		ERR_DETOFF	ERR_DETOFF_SEL	Reserved	Reserved
Default		0	1	0	0	0	1	1	0

Description

RR_NORM_SEL[1:0]: ERR output selection in TCON Normal State.

ERR_NORM_SEL[1:0]	Function
0h	Low level
1h	**High level. (Default)**
2h	System VS signal (Active High)
3h	System VS signal (Active Low).

ERR_ABN_SEL: ERR output selection in TCON ABN (abnormal) State.

ERR_ABN_SEL[1:0]	Function

0h	**Low level (Default)**
1h	High level.
2h	BIST VS signal (Active High)
3h	BIST VS signal (Active Low).

ERR_DETOFF: Set ERR pin in Detection Off Mode or not.

ERR_DETOFF	Function
0	ERR pin is NOT in detection off mode. (Default)
1	ERR pin is in detection off mode.

ERR_DETOFF_SEL: ERR pin output selection in Detection Off Mode.

ERR_DETOFF_SEL	Function
0	Low level.
1	**High level. (Default)**

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	16h	Reserved	Reserved	Reserved	Reserved	ADD_BHBLK[3:0]			
Default		1	0	0	0	0	0	0	0

Description

ADD_BHBLK[3:0]: Add H-blanking time of BIST mode by setting with 0~15, i.e., H-blanking + (0~15)*8.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ch	TP_EN	TP_SYNCV	TP_BLKEN	TP_INV	TP_ABENB	TP_OUT_SEL[2:0]		
Default		0	0	1	0	0	1	0	0

Description

TP_EN: Enable or Disable TP_SYNC function.

TP_EN	Function
0	**Disable. (Default)**
1	Enable.

TP_SYNCV: TP_SYNC function control.

TP_SYNCV	Function
0	**TP_SYNC signal outputs once per each Line. (Default)**
1	TP_SYNC signal outputs once per each Frame.

TP_BLKEN: TP_SYNC output control in blanking area.

TP_BLKEN	Function
0	TP_SYNC does not output in blanking.
1	**TP_SYNC keeps outputting in blanking. (Default).**

TP_INV: TP_SYNC output polarity control.

TP_INV	TP_INV
0	**TP_SYNC positive polarity output. (Default)**
1	TP_SYNC negative polarity output.

TP_ABENB: TP_SYNC gating selection.

TP_ABENB	TP_INV
0	**When Abnormal is active, TP_SYNC keeps toggling. (Default)**
1	When Abnormal is active, TP_SYNC keeps low.

TP_OUT_SEL[2:0]: TP_SYNC output signal selection.

TP_OUT_SEL[2:0]	TP_SYNC output signal
0h	TP_SYNC signal (HS or VS by Register TP_SYNCV)
1h	ERR
2h	Gate driver XON signal (GDSEL=1) GIP GAS signal (GDSEL=0)
3h	V-Blanking
4h	**Internal LD signal (Default)**
Others	(Reserved)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Dh	TPDLY[7:0]							
Default		0	0	0	0	1	0	0	1

Description

TPDLY[7:0]: 8 bits of TPDLY[10:0].

TPDLY[10:0]: Set TP_SYNC rising edge delay time.

When TP_SYNCV=0, (TP_SYNC signal outputs once per each Line)

TPDLY[10:0]	TP_SYNC rising edge delay time
7FFh	2047 Pixel Clock
7FEh	2046 Pixel Clock
⋮	⋮
09h	**9 Pixel Clock (Default)**
08h	8 Pixel Clock
⋮	⋮
01h	1 Pixel Clock
00h	1 Pixel Clock

Note: TPDLY+TPHLD < Htotal

When TP_SYNCV=1, (TP_SYNC signal outputs once per each Frame.)

TPDLY[10:0]	TP_SYNC rising edge delay time
7FFh	2047 HS
7FEh	2046 HS
⋮	⋮
09h	**9 HS (Default)**
08h	8 HS
⋮	⋮
01h	1 HS
00h	1 HS

Note: TPDLY+TPHLD < Vtotal

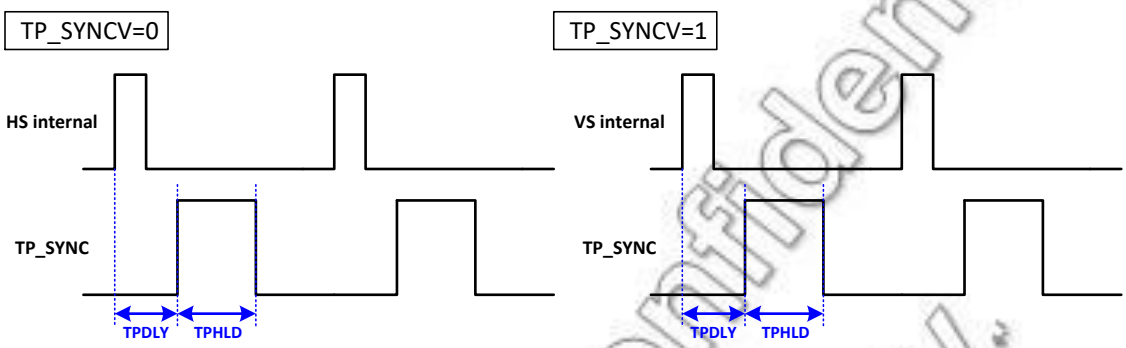
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Eh	TPHLD[7:0]							
Default		0	0	0	1	1	0	0	0

Description

R_TPHLD[7:0]: Set TP_SYNC high period holding time.

R_TPHLD[7:0]	TP_SYNC holding time
FFh	255 Pixel Clock
FEh	254 Pixel Clock
⋮	⋮
18h	**24 Pixel Clock (Default)**
⋮	⋮
01h	1 Pixel Clock
00h	1 Pixel Clock

Note: TPDLY+TPHLD < Vtotal



Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Fh	Reserved	Reserved	Reserved	SD_DET_EN	BVBLK_P1	TPDLY[10:8]		
Default		0	0	0	0	0	0	0	0

Description

SD_DET_EN: Enable or Disable STH_ERR status.

SD_DET_EN	Function
0	**Disable. (Default)**
1	Enable.

BVBLK_P1: Add one V-blanking time of BIST mode or not by setting.

BVBLK_P1	Function
0	**Keep original V-blanking (Default)**
1	V-blanking+1.

TPDLY[10:8]: 3 bits of TPDLY[10:0].
(See the description of Page 0 Add. 1Eh.)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	20h	BCK_DIV[1:0]		2X_BHBLK	BIST_XTALK_W	BIST_VBLK[3:0]			
Default		0	1	0	0	0	1	1	1

Description

BCK_DIV[1:0]: BIST clock selection.

BCK_DIV[1:0]	Function
0h	Divided by 1 (75MHz).
1h	**Divided by 2 (37.5MHz, Default)**
2h	Divided by 4 (18.75MHz)
3h	Divided by 8 (9.375MHz).

2X_BHBLK: Enable the H-blanking time of BIST mode X2 selection.

BIST_XTALK_W: In Crosstalk pattern of BIST mode, set center for black or white pattern.

BIST_XTALK_W	Function
0	**Black (Default).**
1	White

BIST_VBLK[3:0]: Set BIST V-blanking lines.
Note: V-blanking lines in BIST mode = 8* BIST_VBLK[3:0] + BVBLK_P1

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	21h	VGMPHO_2ND_TRIM[2:0]			VGMNHO_2ND_TRIM[2:0]			V15D_RX_2ND_TRIM[1:0]	
Default		0	0	0	0	0	0	0	0

Description

VGMPHO_2ND_TRIM[2:0]: Trim adjustment of VGMPHO voltage.

VGMPHO_2ND_TRIM[2:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Add 3 step trim voltage
4h	Add 4 step trim voltage
5h	Add 5 step trim voltage
6h	Subtract 1 step trim voltage
7h	Subtract 2 step trim voltage

VGMNHO_2ND_TRIM[2:0]: Trim adjustment of VGMNHO voltage.

VGMNHO_2ND_TRIM[2:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Add 3 step trim voltage
4h	Add 4 step trim voltage
5h	Add 5 step trim voltage
6h	Subtract 1 step trim voltage
7h	Subtract 2 step trim voltage

V15D_RX_2ND_TRIM[1:0]: Trim adjustment of V15D_RX voltage.

V15D_RX_2ND_TRIM[1:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Subtract 1 step trim voltage

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	22h	VGH_2ND_TRIM[1:0]		VGL_2ND_TRIM[1:0]		Reserved	VRSP_2ND_TRIM[2:0]		
Default		0	0	0	0	0	0	0	0

Description

VGH_2ND_TRIM[1:0]: Trim adjustment of VGH voltage.

VGH_2ND_TRIM[1:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Subtract 1 step trim voltage

VGL_2ND_TRIM[1:0]: Trim adjustment of VGL voltage.

VGL_2ND_TRIM[1:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Subtract 1 step trim voltage

VRSP_2ND_TRIM[2:0]: Trim adjustment of VRSP voltage.

VRSP_2ND_TRIM[2:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Add 3 step trim voltage
4h	Add 4 step trim voltage
5h	Add 5 step trim voltage
6h	Subtract 1 step trim voltage
7h	Subtract 2 step trim voltage

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	23h	VRSN_2ND_TRIM[2:0]			TS_2ND_TRIM[4:0]				
Default		0	0	0	0	0	0	0	0

Description

VRSN_2ND_TRIM[2:0]: Trim adjustment of VRSN voltage.

VRSN_2ND_TRIM[2:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Add 3 step trim voltage
4h	Add 4 step trim voltage
5h	Add 5 step trim voltage
6h	Subtract 1 step trim voltage
7h	Subtract 2 step trim voltage

TS_2ND_TRIM[4:0]: Trim adjustment of Temperature Sensor.
TS_2ND_TRIM[4]=1: Add trim adjustment value.
TS_2ND_TRIM[4]=0: Subtract trim adjustment value.
TS_2ND_TRIM[3:0]: Trim adjustment value.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	26h	RSTB							
Default		0	1	1	0	1	1	0	0

Description

RSTB	Function
93h	Reset
Others	**Normal Operation (Default)**

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	27h	STBYB							

Default	1	0	1	0	0	1	1	1

Description

STBYB	Function
58h	Standby
Others	Normal Operation (Default)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	29h	LT_ST	HT_ST	Reserved	STV_ST	DE_ST	VS_ST	HS_ST	CLK_ST
Default		0	0	0	0	0	0	0	0

Description

LT_ST: Low temperature status, it is read only.

LT_ST	Status
0	Normal (Default)
1	Abnormal

HT_ST: High temperature status, it is read only.

HT_ST	Status
0	Normal (Default)
1	Abnormal

STV_ST: STV signal status, it is read only.

STV_ST	Status
0	Normal (Default)
1	Abnormal

DE_ST: DE signal status, it is read only.

DE_ST	Status
0	Normal (Default)
1	Abnormal

VS_ST: VS signal status, it is read only.

VS_ST	Status
0	Normal (Default)
1	Abnormal

HS_ST: HS signal status, it is read only.

HS_ST	Status
0	Normal (Default)
1	Abnormal

CLK_ST: CLK signal status, it is read only.

CLK_ST	Status
0	Normal (Default)
1	Abnormal

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	2Ah	TS[7:0]							
Default		0	0	0	0	0	0	0	0

Description	**TS[7:0]:** Read IC Temperature, it is read-only.

TS[7:0]	IC Temperature(°C)
7Fh	127
7Eh	126
7Dh	125
:	:
01h	1
00h	**0 (Default)**
FFh	-1
FEh	-2
:	:
82h	-126
81h	-127
80h	-128

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	2Ch	RLD_ST	LVDS_ST	Reserved	MERGE_ST	Reserved	Reserved	Reserved	Reserved
Default		0	0	0	0	0	0	0	0

Description

RLD_ST: Reload error status, it is read only.

RLD_ST	Status
0	**Normal (Default)**
1	Abnormal

LVDS_ST: LVDS RX error status, it is read only.

LVDS_ST	Status
0	**Normal (Default)**
1	Abnormal

MERGE_ST: LVDS 2-port merge error status, it is read only.

MERGE_ST	Status
0	**Normal (Default)**
1	Abnormal

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	2Eh	Reserved	Reserved	Reserved	Reserved	VSP_LVB	VSN_LVB	VGL_LVB	VGH_LVB
Default		0	0	0	0	0	0	0	0

Description

VSP_LVB: VSP low power error status, it is read only.

VSP_LVB	Status
0	**Normal (Default)**
1	Abnormal

VSN_LVB: VSN low power error status, it is read only.

VSN_LVB	Status
0	**Normal (Default)**
1	Abnormal

VGL_LVB: VGL low power error status, it is read only.

VGL_LVB	Status

	0 Normal (Default) 1 Abnormal VGH_LVB: VGH low power error status, it is read only. VGH_LVB / Status: 0 Normal (Default); 1 Abnormal

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	2Fh	VGH_OVD	VGL_OVD	STB_ST	Reserved	Reserved	Reserved	Reserved	Reserved
Default		0	0	1	0	0	0	0	0

Description

VGH_OVD: VGH over voltage error status, it is read only.

VGH_OVD	Status
0	Normal (Default)
1	Abnormal

VGL_OVD: VGL over voltage error status, it is read only.

VGL_OVD	Status
0	Normal (Default)
1	Abnormal

STB_ST: Standby status, it is read only.

STB_ST	Status
0	Non-Standby
1	Standby (Default)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	31h	VGL_OK	VGH_OK	VSN_DEB_OK	VSP_DEB_OK	VSP_DEB_OCP	VSN_DEB_OCP	VSP_DEB_OVP	VSN_DEB_OVP
Default		0	0	0	0	0	0	0	0

Description

VGL_OK: VGL status, it is read only.

VGL_OK	Status
0	Normal (Default)
1	Abnormal

VGH_OK: VGH status, it is read only.

VGH_OK	Status
0	Normal (Default)
1	Abnormal

VSN_DEB_OK: VSN status, it is read only.

VSN_DEB_OK	Status
0	Non-Standby (Default)
1	Standby

VSP_DEB_OK: VSP status, it is read only.

VSP_DEB_OK	Status
0	Non-Standby (Default)

1	Standby

VSN_DEB_OCP: VSN OCP function status, it is read only.

VSN_DEB_OCP	Status
0	Non-Standby (Default)
1	Standby

VSP_DEB_OCP: VSP OCP function status, it is read only.

VSP_DEB_OCP	Status
0	Non-Standby (Default)
1	Standby

VSN_DEB_OVP: VSN OVP function status, it is read only.

VSN_DEB_OVP	Status
0	Non-Standby (Default)
1	Standby

VSP_DEB_OVP: VSP OVP function status, it is read only.

VSP_DEB_OVP	Status
0	Non-Standby (Default)
1	Standby

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	3Eh~68h	RGB CRC related control registers.							
Default		-	-	-	-	-	-	-	-
Description		For this function, please consult Forcelead about the register settings							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	6Ah~78h	RGB CRC related control registers.							
Default		-	-	-	-	-	-	-	-
Description		(Read only) For this function, please consult Forcelead about the register settings							

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Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	Reserved	GMA_BYP_TMP	x	x	x	x	GMAR0[9:8]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	02h	GMAR0[7:0]							
Default		0	1	1	1	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	03h	x	x	x	x	x	x	GMAR4[9:8]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	04h	GMAR4[7:0]							

Default		0	1	1	1	0	1	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**05h**	x	x	x	x	x	x	GMAR8[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**06h**	GMAR8[7:0]							
Default		0	1	1	1	1	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**07h**	x	x	x	x	x	x	GMAR12[9:8]	
Default		0	0	0	0	0	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**08h**	GMAR12[7:0]							
Default		1	0	0	1	0	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**09h**	x	x	x	x	x	x	GMAR16[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Ah**	GMAR16[7:0]							
Default		1	0	1	1	1	1	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Bh**	x	x	x	x	x	x	GMAR32[9:8]	
Default		0	0	0	0	0	0	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Ch**	GMAR32[7:0]							
Default		0	0	0	0	1	1	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Dh**	x	x	x	x	x	x	GMAR48[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Eh**	GMAR48[7:0]							
Default		0	1	0	0	0	1	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Fh**	x	x	x	x	x	x	GMAR64[9:8]	
Default		0	0	0	0	0	0	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**10h**	GMAR64[7:0]							
Default		0	1	1	1	0	0	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**11h**	x	x	x	x	x	x	GMAR96[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**12h**	GMAR96[7:0]							
Default		1	0	1	1	0	0	0	0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	13h	x	x	x	x	x	x	GMAR128[9:8]	
Default		0	0	0	0	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	14h	GMAR128[7:0]							
Default		1	1	1	0	0	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	15h	x	x	x	x	x	x	GMAR160[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	16h	GMAR160[7:0]							
Default		0	0	0	1	1	1	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	17h	x	x	x	x	x	x	GMAR192[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	18h	GMAR192[7:0]							
Default		0	1	1	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	19h	x	x	x	x	x	x	GMAR208[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ah	GMAR208[7:0]							
Default		1	0	0	0	1	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Bh	x	x	x	x	x	x	GMAR224[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ch	GMAR224[7:0]							
Default		1	1	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Dh	x	x	x	x	x	x	GMAR240[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Eh	GMAR240[7:0]							
Default		0	0	0	0	1	1	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Fh	x	x	x	x	x	x	GMAR244[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	20h	GMAR244[7:0]							
Default		0	0	1	0	0	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0

R/W	21h	x	x	x	x	x	x	GMAR248[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	22h	GMAR248[7:0]							
Default		0	1	0	0	0	1	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	23h	x	x	x	x	x	x	GMAR252[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	24h	GMAR252[7:0]							
Default		0	1	1	1	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	25h	x	x	x	x	x	x	GMAR255[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	26h	GMAR255[7:0]							
Default		1	0	1	1	0	1	0	0

Description

GMA_BYP_TMP: Enable to bypass digital gamma. (Data Out = Data In)

GMA_BYP_TMP	Function
0	Disable (Default)
1	Enable

GMAR0[9:0]: Digital gamma correction register of Red color for data code 255 when NBW=1, or code 0 when NBW=0.
GMAR4[9:0]: Digital gamma correction register of Red color for data code 251 when NBW=1, or code 4 when NBW=0.
GMAR8[9:0]: Digital gamma correction register of Red color for data code 247 when NBW=1, or code 8 when NBW=0.
GMAR12[9:0]: Digital gamma correction register of Red color for data code 243 when NBW=1, or code 12 when NBW=0.
GMAR16[9:0]: Digital gamma correction register of Red color for data code 239 when NBW=1, or code 16 when NBW=0.
GMAR32[9:0]: Digital gamma correction register of Red color for data code 223 when NBW=1, or code 32 when NBW=0.
GMAR48[9:0]: Digital gamma correction register of Red color for data code 207 when NBW=1, or code 48 when NBW=0.
GMAR64[9:0]: Digital gamma correction register of Red color for data code 191 when NBW=1, or code 64 when NBW=0.
GMAR96[9:0]: Digital gamma correction register of Red color for data code 159 when NBW=1, or code 96 when NBW=0.
GMAR128[9:0]: Digital gamma correction register of Red color for data code 127 when NBW=1, or code 128 when NBW=0.
GMAR160[9:0]: Digital gamma correction register of Red color for data code 95 when NBW=1, or code 160 when NBW=0.
GMAR192[9:0]: Digital gamma correction register of Red color for data code 63 when NBW=1, or code 192 when NBW=0.
GMAR208[9:0]: Digital gamma correction register of Red color for data code 47 when NBW=1, or code 208 when NBW=0.
GMAR224[9:0]: Digital gamma correction register of Red color for data code 31 when NBW=1, or code 224 when NBW=0.
GMAR240[9:0]: Digital gamma correction register of Red color for data code 15 when NBW=1, or code 240 when NBW=0.
GMAR244[9:0]: Digital gamma correction register of Red color for data code 11 when NBW=1, or code 244 when NBW=0.
GMAR248[9:0]: Digital gamma correction register of Red color for data code 7 when NBW=1, or code 248 when NBW=0.
GMAR252[9:0]: Digital gamma correction register of Red color for data code 3 when NBW=1, or code 252 when NBW=0.
GMAR255[9:0]: Digital gamma correction register of Red color for data code 0 when NBW=1, or code 255 when NBW=0.

Note: Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

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Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	Reserved	x	x	x	x	x	GMAG0[9:8]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	02h	GMAG0[7:0]							

Default		0	1	1	1	0	0	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**03h**	x	x	x	x	x	x	GMAG4[9:8]	
Default		0	0	0	0	0	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**04h**	GMAG4[7:0]							
Default		0	1	1	1	0	1	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**05h**	x	x	x	x	x	x	GMAG8[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**06h**	GMAG8[7:0]							
Default		0	1	1	1	1	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**07h**	x	x	x	x	x	x	GMAG12[9:8]	
Default		0	0	0	0	0	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**08h**	GMAG12[7:0]							
Default		1	0	0	1	0	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**09h**	x	x	x	x	x	x	GMAG16[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Ah**	GMAG16[7:0]							
Default		1	0	1	1	1	1	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Bh**	x	x	x	x	x	x	GMAG32[9:8]	
Default		0	0	0	0	0	0	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Ch**	GMAG32[7:0]							
Default		0	0	0	0	1	1	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Dh**	x	x	x	x	x	x	GMAG48[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Eh**	GMAG48[7:0]							
Default		0	1	0	0	0	1	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Fh**	x	x	x	x	x	x	GMAG64[9:8]	
Default		0	0	0	0	0	0	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**10h**	GMAG64[7:0]							
Default		0	1	1	1	0	0	0	1

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	11h	x	x	x	x	x	x	GMAG96[9:8]	
Default		0	0	0	0	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	12h	GMAG96[7:0]							
Default		1	0	1	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	13h	x	x	x	x	x	x	GMAG128[9:8]	
Default		0	0	0	0	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	14h	GMAG128[7:0]							
Default		1	1	1	0	0	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	15h	x	x	x	x	x	x	GMAG160[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	16h	GMAG160[7:0]							
Default		0	0	0	1	1	1	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	17h	x	x	x	x	x	x	GMAG192[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	18h	GMAG192[7:0]							
Default		0	1	1	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	19h	x	x	x	x	x	x	GMAG208[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ah	GMAG208[7:0]							
Default		1	0	0	0	1	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Bh	x	x	x	x	x	x	GMAG224[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ch	GMAG224[7:0]							
Default		1	1	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Dh	x	x	x	x	x	x	GMAG240[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Eh	GMAG240[7:0]							
Default		0	0	0	0	1	1	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0

R/W	1Fh	x	x	x	x	x	x	GMAG244[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	20h	GMAG244[7:0]							
Default		0	0	1	0	0	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	21h	x	x	x	x	x	x	GMAG248[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	22h	GMAG248[7:0]							
Default		0	1	0	0	0	1	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	23h	x	x	x	x	x	x	GMAG252[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	24h	GMAG252[7:0]							
Default		0	1	1	1	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	25h	x	x	x	x	x	x	GMAG255[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	26h	GMAG255[7:0]							
Default		1	0	1	1	0	1	0	0

Description	**GMAG0[9:0]:** Digital gamma correction register of Green color for data code 255 when NBW=1, or code 0 when NBW=0. **GMAG4[9:0]:** Digital gamma correction register of Green color for data code 251 when NBW=1, or code 4 when NBW=0. **GMAG8[9:0]:** Digital gamma correction register of Green color for data code 247 when NBW=1, or code 8 when NBW=0. **GMAG12[9:0]:** Digital gamma correction register of Green color for data code 243 when NBW=1, or code 12 when NBW=0. **GMAG16[9:0]:** Digital gamma correction register of Green color for data code 239 when NBW=1, or code 16 when NBW=0. **GMAG32[9:0]:** Digital gamma correction register of Green color for data code 223 when NBW=1, or code 32 when NBW=0. **GMAG48[9:0]:** Digital gamma correction register of Green color for data code 207 when NBW=1, or code 48 when NBW=0. **GMAG64[9:0]:** Digital gamma correction register of Green color for data code 191 when NBW=1, or code 64 when NBW=0. **GMAG96[9:0]:** Digital gamma correction register of Green color for data code 159 when NBW=1, or code 96 when NBW=0. **GMAG128[9:0]:** Digital gamma correction register of Green color for data code 127 when NBW=1, or code 128 when NBW=0. **GMAG160[9:0]:** Digital gamma correction register of Green color for data code 95 when NBW=1, or code 160 when NBW=0. **GMAG192[9:0]:** Digital gamma correction register of Green color for data code 63 when NBW=1, or code 192 when NBW=0. **GMAG208[9:0]:** Digital gamma correction register of Green color for data code 47 when NBW=1, or code 208 when NBW=0. **GMAG224[9:0]:** Digital gamma correction register of Green color for data code 31 when NBW=1, or code 224 when NBW=0. **GMAG240[9:0]:** Digital gamma correction register of Green color for data code 15 when NBW=1, or code 240 when NBW=0. **GMAG244[9:0]:** Digital gamma correction register of Green color for data code 11 when NBW=1, or code 244 when NBW=0. **GMAG248[9:0]:** Digital gamma correction register of Green color for data code 7 when NBW=1, or code 248 when NBW=0. **GMAG252[9:0]:** Digital gamma correction register of Green color for data code 3 when NBW=1, or code 252 when NBW=0. **GMAG255[9:0]:** Digital gamma correction register of Green color for data code 0 when NBW=1, or code 255 when NBW=0. **Note:** Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

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Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	Reserved	x	x	x	x	x	GMAB0[9:8]	
Default		0	0	0	0	0	0	0	0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	02h	GMAB0[7:0]							
Default		0	1	1	1	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	03h	x	x	x	x	x	x	GMAB4[9:8]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	04h	GMAB4[7:0]							
Default		0	1	1	1	0	1	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	05h	x	x	x	x	x	x	GMAB8[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	06h	GMAB8[7:0]							
Default		0	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	07h	x	x	x	x	x	x	GMAB12[9:8]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	08h	GMAB12[7:0]							
Default		1	0	0	1	0	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	09h	x	x	x	x	x	x	GMAB16[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ah	GMAB16[7:0]							
Default		1	0	1	1	1	1	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Bh	x	x	x	x	x	x	GMAB32[9:8]	
Default		0	0	0	0	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ch	GMAB32[7:0]							
Default		0	0	0	0	1	1	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Dh	x	x	x	x	x	x	GMAB48[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Eh	GMAB48[7:0]							
Default		0	1	0	0	0	1	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Fh	x	x	x	x	x	x	GMAB64[9:8]	
Default		0	0	0	0	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0

R/W	10h	GMAB64[7:0]							
Default		0	1	1	1	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	11h	x	x	x	x	x	x	GMAB96[9:8]	
Default		0	0	0	0	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	12h	GMAB96[7:0]							
Default		1	0	1	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	13h	x	x	x	x	x	x	GMAB128[9:8]	
Default		0	0	0	0	0	0	0	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	14h	GMAB128[7:0]							
Default		1	1	1	0	0	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	15h	x	x	x	x	x	x	GMAB160[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	16h	GMAB160[7:0]							
Default		0	0	0	1	1	1	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	17h	x	x	x	x	x	x	GMAB192[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	18h	GMAB192[7:0]							
Default		0	1	1	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	19h	x	x	x	x	x	x	GMAB208[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ah	GMAB208[7:0]							
Default		1	0	0	0	1	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Bh	x	x	x	x	x	x	GMAB224[9:8]	
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ch	GMAB224[7:0]							
Default		1	1	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Dh	x	x	x	x	x	x	GMAB240[9:8]	
Default		0	0	0	0	0	0	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Eh	GMAB240[7:0]							

Default		0	0	0	0	1	1	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**1Fh**	x	x	x	x	x	x	GMAB244[9:8]	
Default		0	0	0	0	0	0	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**20h**	GMAB244[7:0]							
Default		0	0	1	0	0	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**21h**	x	x	x	x	x	x	GMAB248[9:8]	
Default		**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**22h**	GMAB248[7:0]							
Default		0	1	0	0	0	1	1	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**23h**	x	x	x	x	x	x	GMAB252[9:8]	
Default		0	0	0	0	0	0	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**24h**	GMAB252[7:0]							
Default		0	1	1	1	0	0	0	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**25h**	x	x	x	x	x	x	GMAB255[9:8]	
Default		0	0	0	0	0	0	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**26h**	GMAB255[7:0]							
Default		1	0	1	1	0	1	0	0

Description

GMAB0[9:0]: Digital gamma correction register of Blue color for data code 255 when NBW=1, or code 0 when NBW=0.
GMAB4[9:0]: Digital gamma correction register of Blue color for data code 251 when NBW=1, or code 4 when NBW=0.
GMAB8[9:0]: Digital gamma correction register of Blue color for data code 247 when NBW=1, or code 8 when NBW=0.
GMAB12[9:0]: Digital gamma correction register of Blue color for data code 243 when NBW=1, or code 12 when NBW=0.
GMAB16[9:0]: Digital gamma correction register of Blue color for data code 239 when NBW=1, or code 16 when NBW=0.
GMAB32[9:0]: Digital gamma correction register of Blue color for data code 223 when NBW=1, or code 32 when NBW=0.
GMAB48[9:0]: Digital gamma correction register of Blue color for data code 207 when NBW=1, or code 48 when NBW=0.
GMAB64[9:0]: Digital gamma correction register of Blue color for data code 191 when NBW=1, or code 64 when NBW=0.
GMAB96[9:0]: Digital gamma correction register of Blue color for data code 159 when NBW=1, or code 96 when NBW=0.
GMAB128[9:0]: Digital gamma correction register of Blue color for data code 127 when NBW=1, or code 128 when NBW=0.
GMAB160[9:0]: Digital gamma correction register of Blue color for data code 95 when NBW=1, or code 160 when NBW=0.
GMAB192[9:0]: Digital gamma correction register of Blue color for data code 63 when NBW=1, or code 192 when NBW=0.
GMAB208[9:0]: Digital gamma correction register of Blue color for data code 47 when NBW=1, or code 208 when NBW=0.
GMAB224[9:0]: Digital gamma correction register of Blue color for data code 31 when NBW=1, or code 224 when NBW=0.
GMAB240[9:0]: Digital gamma correction register of Blue color for data code 15 when NBW=1, or code 240 when NBW=0.
GMAB244[9:0]: Digital gamma correction register of Blue color for data code 11 when NBW=1, or code 244 when NBW=0.
GMAB248[9:0]: Digital gamma correction register of Blue color for data code 7 when NBW=1, or code 248 when NBW=0.
GMAB252[9:0]: Digital gamma correction register of Blue color for data code 3 when NBW=1, or code 252 when NBW=0.
GMAB255[9:0]: Digital gamma correction register of Blue color for data code 0 when NBW=1, or code 255 when NBW=0.

Note: Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

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Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	02h	GOUTL02_SEL[1:0]		GOUTL01_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	03h	GOUTL03_SEL[3:0]				GOUTL02_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	04h	GOUTL03_SEL[5:4]		GOUTL04_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	05h	GOUTL06_SEL[1:0]		GOUTL05_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	06h	GOUTL07_SEL[3:0]				GOUTL06_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	07h	GOUTL07_SEL[5:4]		GOUTL08_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	08h	GOUTL10_SEL[1:0]		GOUTL09_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	09h	GOUTL11_SEL[3:0]				GOUTL10_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ah	GOUTL11_SEL[5:4]		GOUTL12_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Bh	GOUTL14_SEL[1:0]		GOUTL13_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ch	GOUTL15_SEL[3:0]				GOUTL14_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Dh	GOUTL15_SEL[5:4]		GOUTL16_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Eh	GOUTL18_SEL[1:0]		GOUTL17_SEL[5:0]					

Default		1	1	1	1	1	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**0Fh**	GOUTL19_SEL[3:0]				GOUTL18_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**10h**	GOUTL19_SEL[5:4]		GOUTL20_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**11h**	GIP_SR_L[1:0]		GIP_CSH_SEL_L[1:0]		GIP_CSL_SEL_L[1:0]		GIP_CS_EN_L[1:0]	
Default		0	1	1	0	1	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**12h**	GIP_CS_EN_L[9:2]							
Default		0	0	0	0	0	0	0	0

Description

GOUTL01_SEL[5:0] ~ GOUTL20_SEL[5:0]: Select the output signal of GHV_L[1:20] pad.

GIP_SR_L[1:0]: Driving ability selection of GHV_L[01:20] outputs.

GIP_SR_L[1:0]	Function
0h	Output driving weakest
1h	**Output driving second weak (Default).**
2h	Output driving second strong.
3h	Output driving strongest.

GIP_CSH_SEL_L[1:0]: GIP CS high width.

GIP_CSH_SEL_L[1:0]	Function
0h	0 clock.
1h	1 clock.
2h	**2 clocks. (Default)**
3h	4 clocks

GIP_CSL_SEL_L[1:0]: GIP CS low width.

GIP_CSL_SEL_L[1:0]	Function
0h	0 clock.
1h	1 clock.
2h	**2 clocks. (Default)**
3h	4 clocks

GIP_CS_EN_L[9:0]: GIP CS function enable for GHV_L[1:20].

Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**13h**	Reserved	Reserved	Reserved	Reserved	VSP_SEL[3:0]			
Default		0	0	0	0	1	0	1	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**14h**	Reserved	Reserved	Reserved	Reserved	VSN_SEL[3:0]			
Default		0	0	0	0	1	0	1	0

Description

VSP_SEL[3:0]: PFM VSP voltage selection:
VSN_SEL[3:0]: PFM VSN voltage selection:

VSP_SEL[3:0] VSN_SEL[3:0]	VSP (V)	VSN (V)
0h	6.6	-6.6
1h	5.1	-5.1
2h	5.2	-5.2
3h	5.3	-5.3
:	:	:
7h	5.7	-5.7
8h	5.8	-5.8
9h	5.9	-5.9
Ah (Default)	**6.0**	**-6.0**
Bh	6.1	-6.1
Ch	6.2	-6.2
Dh	6.3	-6.3
Eh	6.4	-6.4
Fh	6.5	-6.5

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	15h	Reserved	Reserved	Reserved	VGH_SEL[4:0]				
Default		0	0	0	0	1	0	1	0

Description

VGH_SEL[4:0]: VGH voltage selection:

VGH_SEL[4:0]	VGH (V)	VGH_SEL[4:0]	VGH (V)
00h	7.0	10h	15.0
01h	7.5	11h	15.5
02h	8.0	12h	16.0
03h	8.5	13h	16.5
04h	9.0	14h	17.0
05h	9.5	15h	17.5
06h	10.0	16h	18.0
07h	10.5	17h	18.5
08h	11.0	18h	19.0
09h	11.5	19h	19.5
0Ah (Default)	**12.0**	1Ah	20.0
0Bh	12.5	1Bh	20.5
0Ch	13.0	1Ch	21.0
0Dh	13.5	1Dh	21.5
0Eh	14.0	1Eh	22.0
0Fh	14.5	1Fh	22.5

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	16h	Reserved	Reserved	Reserved	Reserved	VGL_SEL[0]			
Default		0	0	0	0	1	0	1	0

Description

VGL_SEL[3:0]: VGL voltage selection:

VGL_SEL[3:0]	VGL (V)	VGL_SEL[3:0]	VGL (V)
0h	-7.0	8h	-11.0
1h	-7.5	9h	-11.5
2h	-8.0	**Ah (Default)**	**-12.0**
3h	-8.5	Bh	-12.5

4h	-9.0	Ch	-13.0
5h	-9.5	Dh	-13.5
6h	-10.0	Eh	-14.0
7h	-10.5	Fh	-15.0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	18h	Reserved	Reserved	VCOM_EN_ID[1:0]		Reserved	VCOM_DRV[2:0]		
Default		0	0	0	0	0	0	1	1

Description

VCOM_EN_ID[1:0]: Enable or disable VCOM voltage by ID.

VCOM_EN_ID[1:0]	Driving ability selection.
0h	00: Enable VCOM voltage of CID=00 chip (Master). (Default)
1h	01: Enable VCOM voltage of CID=01 chip (Slave 1).
2h	10: Enable VCOM voltage of CID=10 chip (Slave 2).
3h	11: Enable VCOM voltage of CID=11 chip (Slave 3).

VCOM_DRV[2:0]: VCOM buffer driving ability selection.

VCOM_DRV[2:0]	Driving ability selection.
0h	Weakest
1h	⋮
2h	Weaker
3h	Normal (Default)
4h	Stronger
5h	⋮
6h	⋮
7h	Strongest

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	19h	Reserved	Reserved	Reserved	TS_EN	TS_HYS_FRM[1:0]		TS_HYS[1:0]	
Default		0	0	0	0	0	1	0	1

Description

TS_EN: Enable or Disable embedded Temperature Sensor.

TS_EN	Function
0	Disable. (Default)
1	Enable.

TS_HYS_FRM[1:0]: Set hysteresis frames for embedded Temperature Sensor.

TS_HYS_FRM[1:0]	Function
0h	32 Frames.
1h	64 Frames. (Default)
2h	128 Frames.
3h	(Reserved)

TS_HYS[1:0]: Set hysteresis window for embedded Temperature Sensor.

TS_HYS[1:0]	Function

	0h 2°C. **1h 4°C. (Default)** 2h 6°C. 3h 8°C.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ah	Reserved	HTWARN_MIN[6:0]						
Default		0	1	1	0	1	0	0	1

Description

HTWARN_MIN[6:0]: Set the minimum temperature for high temperature warning function.

HTWARN_MIN[6:0]	Temperature
00h	0°C
01h	1°C
⋮	⋮
3Ch	60°C
3Dh	61°C
⋮	⋮
69h	**105°C (Default)**
⋮	⋮
7Fh	127°C

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Bh	LTWARN_MAX[7:0]							
Default		1	1	0	1	1	0	0	1

Description

HTWARN_MIN[6:0]: Set the minimum temperature for high temperature warning function.

LTWARN_MAX[7:0]	Temperature
00h	0°C
01h~7Fh	(Reserved)
80h	-128°C
81h	-127°C
⋮	⋮
D8h	**-40°C (Default)**
D9h	-39°C
⋮	⋮
FEh	-2°C
FFh	-1°C

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ch	Reserved	HT_MIN[6:0]						
Default		0	0	1	1	1	1	0	0

Description

T_MIN[6:0]: Set the minimum temperature for high temperature compensation.

HT_MIN[6:0]	Temperature
00h	0°C
01h	1°C
⋮	⋮

3Ch	60°C (Default)
3Dh	61°C
⋮	⋮
7Fh	127°C

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Dh	LT_MAX[7:0]							
Default		0	0	0	0	0	0	0	0

Description

LT_MAX[7:0]: Set the maximum temperature for low temperature compensation.

LT_MAX[7:0]	Temperature
00h	0°C (Default)
01h~7Fh	(Reserved)
80h	-128°C
81h	-127°C
⋮	⋮
D8h	-40°C
D9h	-39°C
⋮	⋮
FEh	-2°C
FFh	-1°C

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Fh	Reserved	Reserved	VCOM_HYS_FRM[1:0]		VCOM_FRM[3:0]			
Default		0	0	0	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	20h	VCOM_OFFS[7:0]							
Default		0	0	0	0	0	0	0	0

Description

VCOM_HYS_FRM[1:0]: Set hysteresis frame numbers when VCOM voltage changed by temperature. (For temperature compensation function)

VCOM_HYS_FRM[1:0]	Function
0h	32 Frames.
1h	64 Frames. (Default)
2h	128 Frames.
3h	(Reserved)

VCOM_FRM[3:0]: Set Vcom offset frames.

VCOM_FRM[3:0]	Frames
0h	Function disabled (Default)
1h	2
2h	4
3h	8
4h	16
5h	32
6h	64
7h	128
8h	256

9h	512
Ah	1024
Bh	2048
Ch	(Reserved)
Dh	(Reserved)
Eh	(Reserved)
Fh	(Reserved)

VCOM_OFFS[7:0]: Set Vcom offset voltage.
Note: The output VCOM voltage would be changed with an offset value (R_VCOM_OFFS[7:0]), and last one frame in the selection frames (R_VCOM_FRM[3:0]).

VCOM_OFFS[7]	VCOM_OFFS[6:0]	Offset	VCOM with offset
0	**00h**	**0**	**Original VCOM (Default)**
0	01h	0.01 V	Original VCOM + 0.01V
0	02h	0.02 V	Original VCOM + 0.02V
⋮	⋮	⋮	⋮
0	7Fh	0.63 V	Original VCOM + 0.63V
1	00h	0	Original VCOM
1	01h	0.01 V	Original VCOM - 0.01V
1	02h	0.02 V	Original VCOM - 0.02V
⋮	⋮	⋮	⋮
1	7Fh	0.63 V	Original VCOM - 0.63V

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	21h	Reserved	HTVCOM_EN	HTVCOM[5:0]					
Default		0	0	0	0	0	0	0	0

Description

HTVCOM_EN: Enable or Disable VCOM high temperature compensation function.

HTVCOM_EN	Function
0	**Disable. (Default)**
1	Enable.

HTVCOM[5:0]: Set VCOM offset value for VCOM high temperature compensation function.
Where the high-temp. VCOM after compensation = Normal-temp. VCOM + offset value = VCOM_VSEL[8:0] + HTVCOM[5:0]

HTVCOM[5]	HTVCOM[4:0]	Offset Value	VCOM voltage after high-temp. compensation
0	**00000**	**+ 0 (Default)**	**R_VCOM_VSEL[8:0] + 0 (Default)**
0	00001	+ 10 mV	R_VCOM_VSEL[8:0] + 10 mV
0	00010	+ 20 mV	R_VCOM_VSEL[8:0] + 20 mV
⋮	⋮	⋮	⋮
0	11111	+ 310 mV	R_VCOM_VSEL[8:0] + 310 mV
1	00000	- 0	R_VCOM_VSEL[8:0] – 0
1	00001	- 10 mV	R_VCOM_VSEL[8:0] – 10 mV
1	00010	- 20 mV	R_VCOM_VSEL[8:0] – 20 mV
⋮	⋮	⋮	⋮
1	11111	- 310 mV	R_VCOM_VSEL[8:0] – 310 mV

Note: Offset value is 10mV/ step, which is the same as VCOM register setting in normal temperature.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0

R/W	22h	Reserved	LTVCOM_EN	LTVCOM[5:0]					
Default		0	0	0	0	0	0	0	0

Description

LTVCOM_EN: Enable or Disable VCOM low temperature compensation function.

LTVCOM_EN	Function
0	**Disable. (Default)**
1	Enable.

R_LTVCOM[5:0]: Set VCOM offset value for VCOM low temperature compensation function.
Where the low-temp. VCOM after compensation = Normal-temp. VCOM + offset value = VCOM_VSEL[8:0] + LTVCOM[5:0]

LTVCOM[5]	LTVCOM[4:0]	Offset Value	VCOM voltage for low temp. compensation
0	**00000**	**+ 0 (Default)**	**R_VCOM_VSEL[8:0] + 0 (Default)**
0	00001	+ 10 mV	R_VCOM_VSEL[8:0] + 10 mV
0	00010	+ 20 mV	R_VCOM_VSEL[8:0] + 20 mV
⋮	⋮	⋮	⋮
0	11111	+ 310 mV	R_VCOM_VSEL[8:0] + 310 mV
1	00000	- 0	R_VCOM_VSEL[8:0] – 0
1	00001	- 10 mV	R_VCOM_VSEL[8:0] – 10 mV
1	00010	- 20 mV	R_VCOM_VSEL[8:0] – 20 mV
⋮	⋮	⋮	⋮
1	11111	- 310 mV	R_VCOM_VSEL[8:0] – 310 mV

Note: Offset value is 10mV/ step, which is the same as VCOM register setting in normal temperature.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	23h	VGM_HT_EN	VGM_LT_EN	Reserved	VGMPHO_HT[4:0]				
Default		0	0	0	0	0	0	0	0

Description

VGM_HT_EN: Enable or Disable Gamma voltages' high temperature compensation function.

VGM_HT_EN	Function
0	**Disable. (Default)**
1	Enable.

VGM_LT_EN: Enable or Disable Gamma voltages' low temperature compensation function.

VGM_LT_EN	Function
0	**Disable. (Default)**
1	Enable.

VGMPHO_HT[4:0]: Set VGMPHO offset value for VGMPHO high temperature compensation function.
Where the high-temp. VGMPHO after compensation = Normal-temp. VGMPHO + offset value = VGMPHO_SEL[3:0] + VGMPHO_HT[4:0]
(See the description of Page5, Addr. 0x24)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	24h	VGMPLO_HT[4]	VGMNLO_HT[4]	Reserved	VGMNHO_HT[4:0]				
Default		0	0	0	0	0	0	0	0

Description

VGMPLO_HT[4]: MSB of VGMPLO_HT[4:0]
VGMPLO_HT[4:0]: Set VGMPLO offset value for VGMPLO high temperature compensation function.
Where the high-temp. VGMPLO after compensation = Normal-temp. VGMPLO + offset value = R_VGMPLO_SEL[3:0] + VGMPLO_HT[4:0]
(See the description of Page5, Addr. 0x25)

VGMNLO_HT[4]: MSB of VGMNLO_HT[4:0]
VGMNLO_HT[4:0]: Set VGMNLO offset value for VGMNLO high temperature compensation function.
Where the high-temp. VGMNLO after compensation = Normal-temp. VGMNLO + offset value = R_VGMNLO_SEL[3:0] + VGMNLO_HT[4:0]
(See the description of Page5, Addr. 0x25)

VGMNHO_HT[4:0]: Set VGMNHO offset value for VGMNHO high temperature compensation function.
Where the high-temp. VGMNHO after compensation = Normal-temp. VGMNHO + offset value = VGMNHO_SEL[3:0] + VGMNHO_HT[4:0]

VGMPHO_HT[4] **VGMNHO_HT[4]**	**VGMPHO_HT[3:0]** **VGMNHO_HT[3:0]**	Offset Value	VGMPHO voltage for high temp. compensation VGMNHO voltage for high temp. compensation
0	**00000**	**+ 0 (Default)**	**VGMPHO_SEL[3:0] + 0** **VGMNHO_SEL[3:0] + 0**
0	00001	+ 0.05 V	VGMPHO_SEL[3:0] + 0.05 V VGMNHO_SEL[3:0] + 0.05 V
0	00010	+ 0.10 V	VGMPHO_SEL[3:0] + 0.10V VGMNHO_SEL[3:0] + 0.10V
⋮	⋮	⋮	⋮
0	11111	+ 1.55 V	VGMPHO_SEL[3:0] + 1.55 V VGMNHO_SEL[3:0] + 1.55 V
1	00000	- 0	VGMPHO_SEL[3:0] – 0 VGMNHO_SEL[3:0] – 0
1	00001	- 0.05 V	VGMPHO_SEL[3:0] – 0.05 V VGMNHO_SEL[3:0] – 0.05 V
1	00010	- 0.10 V	VGMPHO_SEL[3:0] – 0.10 V VGMNHO_SEL[3:0] – 0.10 V
⋮	⋮	⋮	⋮
1	11111	- 1.55 V	VGMPHO_SEL[3:0] – 1.55 V VGMNHO_SEL[3:0] – 1.55 V

Note: Offset value is 0.05V/ step, which is the same as VGMPHO/ VGMNHO register setting in normal temperature.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	25h	VGMPLO_HT[3:0]				VGMNLO_HT[3:0]			
Default		0	0	0	0	0	0	0	0

Description

VGMPLO_HT[3:0]: LSB 3bits of VGMPLO_HT[4:0]

VGMNLO_HT[3:0]: LSB 3 bits of VGMNLO_HT[4:0]

VGMPLO_HT[4] **VGMNLO_HT[4]**	**VGMPLO_HT[3:0]** **VGMNLO_HT[3:0]**	Offset Value	VGMPLO voltage for high temp. compensation VGMNLO voltage for high temp. compensation
0	**00000**	**+ 0 (Default)**	**VGMPLO_SEL[3:0] + 0** **VGMNLO_SEL[3:0] + 0**
0	00001	+ 0.05 V	VGMPLO_SEL[3:0] + 0.05 V VGMNLO_SEL[3:0] + 0.05 V
0	00010	+ 0.10 V	VGMPLO_SEL[3:0] + 0.10V VGMNLO_SEL[3:0] + 0.10V
⋮	⋮	⋮	⋮
0	11111	+ 0.75 V	VGMPLO_SEL[3:0] + 0.75 V VGMNLO_SEL[3:0] + 0.75 V
1	00000	- 0	VGMPLO_SEL[3:0] – 0 VGMNLO_SEL[3:0] – 0

1	00001	- 0.05 V	VGMPLO_SEL[3:0] – 0.05 V VGMNLO_SEL[3:0] – 0.05 V
1	00010	- 0.10 V	VGMPLO_SEL[3:0] – 0.10 V VGMNLO_SEL[3:0] – 0.10 V
⋮	⋮	⋮	⋮
1	11111	- 0.75 V	VGMPLO_SEL[3:0] – 0.75 V VGMNLO_SEL[3:0] – 0.75 V

Note: Offset value is 0.05V/ step, which is the same as VGMPLO/ VGMNLO register setting in normal temperature.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	26h	VGHL_HT_EN	VGHL_LT_EN	Reserved	VGMPHO_LT[4:0]				
Default		0	0	0	0	0	0	0	0

Description

VGHL_HT_EN: Enable or Disable VGH/ VGL high temperature compensation function.
VGHL_LT_EN: Enable or Disable VGH/ VGL low temperature compensation function.

VGHL_HT_EN VGHL_LT_EN	Function
0	**Disable. (Default)**
1	Enable.

VGMPHO_LT[4:0]: Set VGMPHO offset value for VGMPHO low temperature compensation function.
Where the low-temp. VGMPHO after compensation = Normal-temp. VGMPHO + offset value = VGMPHO_SEL[3:0] + VGMPHO_LT[4:0]
(See the description of Page5, Addr. 0x27)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	27h	VGMPLO_LT[4]	VGMNLO_LT[4]	Reserved	VGMNHO_LT[4:0]				
Default		0	0	0	0	0	0	0	0

Description

VGMPLO_LT[4]: MSB of VGMPLO_LT[4:0]
VGMPLO_LT[4:0]: Set VGMPLO offset value for VGMPLO high temperature compensation function.
Where the high-temp. VGMPLO after compensation = Normal-temp. VGMPLO + offset value = VGMPLO_SEL[3:0] + VGMPLO_LT[4:0]
(See the description of Page5, Addr. 0x28)

VGMNLO_LT[4]: MSB of VGMNLO_LT[4:0]
VGMNLO_LT[4:0]: Set VGMNLO offset value for VGMNLO high temperature compensation function.
Where the high-temp. VGMNLO after compensation = Normal-temp. VGMNLO + offset value = VGMNLO_SEL[3:0] + VGMNLO_LT[4:0]
(See the description of Page5, Addr. 0x28)

VGMNHO_LT[4:0]: Set VGMNHO offset value for VGMNHO high temperature compensation function.
Where the high-temp. VGMNHO after compensation = Normal-temp. VGMNHO + offset value = VGMNHO_SEL[3:0] + VGMNHO_LT[4:0]

VGMPHO_LT[4] VGMNHO_LT[4]	VGMPHO_LT[3:0] VGMNHO_LT[3:0]	Offset Value	VGMPHO voltage for high temp. compensation VGMNHO voltage for high temp. compensation
0	**00000**	**+ 0 (Default)**	**VGMPHO_SEL[3:0] + 0** **VGMNHO_SEL[3:0] + 0**
0	00001	+ 0.05 V	VGMPHO_SEL[3:0] + 0.05 V VGMNHO_SEL[3:0] + 0.05 V
0	00010	+ 0.10 V	VGMPHO_SEL[3:0] + 0.10V VGMNHO_SEL[3:0] + 0.10V
⋮	⋮	⋮	⋮

0	11111	+ 1.55 V	VGMPHO_SEL[3:0] + 1.55 V VGMNHO_SEL[3:0] + 1.55 V
1	00000	- 0	VGMPHO_SEL[3:0] – 0 VGMNHO_SEL[3:0] – 0
1	00001	- 0.05 V	VGMPHO_SEL[3:0] – 0.05 V VGMNHO_SEL[3:0] – 0.05 V
1	00010	- 0.10 V	VGMPHO_SEL[3:0] – 0.10 V VGMNHO_SEL[3:0] – 0.10 V
⋮	⋮	⋮	⋮
1	11111	- 1.55 V	VGMPHO_SEL[3:0] – 1.55 V VGMNHO_SEL[3:0] – 1.55 V

Note: Offset value is 0.05V/ step, which is the same as VGMPHO/ VGMNHO register setting in normal temperature.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	28h	VGMPLO_LT[3:0]				VGMNLO_LT[3:0]			
Default		0	0	0	0	0	0	0	0

Description

VGMPLO_LT[3:0]: LSB 3bits of VGMPLO_LT[4:0]
VGMNLO_LT[3:0]: LSB 3 bits of VGMNLO_LT[4:0]

VGMPLO_LT[4] VGMNLO_LT[4]	VGMPLO_LT[3:0] VGMNLO_LT[3:0]	Offset Value	VGMPLO voltage for high temp. compensation VGMNLO voltage for high temp. compensation
0	**00000**	**+ 0 (Default)**	**VGMPLO_SEL[3:0] + 0** **VGMNLO_SEL[3:0] + 0**
0	00001	+ 0.05 V	VGMPLO_SEL[3:0] + 0.05 V VGMNLO_SEL[3:0] + 0.05 V
0	00010	+ 0.10 V	VGMPLO_SEL[3:0] + 0.10V VGMNLO_SEL[3:0] + 0.10V
⋮	⋮	⋮	⋮
0	11111	+ 0.75 V	VGMPLO_SEL[3:0] + 0.75 V VGMNLO_SEL[3:0] + 0.75 V
1	00000	- 0	VGMPLO_SEL[3:0] – 0 VGMNLO_SEL[3:0] – 0
1	00001	- 0.05 V	VGMPLO_SEL[3:0] – 0.05 V VGMNLO_SEL[3:0] – 0.05 V
1	00010	- 0.10 V	VGMPLO_SEL[3:0] – 0.10 V VGMNLO_SEL[3:0] – 0.10 V
⋮	⋮	⋮	⋮
1	11111	- 0.75 V	VGMPLO_SEL[3:0] – 0.75 V VGMNLO_SEL[3:0] – 0.75 V

Note: Offset value is 0.05V/ step, which is the same as VGMPLO/ VGMNLO register setting in normal temperature.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	29h	Reserved	Reserved	Reserved	HT_VGH_SEL[4:0]				
Default		0	0	0	0	1	0	1	0

Description

HT_VGH_SEL[4:0]: Set VGH voltage for high temperature compensation function.
(See the description of Page5, Addr. 0x2A)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	2Ah	Reserved	Reserved	Reserved	LT_VGH_SEL[4:0]				
Default		0	0	0	0	1	0	1	0

Description

LT_VGH_SEL[4:0]: Set VGH voltage for low temperature compensation function.

HT_VGH_SEL[4:0] LT_VGH_SEL[4:0]	VGH_HT VGH_LT	HT_VGH_SEL[4:0]] LT_VGH_SEL[4:0]	VGH_HT VGH_LT
00h	7.0 V	10h	15.0V
01h	7.5 V	11h	15.5 V
02h	8.0 V	12h	16.0 V
03h	8.5 V	13h	16.5 V
04h	9.0 V	14h	17.0 V
05h	9.5 V	15h	17.5 V
06h	10.0 V	16h	18.0 V
07h	10.5 V	17h	18.5 V
08h	11.0 V	18h	19.0 V
09h	11.5 V	19h	19.5 V
0Ah	**12.0 V (Default)**	1Ah	20.0 V
0Bh	12.5 V	1Bh	20.5 V
0Ch	13.0 V	1Ch	21.0 V
0Dh	13.5 V	1Dh	21.5 V
0Eh	14.0 V	1Eh	22.0 V
0Fh	14.5 V	1Fh	22.5 V

Note: VGH_HT-VGL_HT ≤ 32V; VGH_LT-VGL_LT ≤ 32V

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	2Bh	HT_VGL_SEL[3:0]				LT_VGL_SEL[3:0]			
Default		1	0	1	0	1	0	1	0

Description

HT_VGL_SEL[3:0]: Set VGL voltage for high temperature compensation function.
LT_VGL_SEL[3:0]: Set VGL voltage for low temperature compensation function.

HT_VGL_SEL[3:0] LT_VGL_SEL[3:0]	VGL_HT VGL_LT
0h	-7.0 V
1h	-7.5 V
2h	-8.0 V
3h	-8.5 V
4h	-9.0 V
5h	-9.5 V
6h	-10.0 V
7h	-10.5 V
8h	-11.0 V
9h	-11.5 V
Ah	**-12.0 V (Default)**
Bh	-12.5 V
Ch	-13.0 V
Dh	-13.5 V
Eh	-14.0 V
Fh	-15.0 V

Note: VGH_HT-VGL_HT ≤ 32V; VGH_LT-VGL_LT ≤ 32V

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	2Ch	Reserved	Reserved	Reserved	Reserved	VGM_HYS_FRM[1:0]		Reserved	Reserved
Default		0	0	0	0	0	0	0	1

Description

VGM_HYS_FRM[1:0]: Set hysteresis frame numbers when gamma voltages changed by temperature. (For temperature compensation function.)

VGM_HYS_FRM[1:0]	Function
0h	**32 Frames. (Default)**
1h	64 Frames.
2h	128 Frames.
3h	(Reserved)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	2Dh	Reserved	VREF_VSP_OCP_SEL[2:0]			Reserved	VREF_VSN_OCP_SEL[2:0]		
Default		0	0	1	0	0	0	1	0

Description

VREF_VSP_OCP_SEL[2:0]: PFM VSP over current (OCP) voltage detection.
VREF_VSN_OCP_SEL[2:0]: PFM VSN over current (OCP) voltage detection.

VREF_VSP_OCP_SEL[2:0] VREF_VSN_OCP_SEL[2:0]	VSP OCP Voltage VSN OCP Voltage
0h	0.20V
1h	0.25V
2h	**0.30V (Default)**
3h	0.35V
4h	0.40V
5h	0.45V
6h	0.50 V
7h	0.55V

Note: Choose Inductor (L) I_{Rating}> 2.5A, R1=R2= 0.1ohm.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	2Eh	VREF_VSP_ON_THR[1:0]		VREF_VSN_ON_THR[1:0]		Reserved	Reserved	Reserved	Reserved
Default		0	0	0	0	0	0	0	1

Description

VREF_VSP_ON_THR[1:0]: Set the detection voltage of PFM VSP power on ready function.

VREF_VSP_ON_THR[1:0]	Description
0h	**4.5V. (Default)**
1h	5.0V.
2h	5.5V.
3h	6.0V.

VREF_VSN_ON_THR[1:0]: Set the detection voltage of PFM VSN power on ready function.

VREF_VSN_ON_THR[1:0]	Description
0h	**- 4.5V. (Default)**
1h	- 5.0V.
2h	- 5.5V.
3h	- 6.0V.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	2Fh	OTP_VCOM_TIMES[7:0]							
Default		0	0	0	0	0	0	0	0

Description

OTP_VCOM_TIMES[7:0]: Read the status of VCOM programming number, it is read only.

OTP_VCOM_TIMES[7:0]	Description
00h	**1ST_VCOM_SEL[7:0] (Default)**
01h	2ND_VCOM_SEL[7:0]
03h	3RD_VCOM_SEL[7:0]
Others	1ST_VCOM_SEL[7:0]

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	30h	1ST_VCOM_SEL[7:0]							
Default		0	1	0	1	1	1	1	1

Description

1ST_VCOM_SEL[7:0]: VCOM voltage selection for 1ST chance programming:

1ST_VCOM_SEL[7:0]	VCOM(V)
00h	-1.81
01h	-1.82
:	:
13h	-2.00
14h	0.55
15h	0.54
:	:
5Dh	-0.18
5Eh	-0.19
5Fh	**-0.20 (Default)**
:	:
FDh	-1.78
FEh	-1.79
FFh	-1.80

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	31h	2ND_VCOM_SEL[7:0]							
Default		0	0	0	0	0	0	0	0

Description

2ND_VCOM_SEL[7:0]: VCOM voltage selection for 2ND chance programming:

2ND_VCOM_SEL[7:0]	VCOM(V)
00h	-1.81 **(Default)**
01h	-1.82
:	:
13h	-2.00
14h	0.55
15h	0.54
:	:
5Dh	-0.18
5Eh	-0.19
5Fh	**-0.20**
:	:
FDh	-1.78

	FEh -1.79 FFh -1.80

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	32h	3RD_VCOM_SEL[7:0]							
Default		0	0	0	0	0	0	0	0

Description

3RD_VCOM_SEL[7:0]: VCOM voltage selection for 3RD chance programming:

3RD_VCOM_SEL[7:0]	VCOM(V)
00h	-1.81 **(Default)**
01h	-1.82
:	:
13h	-2.00
14h	0.55
15h	0.54
:	:
5Dh	-0.18
5Eh	-0.19
5Fh	**-0.20**
:	:
FDh	-1.78
FEh	-1.79
FFh	-1.80

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Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OTP_PWR_RDY_TO_WR	OTP_AUTO_WRITE
Default		0	0	0	0	0	0	0	0

Description

OTP_PWR_RDY_TO_WR: Check power is ready or not for OTP programming.

OTP_PWR_RDY_TO_WR	Function
0 (Default)	If OTP_PASSWORD1[7:0]≠ AA & OTP_WORDPASS2[7:0]≠ 55, it's NOT ready for OTP programming.
1	If OTP_PASSWORD1[7:0]= AA & OTP_PASSWORD2[7:0]=55, it's ready for OTP programming.

OTP_AUTO_WRITE: OTP all page registers program.

OTP_AUTO_WRITE	Function
0	**Disable (Default)**
1	Enable

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	02h	OTP_PWR_RDY_FLAG	Reserved	Reserved	Reserved	AUTO_WR_EN_FLAG	Reserved	Reserved	MARGIN_READY_OK
Default		0	0	0	0	0	0	0	0
Description		**OTP_PWR_RDY_FLAG:** OTP power ready flag, it is read only.							

OTP_PWR_RDY_FLAG	Function
0	OTP power is NOT ready (Default)
1	OTP power is ready

AUTO_WR_EN_FLAG: OTP auto write enable flag, it is read only.

AUTO_WR_EN_FLAG	Function
0	OTP write enable function fail. (Default)
1	OTP write enable function OK

MARGIN_READ_OK: Margin read OK flag, it is read only.

MARGIN_READ_OK	Function
0	Margin read fail. (Default)
1	Margin read OK

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	03h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OTP_READ
Default		0	0	0	0	0	0	0	0

Description

OTP_READ: Single OTP read.

OTP_READ	Function
0	Disable (Default)
1	Enable

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	04h	OTP_RD_DATA[7:0]							
Default		0	0	0	0	0	0	0	0

Description: **OTP_RD_DATA[7:0]:** Read OTP Data, it is read only.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	05h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RDADDR[8]
Default		0	0	0	0	0	0	0	0

Description: **RDADDR[8]:** Address[8] for Single OTP write/read.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	06h	RDADDR[7:0]							
Default		1	1	1	1	1	1	1	1

Description: **RDADDR[7:0]:** Address[7:0] for Single OTP write/read.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0

R/W	07h	SINGLE_WRITE[7:0]							
Default		0	0	0	0	0	0	0	0

Description

SINGLE_WRITE[7:0]: Access for OTP single write.

SINGLE_WRITE[7:0]	Function
00'h	**Disable OTP single write (Default)**
AA'h	Enable OTP single write (Note)
others	Disable OTP single write

Note: This register works when OTP_PWR_RDY_TO_WR=1.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R	08h	PROG_NUM_COUNT[7:0]							
Default		0	0	0	0	0	0	0	0

Description

PROG_NUM_COUNT[7:0]: Program number counter, it is read only..

PROG_NUM_COUNT[7:0]	Number of programming
00'h	0
01'h	**1 (Default)**
03'h	2
07'h	3
0F'h	4
1F'h	5
3F'h	6

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Dh	OTP_PASSWORD1							
Default		0	1	0	1	0	1	0	1

Description

OTP_PASSWORD1: OTP write permission control_no.1.

OTP_PASSWORD1	Function
55'h	**Disable OTP programming process (Default)**
AA'h	OTP get the write permission and programming process can start.
others	Disable OTP programming process

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Eh	OTP_PASSWORD2							
Default		1	0	1	0	1	0	1	0

Description

OTP_PASSWORD2: OTP write permission control_no.2.

OTP_PASSWORD2	Function
AA'h	**Disable OTP programming process (Default)**
55'h	OTP auto-reload
others	Disable OTP programming process

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Fh	OTP_NOT_RLD							
Default		0	1	0	1	0	1	0	1
Description		**OTP_NOT_RLD:** Disable OTP reload function							

OTP_NOT_RLD	Function
55'h	**OTP auto-reload. (Default)**
AA'h	Disable OTP auto-reload function
others	OTP auto-reload.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	10h	SOFT-WARE RELOAD SETTING[7:0]							
Default		0	0	0	0	0	0	0	0
Description		**SOFT-WARE RELOAD SETTING[7:0]:** OTP selected area reload setting. Note: Please consult Forcelead about this function.							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	11h	OTP_SINGLE_WR_DIN[7:0]							
Default		0	0	0	0	0	0	0	0
Description		**OTP_SINGLE_WR_DIN[7:0]:** Input data for OTP single write.							

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Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	PFM_VSP_DUTY[3]	Reserved	PFM_VSP_TOFF_DUTY[1:0]		PFM_VSN_DUTY[3]	Reserved	PFM_VSN_TOFF_DUTY[1:0]	
Default		0	0	0	0	0	0	0	0
Description		**PFM_VSP_DUTY[3]:** MSB of PFM_VSP_DUTY[3:0] (See the description of Page7, Addr. 0x17). **PFM_VSP_TOFF_DUTY[1:0]:** VSP PWM TOFF duty setting.							

PFM_VSP_TOFF_DUTY[1:0]	Function
0h	**0ns & VSP_TOFF_EN = 0 (Default)**
1h	60ns & VSP_TOFF_EN = 1
2h	100ns & VSP_TOFF_EN = 1
3h	200ns & VSP_TOFF_EN = 1

PFM_VSN_DUTY[3]: MSB of PFM_VSN_DUTY[3:0] (See the description of Page7, Addr. 0x19).

PFM_VSN_TOFF_DUTY[1:0]: VSN PWM TOFF duty setting.

PFM_VSN_TOFF_DUTY[1:0]	Function
0h	**0ns & VSN_TOFF_EN = 0 (Default)**
1h	60ns & VSN_TOFF_EN = 1
2h	100ns & VSN_TOFF_EN = 1
3h	200ns & VSN_TOFF_EN = 1

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0

R/W	02h	GOUTR02_SEL[1:0]		GOUTR01_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	03h	GOUTR03_SEL[3:0]				GOUTR02_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	04h	GOUTR03_SEL[5:4]		GOUTR04_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	05h	GOUTR06_SEL[1:0]		GOUTR05_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	06h	GOUTR07_SEL[3:0]				GOUTR06_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	07h	GOUTR07_SEL[5:4]		GOUTR08_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	08h	GOUTR10_SEL[1:0]		GOUTR09_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	09h	GOUTR11_SEL[3:0]				GOUTR10_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ah	GOUTR11_SEL[5:4]		GOUTR12_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Bh	GOUTR14_SEL[1:0]		GOUTR13_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ch	GOUTR15_SEL[3:0]				GOUTR14_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Dh	GOUTR15_SEL[5:4]		GOUTR16_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Eh	GOUTR18_SEL[1:0]		GOUTR17_SEL[5:0]					
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Fh	GOUTR19_SEL[3:0]				GOUTR18_SEL[5:2]			
Default		1	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	10h	GOUTR19_SEL[5:4]		GOUTR20_SEL[5:0]					

Default		1	1	1	1	1	1	1	1
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**11h**	GIP_SR_R[1:0]		GIP_CSH_SEL_R[1:0]		GIP_CSL_SEL_R[1:0]		GIP_CS_EN_R[1:0]	
Default		0	1	1	0	1	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**12h**	GIP_CS_EN_R[9:2]							
Default		0	0	0	0	0	0	0	0

Description

GOUTR01_SEL[5:0] ~ GOUTR20_SEL[5:0]: Select the output signal of GHV_R[1:20] pad.

GIP_SR_R[1:0]: Driving ability selection of GHV_R[01:20] outputs.

GIP_SR_R[1:0]	Function
0h	Output driving weakest
1h	**Output driving second weak (Default).**
2h	Output driving second strong.
3h	Output driving strongest.

GIP_CSH_SEL_R[1:0]: GIP CS high width.

GIP_CSH_SEL_R[1:0]	Function
0h	0 clock.
1h	1 clock.
2h	**2 clocks. (Default)**
3h	4 clocks

GIP_CSL_SEL_R[1:0]: GIP CS low width.

GIP_CSL_SEL_R[1:0]	Function
0h	0 clock.
1h	1 clock.
2h	**2 clocks. (Default)**
3h	4 clocks

GIP_CS_EN_R[9:0]: GIP CS function enable for GHV_R[1:20].

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	**13h**	VRSP_SEL[3:0]				VRSN_SEL[3:0]			
Default		1	1	0	1	1	1	0	1

Description

VRSP_SEL[3:0]: VRSP voltage selection
VRSN_SEL[3:0]: VRSN voltage selection:

VRSP_SEL[3:0]	VRSP (V)
0h	6.1
1h	6.2
2h	6.3
3h	6.4
4h	4.9
5h	5.0
:	:
Ch	5.7
Dh	**5.8 (Default)**
Eh	5.9
Fh	6.0

VRSN_SEL[3:0]	VRSN (V)
0h	-6.1
1h	-6.2
2h	-6.3
3h	-6.4
4h	-4.9
5h	-5.0
:	:
Ch	-5.7
Dh	**-5.8 (Default)**
Eh	-5.9
Fh	-6.0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	14h	PFM_VSP_DUTY_CTL_EN	PFM_VSP_TOFF_EN	VSP_CMPR_SEL	HPFM_EN	PFM_VSN_DUTY_CTL_EN	PFM_VSN_TOFF_EN	VSN_CMPR_SEL	PFM_DIVF
Default		0	0	0	0	0	0	0	0

Description

PFM_VSP_DUTY_CTL_EN: Parameter of PFWM VSP Duty Control function.

PFM_VSP_DUTY_CTL_EN	Function
0	**Disable (Default)**
1	Enable

PFM_VSP_TOFF_EN: Parameter of PFWM VSP Duty Control function.

PFM_VSP_TOFF_EN	Function
0	**Disable (Default)**
1	Enable

VSP_CMPR_SEL: Parameter of PFWM VSP Duty Control function.

VSP_CMPR_SEL	Function
0	**Disable (Default)**
1	Enable

HPFM_EN: Parameter of PFWM Duty Control function.

HPFM_EN	Function
0	**Disable (Default)**
1	Enable

PFM_VSN_DUTY_CTL_EN: Parameter of PFWM VSN Duty Control function..

PFM_VSN_DUTY_CTL_EN	Function
0	**Disable (Default)**
1	Enable

PFM_VSN_TOFF_EN: Parameter of PFWM VSN Duty Control function.

PFM_VSN_TOFF_EN	Function
0	**Disable (Default)**
1	Enable

VSN_CMPR_SEL: Parameter of PFWM VSN Duty Control function.

VSN_CMPR_SEL	Function
0	Disable (Default)
1	Enable

PFM_DIVF: Parameter of PFWM Duty Control function.

PFM_DIVF	Function
0	Disable (Default)
1	Enable

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	15h	VGMPHO_SEL[3:0]				VGMNHO_SEL[3:0]			
Default		1	1	0	1	1	1	0	1

Description

VGMPHO_SEL[3:0]: VGMPHO voltage selection
VGMNHO_SEL[3:0]: VGMNHO voltage selection

VGMPHO_SEL[3:0]	VGMPHO (V)
0h	5.9
1h	6.0
2h	6.1
3h	6.2
4h	4.7
5h	4.8
:	:
Ch	5.5
Dh	5.6 (Default)
Eh	5.7
Fh	5.8

VGMNHO_SEL[3:0]	VGMNHO (V)
0h	-5.9
1h	-6.0
2h	-6.1
3h	-6.2
4h	-4.7
5h	-4.8
:	:
Ch	-5.5
Dh	-5.6 (Default)
Eh	-5.7
Fh	-5.8

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	16h	VGMPLO_SEL[3:0]				VGMNLO_SEL[3:0]			
Default		0	0	0	1	0	0	0	1

Description

VGMPLO_SEL[3:0]: VGMPLO voltage selection
VGMNLO_SEL[3:0]: VGMNLO voltage selection

VGMPLO_SEL[3:0]	VGMPLO (V)
0h	0.1
1h	0.2 (Default)
2h	0.3
3h	0.4
:	:
Ch	1.3
Dh	1.4
Eh	1.5
Fh	1.6

VGMNLO_SEL[3:0]	VGMNLO (V)
0h	-0.1
1h	-0.2 (Default)
2h	-0.3
3h	-0.4
:	:
Ch	-1.3
Dh	-1.4
Eh	-1.5
Fh	-1.6

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	17h	PFM_VSP_DUTY[2:0]			PFM_VSP_FREQ[2:0]			PFM_VSP_CYC[2:0]	
Default		1	0	1	0	1	1	0	1

Description

PFM_VSP_DUTY[2:0]: LSB 3 bits of PFM_VSP_DUTY[3:0]
PFM_VSP_DUTY[3:0]: PFM function for DRVP duty cycle selection.

PFM_VSP_DUTY[3:0]	Duty (%)
0h	5 %
1h	10 %
2h	15 %
3h	20 %
4h	25 %
5h	**30 % (Default)**
6h	35 %
7h	40 %
8h	45 %
9h	50 %
Ah	55 %
Bh	60 %
Ch	65 %
Dh	70 %
Eh	75 %
Fh	80 %

PFM_VSP_FREQ[2:0]: PFM function for DRVP frequency selection.

PFM_VSP_FREQ[2:0]	Frequency (Hz)
0h	100K
1h	300K
2h	500K
3h	**700K (Default)**
4h	900K
5h	1.1M
6h	1.3M
7h	1.5M

PFM_VSP_CYC[1:0]: PFM function for VSP voltage soft start cycle selection.

PFM_VSP_CYC [1:0]	Cycle
0h	128
1h	**256**
2h	384
3h	512

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	18h	PFM_VSP_OCP_EN	PFM_OVP_EN	PFM_DRVP_BUF[1:0]		PFM_VSP_EN	PFM_VSN_EN	PFM_DRVN_BUF[1:0]	
Default		1	1	1	0	1	1	1	0

Description

PFM_VSP_OCP_EN: PFM for VSP over current protection (OCP) function.

PFM_VSP_OCP_EN	Function
0	Disable
1	**Enable (Default)**

PFM_OVP_EN: PFM for over voltage protection function.

PFM_OVP_EN	Function
0	Disable
1	**Enable (Default)**

PFM_DRVP_BUF[1:0]: PFM function for VSP voltage DRVP driving ability selection.

PFM_DRVP_BUF [1:0]	Ability (%)
0h	25
1h	50
2h	**100 (Default)**
3h	150

PFM_VSP_EN: PFM for VSP voltage function.

PFM_VSP_EN	Function
0	Disable
1	**Enable (Default)**

PFM_VSN_EN: PFM for VSN voltage function.

PFM_VSN_EN	Function
0	Disable
1	**Enable (Default)**

PFM_DRVN_BUF[1:0]: PFM function for VSN voltage DRVN driving ability selection.

PFM_DRVN_BUF [1:0]	Ability (%)
0h	25
1h	50
2h	**100 (Default)**
3h	150

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	19h	PFM_VSN_DUTY[2:0]			PFM_VSN_FREQ[2:0]			PFM_VSN_CYC2:0]	
Default		1	0	1	0	1	1	0	1

Description

PFM_VSN_DUTY[2:0]: LSB 3 bits of PFM_VSN_DUTY[3:0]

PFM_VSN_DUTY[3:0]: PFM function for DRVN duty cycle selection.

PFM_VSN_DUTY[3:0]	Duty (%)
0h	5 %
1h	10 %
2h	15 %
3h	20 %
4h	25 %
5h	**30 % (Default)**
6h	35 %
7h	40 %
8h	45 %
9h	50 %
Ah	55 %
Bh	60 %
Ch	65 %
Dh	70 %
Eh	75 %
Fh	80 %

PFM_VSN_FREQ[2:0]: PFM function for DRVN frequency selection.

PFM_VSN_Freq[2:0]	Frequency (Hz)
0h	100K

1h	300K
2h	500K
3h	**700K (Default)**
4h	900K
5h	1.1M
6h	1.3M
7h	1.5M

PFM_VSN_CYC[1:0]: PFM function for VSN voltage soft start cycle selection.

PFM_VSN_CYC [1:0]	Cycle
0h	128
1h	**256 (Default)**
2h	384
"11"	512

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ah	LVD_VSP_EN	LVD_VSP_SET[2:0]			GAS_VDD_EN	GAS_VDD_SET[2:0]		
Default		0	1	0	0	1	1	0	0

Description

LVD_VSP_EN: LVD function for VSP voltage detection.

LVD_VSP_EN	Function
0	**Disable (Default)**
1	Enable

LVD_VSP_SET[2:0]: LVD function for VSP trigger voltage

LVD_VSP_SET[2:0]	LVD threshold (V)
0h	3.3
1h	3.6
2h	4.0
3h	4.4
4h	**4.8 (Default)**
5h	5.0
6h	5.4
7h	reserved

GAS_VDD_EN: GAS function for VDD voltage detection.

GAS_VDD_EN	Function
0	Disable
1	**Enable (Default)**

GAS_VDD_SET[2:0]: GAS function for VDD trigger voltage.

GAS_VDD_SET[2:0]	GAS threshold (V)
0h	2.2
1h	2.3
2h	2.4
3h	2.5
4h	**2.6 (Default)**
5h	2.7
6h	2.8
7h	2.9

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Bh	LVD_VSN_EN	LVD_VSN_SET[2:0]			LVD_VGL_EN	LVD_VGL_SET[2:1]		Reserved
Default		0	1	0	0	0	0	1	1

Description

LVD_VSN_EN: LVD function for VSN voltage detection.

LVD_VSN_EN	Function
0	**Disable (Default)**
1	Enable

Description

LVD_VSN_SET[2:0]: LVD function for VSN trigger voltage.

LVD_VSN_SET[2:0]	LVD threshold (V)
0h	-3.3
1h	-3.6
2h	-4.0
3h	-4.4
4h	**-4.8 (Default)**
5h	-5.0
6h	-5.4
7h	reserved

LVD_VGL_EN: LVD function for VGL voltage detection..

LVD_VGL_EN	Function
0	**Disable (Default)**
1	Enable

LVD_VGL_SET[2:1]: LVD function for VGL trigger voltage

LVD_VGL_SET[2:1]	LVD threshold (V)
0h	-6.9
1h	**-8.0 (Default)**
2h	-8.7
3h	reserved

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ch	VDD_LV_SEL[1:0]		GAS_SCALE[1:0]		LVD_VGH_EN	LVD_VGH_SET[2:0]		
Default		0	0	0	0	0	1	0	0

Description

VDD_LV_SEL[1:0]: VDD GAS debounce time selection.

VDD_LV_SEL[1:0]	Function
00	10us
01	**25us (Default)**
10	50us
11	100us

GAS_SCALE[1:0]: Time scale selection for GAS power off sequence.

GAS_SCALE[1:0]	Function
00	80us
01	**160us (Default)**
10	320us
11	640us

LVD_VGH_EN: LVD function for VGH voltage detection.

LVD_VGH_EN	Function
0	**Disable (Default)**
1	Enable

LVD_VGH_SET[2:0]: LVD function for VGH trigger voltage

LVD_VGH_SET[2:0]	LVD threshold (V)
0h	5.0
1h	7.1

2h	8.0
3h	10.0
4h	**13.3 (Default)**
5h	16.7
6h	18.2
7h	20.0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Dh	Reserved	Reserved	VSN_DEB_FREQ[1:0]		Reserved	VSN_DEB_EN	Reserved	Reserved
Default		0	0	0	1	0	0	0	0

Description

VSN_DEB_FREQ[1:0]: VSN noise debounce ck selection

VSN_DEB_FREQ[1:0]	Function
0h	1MHz
1h	**2MHz (Default)**
2h	4MHz
3h	8MHz

VSN_DEB_EN: Enable or disable VSN noise debounce function.

VSN_DEB_EN	Function
0	**Disable (Default)**
1	Enable

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Eh	PFM_VSN_OCP_EN	PFM_OCP_DEB[2:0]			PFM_SEQ_EN	PFM_OVP_DEB[2:0]		
Default		1	0	1	1	0	0	1	1

Description

PFM_VSN_OCP_EN: PFM for VSN over current protection (OCP) function.

PFM_VSN_OCP_EN	Function
0	Disable
1	**Enable (Default)**

PFM_OCP_DEB[2:0]: Set PFM OCP debounce time

PFM_OCP_DEB[2:0]	Function
0h	1ms
1h	2ms
2h	4ms
3h	**8ms (Default)**
4h	16ms
5h	32ms
6h	64ms
7h	128ms

PFM_SEQ_EN: PFM for VSP/VSN GAS sequence selection.

PFM_SEQ_EN	Function
0	Same time **(Default)**
1	Sequence

	PFM_OVP_DEB[2:0]: Set PFM OVP debounce time

PFM_OVP_DEB[2:0]	Function
0h	1ms
1h	2ms
2h	4ms
3h	**8ms (Default)**
4h	16ms
5h	32ms
6h	64ms
7h	128ms

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Fh	Reserved	Reserved	PFM_VSP_PD_EN	PFM_VSN_PD_EN	OCP_PROT_EN	PFM_OK_DEB[2:0]		
Default		0	0	1	1	0	0	1	1

Description

PFM_VSP_PD_EN: Enable or Disable PFM VSP power down function during power off sequence.

PFM_VSP_PD_EN	Function
0	Disable
1	**Enable (Default)**

PFM_VSN_PD_EN: Enable or Disable PFM VSN power down function during power off sequence.

PFM_VSN_PD_EN	Function
0	Disable
1	**Enable (Default)**

OCP_PROT_EN: Shut down PFM VSP/ VSN voltage when over current is detected (OCD).

OCP_PROT_EN	Function
0	**PFM works (Default)**
1	SHUT down PFM

PFM_OK_DEB[2:0]: Select the debounce time for charge PFM VSP/ VSN voltage power on ready function.

PFM_OK_DEB[2:0]	Function
0h	1ms
1h	2ms
2h	4ms
3h	**8ms (Default)**
4h	16ms
5h	32ms
6h	64ms
7h	128ms

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	20h	Reserved	Reserved	PFM_VSN_DEB_SEL[1:0]		Reserved	Reserved	PFM_VSN_HYS_SEL[1:0]	
Default		0	0	0	0	0	0	0	0

Description	**PFM_VSN_DEB_SEL[1:0]:** VSN noise debounce count selection. **PFM_VSN_HYS_SEL[1:0]:** PFM VSN hysteresis window selection.

PFM_VSN_DEB_SEL[1:0]	Function
0h	**3 counts (Default)**
1h	4 counts
2h	5 counts
3h	6 counts

PFM_VSN_HYS_SEL[1:0]	Function
0h	**10mV (Default)**
1h	20mV
2h	30mV
3h	40mV

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	21h	PFM_VSP_ADD_NUM[3:0]				PFM_VSP_SUB_NUM[3:0]			
Default		0	0	0	0	0	0	0	0
Description		**PFM_VSP_ADD_NUM[3:0]:** Parameter of PFWM Duty Control function. **PFM_VSP_SUB_NUM[3:0]:** Parameter of PFWM Duty Control function.							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	22h	PFM_VSN_ADD_NUM[3:0]				PFM_VSN_SUB_NUM[3:0]			
Default		0	0	0	0	0	0	0	0
Description		**PFM_VSN_ADD_NUM[3:0]:** Parameter of PFWM Duty Control function. **PFM_VSN_SUB_NUM[3:0]:** Parameter of PFWM Duty Control function.							

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	23h	Reserved	PFM_VSP_2ND_TRIM[2:0]			Reserved	PFM_VSP_VOF_SEL[2:0]		
Default		0	0	0	0	0	0	1	1

Description

PFM_VSP_2ND_TRIM[2:0]: Trim adjustment of PFM VSP voltage.

PFM_VSP_2ND_TRIM[2:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Add 3 step trim voltage
4h	Add 4 step trim voltage
5h	Add 5 step trim voltage
6h	Subtract 1 step trim voltage
7h	Subtract 2 step trim voltage

PFM_VSP_VOF_SEL[2:0]: PFM VSP voltage offset selection.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	24h	Reserved	PFM_VSN_2ND_TRIM[2:0]			Reserved	PFM_VSN_VOF_SEL[2:0]		
Default		0	0	0	0	0	0	1	1

Description

PFM_VSN_2ND_TRIM[2:0]: Trim adjustment of PFM VSP voltage.

PFM_VSN_2ND_TRIM[2:0]	Function
0h	**No adjustment (Default)**
1h	Add 1 step trim voltage
2h	Add 2 step trim voltage
3h	Add 3 step trim voltage
4h	Add 4 step trim voltage
5h	Add 5 step trim voltage
6h	Subtract 1 step trim voltage
7h	Subtract 2 step trim voltage

PFM_VSN_VOF_SEL[2:0]: PFM VSN voltage offset selection.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	25h	CP_VGH_RATIO_SEL[1:0]		CP_VGH_MODE_SEL[1:0]		Reserved	CP_VGH_CLK[2:0]		
Default		0	1	1	1	0	1	0	0

Description

CP_VGH_RATIO_SEL[1:0]: Charge pump VGH voltage X2~X4 selection.

CP_VGH_RATIO_SEL[1:0]	Function
0h	X2
1h	**X3 (Default)**
2h	X4
3h	X4

CP_VGH_MODE_SEL: Charge pump flying cap mode selection for VGH.

CP_VGH_MODE_SEL[1:0]	Function
0h	One flying cap for 2X, 3X.
1h	Two flying caps for 2X, 3X, 4X.
2h	Two flying caps for 2X, 3X, 4X.
3h	**Three flying caps for 2X, 3X, 4X. (Default)**

CP_VGH_CLK[2:0]: Set Charge Pump VGH's pumping clock frequency.
(See the description of Page7, Addr. 0x26)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	26h	CP_VGL_ RATIO_SEL	CP_VGL_ MODE_SEL	Reserved	Reserved	Reserved	CP_VGL_CLK[2:0]		
Default		1	1	0	0	0	1	0	0

Description

CP_VGL_RATIO_SEL: Charge pump VGL voltage X2~X3 selection.

CP_VGL_RATIO_SEL	Function
0	X2
1	**X2 (Default)**

CP_VGL_MODE_SEL: Charge pump flying cap mode selection for VGH.

CP_VGL_MODE_SEL	Function
0	One flying cap for 2X, 3X.
1	**Two flying caps for 2X, 3X. (Default)**

CP_VGL_CLK[2:0]: Set Charge Pump VGL's pumping clock frequency.

CP_VGH_CLK[2:0] CP_VGL_CLK[2:0]	Function
0h	1/4 * HS
1h	1/2 * HS
2h	1 * HS
3h	2 * HS
4h	**100 KHz (Default)**
5h	150 KHz
6h	200 KHz
7h	250 KHz

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	27h	CP_VGH_OVD	CP_VGL_OVD	CP_OVD_DEB[2:0]			CP_OK_DEB[2:0]		
Default		1	1	0	1	0	0	1	0

Description

CP_VGH_OVD: On or off charge pump VGH OVD (Over Voltage Detection) function.

CP_VGH_OVD	Function
0	Detect OFF*
1	**Detect ON (Default)**

CP_VGL_OVD: On or off charge pump VGL OVD (Over Voltage Detection) function.

CP_VGL_OVD	Function
0	Detect OFF*
1	**Detect ON (Default)**

Note: When selecting detect OFF, Error is not reported if OVD happens

CP_OVD_DEB[2:0]: Select the debounce time for charge pump VGH/ VGL OVD (over voltage detection) function.

CP_OVD_DEB[2:0]	Function
0h	2ms
1h	4ms
2h	**8ms (Default)**
3h	16ms
4h	32ms
5h	64ms
6h	128ms
7h	256ms

CP_OK_DEB[2:0]: Select the debounce time for charge pump VGH/ VGL voltage power on ready function.

CP_OK_DEB[2:0]	Function
0h	2ms
1h	4ms
2h	**8ms (Default)**
3h	16ms
4h	32ms
5h	64ms
6h	128ms
7h	256ms

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	28h	CP_VGH_OVD_SEL[1:0]		CP_VGL_OVD_SEL[1:0]		CP_VGH_SR[1:0]		CP_VGL_SR[1:0]	
Default		0	0	0	0	1	1	1	1

Description

CP_VGH_OVD_SEL[1:0]: Set charge pump VGH OVD (Over Voltage Detection) voltage.
CP_VGL_OVD_SEL[1:0]: Set charge pump VGL OVD (Over Voltage Detection) voltage.

CP_VGH_OVD_SEL[1:0] CP_VGL_OVD_SEL[1:0]	Function
0h	**Voltage over 15% (Default)**
1h	Voltage over 20%
2h	Voltage over 30%
3h	Voltage over 40%

CP_VGH_SR[1:0]: VGH slew rate control selection.
CP_VGL_SR[1:0]: VGH slew rate control selection.

CP_VGH_SR[1:0] CP_VGL_SR[1:0]	Function
0h	25%
1h	50%
2h	75%
3h	**100% (Default)**

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	29h	CP_CLK_DLY[1:0]		CP_EN_TO_PD_DLY[2:0]			Reserved	Reserved	Reserved
Default		1	0	0	0	0	1	0	0

Description

CP_CLK_DLY[1:0]: Set Charge Pump CK delay time.

CP_CLK_DLY[1:0]	Function
0h	No delay.
1h	Delay 1/4 high pulse width time.
2h	**Delay 1/2 high pulse width time. (Default)**
3h	Delay 3/4 high pulse width time.

CP_EN_TO_PD_DLY[2:0]: Set the non-overlap timing between Charge Pump enable end point and Charge Pump Power Down enable start point during power off sequence.

CP_EN_TO_PD_DLY[2:0]	Function
0h	**0 (Default)**
1h	80 ns
2h	160 ns
3h	240 ns
4h	320 ns
5h	400 ns
6h	480 ns
7h	560 ns

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Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	D3_SKEW_A_ID0[1:0]		D2_SKEW_A_ID0[1:0]		D1_SKEW_A_ID0[1:0]		D0_SKEW_A_ID0[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	02h	CK_SKEW_A_ID0[1:0]		D3_SKEW_B_ID0[1:0]		D2_SKEW_B_ID0[1:0]		D1_SKEW_B_ID0[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	03h	D0_SKEW_B_ID0[1:0]		CK_SKEW_B_ID0[1:0]		D3_SKEW_A_ID1[1:0]		D2_SKEW_A_ID1[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	04h	D1_SKEW_A_ID1[1:0]		D0_SKEW_A_ID1[1:0]		CK_SKEW_A_ID1[1:0]		D3_SKEW_B_ID1[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	05h	D2_SKEW_B_ID1[1:0]		D1_SKEW_B_ID1[1:0]		D0_SKEW_B_ID1[1:0]		CK_SKEW_B_ID1[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	06h	D3_SKEW_A_ID2[1:0]		D2_SKEW_A_ID2[1:0]		D1_SKEW_A_ID2[1:0]		D0_SKEW_A_ID2[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	07h	CK_SKEW_A_ID2[1:0]		D3_SKEW_B_ID2[1:0]		D2_SKEW_B_ID2[1:0]		D1_SKEW_B_ID2[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	08h	D0_SKEW_B_ID2[1:0]		CK_SKEW_B_ID2[1:0]		DLL_IF_ID3	DLL_IF_ID2	DLL_IF_ID1	DLL_IF_ID0
Default		0	0	0	0	0	0	0	0

Description

DX_SKEW_Y_IDZ[1:0]: Delay selection of data path at port A and port B in the chip ID0~ID2.

DX_SKEW_Y_IDZ[1:0]	Function
0h	No delay (Default)
1h	Minimum
2h	Middle
3h	Maximum

X: means data pair (0= D0 data pair / 1= D1 data pair / 2= D2 data pair / 3= D3 data pair)
Y: means data port (A= port A / B=port B)
Z: means chip ID (0= chip ID0 / 1= chip ID1 / 2= chip ID2)

DLL_IF_IDZ[1:0]: Enable LVDS low frequency section.

DLL_IF_IDZ[1:0]	Function
0	Disable, and the setting is for 160MHz ~ 50MHz (Default)
1	Enable, and the setting is for 50MHz ~ 15MHz

Z: means chip ID (0= chip ID0 / 1= chip ID1 / 2= chip ID2 / 3= chip ID3)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	09h	TR_ID3[1:0]		TR_ID2[1:0]		TR_ID1[1:0]		TR_ID0[1:0]	
Default		1	1	1	1	1	1	1	1

Description

TR_IDZ[1:0]: Termination resistor setting for LVDS differential input.

TR_IDZ[1:0]	Function
0h	Open
1h	300 ohm
2h	200 ohm
3h	**100 ohm (Default)**

Z: means chip ID (0= chip ID0 / 1= chip ID1 / 2= chip ID2 / 3= chip ID3)

Note: If **TR_EN**=0, termination resistor will be set to open status.

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ah	Reserved	Reserved	Reserved	Reserved	D3_SKEW_A_ID3[1:0]		D2_SKEW_A_ID3[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Bh	D1_SKEW_A_ID3[1:0]		D0_SKEW_A_ID3[1:0]		CK_SKEW_A_ID3[1:0]		D3_SKEW_B_ID3[1:0]	
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ch	D2_SKEW_B_ID3[1:0]		D1_SKEW_B_ID3[1:0]		D0_SKEW_B_ID3[1:0]		CK_SKEW_B_ID3[1:0]	
Default		0	0	0	0	0	0	0	0

Description

DX_SKEW_Y_ID3[1:0]: Delay selection of data path at port A and port B in the chip ID3.

DX_SKEW_Y_ID3[1:0]	Function
0h	**No delay (Default)**
1h	Minimum
2h	Middle
3h	Maximum

X: means data pair (0= D0 data pair / 1= D1 data pair / 2= D2 data pair / 3= D3 data pair)

Y: means data port (A= port A / B=port B)

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Dh	Reserved	EN_LVDS_MX	DIO_SR[1:0]		TR_EN	LVDS_CKPOL	EN_LVDS_MX_VB	RX_DATSWAP
Default		0	0	0	1	1	0	0	0

Description

EN_LVDS_MX: Gated input LVDS signals to 0 when RX is not stable.

EN_LVDS_MX	Function
0	**Disable (Default)**
1	Enable

DIO_SR[1:0]: Output pad driving selection.

DIO_SR[1:0]	Function
0h	Output driving weakest
1h	**Output driving second weak (Default).**
2h	Output driving second strong.
3h	Output driving strongest.

	TR_EN: Enable or disable termination resistance. **TR_EN** / Function 0 / Disable **1** / **Enable (Default)** **LVDS_CKPOL:** LVDS input clock polarity inverse control. **LVDS_CKPOL** / Function **0** / **Normal (Default)** 1 / Inverse **EN_LVDS_MX_VB:** Gated input LVDS signals to 0 during V-blanking when RX is not stable. **EN_LVDS_MX_VB** / Function **0** / **Disable (Default)** 1 / Enable **RX_DATSWAP:** Swap LVDS lane0 and lane3 of both port A and B. **RX_DATSWAP** / Function **0** / **No swap (Default)** 1 / Swap

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	20h	Reserved	MP_LANE[1:0]		MP_EoTP	Reserved	Reserved	Reserved	Reserved
Default		0	0	0	0	0	0	1	1

Description

MP_LANE[1:0]: MIPI Lane selection.

MP_LANE[1:0]	Function
0h	**4 Lanes (Default)**
1h	2 Lanes
2h	1 Lane
3h	1 Lane

MP_EoTP: EoTP mode enable function.

MP_EoTP	Function
0	**Disable (Default)**
1	Enable

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Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	01h	Reserved	GMAP_A0[6:0]						
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	02h	Reserved	GMAP_A2[6:0]						
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	03h	Reserved	GMAP_A4[6:0]						
Default		0	0	0	0	0	1	0	0

Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	04h	Reserved	GMAP_A8[6:0]						
Default		0	0	0	0	1	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	05h	Reserved	GMAP_A16[6:0]						
Default		0	0	0	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	06h	Reserved	GMAP_A24[6:0]						
Default		0	0	0	1	1	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	07h	Reserved	GMAP_A32[6:0]						
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	08h	Reserved	GMAP_A48[6:0]						
Default		0	0	0	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	09h	Reserved	GMAP_A80[6:0]						
Default		0	0	0	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ah	Reserved	GMAP_A128[6:0]						
Default		0	1	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Bh	Reserved	GMAP_A176[6:0]						
Default		0	1	1	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Ch	Reserved	GMAP_A208[6:0]						
Default		0	1	1	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Dh	Reserved	GMAP_A224[6:0]						
Default		0	1	1	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Eh	Reserved	GMAP_A232[6:0]						
Default		0	1	1	0	1	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	0Fh	Reserved	GMAP_A240[6:0]						
Default		0	1	1	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	10h	Reserved	GMAP_A248[6:0]						
Default		0	1	1	1	1	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	11h	Reserved	GMAP_A252[6:0]						
Default		0	1	1	1	1	1	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0

R/W	12h	Reserved	GMAP_A254[6:0]						
Default		0	1	1	1	1	1	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	13h	Reserved	GMAP_A255[6:0]						
Default		0	1	1	1	1	1	1	1
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	14h	Reserved	GMAN_A0[6:0]						
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	15h	Reserved	GMAN_A2[6:0]						
Default		0	0	0	0	0	0	1	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	16h	Reserved	GMAN_A4[6:0]						
Default		0	0	0	0	0	1	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	17h	Reserved	GMAN_A8[6:0]						
Default		0	0	0	0	1	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	18h	Reserved	GMAN_A16[6:0]						
Default		0	0	0	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	19h	Reserved	GMAN_A24[6:0]						
Default		0	0	0	1	1	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ah	Reserved	GMAN_A32[6:0]						
Default		0	0	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Bh	Reserved	GMAN_A48[6:0]						
Default		0	0	0	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Ch	Reserved	GMAN_A80[6:0]						
Default		0	0	0	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Dh	Reserved	GMAN_A128[6:0]						
Default		0	1	0	0	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Eh	Reserved	GMAN_A176[6:0]						
Default		0	1	1	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	1Fh	Reserved	GMAN_A208[6:0]						
Default		0	1	1	1	0	0	0	0
Type	Add.	D7	D6	D5	D4	D3	D2	D1	D0
R/W	20h	Reserved	GMAN_A224[6:0]						

Default		0	1	1	1	0	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**21h**	Reserved	GMAN_A232[6:0]						
Default		0	1	1	0	1	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**22h**	Reserved	GMAN_A240[6:0]						
Default		0	1	1	1	0	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**23h**	Reserved	GMAN_A248[6:0]						
Default		0	1	1	1	1	0	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**24h**	Reserved	GMAN_A252[6:0]						
Default		0	1	1	1	1	1	0	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**25h**	Reserved	GMAN_A254[6:0]						
Default		0	1	1	1	1	1	1	0
Type	**Add.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	**26h**	Reserved	GMAN_A255[6:0]						
Default		0	1	1	1	1	1	1	1

Description

GMAP_A0[6:0]: Positive gamma correction register for gray level 0 when NBW=1, or gray level 255 when NBW=0.
GMAP_A2[6:0]: Positive gamma correction register for gray level 2 when NBW=1, or gray level 253 when NBW=0.
GMAP_A4[6:0]: Positive gamma correction register for gray level 4 when NBW=1, or gray level 251 when NBW=0.
GMAP_A8[6:0]: Positive gamma correction register for gray level 8 when NBW=1, or gray level 247 when NBW=0.
GMAP_A16[6:0]: Positive gamma correction register for gray level 16 when NBW=1, or gray level 239 when NBW=0.
GMAP_A24[6:0]: Positive gamma correction register for gray level 24 when NBW=1, or gray level 231 when NBW=0.
GMAP_A32[6:0]: Positive gamma correction register for gray level 32 when NBW=1, or gray level 223 when NBW=0.
GMAP_A48[6:0]: Positive gamma correction register for gray level 48 when NBW=1, or gray level 207 when NBW=0.
GMAP_A80[6:0]: Positive gamma correction register for gray level 80 when NBW=1, or gray level 175 when NBW=0.
GMAP_A128[6:0]: Positive gamma correction register for gray level 128 when NBW=1, or gray level 127 when NBW=0.
GMAP_A176[6:0]: Positive gamma correction register for gray level 176 when NBW=1, or gray level 79 when NBW=0.
GMAP_A208[6:0]: Positive gamma correction register for gray level 208 when NBW=1, or gray level 47 when NBW=0.
GMAP_A224[6:0]: Positive gamma correction register for gray level 224 when NBW=1, or gray level 31 when NBW=0.
GMAP_A232[6:0]: Positive gamma correction register for gray level 232 when NBW=1, or gray level 23 when NBW=0.
GMAP_A240[6:0]: Positive gamma correction register for gray level 240 when NBW=1, or gray level 15 when NBW=0.
GMAP_A248[6:0]: Positive gamma correction register for gray level 248 when NBW=1, or gray level 7 when NBW=0.
GMAP_A252[6:0]: Positive gamma correction register for gray level 252 when NBW=1, or gray level 3 when NBW=0.
GMAP_A254[6:0]: Positive gamma correction register for gray level 254 when NBW=1, or gray level 1 when NBW=0.
GMAP_A255[6:0]: Positive gamma correction register for gray level 255 when NBW=1, or gray level 0 when NBW=0.
GMAN_A0[6:0]: Negative gamma correction register for gray level 0 when NBW=1, or gray level 255 when NBW=0.
GMAN_A2[6:0]: Negative gamma correction register for gray level 2 when NBW=1, or gray level 253 when NBW=0.
GMAN_A4[6:0]: Negative gamma correction register for gray level 4 when NBW=1, or gray level 251 when NBW=0.
GMAN_A8[6:0]: Negative gamma correction register for gray level 8 when NBW=1, or gray level 247 when NBW=0.
GMAN_A16[6:0]: Negative gamma correction register for gray level 16 when NBW=1, or gray level 239 when NBW=0.
GMAN_A24[6:0]: Negative gamma correction register for gray level 24 when NBW=1, or gray level 231 when NBW=0.
GMAN_A32[6:0]: Negative gamma correction register for gray level 32 when NBW=1, or gray level 223 when NBW=0.
GMAN_A48[6:0]: Negative gamma correction register for gray level 48 when NBW=1, or gray level 207 when NBW=0.
GMAN_A80[6:0]: Negative gamma correction register for gray level 80 when NBW=1, or gray level 175 when NBW=0.
GMAN_A128[6:0]: Negative gamma correction register for gray level 128 when NBW=1, or gray level 127 when NBW=0.
GMAN_A176[6:0]: Negative gamma correction register for gray level 176 when NBW=1, or gray level 79 when NBW=0.
GMAN_A208[6:0]: Negative gamma correction register for gray level 208 when NBW=1, or gray level 47 when NBW=0.
GMAN_A224[6:0]: Negative gamma correction register for gray level 224 when NBW=1, or gray level 31 when NBW=0.
GMAN_A232[6:0]: Negative gamma correction register for gray level 232 when NBW=1, or gray level 23 when NBW=0.
GMAN_A240[6:0]: Negative gamma correction register for gray level 240 when NBW=1, or gray level 15 when NBW=0.
GMAN_A248[6:0]: Negative gamma correction register for gray level 248 when NBW=1, or gray level 7 when NBW=0.
GMAN_A252[6:0]: Negative gamma correction register for gray level 252 when NBW=1, or gray level 3 when NBW=0.

	GMAN_A254[6:0]: Negative gamma correction register for gray level 254 when NBW=1, or gray level 1 when NBW=0. **GMAN_A255[6:0]:** Negative gamma correction register for gray level 255 when NBW=1, or gray level 0 when NBW=0. **Note:** Reserved registers above are for Forcelead's engineering mode to use. Please do not change the default values.

6.3 MIPI Command List

Command	Operation code	R/W	Parameter	D7	D6	D5	D4	D3	D2	D1	D0	LP Mode	HS Mode
00h	NOP	W	-	No Argument								V	V
01h	SWRESET	W	-	No Argument								V	X
0Ah	GET_PWR_MODE	R	1st Parameter	0	D6	0	D4	D3	D2	0	0	V	X
0Dh	GET_DISP_MODE	R	1st Parameter	0	0	D5	0	0	0	0	0	V	X
0Eh	GET_SIG_MODE	R	1st Parameter	D7	D6	0	0	0	0	0	0	V	X
10h	SLPIN	W	-	No Argument								V	V
11h	SLPOUT	W	-	No Argument								V	X
20h	INVOFF	W	-	No Argument								V	V
21h	INVON	W	-	No Argument								V	V
28h	DISPOFF	W	-	No Argument								V	V
29h	DISPON	W	-	No Argument								V	V
34h	SET_TEAR_OFF	W	-	No Argument								V	V
35h	SET_TEAR_ON	W	1st Parameter	0	0	0	0	0	0	0	M	V	V
38h	IDMOFF	W	-	No Argument								V	V
39h	IDMON	W	-	No Argument								V	V
A1h	READ_DDB_START	R	1st Parameter	ID1								V	V
		R	2nd Parameter	ID2									

6.4 MIPI Command Description

(00h) NOP: No Operation

00h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	0	0	0	00
Parameter	No Argument									
Description	This command is an empty command; it does not have any effect on the display module.									
Restriction	-									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

(01h) SWRESET: Software Reset

01h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	0	0	1	01
Parameter	No Argument									
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to S/W Reset default values. The display is blank immediately.									
Restriction	(1) It will be necessary to wait 5 msec before sending new command following software reset. (2) The display module loads all display suppliers' factory default values to the registers during this 5 msec. (3) If software reset is applied during Sleep Out mode, it will be necessary to wait 120 msec before sending Sleep Out command. (4) Software reset command cannot be sent during Sleep Out sequence.									
Register Availability										
Default	-									

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

(0Ah) GET_PWR_MODE: Read Display Power Mode

0Ah	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	0	1	0	0A
1st Parameter		D7	D6	D5	D4	D3	D2	D1	D0	1C

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Defined	"0"
D6	Idle Mode On/Off	"1" = Idle Mode on, "0" = Idle Mode off
D5	Not Defined	"0"
D4	Sleep In/Out	"1" = Sleep out , "0" = Sleep in
D3	Display Normal Mode On	"1" = Display Normal on
D2	Display On/Off	"1" = Display on, "0" = Display off
D1	Not Defined	"0"
D0	Not Defined	"0"

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	1Ch
S/W Reset	1Ch
H/W Reset	1Ch

(0Dh) GET_DISP_MODE: Read the Current Display Mode

0Dh	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	0	1	0D
1st Parameter	-	0	0	D5	0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Defined	"0"
D6	Not Defined	"0"
D5	Inversion On/Off	"1" = Inversion on, "0" = Inversion off
D4	Not Defined	"0"
D3	Not Defined	"0"
D2	Not Defined	"0"
D1	Not Defined	"0"
D0	Not Defined	"0"

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(0Eh) GET_SIG_MODE: Get Display Module Signaling Mode

0Eh	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	1	0	0E
1st Parameter	-	D7	D6	0	0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Frame Tearing Effect Line On/Off	“1” = TE On, “0” = TE Off
D6	Tearing Effect Line Output Mode	“1” = Mode B, “0” = Mode A
D4	Not Defined	“0”
D4	Not Defined	“0”
D3	Not Defined	“0”
D2	Not Defined	“0”
D1	Not Defined	“0”
D0	Not Defined	“0”

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(10h) SLPIN: Enter the Sleep-In Mode

10h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	0	10
Parameter	No Argument									
Description	This command causes the display module to enter the Sleep mode. In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports.									
Restriction	This command has no effect when the display module is already in Sleep Mode.									

Register Availability

When r_mipi_stbyb_sel=1 (register: page8 address=2Bh bit7), enter standby mode will not refer to HW pin and STBYB command. Enter standby mode only use DCS command (10h).

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

When r_mipi_stbyb_sel=0 (register: page8 address=2Bh bit7), enter standby mode will refer to HW pin or STBYB command

Status	**Availability**
Normal Mode On, Idle Mode Off, Sleep Out	No
Normal Mode On, Idle Mode On, Sleep Out	No
Sleep In or Booster Off	No

Default

Status	Default Value
Power On Sequence	Sleep-In
S/W Reset	Sleep-In
H/W Reset	Sleep-In

(11h) SLPOUT: Exit the Sleep-In Mode

11h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	1	11
Parameter	No Argument									
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled.									
Restriction	This command has no effect when module is already in sleep out mode.									

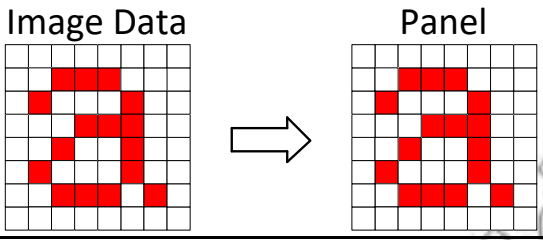
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Sleep-In
S/W Reset	Sleep-In
H/W Reset	Sleep-In

(20h) INVOFF: Display Inversion Off

20h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	0	20
Parameter	No Argument									
Description	This command is used to recover from display reverse mode, makes no change of contents of image data, and does not change any other status. **Example** 									
Restriction	This command has no effect when module is already in inversion off mode									

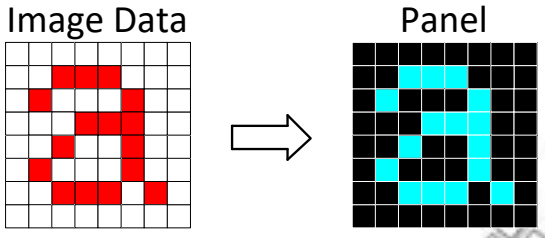
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

(21h) INVON: Display Inversion On

21h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	1	21
Parameter	No Argument									
Description	This command causes the display module to invert the image data only on the display device. The image data contents remain unchanged. No status bits are changed. **Example** 									
Restriction	This command has no effect when module is already in inversion on mode									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

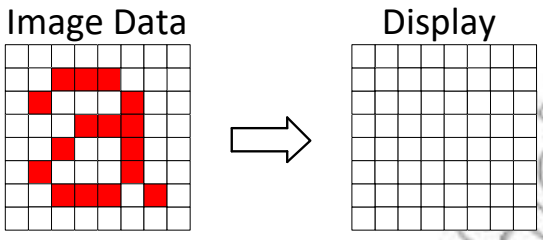
(28h) DISPOFF: Display Off

28h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	0	28
Parameter	No Argument									

Description

This command causes the display module to stop displaying the image data on the display device. The image data contents remain unchanged. No status bits are changed.
Exit from this command by the Display On command (29h)

Example



Restriction

This command has no effect when module is already in display off mode.

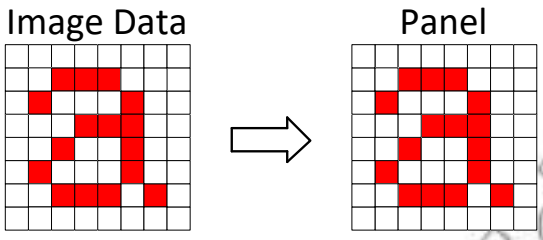
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

(29h) DISPON: Display On

29h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	1	29
Parameter	No Argument									
Description	This command causes the display module to start displaying the image data on the display device. The image data contents remain unchanged. No status bits are changed. **Example** 									
Restriction	This command has no effect when the module is already in Display On mode									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

(34h) SET_TEAR_OFF: Tearing Effect Line OFF

34h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	1	0	0	34
Parameter	No Argument									
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.									
Restriction	This command has no effect when TE is already OFF. Write this command only using DT=05h(no parameter).									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	TE Line Off
S/W Reset	TE Line Off
H/W Reset	TE Line Off

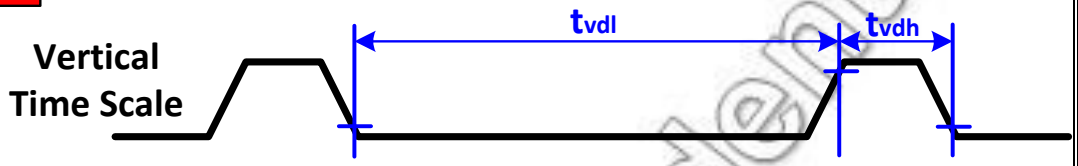
(35h) SET_TEAR_ON: Tearing Effect Line ON

0Dh	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	1	0	1	0D
1st Parameter	-	0	0	0	0	0	0	0	M	00

Description

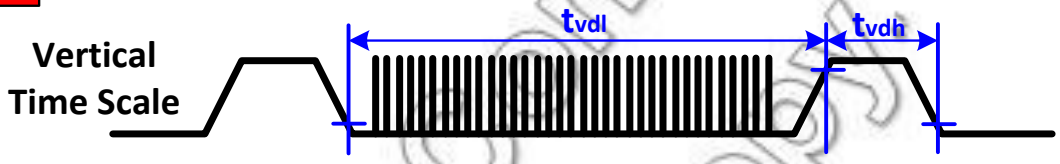
This command is used to turn ON the Tearing Effect output from the TE signal.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.
When M=0 : The Tearing Effect Output line consists of V-Blanking information only.

A



When M = 1 : The Tearing Effect Output line consists of both V-Blanking and H-Blanking information

B



Notes: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

(38h) IDLEOFF: Idle Mode Off

38h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	0	38
Parameter	No Argument									
Description	This command causes the display module to exit Idle mode. There will be no abnormal visible effect on the display mode change transition. When the idle mode is “Off” : (1) Display panel can display maximum 262K or 16.7M colors. (2) Normal frame frequency is applied.									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

(39h) IDLEON: Idle Mode On

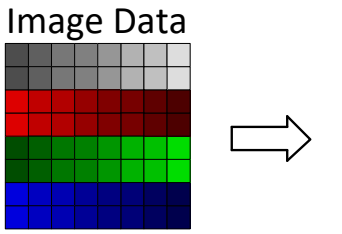
39h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	1	39
Parameter	No Argument									

Description

This command is used to enter into idle mode on.
When the Idle mode is “On” :

(1) Color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
(2) Exit from IDLEON by Idle Mode Off (38h) command.

Example



Color	R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	G_7 G_6 G_5 G_4 G_3 G_2 G_1 G_0	B_7 B_6 B_5 B_4 B_3 B_4 B_1 B_0
Black	0xxx xxxx	0xxx xxxx	0xxx xxxx
Blue	0xxx xxxx	0xxx xxxx	1xxx xxxx
Red	1xxx xxxx	0xxx xxxx	0xxx xxxx
Magenta	1xxx xxxx	0xxx xxxx	1xxx xxxx
Green	0xxx xxxx	1xxx xxxx	0xxx xxxx
Cyan	0xxx xxxx	1xxx xxxx	1xxx xxxx
Yellow	1xxx xxxx	1xxx xxxx	0xxx xxxx
White	1xxx xxxx	1xxx xxxx	1xxx xxxx

Restriction

This command has no effect when module is already in Idle On Mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

(A1h) READ_DDB_START: Read DDB Start

A1h	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	0	1	0	0	0	0	1	A1
1st Parameter	-	ID1								-
2nd Parameter	-	ID2								-
Description	This command returns supplier identification and display module model / revision information. ID1 : TBD ID2 : TBD									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

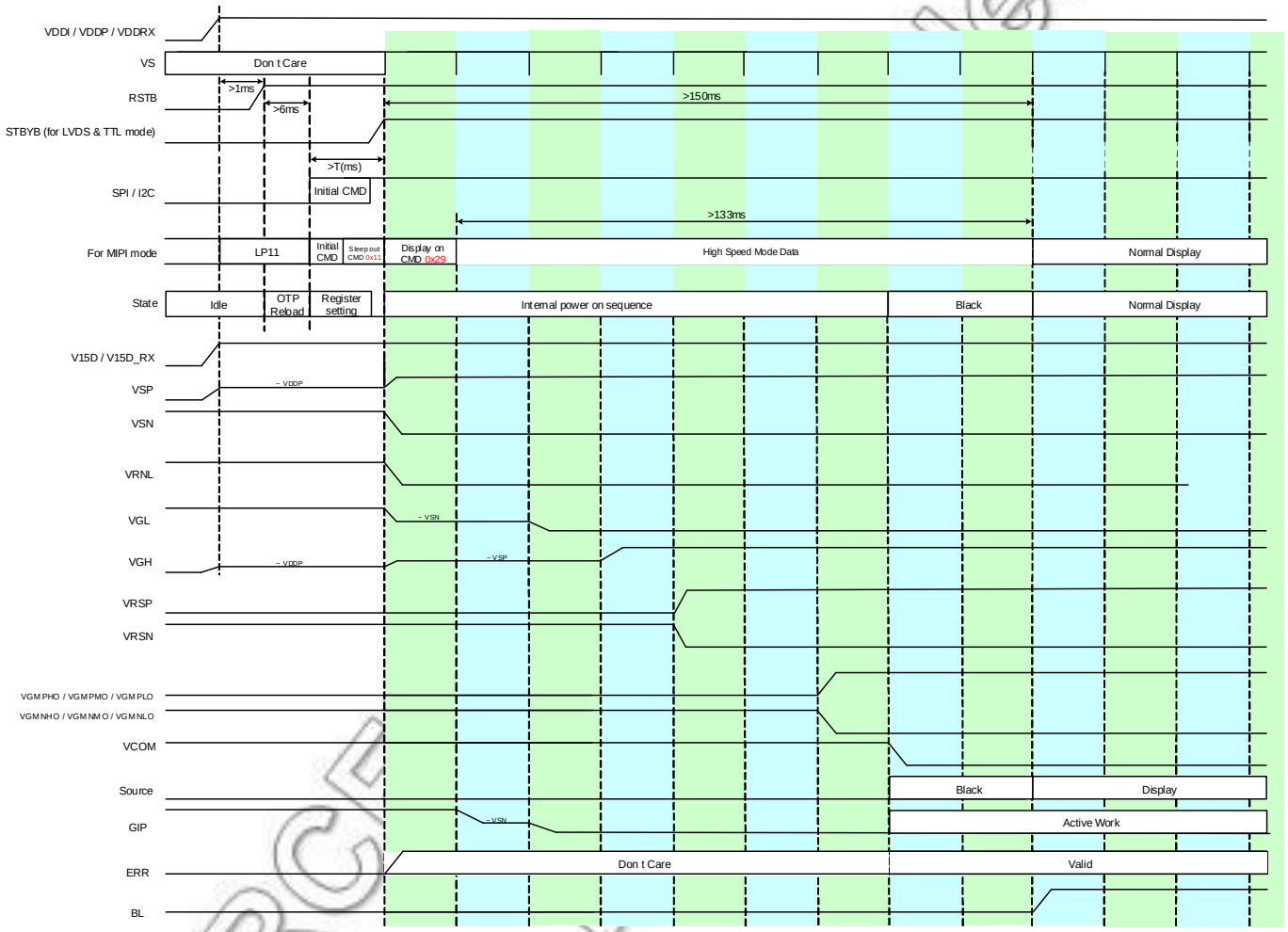
Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

7. OPERATION FLOW

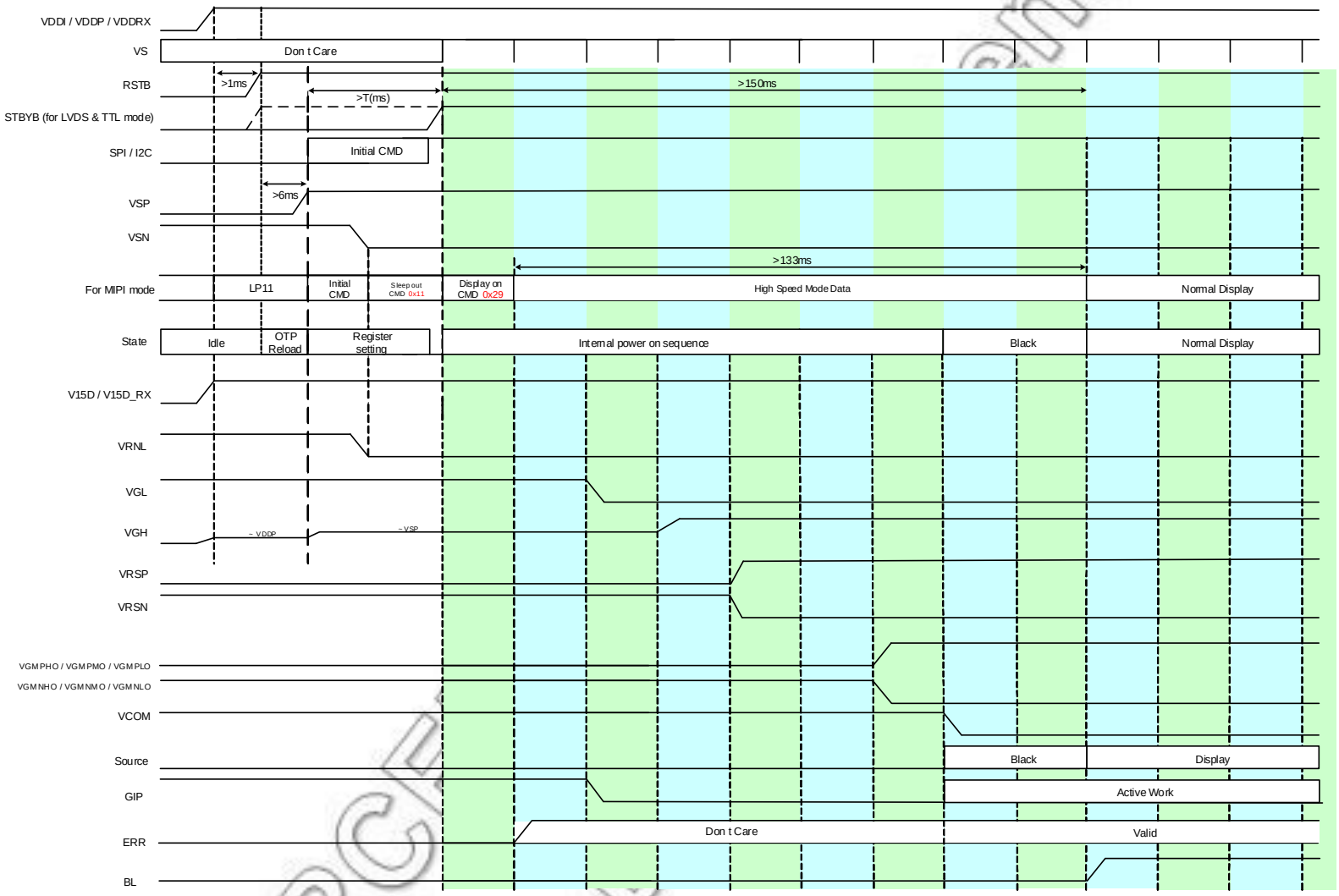
7.1 Power on Sequence

7.1.1 1 Power Mode



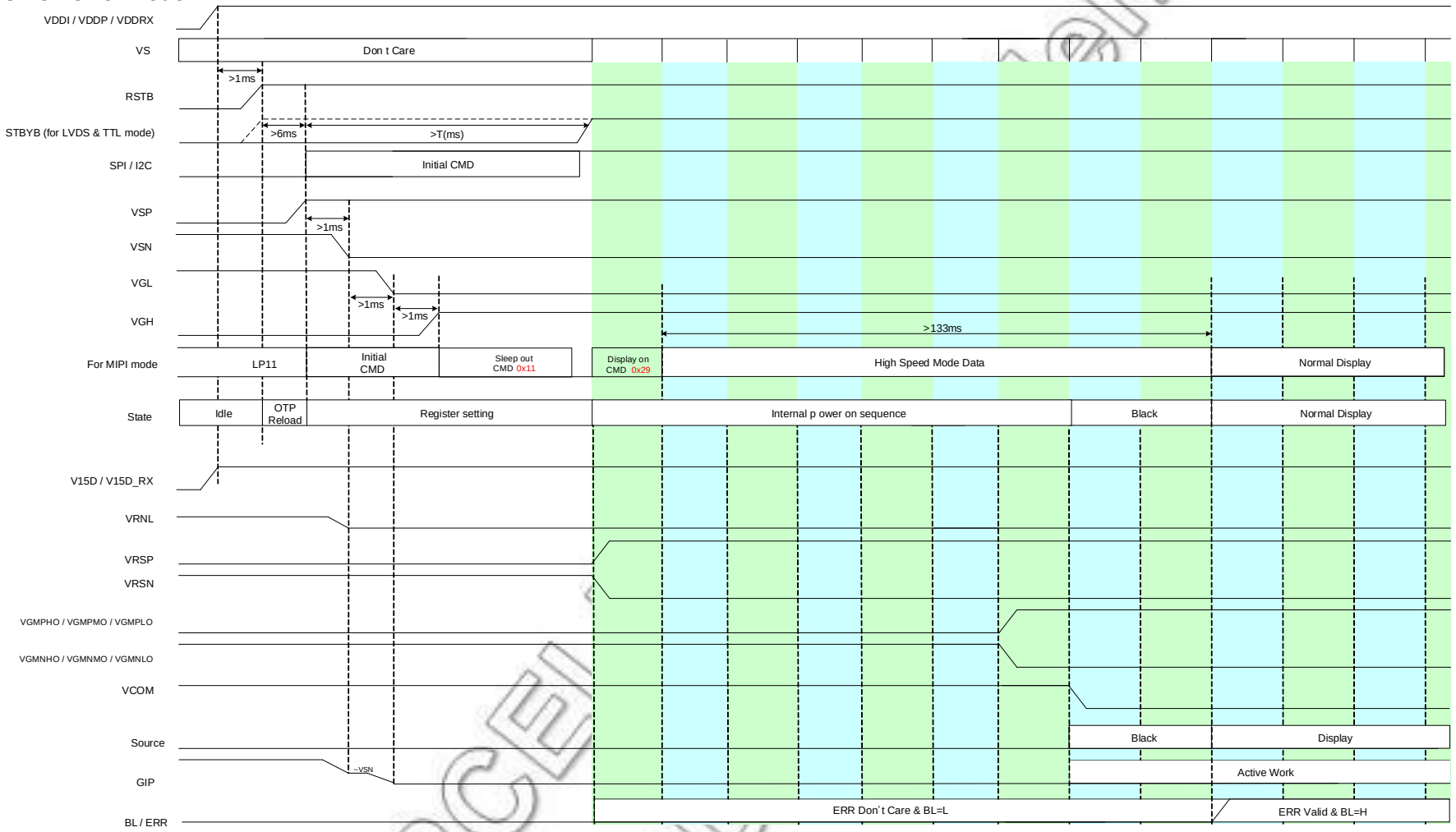
Note: T(ms) is initial CMD time

7.1.2 3 Power Mode



Note1: T(ms) is initial CMD time
Note2: User can set STBYB the same as RSTB when initial CMD is not needed.

7.1.3 5 Power Mode

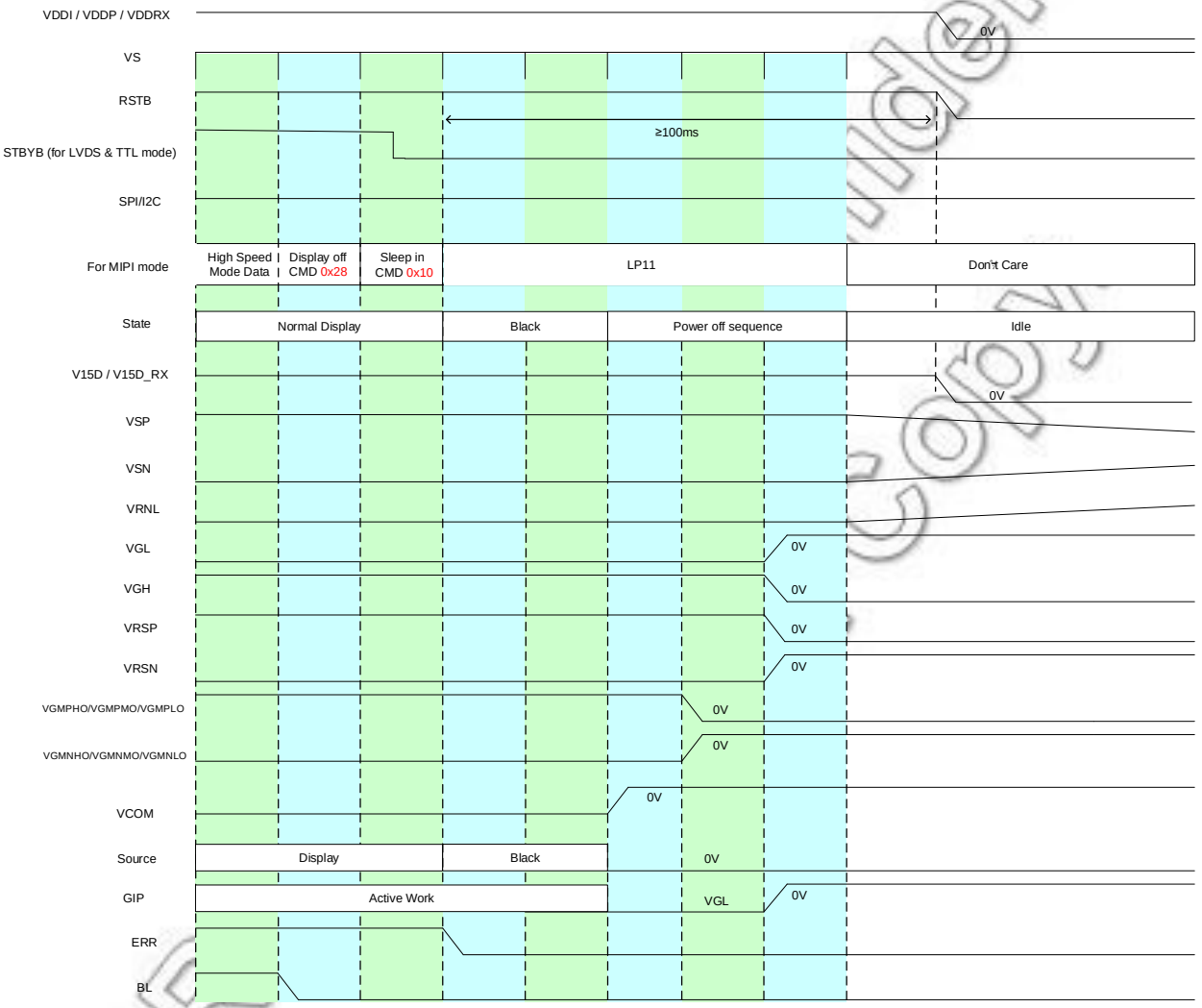


Note1: T(ms) is initial CMD time

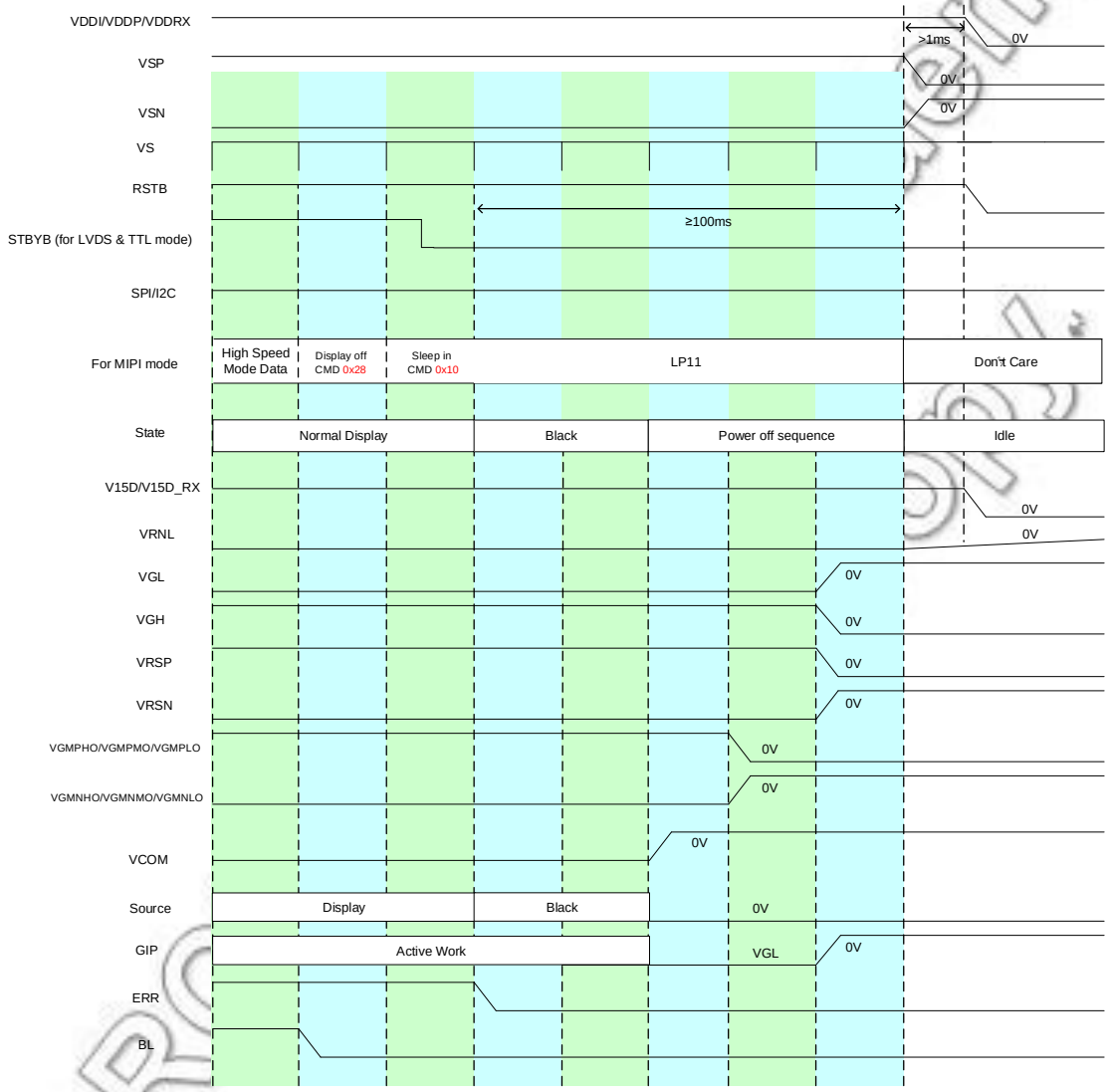
Note2: User can set STBYB the same as RSTB when initial CMD is not needed.

7.2 Stand-by and Power-off Sequence

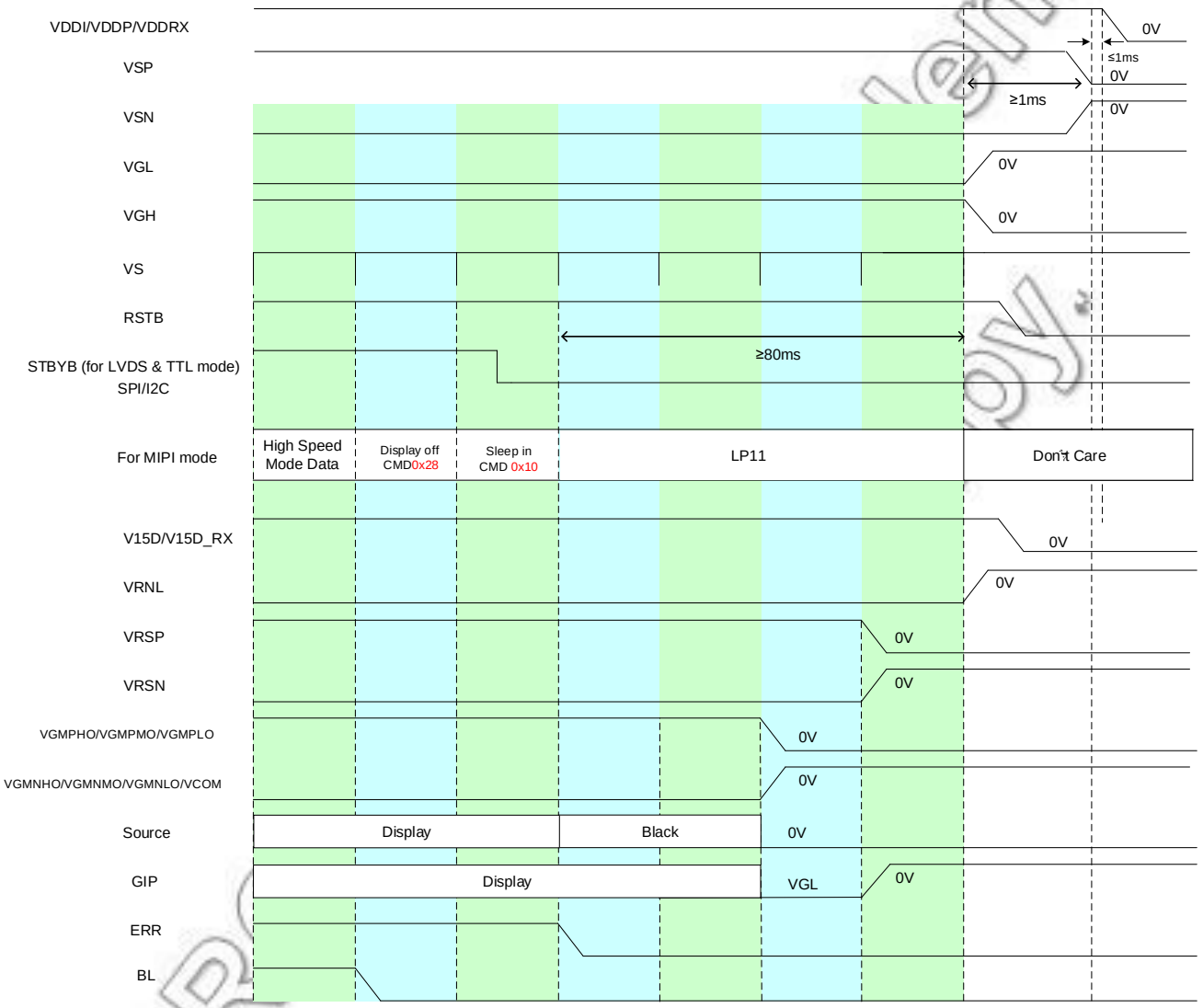
7.2.1 1 Power Mode



7.2.2 3 Power Mode

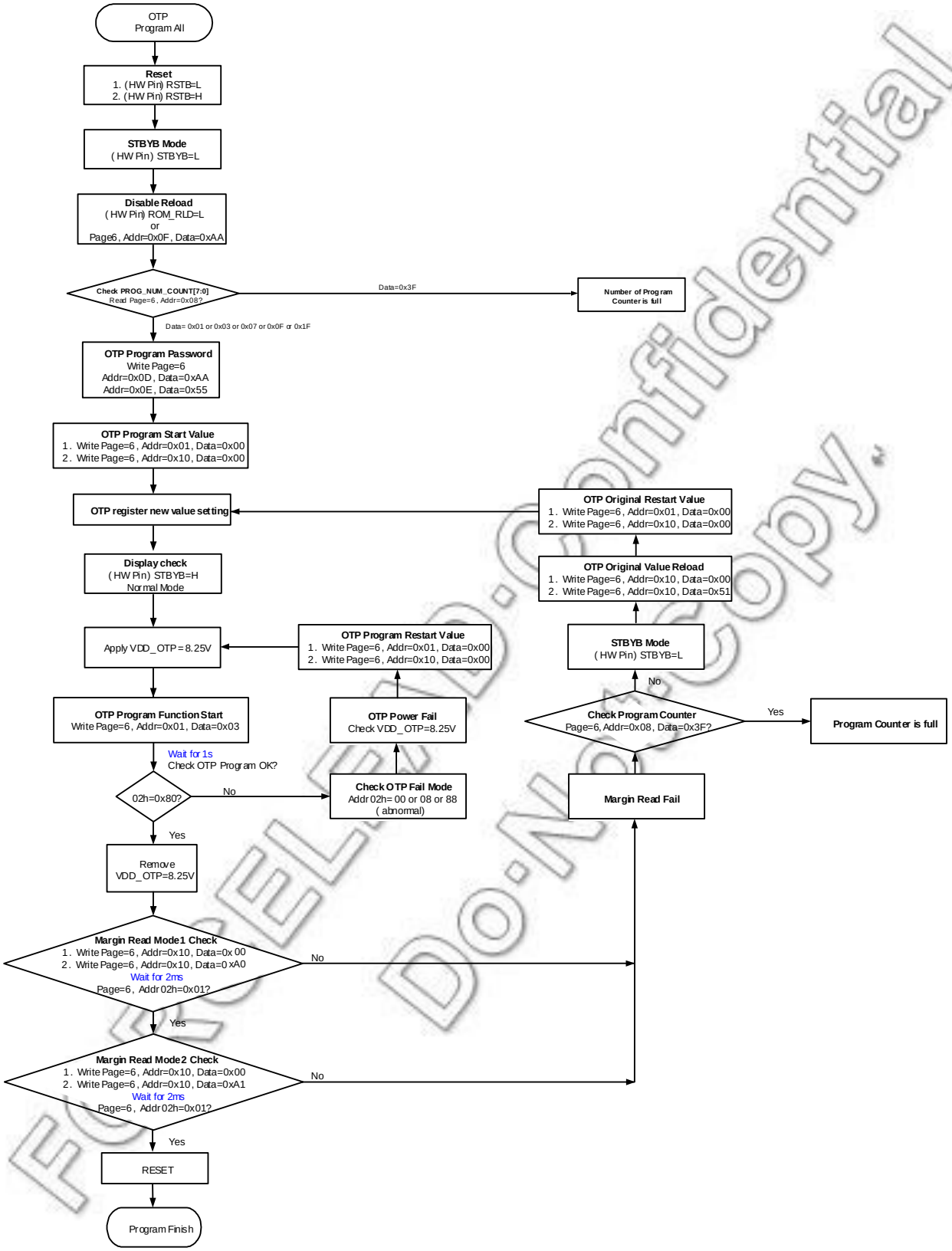


7.2.3 5 Power Mode



7.3 OTP Flow

OTP Program All



Note: The recommended VDDI voltage for OTP programming is >= 3.3V.

8. ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
I/O Power Supply Voltage	VDDI	-0.3 ~ 4.0	V
Interface Power supply voltage	VDDRX	-0.3 ~ 4.0	V
Analog Power supply voltage	VDDP, VDD_PFM	-0.3 ~ 4.0	V
	VSP	-0.3 ~ 7.0	V
	VSN	-7.0 ~ -0.3	V
	VGH – VGL	-0.5 ~ 35.2	V
SPI and I2C Interface Input Voltage	V_{IN}	-0.3 ~ VDDI +0.3	V
OTP Power supply voltage	VDD_OTP	-0.3 ~ 8.5	V
Storage temperature	T_{STR}	-55 ~ 125	°C
Junction temperature	T_{JC}	-40~125	°C

Notes:

1. Stresses exceed the absolute maximum ratings listed above may cause permanent damage to IC. The IC should be operated under the condition of DC/AC characteristics for normal operation. If this condition is not met, the IC may be malfunctioned, or the reliability may drop.
2. Parameters are valid in the operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

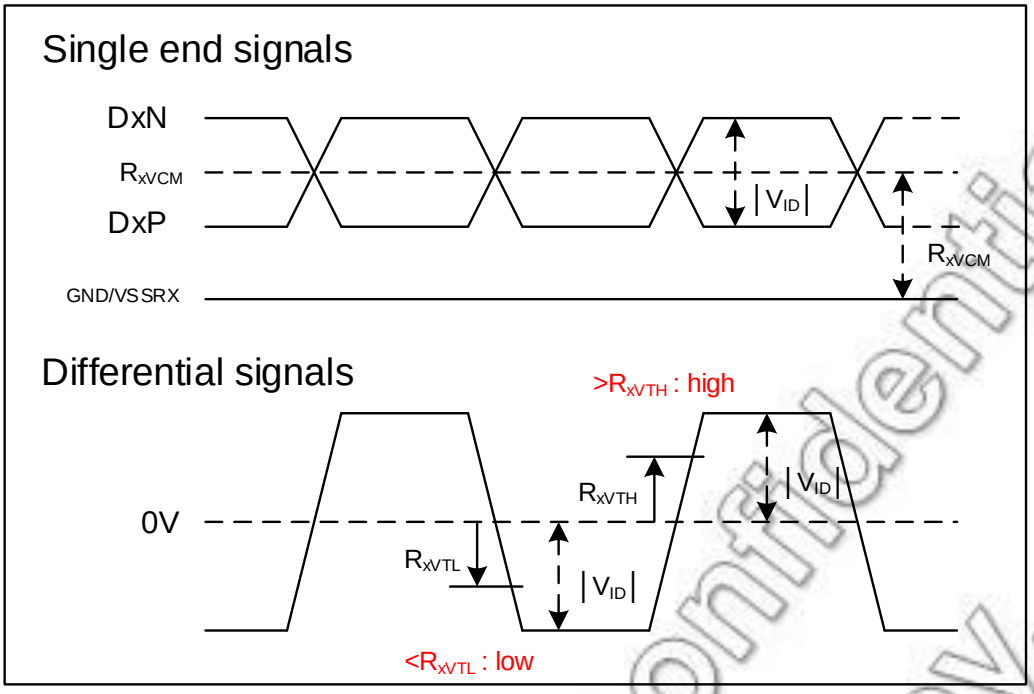
9. DC CHARACTERISTICS

9.1 Source Driver and LVDS

VSSI = VSSRX = VSSP = 0V

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage	VDDI	External Supply	3.0	3.3	3.6	V	VDDI
Operating Voltage	VDDRX	External Supply	3.0	3.3	3.6	V	VDDRX
Operating Voltage	VDDP	External Supply	3.0	3.3	3.6	V	VDDP
Operating Voltage	VDD_PFM	External Supply	3.0	3.3	3.6	V	VDD_PFM
Operating Voltage	VDD_OTP	External Supply	8.0	8.25	8.5	V	VDD_OTP
Operating Voltage	VSP	External Supply	5.1	-	6.6	V	VSP
Operating Voltage	VSN	External Supply	-6.6	-	-5.1	V	VSN
Operating Voltage	V15D	Built-In Power Supply	-	1.5	-	V	V15D
Operating Voltage	V15D_RX	Built-In Power Supply	-	1.5	-	V	V15D_RX
Operating Voltage	VRSP	Built-In Power Supply	4.9	-	6.4	V	VRSP
Operating Voltage	VRSN	Built-In Power Supply	-6.4	-	-4.9	V	VRSN
Operating Voltage	VRNL	Built-In Power Supply	-	-2.5	-	V	VRNL
Operating Voltage	VGMPHO	Built-In Power Supply	4.7	-	6.2	V	VGMPHO
Operating Voltage	VGMPMO	Built-In Power Supply	2.2		3.7	V	VGMPMO
Operating Voltage	VGMPLO	Built-In Power Supply	0.1	-	1.6	V	VGMPLO
Operating Voltage	VGMNHO	Built-In Power Supply	-6.2	-	-4.7	V	VGMNHO
Operating Voltage	VGMNMO	Built-In Power Supply	-3.7		-2.2	V	VGMNMO
Operating Voltage	VGMNLO	Built-In Power Supply	-1.6	-	-0.1	V	VGMNLO
Operating Voltage	VGH	Built-In Power Supply	7.0		22.5	V	VGH
Operating Voltage	VGL	Built-In Power Supply	-15.0	-	-7.0	V	VGL
Operating Voltage	VCOM	Built-In Power Supply	-1.80	-	0.75	V	VCOM
Input High-level Voltage	V_{IH}		0.8 VDDI	-	VDDI	V	SPI Interface
Input Low-level Voltage	V_{IL}		VSS	-	0.2 VDDI	V	SPI Interface
Output High-level Voltage	V_{VOH}	VDDI=3.0V, IOL=1mA	0.8 VDDI	-	VDDI	V	SPI Interface
Output Low-level Voltage	V_{OL}	VDDI=3.0V, IOL=1mA	VSS	-	0.2 VDDI	V	SPI Interface
Input Leakage Current	I_{LI}	V_{IN}=VDDI or DGND	-1.0	-	1.0	μA	SPI Interface
Differential input high threshold voltage	R_{xVTH}	RxVCM = 1.2V (Note1)	-	-	0.1	V	LVDS Interface
Differential input low threshold voltage	R_{xVTL}		-0.1	-	-	V	LVDS Interface
Input voltage range (singled-end)	R_{xVIN}	(Note1)	0	-	VDD-1.0	V	LVDS Interface
Differential input common mode voltage	R_{xVCM}	(Note1)	0.6	1.2	2.4-$\|V_{ID}\|/2$	V	LVDS Interface
Differential input voltage	$\|V_{ID}\|$	$R_{xVT=}\|R_{xVTH}\|$ or $\|R_{xVTL}\|$	> R_{xVT}	0.4	0.6	V	LVDS Interface
Differential input leakage current	RV_{xliz}	(Note1)	-10	-	10	uA	LVDS Interface
Output Voltage Deviation	V_{OD1}	SO ≥ VSP-1.5V, SO ≤ VSSA+1.5V	-	±20	±40	mV	Source Pad
	V_{OD2}	VSSA+1.5V < SO < VSP-1.5V	-	±15	±20	mV	
	V_{OD3}	SO ≥ VSSA-1.5V, SO ≤ VSN+1.5V	-	±20	±40	mV	
	V_{OD4}	VSSA+1.5V < SO < VSP-1.5V, VSSA-1.5V > SO > VSN+1.5V	-	±15	±20	mV	
Pull low/high resistor	R_{PULL}	VDDI=3.3V	200	350	500	Kohm	Digital input pin

Note1:



The current consumed by whole IC (bare die) with external power system (5 power mode):

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Digital Operating Current	I_{VDD}	FCLK =90MHz, 1-Port LVDS, 1920x720 Data pattern= 256 Gray scale	-	25	-	mA
Digital Stand-by Current	I_{STBD}	RSTB=0 or STBYB=0, Clock & all functions are stopped.		0.5		
Analog Operating Current	I_{OPA_VSP} I_{OPA_VSN}	1920 channels without load, VSP= 6V, VSN= -6V VRSP= 5.8V, VRSN= -5.8V VGMPHO= 5.6V, VGMNHO= -5.6V FCLK =90MHz, 1-Port LVDS, 1920x720 Data pattern= 256 Gray scale	-	8 8	-	mA
Standby	I_{STBA_VSP} I_{STPA_VSN}	RSTB=0 or STBYB=0, Clock & all functions are stopped.	-	10 170	-	μA

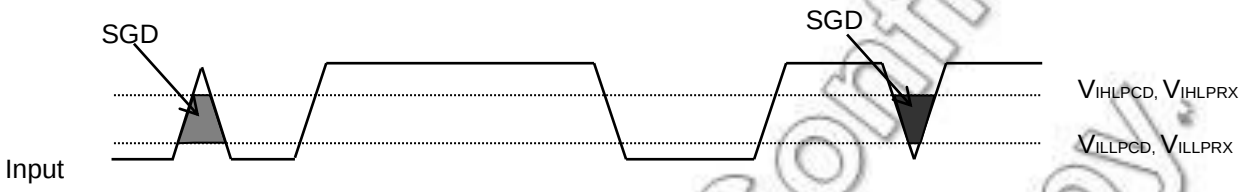
Note: The current is DC characteristic of a "Bare Chip".

9.2 MIPI DC Characteristics

LP Mode

VSSI = VSSRX = VSSP = 0V

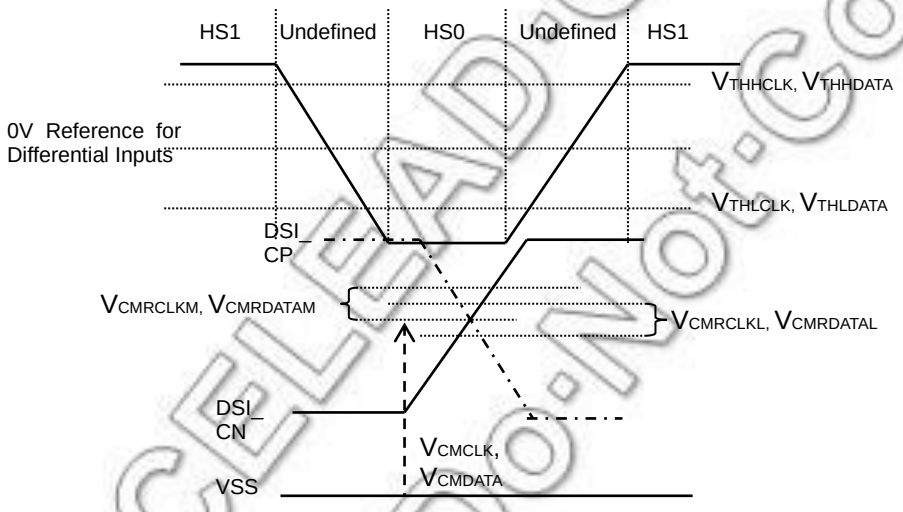
Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Logic High Level Input Voltage	V_{IHLPCD}	450	-	1350	mV	LP-CD
Logic Low Level Input Voltage	V_{ILLPCD}	0	-	200	mV	LP-CD
Logic High Level Input Voltage	V_{ILLPRX}	880	-	1350	mV	LP-RX(CLK, D0)
Logic Low Level Input Voltage	V_{ILLPRX}	0	-	550	mV	LP-RX(CLK, D0)
Logic Low Level Input Voltage	$V_{ILLPRXULP}$	0	-	300	mV	LP-RX(CLK ULP mode)
Logic High Level Input Voltage	V_{OHLPTX}	1.1	-	1.3	V	LP-TX(D0)
Logic Low Level Input Voltage	V_{OLLPTX}	-50	-	50	mV	LP-TX(D0)
Logic High Level Input Voltage	V_{IH}	-	-	10	uA	LP-CD, LP-RX
Logic Low Level Input Voltage	V_{IL}	-10	-	-	uA	LP-CD, LP-RX
Input Pulse rejection	SGD	-	-	300	Vps	DSI-CLK+/-, DSI-D0+/-



High Speed Mode

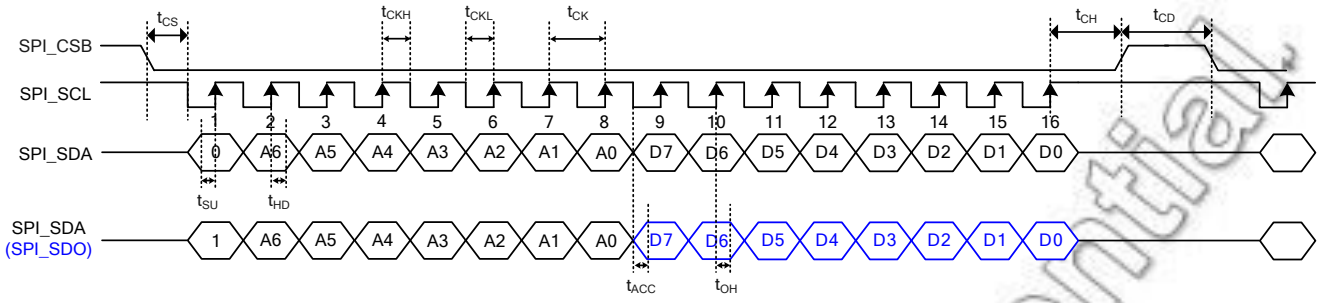
VSSI = VSSRX = VSSP = 0V

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Input Common Mode	V_{CMCLK} V_{CMDATA}	70	-	330	mV	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
Input Common Mode Variation<450MHz	$V_{CMRCLKL}$ $V_{CMRCLKL}$	-50	-	50	mV	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
Input Common Mode Variation>450MHz	$V_{CMRCLKM}$ $V_{CMRCLKM}$	-	-	100	mV	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
Low-Level Differential Input Threshold	V_{THLCLK} $V_{THLDATA}$	-70	-	-	mV	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
High-Level Differential Input Threshold	V_{THHCLK} $V_{THHDATAL}$	-	-	70	mV	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
Single Ended Input Low Voltage	V_{ILHS}	-40	-	-	mV	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
Single Ended Input High Voltage	V_{IHHS}	-	-	460	mV	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
Differential Input Termination Resistor	R_{TERM}	80-	100	125	Ω	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
Single-Ended Threshold Voltage for Termination Enable	V_{TERMEN}	-	-	450	mV	DSI_CP/DSI_CN DSI_DxP/DSI_DxN
Termination Capacitor	C_{TERM}	-	-	-	pF	DSI_CP/DSI_CN DSI_DxP/DSI_DxN



10. AC CHARACTERISTICS

10.1 SPI AC Timing

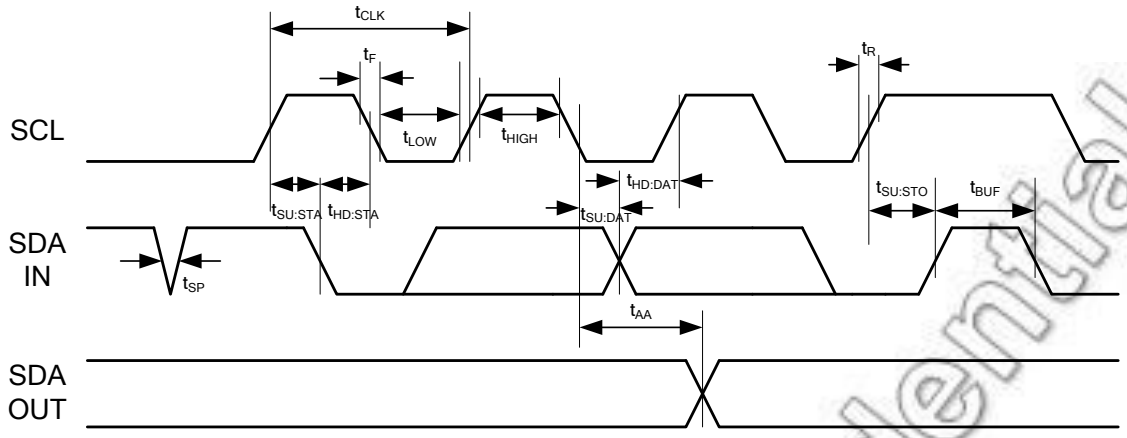


VSSI = VSSRX = VSSP = 0V, VDDI = VDDP= VDDRX = 3.0 ~ 3.6V

Parameter	Signal	Symbol	Min	Typ.	Max.	Unit	Condition
Serial clock period (Write)	SPI_SCL	t_{CK}	250	-	-	ns	
Serial clock period (Read)			250	-	-		
SCL “H” pulse width (Write)		t_{CKH}	125	-	-		
SCL “H” pulse width (Read)			125	-	-		
SCL “L” pulse width (Write)		t_{CKL}	125	-	-		
SCL “L” pulse width (Read)			125	-	-		
Write data input setup time	SPI_SDA	t_{SU}	100	-	-		
Write data input hold time		t_{HD}	100	-	-		
Read Data access time		t_{ACC}	-	-	100		
Read Data output disable time		t_{OH}	20	-	100		
SCL-SDO output delay time		t_{DLY}	-	-	50		
CSB-SCL time	SPI_CSB	t_{CS}	330	-	-		
CSB-SCL time		t_{CH}	250	-	-		
CSB “H” pulse width		t_{CD}	1000	-	-		

Note:
1. The input signal rise and fall time (tr, tf) are specified at 15ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

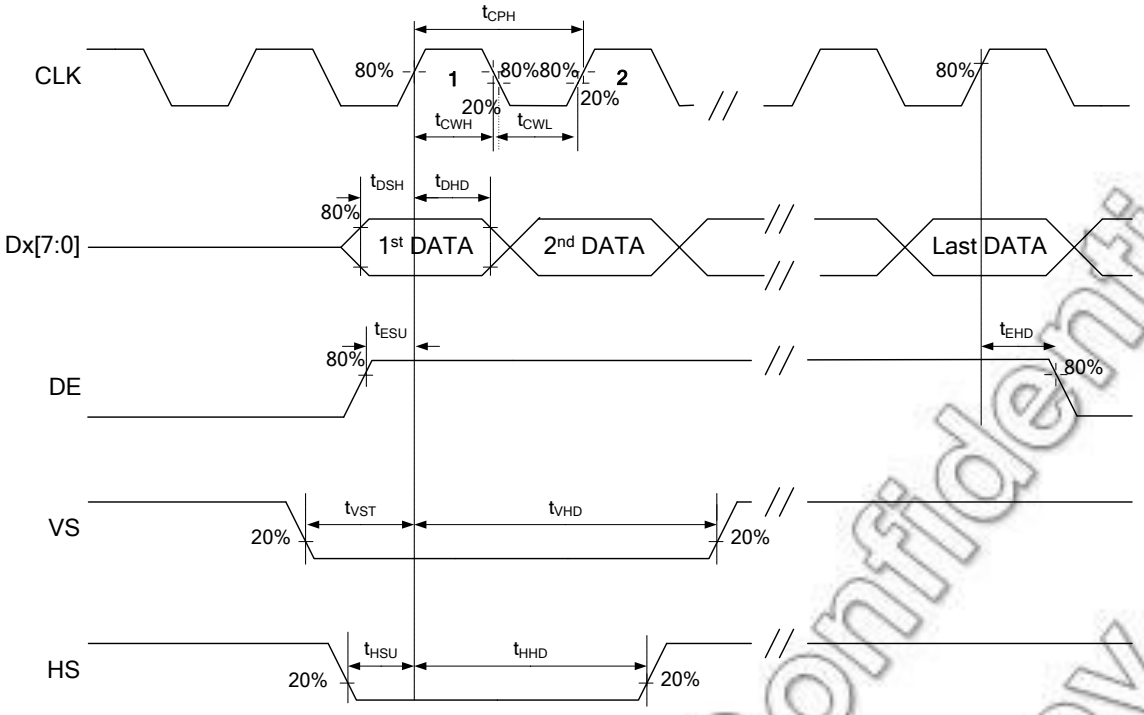
10.2 I2C AC Timing



VSSI = VSSRX = VSSP = 0V, VDDI = VDDP= VDDRX = 3.0 ~ 3.6V

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Clock frequency	SCL	f_{CLK}		2500		ns
Clock high time		t_{HIGH}		1250		
Clock low time		t_{LOW}		1250		
SDA and SCL rise time		t_R			300	
SDA and SCL fall time		t_F			300	
Start condition hold time	SDA IN	$t_{HD:STA}$		600		
Start condition setup time		$t_{SU:STA}$		600		
Data input hold time		$t_{HD:DAT}$		0		
Data input setup time		$t_{SU:DAT}$		100		
Stop condition setup time		$t_{SU:STO}$		600		
Output valid from clock		t_{AA}			900	
Input filter spike suppression (SDA and SCL pins)		t_{SP}			50	
Bus free-time: Time the bus must be free before a new transmission can start	SDA OUT	t_{BUF}		1300		

10.3 CMOS AC Timing



VSSI = VSSRX = VSSP = 0V, VDDI = VDDP= VDDRX = 3.0 ~ 3.6V

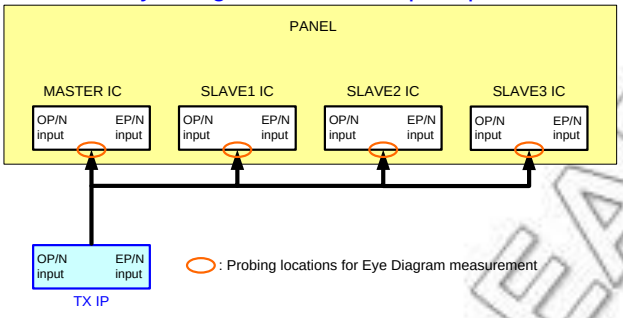
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
CLK cycle time	CLK	t_{CPH}		20	200	ns
CLK pulse high duty		t_{CWH}		40	60	%
CLK pulse low duty		t_{CWL}		40	60	
VS setup time	VS	t_{VST}		4	-	ns
VS hold time		t_{VHD}		2	-	
HS setup time	HS	t_{HST}		4	-	
HS hold time		t_{HHD}		2	-	
Data setup time	Dx[7:0]	t_{DSH}		4	-	
Date hold time		t_{DHD}		2	-	
DE setup time	DE	t_{ESU}		4	-	
DE hold time		t_{EHD}		2	-	

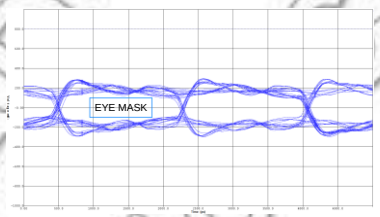
10.4 LVDS AC Timing

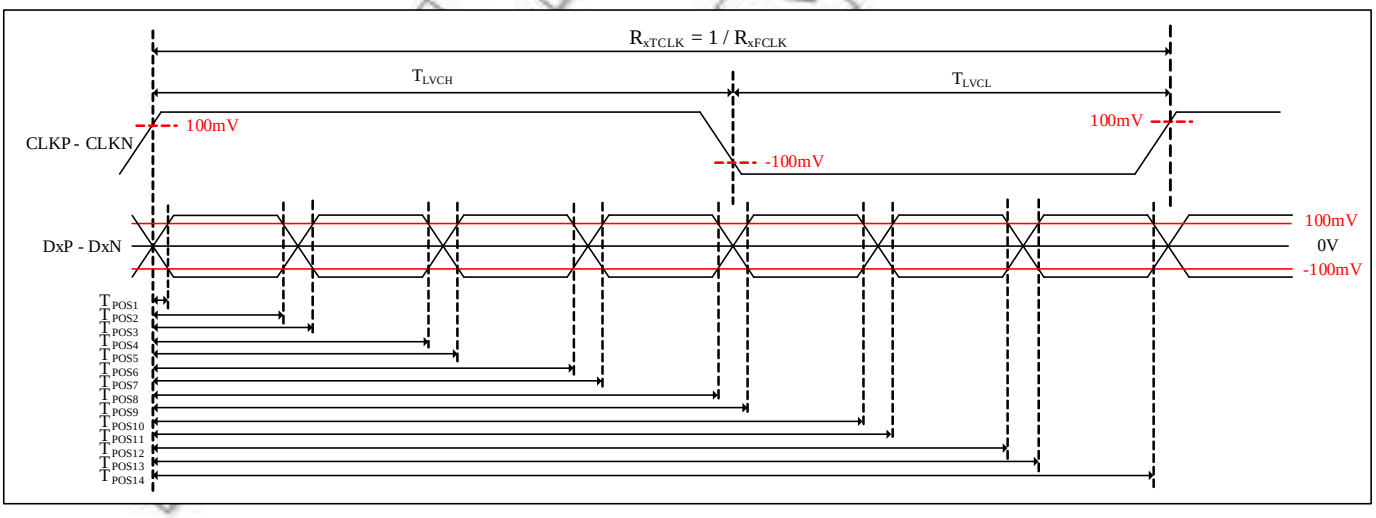
VSSI = VSSRX = VSSP = 0V, VDDI = VDDP= VDDRX = 3.0 ~ 3.6V

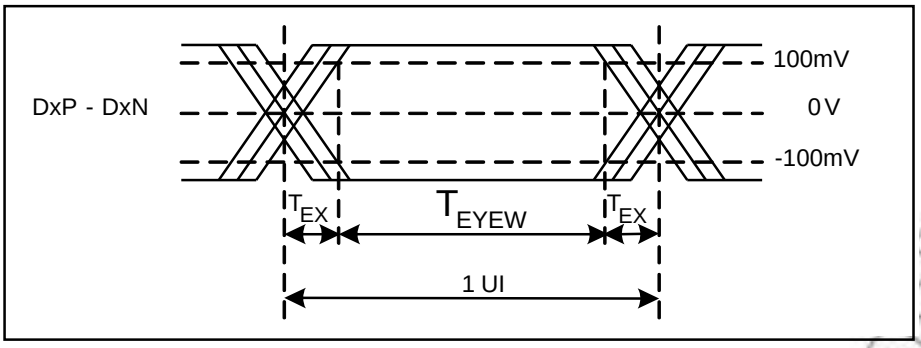
Item	Signal	Symbol	Rating			Unit
			Min.	Typ.	Max.	
Clock Frequency	CLK	R_{xFCLK}	20	-	100	MHz
Clock Period		R_{xTCLK}	10	-	50	ns
1 data bit time		UI	-	1/7	-	R_{xTCLK}
Clock high time	CLK	T_{LVCH}		4		UI
Clock low time		T_{LVCL}		3		UI
Position 1	DATA	T_{POS1}	-0.25	0	0.25	UI
Position 2		T_{POS2}	0.75	-	1.25	
Position 3		T_{POS3}	0.75	1	1.25	
Position 4		T_{POS4}	1.75	-	2.25	
Position 5		T_{POS5}	1.75	2	2.25	
Position 6		T_{POS6}	2.75	-	3.25	
Position 7		T_{POS7}	2.75	3	3.25	
Position 8		T_{POS8}	3.75	-	4.25	
Position 9		T_{POS9}	3.75	4	4.25	
Position 10		T_{POS10}	4.75	-	5.25	
Position 11		T_{POS11}	4.75	5	5.25	
Position 12		T_{POS12}	5.75	-	6.25	
Position 13		T_{POS13}	5.75	6	6.25	
Position 14		T_{POS14}	6.75	-	7.25	
Input eye width		T_{EYEW}	0.5	-	-	
Input eye border		T_{EX}	-	-	0.25	
PLL wake-up time		TenPLL	-	-	150	us

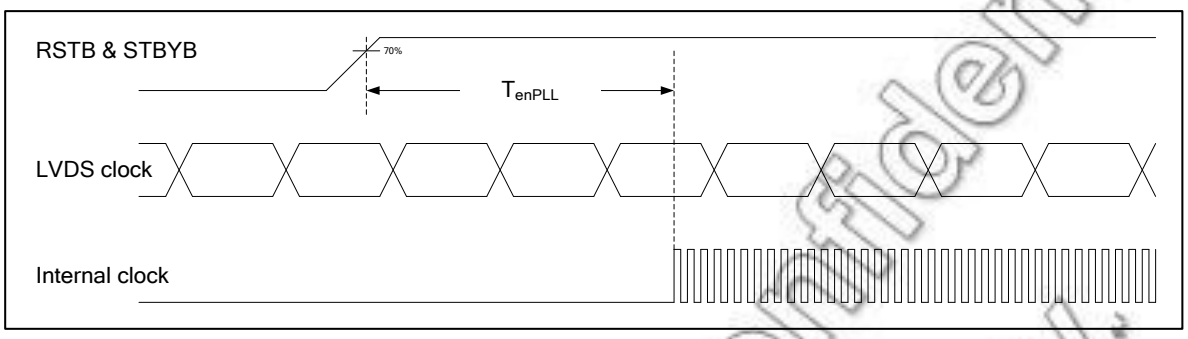
Note: The eye diagram of each chip on panel should satisfy the LVDS specification above.











10.4.1 Spread Spectrum Clocking (SSC) tolerance of LVDS receiver

VSSI = VSSRX = VSSP = 0V, VDDI = VDDP= VDDRX = 3.0 ~ 3.6V

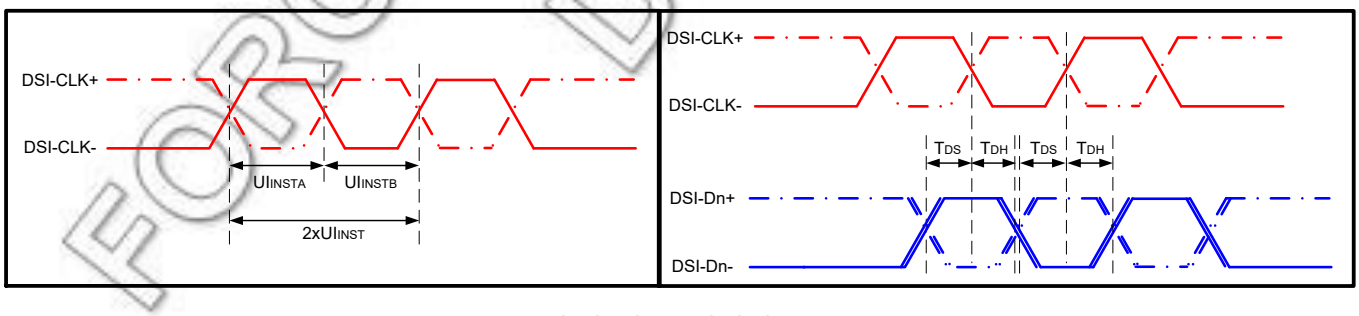
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Modulation frequency		SSC_{MF}		1	100	kHz
Modulation rate		SSC_{MR}	R_{xFCLK}=70MHz		+/-3	%
			R_{xFCLK}=50MHz		+/-4	%

10.5 MIPI AC Characteristics

VSSI = VSSRX = VSSP = 0V, VDDI = VDDP= VDDRX = 3.0 ~ 3.6V

Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Double UI Instantaneous	$2xUI_{INSTA}$	2.10	-	25	ns	DSI-CLK+/-
UI Instantaneous Half	UI_{INSTA} UI_{INSTB}	1.05	-	12.5	ns	DSI-CLK+/-
Data to Clock Setup Time	T_{DS}	0.15	-	-	UI	DSI-Dn+/-
Data to Clock Hold Time	T_{DH}	0.15	-	-	UI	DSI-Dn+/-

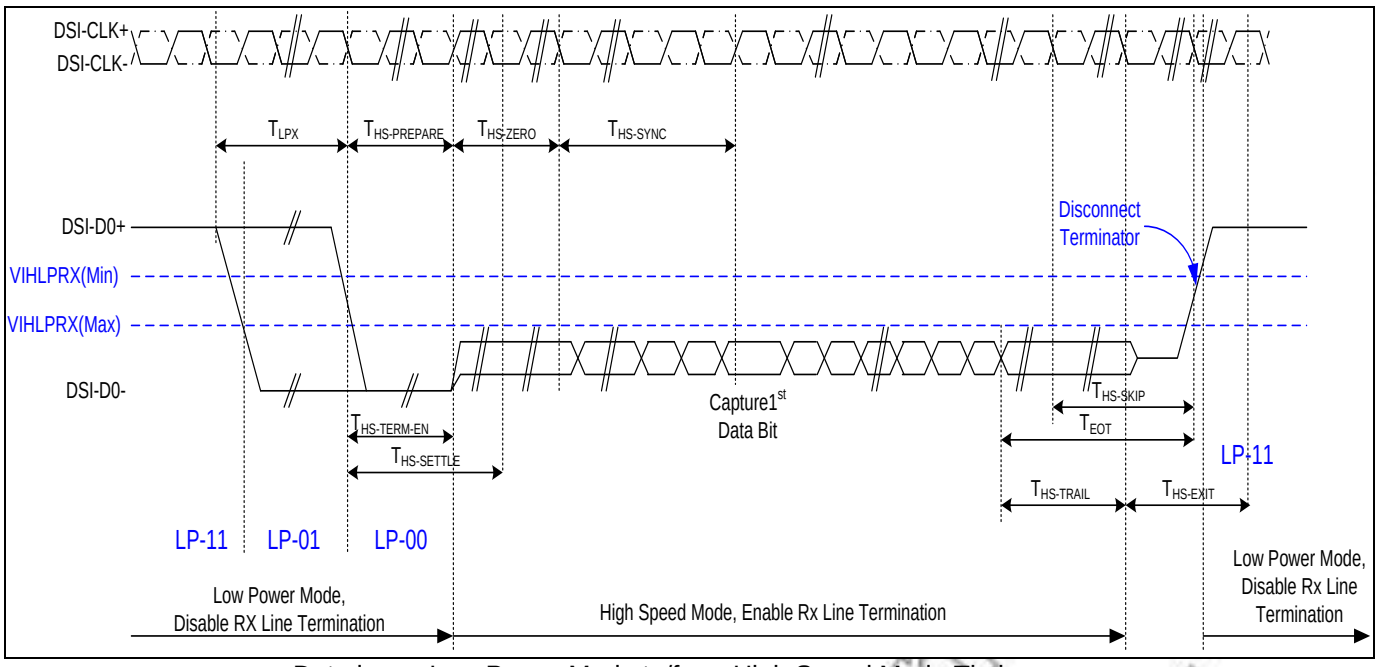
Note. This chip supports MIPI maximum frequency 950Mbps data rate.



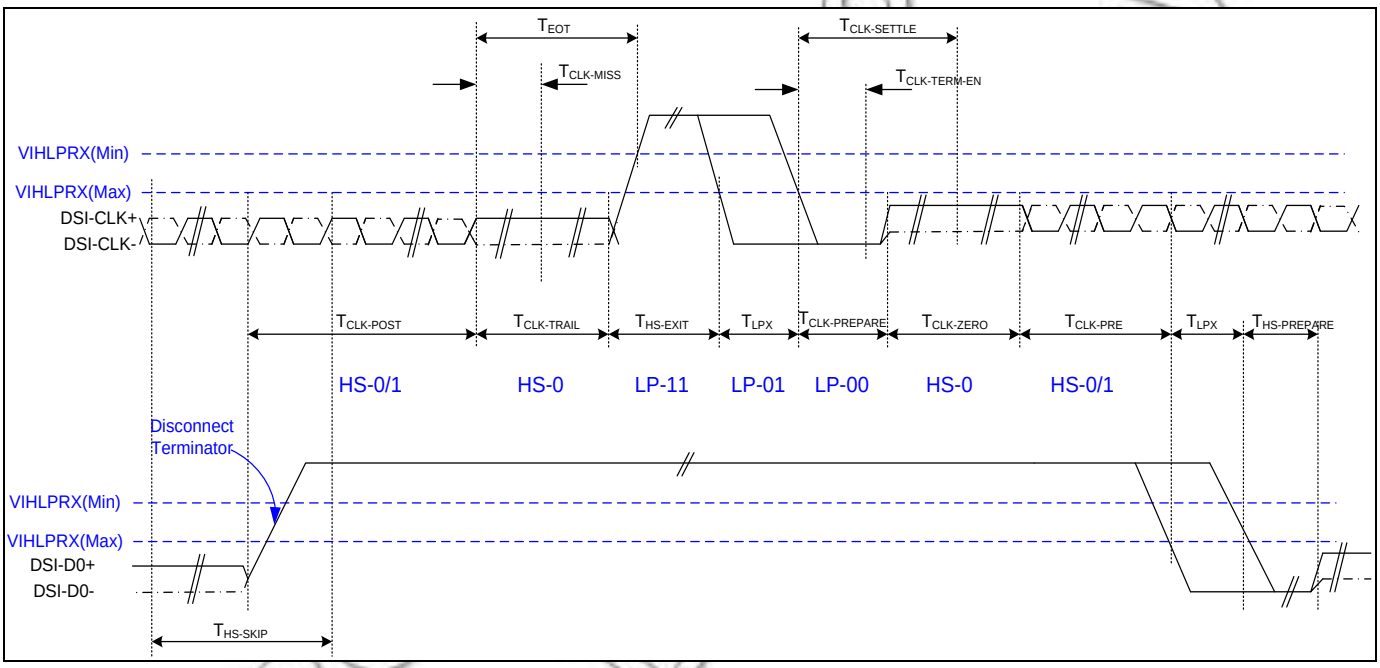
Clock Channel Timing

VSSI = VSSRX = VSSP = 0V, VDDI = VDDP= VDDRX = 3.0 ~ 3.6V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4UI	85+6UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105ns+12UI	ns	Input



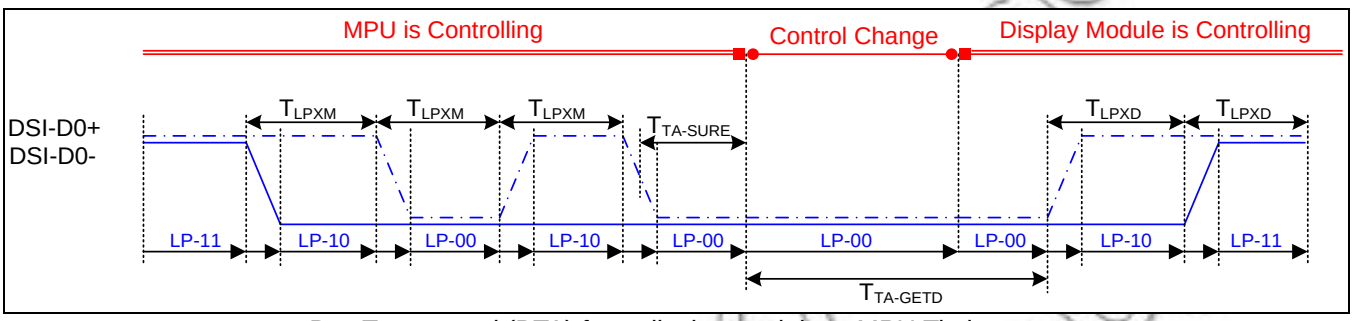
Data lanes-Low Power Mode to/from High Speed Mode Timing



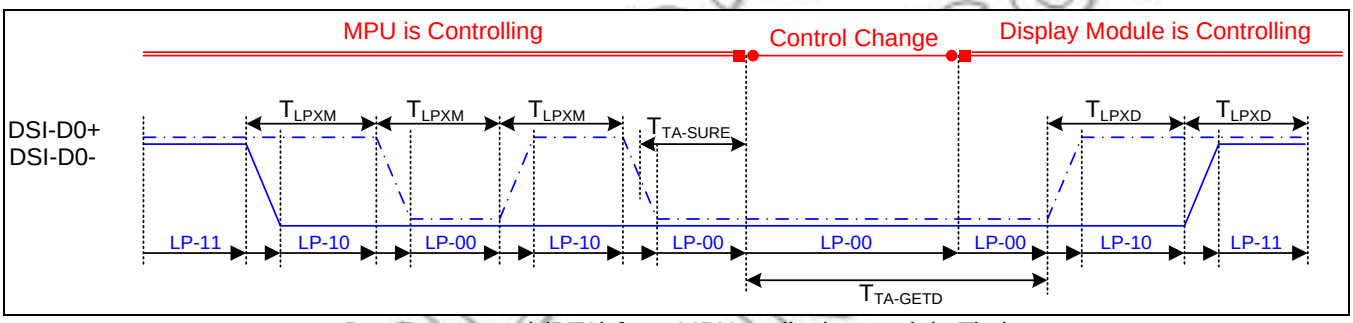
Clock lanes- High Speed Mode to/from Low Power Mode Timing

VSSI = VSSRX = VSSP = 0V, VDDI = VDDP= VDDRX = 3.0 ~ 3.6V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

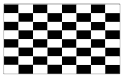
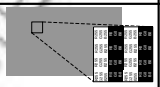


Bus Turnaround (BTA) from display module to MPU Timing



Bus Turnaround (BTA) from MPU to display module Timing

11. BIST PATTERN TABLE

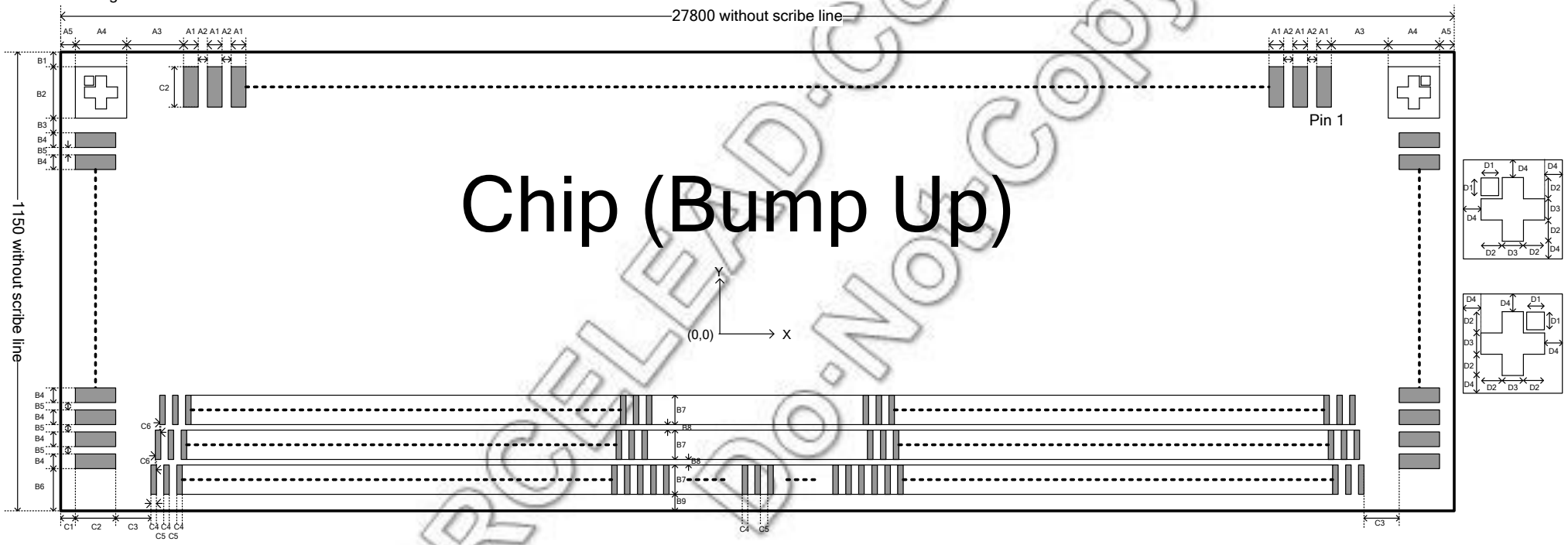
BIST_PAT[3:0]	Pattern	Pattern description	Notice
0000		**White**	Gray level of white pattern can be set by R_BIST_W[7:0]
0001		**Black**	
0010		**Red**	
0011		**Green**	
0100		**Blue**	
0101		**8 x8 chess board**	
0110		**Horizontal gray scale**	
0111		**Vertical gray scale**	
1000		**gray level 192**	
1001		**Crosstalk**	(Reg) R_BIST_XTALK_W for center black or white
1010		**Horizontal black and white lines**	
1011		**Vertical black and white lines**	
1100		**Flicker**	
1101	**(Reserved)**	**(Reserved)**	**(Reserved)**
1110	**0000 ~ 1100 loop**	**Auto Run**	Auto run pattern 0000 to 1100.
1111	**(Reserved)**	**(Reserved)**	**(Reserved)**

12. PIN ASSIGNMENT

12.1 COG Outline

Item	Dimension(um)	Item	Dimension(um)	Item	Dimension(um)	Item	Dimension(um)	Item	Dimension(um)	Item	Dimension(um)
*Chip length (x)	27830±30	A1	40±3	B1	13±2	B7	80±3	C1	20±5	D1	20±2
*Chip width (y)	1180±30	A2	15±3	B2	130±2	B8	15±3	C2	110±3	D2	25.5±2
Chip thickness	200±20	A3	97±5	B3	52±5	B9	20±5	C3	82.5±3	D3	29.5±2
Bump height	12±3	A4	130±3	B4	40±3			C4	15±3	D4	24.75±2
		A5	13±3	B5	20±3			C5	21±3		
				B6	75±5			C6	3±3		

*Note: including half width of the scribe line



12.2 Pad Center Coordinates

Pad	Name	X	Y
1	DUMMY	13640	500
2	VGL	13585	500
3	VGL	13530	500
4	VGL	13475	500
5	VGL	13420	500
6	Dummy	13365	500
7	VGH	13310	500
8	VGH	13255	500
9	VGH	13200	500
10	VSSA	13145	500
11	VSSA	13090	500
12	VSSI	13035	500
13	VSSI	12980	500
14	DUMMY	12925	500
15	VCOM_R	12870	500
16	VCOM_R	12815	500
17	VCOM_R	12760	500
18	VCOM_R	12705	500
19	THROUGH_1	12650	500
20	THROUGH_1	12595	500
21	VDD_OTP	12540	500
22	VDD_OTP	12485	500
23	VDD_OTP	12430	500
24	VDD_OTP	12375	500
25	VDD_OTP	12320	500
26	DUMMY	12265	500
27	DUMMY	12210	500
28	CLN2	12155	500
29	CLN2	12100	500
30	CLN2	12045	500
31	CLN2	11990	500
32	CLP2	11935	500
33	CLP2	11880	500
34	CLP2	11825	500
35	CLP2	11770	500
36	CLP1	11715	500
37	CLP1	11660	500

Pad	Name	X	Y
38	CLP1	11605	500
39	CLP1	11550	500
40	CLN1	11495	500
41	CLN1	11440	500
42	CLN1	11385	500
43	CLN1	11330	500
44	VREGN	11275	500
45	VREGN	11220	500
46	VREGN	11165	500
47	VREGN	11110	500
48	VGL	11055	500
49	VGL	11000	500
50	VGL	10945	500
51	VGL	10890	500
52	VGL	10835	500
53	VGL	10780	500
54	DUMMY	10725	500
55	VGH	10670	500
56	VGH	10615	500
57	VGH	10560	500
58	VGH	10505	500
59	VGH	10450	500
60	VGH	10395	500
61	CHP3	10340	500
62	CHP3	10285	500
63	CHP3	10230	500
64	CHP3	10175	500
65	CHN3	10120	500
66	CHN3	10065	500
67	CHN3	10010	500
68	CHN3	9955	500
69	CHP2	9900	500
70	CHP2	9845	500
71	CHP2	9790	500
72	CHP2	9735	500
73	CHN2	9680	500
74	CHN2	9625	500

Pad	Name	X	Y
75	CHN2	9570	500
76	CHN2	9515	500
77	CHP1	9460	500
78	CHP1	9405	500
79	CHP1	9350	500
80	CHP1	9295	500
81	CHN1	9240	500
82	CHN1	9185	500
83	CHN1	9130	500
84	CHN1	9075	500
85	VREGP	9020	500
86	VREGP	8965	500
87	VREGP	8910	500
88	VREGP	8855	500
89	VSS_PFM	8800	500
90	VSS_PFM	8745	500
91	VSS_PFM	8690	500
92	VSS_PFM	8635	500
93	VSS_PFM	8580	500
94	VSS_PFM	8525	500
95	VRNL	8470	500
96	VRNL	8415	500
97	VRNL	8360	500
98	VRNL	8305	500
99	VRNL	8250	500
100	VRNL	8195	500
101	VMONN	8140	500
102	VMONN	8085	500
103	VSN	8030	500
104	VSN	7975	500
105	VSN	7920	500
106	VSN	7865	500
107	VSN	7810	500
108	VSN	7755	500
109	VSN	7700	500
110	VSN	7645	500
111	DRVN	7590	500
112	DRVN	7535	500

Pad	Name	X	Y
113	DRVN	7480	500
114	DRVN	7425	500
115	VDD_PFM	7370	500
116	VDD_PFM	7315	500
117	VDD_PFM	7260	500
118	VDD_PFM	7205	500
119	VDD_PFM	7150	500
120	VDD_PFM	7095	500
121	VRSN	7040	500
122	VRSN	6985	500
123	VRSN	6930	500
124	VRSN	6875	500
125	VRSN	6820	500
126	VRSN	6765	500
127	VRSN	6710	500
128	VRSN	6655	500
129	VSSA	6600	500
130	VSSA	6545	500
131	VSSA	6490	500
132	VSSA	6435	500
133	VSSA	6380	500
134	VSSA	6325	500
135	VSSA	6270	500
136	VSSA	6215	500
137	VSSA	6160	500
138	VRSP	6105	500
139	VRSP	6050	500
140	VRSP	5995	500
141	VRSP	5940	500
142	VRSP	5885	500
143	VRSP	5830	500
144	VRSP	5775	500
145	VRSP	5720	500
146	DRVP	5665	500
147	DRVP	5610	500
148	DRVP	5555	500
149	DRVP	5500	500
150	VSP	5445	500

Pad	Name	X	Y
151	VSP	5390	500
152	VSP	5335	500
153	VSP	5280	500
154	VSP	5225	500
155	VSP	5170	500
156	VSP	5115	500
157	VSP	5060	500
158	VMONP	5005	500
159	VMONP	4950	500
160	DUMMY	4895	500
161	SPI_SDAO	4840	500
162	SPI_SDAO	4785	500
163	SPI_SDAI	4730	500
164	SPI_SCL	4675	500
165	SPI_CSB	4620	500
166	I2C_SDA	4565	500
167	I2C_SDA	4510	500
168	I2C_SDA	4455	500
169	I2C_SCL	4400	500
170	I2C_SPI_SEL	4345	500
171	DUMMY	4290	500
172	VESA	4235	500
173	ECS	4180	500
174	ECS	4125	500
175	ECS	4070	500
176	ESCL	4015	500
177	ESCL	3960	500
178	ESCL	3905	500
179	ESDAO	3850	500
180	ESDAO	3795	500
181	ESDAI	3740	500
182	VDDI	3685	500
183	VDDI	3630	500
184	VDDI	3575	500
185	VDDI	3520	500
186	VDDI	3465	500
187	VDDI	3410	500
188	VDDRX	3355	500

Pad	Name	X	Y
189	VDDRX	3300	500
190	VDDRX	3245	500
191	VDDRX	3190	500
192	V15D	3135	500
193	V15D	3080	500
194	V15D	3025	500
195	V15D	2970	500
196	V15D	2915	500
197	V15D	2860	500
198	V15D_RX	2805	500
199	V15D_RX	2750	500
200	V15D_RX	2695	500
201	V15D_RX	2640	500
202	VSSI	2585	500
203	VSSI	2530	500
204	VSSI	2475	500
205	VSSI	2420	500
206	VSSI	2365	500
207	VSSI	2310	500
208	VSSRX	2255	500
209	VSSRX	2200	500
210	VSSRX	2145	500
211	VSSRX	2090	500
212	D2[0]	2035	500
213	D2[0]	1980	500
214	D2[1]	1925	500
215	D2[1]	1870	500
216	VSSRX	1815	500
217	D2[2]	1760	500
218	D2[2]	1705	500
219	D2[3]	1650	500
220	D2[3]	1595	500
221	VSSRX	1540	500
222	D2[4]	1485	500
223	D2[4]	1430	500
224	D2[5]	1375	500
225	D2[5]	1320	500
226	VSSRX	1265	500

Pad	Name	X	Y
227	D2[6]	1210	500
228	D2[6]	1155	500
229	D2[7]	1100	500
230	D2[7]	1045	500
231	VSSRX	990	500
232	D1[0]	935	500
233	D1[0]	880	500
234	D1[1]	825	500
235	D1[1]	770	500
236	VSSRX	715	500
237	D1[2]	660	500
238	D1[2]	605	500
239	D1[3]	550	500
240	D1[3]	495	500
241	VSSRX	440	500
242	D1[4]	385	500
243	D1[4]	330	500
244	D1[5]	275	500
245	D1[5]	220	500
246	VSSRX	165	500
247	D1[6]	110	500
248	D1[6]	55	500
249	D1[7]	0	500
250	D1[7]	-55	500
251	VSSRX	-110	500
252	D0[0]	-165	500
253	D0[0]	-220	500
254	D0[1]	-275	500
255	D0[1]	-330	500
256	VSSRX	-385	500
257	D0[2]	-440	500
258	D0[2]	-495	500
259	D0[3]	-550	500
260	D0[3]	-605	500
261	VSSRX	-660	500
262	D0[4]	-715	500
263	D0[4]	-770	500
264	D0[5]	-825	500

Pad	Name	X	Y
265	D0[5]	-880	500
266	VSSRX	-935	500
267	D0[6]	-990	500
268	D0[6]	-1045	500
269	D0[7]	-1100	500
270	D0[7]	-1155	500
271	VSSRX	-1210	500
272	DCLK	-1265	500
273	DCLK	-1320	500
274	HS	-1375	500
275	HS	-1430	500
276	VS	-1485	500
277	VS	-1540	500
278	DE	-1595	500
279	DE	-1650	500
280	VSSRX	-1705	500
281	VSSRX	-1760	500
282	VSSRX	-1815	500
283	VSSRX	-1870	500
284	VSSRX	-1925	500
285	VSSRX	-1980	500
286	VSSI	-2035	500
287	VSSI	-2090	500
288	VSSI	-2145	500
289	VSSI	-2200	500
290	VSSI	-2255	500
291	VSSI	-2310	500
292	V15D	-2365	500
293	V15D	-2420	500
294	V15D	-2475	500
295	V15D	-2530	500
296	V15D	-2585	500
297	V15D	-2640	500
298	VGMPHI	-2695	500
299	VGMPHI	-2750	500
300	VGMPHI	-2805	500
301	VGMPHI	-2860	500
302	VGMPMI	-2915	500

Pad	Name	X	Y
303	VGMPMI	-2970	500
304	VGMPMI	-3025	500
305	VGMPMI	-3080	500
306	VGMPLI	-3135	500
307	VGMPLI	-3190	500
308	VGMPLI	-3245	500
309	VGMPLI	-3300	500
310	VGMNHI	-3355	500
311	VGMNHI	-3410	500
312	VGMNHI	-3465	500
313	VGMNHI	-3520	500
314	VGMNMI	-3575	500
315	VGMNMI	-3630	500
316	VGMNMI	-3685	500
317	VGMNMI	-3740	500
318	VGMNLI	-3795	500
319	VGMNLI	-3850	500
320	VGMNLI	-3905	500
321	VGMNLI	-3960	500
322	DUMMY	-4015	500
323	DUMMY	-4070	500
324	VGMPHO	-4125	500
325	VGMPHO	-4180	500
326	VGMPHO	-4235	500
327	VGMPHO	-4290	500
328	VGMPMO	-4345	500
329	VGMPMO	-4400	500
330	VGMPMO	-4455	500
331	VGMPMO	-4510	500
332	VGMPLO	-4565	500
333	VGMPLO	-4620	500
334	VGMPLO	-4675	500
335	VGMPLO	-4730	500
336	VGMNHO	-4785	500
337	VGMNHO	-4840	500
338	VGMNHO	-4895	500
339	VGMNHO	-4950	500
340	VGMNMO	-5005	500

Pad	Name	X	Y
341	VGMNMO	-5060	500
342	VGMNMO	-5115	500
343	VGMNMO	-5170	500
344	VGMNLO	-5225	500
345	VGMNLO	-5280	500
346	VGMNLO	-5335	500
347	VGMNLO	-5390	500
348	DUMMY	-5445	500
349	DUMMY	-5500	500
350	DUMMY	-5555	500
351	DUMMY	-5610	500
352	DUMMY	-5665	500
353	DUMMY	-5720	500
354	TEST_IN[0]	-5775	500
355	CPUS[0]	-5830	500
356	CPUS[1]	-5885	500
357	TEST_O[0]	-5940	500
358	TEST_O[0]	-5995	500
359	TEST_O[1]	-6050	500
360	TEST_O[1]	-6105	500
361	TEST_O[2]	-6160	500
362	TEST_O[2]	-6215	500
363	TEST_O[3]	-6270	500
364	TEST_O[3]	-6325	500
365	DUMMY	-6380	500
366	TEST_I_MIPI	-6435	500
367	TEST_O[4]	-6490	500
368	TEST_O[4]	-6545	500
369	TEST_O[5]	-6600	500
370	TEST_O[5]	-6655	500
371	ERR2	-6710	500
372	ERR2	-6765	500
373	TP_SYNC	-6820	500
374	TP_SYNC	-6875	500
375	ERR	-6930	500
376	ERR	-6985	500
377	DUMMY	-7040	500
378	DUMMY	-7095	500

Pad	Name	X	Y
379	VRSP	-7150	500
380	VRSP	-7205	500
381	VRSP	-7260	500
382	VRSP	-7315	500
383	VRSP	-7370	500
384	VRSP	-7425	500
385	VRSP	-7480	500
386	VRSP	-7535	500
387	VSSA	-7590	500
388	VSSA	-7645	500
389	VSSA	-7700	500
390	VSSA	-7755	500
391	VSSA	-7810	500
392	VSSA	-7865	500
393	VSSA	-7920	500
394	VSSA	-7975	500
395	VSSA	-8030	500
396	VRSN	-8085	500
397	VRSN	-8140	500
398	VRSN	-8195	500
399	VRSN	-8250	500
400	VRSN	-8305	500
401	VRSN	-8360	500
402	VRSN	-8415	500
403	VRSN	-8470	500
404	DUMMY	-8525	500
405	TEST_I[1]	-8580	500
406	TEST_I[0]	-8635	500
407	TEST_V[2]	-8690	500
408	TEST_V[1]	-8745	500
409	TEST_V[0]	-8800	500
410	VDDI	-8855	500
411	VDDI	-8910	500
412	VDDI	-8965	500
413	VDDI	-9020	500
414	VDDI	-9075	500
415	VDDI	-9130	500
416	VDDI	-9185	500

Pad	Name	X	Y
417	VDDP	-9240	500
418	VDDP	-9295	500
419	VDDP	-9350	500
420	VDDP	-9405	500
421	VDDP	-9460	500
422	VSSI	-9515	500
423	VSSI	-9570	500
424	VSSI	-9625	500
425	VSSI	-9680	500
426	VSSI	-9735	500
427	VSSI	-9790	500
428	VSSI	-9845	500
429	VSSP	-9900	500
430	VSSP	-9955	500
431	VSSP	-10010	500
432	VSSP	-10065	500
433	VSSP	-10120	500
434	STBYB	-10175	500
435	RSTB	-10230	500
436	UD	-10285	500
437	RL	-10340	500
438	NB	-10395	500
439	MODE	-10450	500
440	BIT8	-10505	500
441	IFSEL[0]	-10560	500
442	IFSEL[1]	-10615	500
443	DUMMY	-10670	500
444	DUMMY	-10725	500
445	EXT_PWR2	-10780	500
446	ROM_RLD	-10835	500
447	GDMAP	-10890	500
448	WRBYCID	-10945	500
449	CID[0]	-11000	500
450	CID[1]	-11055	500
451	HW_CTRL	-11110	500
452	GDSEL	-11165	500
453	DUMMY	-11220	500
454	DUMMY	-11275	500

Pad	Name	X	Y
455	DUMMY	-11330	500
456	BIST	-11385	500
457	GDPOS[0]	-11440	500
458	GDPOS[1]	-11495	500
459	RES[0]	-11550	500
460	RES[1]	-11605	500
461	RES[2]	-11660	500
462	RES[3]	-11715	500
463	INV[0]	-11770	500
464	INV[1]	-11825	500
465	EXT_PWR	-11880	500
466	DUMMY	-11935	500
467	DUMMY	-11990	500
468	VCOM	-12045	500
469	VCOM	-12100	500
470	VCOM	-12155	500
471	VCOM	-12210	500
472	THROUGH_2	-12265	500
473	THROUGH_2	-12320	500
474	VCOM_L	-12375	500
475	VCOM_L	-12430	500
476	VCOM_L	-12485	500
477	VCOM_L	-12540	500
478	DUMMY	-12595	500
479	DUMMY	-12650	500
480	DUMMY	-12705	500
481	DUMMY	-12760	500
482	VSSI	-12815	500
483	VSSI	-12870	500
484	VSSA	-12925	500
485	VSSA	-12980	500
486	VGH	-13035	500
487	VGH	-13090	500
488	VGH	-13145	500
489	Dummy	-13200	500
490	VGL	-13255	500
491	VGL	-13310	500
492	VGL	-13365	500

Pad	Name	X	Y
493	VGL	-13420	500
494	DUMMY	-13475	500
495	DUMMY	-13530	500
496	DUMMY	-13585	500
497	DUMMY	-13640	500
498	GPO_L[1]	-13825	360
499	GPO_L[2]	-13825	300
500	GPO_L[3]	-13825	240
501	GPO_L[4]	-13825	180
502	GPO_L[5]	-13825	120
503	GPO_L[6]	-13825	60
504	GPO_L[7]	-13825	0
505	GPO_L[8]	-13825	-60
506	GPO_L[9]	-13825	-120
507	GPO_L[10]	-13825	-180
508	GPO_L[11]	-13825	-240
509	GPO_L[12]	-13825	-300
510	GPO_L[13]	-13825	-360
511	TEST_VL	-13825	-420
512	Dummy	-13825	-480
513	DUMMY	-13680	-515
514	DUMMY	-13668	-420
515	DUMMY	-13656	-325
516	GHV_L[1]	-13644	-515
517	GHV_L[1]	-13632	-420
518	GHV_L[1]	-13620	-325
519	GHV_L[2]	-13608	-515
520	GHV_L[2]	-13596	-420
521	GHV_L[2]	-13584	-325
522	GHV_L[3]	-13572	-515
523	GHV_L[3]	-13560	-420
524	GHV_L[3]	-13548	-325
525	GHV_L[4]	-13536	-515
526	GHV_L[4]	-13524	-420
527	GHV_L[4]	-13512	-325
528	GHV_L[5]	-13500	-515
529	GHV_L[5]	-13488	-420
530	GHV_L[5]	-13476	-325

Pad	Name	X	Y
531	GHV_L[6]	-13464	-515
532	GHV_L[6]	-13452	-420
533	GHV_L[6]	-13440	-325
534	GHV_L[7]	-13428	-515
535	GHV_L[7]	-13416	-420
536	GHV_L[7]	-13404	-325
537	GHV_L[8]	-13392	-515
538	GHV_L[8]	-13380	-420
539	GHV_L[8]	-13368	-325
540	VGL	-13356	-515
541	VGL	-13344	-420
542	VGL	-13332	-325
543	VGL	-13320	-515
544	VGL	-13308	-420
545	VGL	-13296	-325
546	GHV_L[9]	-13284	-515
547	GHV_L[9]	-13272	-420
548	GHV_L[9]	-13260	-325
549	GHV_L[10]	-13248	-515
550	GHV_L[10]	-13236	-420
551	GHV_L[10]	-13224	-325
552	GHV_L[11]	-13212	-515
553	GHV_L[11]	-13200	-420
554	GHV_L[11]	-13188	-325
555	GHV_L[12]	-13176	-515
556	GHV_L[12]	-13164	-420
557	GHV_L[12]	-13152	-325
558	GHV_L[13]	-13140	-515
559	GHV_L[13]	-13128	-420
560	GHV_L[13]	-13116	-325
561	GHV_L[14]	-13104	-515
562	GHV_L[14]	-13092	-420
563	GHV_L[14]	-13080	-325
564	GHV_L[15]	-13068	-515
565	GHV_L[15]	-13056	-420
566	GHV_L[15]	-13044	-325
567	GHV_L[16]	-13032	-515
568	GHV_L[16]	-13020	-420

Pad	Name	X	Y
569	GHV_L[16]	-13008	-325
570	GHV_L[17]	-12996	-515
571	GHV_L[17]	-12984	-420
572	GHV_L[17]	-12972	-325
573	GHV_L[18]	-12960	-515
574	GHV_L[18]	-12948	-420
575	GHV_L[18]	-12936	-325
576	GHV_L[19]	-12924	-515
577	GHV_L[19]	-12912	-420
578	GHV_L[19]	-12900	-325
579	GHV_L[20]	-12888	-515
580	GHV_L[20]	-12876	-420
581	GHV_L[20]	-12864	-325
582	VGH	-12852	-515
583	VGH	-12840	-420
584	VGH	-12828	-325
585	VGH	-12816	-515
586	VGH	-12804	-420
587	VGH	-12792	-325
588	VSSA	-12780	-515
589	VSSA	-12768	-420
590	VSSA	-12756	-325
591	VSSA	-12744	-515
592	VSSA	-12732	-420
593	VSSA	-12720	-325
594	VCOM_L	-12708	-515
595	VCOM_L	-12696	-420
596	VCOM_L	-12684	-325
597	VCOM_L	-12672	-515
598	VCOM_L	-12660	-420
599	VCOM_L	-12648	-325
600	VSSA	-12636	-515
601	VSSA	-12624	-420
602	VSSA	-12612	-325
603	VSSA	-12600	-515
604	VSSA	-12588	-420
605	VSSA	-12576	-325
606	S[1]	-12564	-515

Pad	Name	X	Y
607	S[2]	-12552	-420
608	S[3]	-12540	-325
609	S[4]	-12528	-515
610	S[5]	-12516	-420
611	S[6]	-12504	-325
612	S[7]	-12492	-515
613	S[8]	-12480	-420
614	S[9]	-12468	-325
615	S[10]	-12456	-515
616	S[11]	-12444	-420
617	S[12]	-12432	-325
618	S[13]	-12420	-515
619	S[14]	-12408	-420
620	S[15]	-12396	-325
621	S[16]	-12384	-515
622	S[17]	-12372	-420
623	S[18]	-12360	-325
624	S[19]	-12348	-515
625	S[20]	-12336	-420
626	S[21]	-12324	-325
627	S[22]	-12312	-515
628	S[23]	-12300	-420
629	S[24]	-12288	-325
630	S[25]	-12276	-515
631	S[26]	-12264	-420
632	S[27]	-12252	-325
633	S[28]	-12240	-515
634	S[29]	-12228	-420
635	S[30]	-12216	-325
636	S[31]	-12204	-515
637	S[32]	-12192	-420
638	S[33]	-12180	-325
639	S[34]	-12168	-515
640	S[35]	-12156	-420
641	S[36]	-12144	-325
642	S[37]	-12132	-515
643	S[38]	-12120	-420
644	S[39]	-12108	-325

Pad	Name	X	Y
645	S[40]	-12096	-515
646	S[41]	-12084	-420
647	S[42]	-12072	-325
648	S[43]	-12060	-515
649	S[44]	-12048	-420
650	S[45]	-12036	-325
651	S[46]	-12024	-515
652	S[47]	-12012	-420
653	S[48]	-12000	-325
654	S[49]	-11988	-515
655	S[50]	-11976	-420
656	S[51]	-11964	-325
657	S[52]	-11952	-515
658	S[53]	-11940	-420
659	S[54]	-11928	-325
660	S[55]	-11916	-515
661	S[56]	-11904	-420
662	S[57]	-11892	-325
663	S[58]	-11880	-515
664	S[59]	-11868	-420
665	S[60]	-11856	-325
666	S[61]	-11844	-515
667	S[62]	-11832	-420
668	S[63]	-11820	-325
669	S[64]	-11808	-515
670	S[65]	-11796	-420
671	S[66]	-11784	-325
672	S[67]	-11772	-515
673	S[68]	-11760	-420
674	S[69]	-11748	-325
675	S[70]	-11736	-515
676	S[71]	-11724	-420
677	S[72]	-11712	-325
678	S[73]	-11700	-515
679	S[74]	-11688	-420
680	S[75]	-11676	-325
681	S[76]	-11664	-515
682	S[77]	-11652	-420

Pad	Name	X	Y
683	S[78]	-11640	-325
684	S[79]	-11628	-515
685	S[80]	-11616	-420
686	S[81]	-11604	-325
687	S[82]	-11592	-515
688	S[83]	-11580	-420
689	S[84]	-11568	-325
690	S[85]	-11556	-515
691	S[86]	-11544	-420
692	S[87]	-11532	-325
693	S[88]	-11520	-515
694	S[89]	-11508	-420
695	S[90]	-11496	-325
696	S[91]	-11484	-515
697	S[92]	-11472	-420
698	S[93]	-11460	-325
699	S[94]	-11448	-515
700	S[95]	-11436	-420
701	S[96]	-11424	-325
702	S[97]	-11412	-515
703	S[98]	-11400	-420
704	S[99]	-11388	-325
705	S[100]	-11376	-515
706	S[101]	-11364	-420
707	S[102]	-11352	-325
708	S[103]	-11340	-515
709	S[104]	-11328	-420
710	S[105]	-11316	-325
711	S[106]	-11304	-515
712	S[107]	-11292	-420
713	S[108]	-11280	-325
714	S[109]	-11268	-515
715	S[110]	-11256	-420
716	S[111]	-11244	-325
717	S[112]	-11232	-515
718	S[113]	-11220	-420
719	S[114]	-11208	-325
720	S[115]	-11196	-515

Pad	Name	X	Y
721	S[116]	-11184	-420
722	S[117]	-11172	-325
723	S[118]	-11160	-515
724	S[119]	-11148	-420
725	S[120]	-11136	-325
726	S[121]	-11124	-515
727	S[122]	-11112	-420
728	S[123]	-11100	-325
729	S[124]	-11088	-515
730	S[125]	-11076	-420
731	S[126]	-11064	-325
732	S[127]	-11052	-515
733	S[128]	-11040	-420
734	S[129]	-11028	-325
735	S[130]	-11016	-515
736	S[131]	-11004	-420
737	S[132]	-10992	-325
738	S[133]	-10980	-515
739	S[134]	-10968	-420
740	S[135]	-10956	-325
741	S[136]	-10944	-515
742	S[137]	-10932	-420
743	S[138]	-10920	-325
744	S[139]	-10908	-515
745	S[140]	-10896	-420
746	S[141]	-10884	-325
747	S[142]	-10872	-515
748	S[143]	-10860	-420
749	S[144]	-10848	-325
750	S[145]	-10836	-515
751	S[146]	-10824	-420
752	S[147]	-10812	-325
753	S[148]	-10800	-515
754	S[149]	-10788	-420
755	S[150]	-10776	-325
756	S[151]	-10764	-515
757	S[152]	-10752	-420
758	S[153]	-10740	-325

Pad	Name	X	Y
759	S[154]	-10728	-515
760	S[155]	-10716	-420
761	S[156]	-10704	-325
762	S[157]	-10692	-515
763	S[158]	-10680	-420
764	S[159]	-10668	-325
765	S[160]	-10656	-515
766	S[161]	-10644	-420
767	S[162]	-10632	-325
768	S[163]	-10620	-515
769	S[164]	-10608	-420
770	S[165]	-10596	-325
771	S[166]	-10584	-515
772	S[167]	-10572	-420
773	S[168]	-10560	-325
774	S[169]	-10548	-515
775	S[170]	-10536	-420
776	S[171]	-10524	-325
777	S[172]	-10512	-515
778	S[173]	-10500	-420
779	S[174]	-10488	-325
780	S[175]	-10476	-515
781	S[176]	-10464	-420
782	S[177]	-10452	-325
783	S[178]	-10440	-515
784	S[179]	-10428	-420
785	S[180]	-10416	-325
786	S[181]	-10404	-515
787	S[182]	-10392	-420
788	S[183]	-10380	-325
789	S[184]	-10368	-515
790	S[185]	-10356	-420
791	S[186]	-10344	-325
792	S[187]	-10332	-515
793	S[188]	-10320	-420
794	S[189]	-10308	-325
795	S[190]	-10296	-515
796	S[191]	-10284	-420

Pad	Name	X	Y
797	S[192]	-10272	-325
798	S[193]	-10260	-515
799	S[194]	-10248	-420
800	S[195]	-10236	-325
801	S[196]	-10224	-515
802	S[197]	-10212	-420
803	S[198]	-10200	-325
804	S[199]	-10188	-515
805	S[200]	-10176	-420
806	S[201]	-10164	-325
807	S[202]	-10152	-515
808	S[203]	-10140	-420
809	S[204]	-10128	-325
810	S[205]	-10116	-515
811	S[206]	-10104	-420
812	S[207]	-10092	-325
813	S[208]	-10080	-515
814	S[209]	-10068	-420
815	S[210]	-10056	-325
816	S[211]	-10044	-515
817	S[212]	-10032	-420
818	S[213]	-10020	-325
819	S[214]	-10008	-515
820	S[215]	-9996	-420
821	S[216]	-9984	-325
822	S[217]	-9972	-515
823	S[218]	-9960	-420
824	S[219]	-9948	-325
825	S[220]	-9936	-515
826	S[221]	-9924	-420
827	S[222]	-9912	-325
828	S[223]	-9900	-515
829	S[224]	-9888	-420
830	S[225]	-9876	-325
831	S[226]	-9864	-515
832	S[227]	-9852	-420
833	S[228]	-9840	-325
834	S[229]	-9828	-515

Pad	Name	X	Y
835	S[230]	-9816	-420
836	S[231]	-9804	-325
837	S[232]	-9792	-515
838	S[233]	-9780	-420
839	S[234]	-9768	-325
840	S[235]	-9756	-515
841	S[236]	-9744	-420
842	S[237]	-9732	-325
843	S[238]	-9720	-515
844	S[239]	-9708	-420
845	S[240]	-9696	-325
846	S[241]	-9684	-515
847	S[242]	-9672	-420
848	S[243]	-9660	-325
849	S[244]	-9648	-515
850	S[245]	-9636	-420
851	S[246]	-9624	-325
852	S[247]	-9612	-515
853	S[248]	-9600	-420
854	S[249]	-9588	-325
855	S[250]	-9576	-515
856	S[251]	-9564	-420
857	S[252]	-9552	-325
858	S[253]	-9540	-515
859	S[254]	-9528	-420
860	S[255]	-9516	-325
861	S[256]	-9504	-515
862	S[257]	-9492	-420
863	S[258]	-9480	-325
864	S[259]	-9468	-515
865	S[260]	-9456	-420
866	S[261]	-9444	-325
867	S[262]	-9432	-515
868	S[263]	-9420	-420
869	S[264]	-9408	-325
870	S[265]	-9396	-515
871	S[266]	-9384	-420
872	S[267]	-9372	-325

Pad	Name	X	Y
873	S[268]	-9360	-515
874	S[269]	-9348	-420
875	S[270]	-9336	-325
876	S[271]	-9324	-515
877	S[272]	-9312	-420
878	S[273]	-9300	-325
879	S[274]	-9288	-515
880	S[275]	-9276	-420
881	S[276]	-9264	-325
882	S[277]	-9252	-515
883	S[278]	-9240	-420
884	S[279]	-9228	-325
885	S[280]	-9216	-515
886	S[281]	-9204	-420
887	S[282]	-9192	-325
888	S[283]	-9180	-515
889	S[284]	-9168	-420
890	S[285]	-9156	-325
891	S[286]	-9144	-515
892	S[287]	-9132	-420
893	S[288]	-9120	-325
894	S[289]	-9108	-515
895	S[290]	-9096	-420
896	S[291]	-9084	-325
897	S[292]	-9072	-515
898	S[293]	-9060	-420
899	S[294]	-9048	-325
900	S[295]	-9036	-515
901	S[296]	-9024	-420
902	S[297]	-9012	-325
903	S[298]	-9000	-515
904	S[299]	-8988	-420
905	S[300]	-8976	-325
906	S[301]	-8964	-515
907	S[302]	-8952	-420
908	S[303]	-8940	-325
909	S[304]	-8928	-515
910	S[305]	-8916	-420

Pad	Name	X	Y
911	S[306]	-8904	-325
912	S[307]	-8892	-515
913	S[308]	-8880	-420
914	S[309]	-8868	-325
915	S[310]	-8856	-515
916	S[311]	-8844	-420
917	S[312]	-8832	-325
918	S[313]	-8820	-515
919	S[314]	-8808	-420
920	S[315]	-8796	-325
921	S[316]	-8784	-515
922	S[317]	-8772	-420
923	S[318]	-8760	-325
924	S[319]	-8748	-515
925	S[320]	-8736	-420
926	S[321]	-8724	-325
927	S[322]	-8712	-515
928	S[323]	-8700	-420
929	S[324]	-8688	-325
930	S[325]	-8676	-515
931	S[326]	-8664	-420
932	S[327]	-8652	-325
933	S[328]	-8640	-515
934	S[329]	-8628	-420
935	S[330]	-8616	-325
936	S[331]	-8604	-515
937	S[332]	-8592	-420
938	S[333]	-8580	-325
939	S[334]	-8568	-515
940	S[335]	-8556	-420
941	S[336]	-8544	-325
942	S[337]	-8532	-515
943	S[338]	-8520	-420
944	S[339]	-8508	-325
945	S[340]	-8496	-515
946	S[341]	-8484	-420
947	S[342]	-8472	-325
948	S[343]	-8460	-515

Pad	Name	X	Y
949	S[344]	-8448	-420
950	S[345]	-8436	-325
951	S[346]	-8424	-515
952	S[347]	-8412	-420
953	S[348]	-8400	-325
954	S[349]	-8388	-515
955	S[350]	-8376	-420
956	S[351]	-8364	-325
957	S[352]	-8352	-515
958	S[353]	-8340	-420
959	S[354]	-8328	-325
960	S[355]	-8316	-515
961	S[356]	-8304	-420
962	S[357]	-8292	-325
963	S[358]	-8280	-515
964	S[359]	-8268	-420
965	S[360]	-8256	-325
966	S[361]	-8244	-515
967	S[362]	-8232	-420
968	S[363]	-8220	-325
969	S[364]	-8208	-515
970	S[365]	-8196	-420
971	S[366]	-8184	-325
972	S[367]	-8172	-515
973	S[368]	-8160	-420
974	S[369]	-8148	-325
975	S[370]	-8136	-515
976	S[371]	-8124	-420
977	S[372]	-8112	-325
978	S[373]	-8100	-515
979	S[374]	-8088	-420
980	S[375]	-8076	-325
981	S[376]	-8064	-515
982	S[377]	-8052	-420
983	S[378]	-8040	-325
984	S[379]	-8028	-515
985	S[380]	-8016	-420
986	S[381]	-8004	-325

Pad	Name	X	Y
987	S[382]	-7992	-515
988	S[383]	-7980	-420
989	S[384]	-7968	-325
990	S[385]	-7956	-515
991	S[386]	-7944	-420
992	S[387]	-7932	-325
993	S[388]	-7920	-515
994	S[389]	-7908	-420
995	S[390]	-7896	-325
996	S[391]	-7884	-515
997	S[392]	-7872	-420
998	S[393]	-7860	-325
999	S[394]	-7848	-515
1000	S[395]	-7836	-420
1001	S[396]	-7824	-325
1002	S[397]	-7812	-515
1003	S[398]	-7800	-420
1004	S[399]	-7788	-325
1005	S[400]	-7776	-515
1006	S[401]	-7764	-420
1007	S[402]	-7752	-325
1008	S[403]	-7740	-515
1009	S[404]	-7728	-420
1010	S[405]	-7716	-325
1011	S[406]	-7704	-515
1012	S[407]	-7692	-420
1013	S[408]	-7680	-325
1014	S[409]	-7668	-515
1015	S[410]	-7656	-420
1016	S[411]	-7644	-325
1017	S[412]	-7632	-515
1018	S[413]	-7620	-420
1019	S[414]	-7608	-325
1020	S[415]	-7596	-515
1021	S[416]	-7584	-420
1022	S[417]	-7572	-325
1023	S[418]	-7560	-515
1024	S[419]	-7548	-420

Pad	Name	X	Y
1025	S[420]	-7536	-325
1026	S[421]	-7524	-515
1027	S[422]	-7512	-420
1028	S[423]	-7500	-325
1029	S[424]	-7488	-515
1030	S[425]	-7476	-420
1031	S[426]	-7464	-325
1032	S[427]	-7452	-515
1033	S[428]	-7440	-420
1034	S[429]	-7428	-325
1035	S[430]	-7416	-515
1036	S[431]	-7404	-420
1037	S[432]	-7392	-325
1038	S[433]	-7380	-515
1039	S[434]	-7368	-420
1040	S[435]	-7356	-325
1041	S[436]	-7344	-515
1042	S[437]	-7332	-420
1043	S[438]	-7320	-325
1044	S[439]	-7308	-515
1045	S[440]	-7296	-420
1046	S[441]	-7284	-325
1047	S[442]	-7272	-515
1048	S[443]	-7260	-420
1049	S[444]	-7248	-325
1050	S[445]	-7236	-515
1051	S[446]	-7224	-420
1052	S[447]	-7212	-325
1053	S[448]	-7200	-515
1054	S[449]	-7188	-420
1055	S[450]	-7176	-325
1056	S[451]	-7164	-515
1057	S[452]	-7152	-420
1058	S[453]	-7140	-325
1059	S[454]	-7128	-515
1060	S[455]	-7116	-420
1061	S[456]	-7104	-325
1062	S[457]	-7092	-515

Pad	Name	X	Y
1063	S[458]	-7080	-420
1064	S[459]	-7068	-325
1065	S[460]	-7056	-515
1066	S[461]	-7044	-420
1067	S[462]	-7032	-325
1068	S[463]	-7020	-515
1069	S[464]	-7008	-420
1070	S[465]	-6996	-325
1071	S[466]	-6984	-515
1072	S[467]	-6972	-420
1073	S[468]	-6960	-325
1074	S[469]	-6948	-515
1075	S[470]	-6936	-420
1076	S[471]	-6924	-325
1077	S[472]	-6912	-515
1078	S[473]	-6900	-420
1079	S[474]	-6888	-325
1080	S[475]	-6876	-515
1081	S[476]	-6864	-420
1082	S[477]	-6852	-325
1083	S[478]	-6840	-515
1084	S[479]	-6828	-420
1085	S[480]	-6816	-325
1086	S[481]	-6804	-515
1087	S[482]	-6792	-420
1088	S[483]	-6780	-325
1089	S[484]	-6768	-515
1090	S[485]	-6756	-420
1091	S[486]	-6744	-325
1092	S[487]	-6732	-515
1093	S[488]	-6720	-420
1094	S[489]	-6708	-325
1095	S[490]	-6696	-515
1096	S[491]	-6684	-420
1097	S[492]	-6672	-325
1098	S[493]	-6660	-515
1099	S[494]	-6648	-420
1100	S[495]	-6636	-325

Pad	Name	X	Y
1101	S[496]	-6624	-515
1102	S[497]	-6612	-420
1103	S[498]	-6600	-325
1104	S[499]	-6588	-515
1105	S[500]	-6576	-420
1106	S[501]	-6564	-325
1107	S[502]	-6552	-515
1108	S[503]	-6540	-420
1109	S[504]	-6528	-325
1110	S[505]	-6516	-515
1111	S[506]	-6504	-420
1112	S[507]	-6492	-325
1113	S[508]	-6480	-515
1114	S[509]	-6468	-420
1115	S[510]	-6456	-325
1116	S[511]	-6444	-515
1117	S[512]	-6432	-420
1118	S[513]	-6420	-325
1119	S[514]	-6408	-515
1120	S[515]	-6396	-420
1121	S[516]	-6384	-325
1122	S[517]	-6372	-515
1123	S[518]	-6360	-420
1124	S[519]	-6348	-325
1125	S[520]	-6336	-515
1126	S[521]	-6324	-420
1127	S[522]	-6312	-325
1128	S[523]	-6300	-515
1129	S[524]	-6288	-420
1130	S[525]	-6276	-325
1131	S[526]	-6264	-515
1132	S[527]	-6252	-420
1133	S[528]	-6240	-325
1134	S[529]	-6228	-515
1135	S[530]	-6216	-420
1136	S[531]	-6204	-325
1137	S[532]	-6192	-515
1138	S[533]	-6180	-420

Pad	Name	X	Y
1139	S[534]	-6168	-325
1140	S[535]	-6156	-515
1141	S[536]	-6144	-420
1142	S[537]	-6132	-325
1143	S[538]	-6120	-515
1144	S[539]	-6108	-420
1145	S[540]	-6096	-325
1146	S[541]	-6084	-515
1147	S[542]	-6072	-420
1148	S[543]	-6060	-325
1149	S[544]	-6048	-515
1150	S[545]	-6036	-420
1151	S[546]	-6024	-325
1152	S[547]	-6012	-515
1153	S[548]	-6000	-420
1154	S[549]	-5988	-325
1155	S[550]	-5976	-515
1156	S[551]	-5964	-420
1157	S[552]	-5952	-325
1158	S[553]	-5940	-515
1159	S[554]	-5928	-420
1160	S[555]	-5916	-325
1161	S[556]	-5904	-515
1162	S[557]	-5892	-420
1163	S[558]	-5880	-325
1164	S[559]	-5868	-515
1165	S[560]	-5856	-420
1166	S[561]	-5844	-325
1167	S[562]	-5832	-515
1168	S[563]	-5820	-420
1169	S[564]	-5808	-325
1170	S[565]	-5796	-515
1171	S[566]	-5784	-420
1172	S[567]	-5772	-325
1173	S[568]	-5760	-515
1174	S[569]	-5748	-420
1175	S[570]	-5736	-325
1176	S[571]	-5724	-515

Pad	Name	X	Y
1177	S[572]	-5712	-420
1178	S[573]	-5700	-325
1179	S[574]	-5688	-515
1180	S[575]	-5676	-420
1181	S[576]	-5664	-325
1182	S[577]	-5652	-515
1183	S[578]	-5640	-420
1184	S[579]	-5628	-325
1185	S[580]	-5616	-515
1186	S[581]	-5604	-420
1187	S[582]	-5592	-325
1188	S[583]	-5580	-515
1189	S[584]	-5568	-420
1190	S[585]	-5556	-325
1191	S[586]	-5544	-515
1192	S[587]	-5532	-420
1193	S[588]	-5520	-325
1194	S[589]	-5508	-515
1195	S[590]	-5496	-420
1196	S[591]	-5484	-325
1197	S[592]	-5472	-515
1198	S[593]	-5460	-420
1199	S[594]	-5448	-325
1200	S[595]	-5436	-515
1201	S[596]	-5424	-420
1202	S[597]	-5412	-325
1203	S[598]	-5400	-515
1204	S[599]	-5388	-420
1205	S[600]	-5376	-325
1206	S[601]	-5364	-515
1207	S[602]	-5352	-420
1208	S[603]	-5340	-325
1209	S[604]	-5328	-515
1210	S[605]	-5316	-420
1211	S[606]	-5304	-325
1212	S[607]	-5292	-515
1213	S[608]	-5280	-420
1214	S[609]	-5268	-325

Pad	Name	X	Y
1215	S[610]	-5256	-515
1216	S[611]	-5244	-420
1217	S[612]	-5232	-325
1218	S[613]	-5220	-515
1219	S[614]	-5208	-420
1220	S[615]	-5196	-325
1221	S[616]	-5184	-515
1222	S[617]	-5172	-420
1223	S[618]	-5160	-325
1224	S[619]	-5148	-515
1225	S[620]	-5136	-420
1226	S[621]	-5124	-325
1227	S[622]	-5112	-515
1228	S[623]	-5100	-420
1229	S[624]	-5088	-325
1230	S[625]	-5076	-515
1231	S[626]	-5064	-420
1232	S[627]	-5052	-325
1233	S[628]	-5040	-515
1234	S[629]	-5028	-420
1235	S[630]	-5016	-325
1236	S[631]	-5004	-515
1237	S[632]	-4992	-420
1238	S[633]	-4980	-325
1239	S[634]	-4968	-515
1240	S[635]	-4956	-420
1241	S[636]	-4944	-325
1242	S[637]	-4932	-515
1243	S[638]	-4920	-420
1244	S[639]	-4908	-325
1245	S[640]	-4896	-515
1246	S[641]	-4884	-420
1247	S[642]	-4872	-325
1248	S[643]	-4860	-515
1249	S[644]	-4848	-420
1250	S[645]	-4836	-325
1251	S[646]	-4824	-515
1252	S[647]	-4812	-420

Pad	Name	X	Y
1253	S[648]	-4800	-325
1254	S[649]	-4788	-515
1255	S[650]	-4776	-420
1256	S[651]	-4764	-325
1257	S[652]	-4752	-515
1258	S[653]	-4740	-420
1259	S[654]	-4728	-325
1260	S[655]	-4716	-515
1261	S[656]	-4704	-420
1262	S[657]	-4692	-325
1263	S[658]	-4680	-515
1264	S[659]	-4668	-420
1265	S[660]	-4656	-325
1266	S[661]	-4644	-515
1267	S[662]	-4632	-420
1268	S[663]	-4620	-325
1269	S[664]	-4608	-515
1270	S[665]	-4596	-420
1271	S[666]	-4584	-325
1272	S[667]	-4572	-515
1273	S[668]	-4560	-420
1274	S[669]	-4548	-325
1275	S[670]	-4536	-515
1276	S[671]	-4524	-420
1277	S[672]	-4512	-325
1278	S[673]	-4500	-515
1279	S[674]	-4488	-420
1280	S[675]	-4476	-325
1281	S[676]	-4464	-515
1282	S[677]	-4452	-420
1283	S[678]	-4440	-325
1284	S[679]	-4428	-515
1285	S[680]	-4416	-420
1286	S[681]	-4404	-325
1287	S[682]	-4392	-515
1288	S[683]	-4380	-420
1289	S[684]	-4368	-325
1290	S[685]	-4356	-515

Pad	Name	X	Y
1291	S[686]	-4344	-420
1292	S[687]	-4332	-325
1293	S[688]	-4320	-515
1294	S[689]	-4308	-420
1295	S[690]	-4296	-325
1296	S[691]	-4284	-515
1297	S[692]	-4272	-420
1298	S[693]	-4260	-325
1299	S[694]	-4248	-515
1300	S[695]	-4236	-420
1301	S[696]	-4224	-325
1302	S[697]	-4212	-515
1303	S[698]	-4200	-420
1304	S[699]	-4188	-325
1305	S[700]	-4176	-515
1306	S[701]	-4164	-420
1307	S[702]	-4152	-325
1308	S[703]	-4140	-515
1309	S[704]	-4128	-420
1310	S[705]	-4116	-325
1311	S[706]	-4104	-515
1312	S[707]	-4092	-420
1313	S[708]	-4080	-325
1314	S[709]	-4068	-515
1315	S[710]	-4056	-420
1316	S[711]	-4044	-325
1317	S[712]	-4032	-515
1318	S[713]	-4020	-420
1319	S[714]	-4008	-325
1320	S[715]	-3996	-515
1321	S[716]	-3984	-420
1322	S[717]	-3972	-325
1323	S[718]	-3960	-515
1324	S[719]	-3948	-420
1325	S[720]	-3936	-325
1326	S[721]	-3924	-515
1327	S[722]	-3912	-420
1328	S[723]	-3900	-325

Pad	Name	X	Y
1329	S[724]	-3888	-515
1330	S[725]	-3876	-420
1331	S[726]	-3864	-325
1332	S[727]	-3852	-515
1333	S[728]	-3840	-420
1334	S[729]	-3828	-325
1335	S[730]	-3816	-515
1336	S[731]	-3804	-420
1337	S[732]	-3792	-325
1338	S[733]	-3780	-515
1339	S[734]	-3768	-420
1340	S[735]	-3756	-325
1341	S[736]	-3744	-515
1342	S[737]	-3732	-420
1343	S[738]	-3720	-325
1344	S[739]	-3708	-515
1345	S[740]	-3696	-420
1346	S[741]	-3684	-325
1347	S[742]	-3672	-515
1348	S[743]	-3660	-420
1349	S[744]	-3648	-325
1350	S[745]	-3636	-515
1351	S[746]	-3624	-420
1352	S[747]	-3612	-325
1353	S[748]	-3600	-515
1354	S[749]	-3588	-420
1355	S[750]	-3576	-325
1356	S[751]	-3564	-515
1357	S[752]	-3552	-420
1358	S[753]	-3540	-325
1359	S[754]	-3528	-515
1360	S[755]	-3516	-420
1361	S[756]	-3504	-325
1362	S[757]	-3492	-515
1363	S[758]	-3480	-420
1364	S[759]	-3468	-325
1365	S[760]	-3456	-515
1366	S[761]	-3444	-420

Pad	Name	X	Y
1367	S[762]	-3432	-325
1368	S[763]	-3420	-515
1369	S[764]	-3408	-420
1370	S[765]	-3396	-325
1371	S[766]	-3384	-515
1372	S[767]	-3372	-420
1373	S[768]	-3360	-325
1374	S[769]	-3348	-515
1375	S[770]	-3336	-420
1376	S[771]	-3324	-325
1377	S[772]	-3312	-515
1378	S[773]	-3300	-420
1379	S[774]	-3288	-325
1380	S[775]	-3276	-515
1381	S[776]	-3264	-420
1382	S[777]	-3252	-325
1383	S[778]	-3240	-515
1384	S[779]	-3228	-420
1385	S[780]	-3216	-325
1386	S[781]	-3204	-515
1387	S[782]	-3192	-420
1388	S[783]	-3180	-325
1389	S[784]	-3168	-515
1390	S[785]	-3156	-420
1391	S[786]	-3144	-325
1392	S[787]	-3132	-515
1393	S[788]	-3120	-420
1394	S[789]	-3108	-325
1395	S[790]	-3096	-515
1396	S[791]	-3084	-420
1397	S[792]	-3072	-325
1398	S[793]	-3060	-515
1399	S[794]	-3048	-420
1400	S[795]	-3036	-325
1401	S[796]	-3024	-515
1402	S[797]	-3012	-420
1403	S[798]	-3000	-325
1404	S[799]	-2988	-515

Pad	Name	X	Y
1405	S[800]	-2976	-420
1406	S[801]	-2964	-325
1407	S[802]	-2952	-515
1408	S[803]	-2940	-420
1409	S[804]	-2928	-325
1410	S[805]	-2916	-515
1411	S[806]	-2904	-420
1412	S[807]	-2892	-325
1413	S[808]	-2880	-515
1414	S[809]	-2868	-420
1415	S[810]	-2856	-325
1416	S[811]	-2844	-515
1417	S[812]	-2832	-420
1418	S[813]	-2820	-325
1419	S[814]	-2808	-515
1420	S[815]	-2796	-420
1421	S[816]	-2784	-325
1422	S[817]	-2772	-515
1423	S[818]	-2760	-420
1424	S[819]	-2748	-325
1425	S[820]	-2736	-515
1426	S[821]	-2724	-420
1427	S[822]	-2712	-325
1428	S[823]	-2700	-515
1429	S[824]	-2688	-420
1430	S[825]	-2676	-325
1431	S[826]	-2664	-515
1432	S[827]	-2652	-420
1433	S[828]	-2640	-325
1434	S[829]	-2628	-515
1435	S[830]	-2616	-420
1436	S[831]	-2604	-325
1437	S[832]	-2592	-515
1438	S[833]	-2580	-420
1439	S[834]	-2568	-325
1440	S[835]	-2556	-515
1441	S[836]	-2544	-420
1442	S[837]	-2532	-325

Pad	Name	X	Y
1443	S[838]	-2520	-515
1444	S[839]	-2508	-420
1445	S[840]	-2496	-325
1446	S[841]	-2484	-515
1447	S[842]	-2472	-420
1448	S[843]	-2460	-325
1449	S[844]	-2448	-515
1450	S[845]	-2436	-420
1451	S[846]	-2424	-325
1452	S[847]	-2412	-515
1453	S[848]	-2400	-420
1454	S[849]	-2388	-325
1455	S[850]	-2376	-515
1456	S[851]	-2364	-420
1457	S[852]	-2352	-325
1458	S[853]	-2340	-515
1459	S[854]	-2328	-420
1460	S[855]	-2316	-325
1461	S[856]	-2304	-515
1462	S[857]	-2292	-420
1463	S[858]	-2280	-325
1464	S[859]	-2268	-515
1465	S[860]	-2256	-420
1466	S[861]	-2244	-325
1467	S[862]	-2232	-515
1468	S[863]	-2220	-420
1469	S[864]	-2208	-325
1470	S[865]	-2196	-515
1471	S[866]	-2184	-420
1472	S[867]	-2172	-325
1473	S[868]	-2160	-515
1474	S[869]	-2148	-420
1475	S[870]	-2136	-325
1476	S[871]	-2124	-515
1477	S[872]	-2112	-420
1478	S[873]	-2100	-325
1479	S[874]	-2088	-515
1480	S[875]	-2076	-420

Pad	Name	X	Y
1481	S[876]	-2064	-325
1482	S[877]	-2052	-515
1483	S[878]	-2040	-420
1484	S[879]	-2028	-325
1485	S[880]	-2016	-515
1486	S[881]	-2004	-420
1487	S[882]	-1992	-325
1488	S[883]	-1980	-515
1489	S[884]	-1968	-420
1490	S[885]	-1956	-325
1491	S[886]	-1944	-515
1492	S[887]	-1932	-420
1493	S[888]	-1920	-325
1494	S[889]	-1908	-515
1495	S[890]	-1896	-420
1496	S[891]	-1884	-325
1497	S[892]	-1872	-515
1498	S[893]	-1860	-420
1499	S[894]	-1848	-325
1500	S[895]	-1836	-515
1501	S[896]	-1824	-420
1502	S[897]	-1812	-325
1503	S[898]	-1800	-515
1504	S[899]	-1788	-420
1505	S[900]	-1776	-325
1506	S[901]	-1764	-515
1507	S[902]	-1752	-420
1508	S[903]	-1740	-325
1509	S[904]	-1728	-515
1510	S[905]	-1716	-420
1511	S[906]	-1704	-325
1512	S[907]	-1692	-515
1513	S[908]	-1680	-420
1514	S[909]	-1668	-325
1515	S[910]	-1656	-515
1516	S[911]	-1644	-420
1517	S[912]	-1632	-325
1518	S[913]	-1620	-515

Pad	Name	X	Y
1519	S[914]	-1608	-420
1520	S[915]	-1596	-325
1521	S[916]	-1584	-515
1522	S[917]	-1572	-420
1523	S[918]	-1560	-325
1524	S[919]	-1548	-515
1525	S[920]	-1536	-420
1526	S[921]	-1524	-325
1527	S[922]	-1512	-515
1528	S[923]	-1500	-420
1529	S[924]	-1488	-325
1530	S[925]	-1476	-515
1531	S[926]	-1464	-420
1532	S[927]	-1452	-325
1533	S[928]	-1440	-515
1534	S[929]	-1428	-420
1535	S[930]	-1416	-325
1536	S[931]	-1404	-515
1537	S[932]	-1392	-420
1538	S[933]	-1380	-325
1539	S[934]	-1368	-515
1540	S[935]	-1356	-420
1541	S[936]	-1344	-325
1542	S[937]	-1332	-515
1543	S[938]	-1320	-420
1544	S[939]	-1308	-325
1545	S[940]	-1296	-515
1546	S[941]	-1284	-420
1547	S[942]	-1272	-325
1548	S[943]	-1260	-515
1549	S[944]	-1248	-420
1550	S[945]	-1236	-325
1551	S[946]	-1224	-515
1552	S[947]	-1212	-420
1553	S[948]	-1200	-325
1554	S[949]	-1188	-515
1555	S[950]	-1176	-420
1556	S[951]	-1164	-325

Pad	Name	X	Y
1557	S[952]	-1152	-515
1558	S[953]	-1140	-420
1559	S[954]	-1128	-325
1560	S[955]	-1116	-515
1561	S[956]	-1104	-420
1562	S[957]	-1092	-325
1563	S[958]	-1080	-515
1564	S[959]	-1068	-420
1565	S[960]	-1056	-325
1566	DUMMY	-1044	-515
1567	DUMMY	-1008	-515
1568	DUMMY	-972	-515
1569	DUMMY	-936	-515
1570	DUMMY	-900	-515
1571	DUMMY	-864	-515
1572	DUMMY	-828	-515
1573	DUMMY	-792	-515
1574	DUMMY	-756	-515
1575	DUMMY	-720	-515
1576	DUMMY	-684	-515
1577	DUMMY	-648	-515
1578	DUMMY	-612	-515
1579	DUMMY	-576	-515
1580	DUMMY	-540	-515
1581	DUMMY	-504	-515
1582	DUMMY	-468	-515
1583	DUMMY	-432	-515
1584	DUMMY	-396	-515
1585	DUMMY	-360	-515
1586	DUMMY	-324	-515
1587	DUMMY	-288	-515
1588	DUMMY	-252	-515
1589	DUMMY	-216	-515
1590	DUMMY	-180	-515
1591	DUMMY	-144	-515
1592	DUMMY	-108	-515
1593	DUMMY	-72	-515
1594	DUMMY	-36	-515

Pad	Name	X	Y
1595	DUMMY	0	-515
1596	DUMMY	36	-515
1597	DUMMY	72	-515
1598	DUMMY	108	-515
1599	DUMMY	144	-515
1600	DUMMY	180	-515
1601	DUMMY	216	-515
1602	DUMMY	252	-515
1603	DUMMY	288	-515
1604	DUMMY	324	-515
1605	DUMMY	360	-515
1606	DUMMY	396	-515
1607	DUMMY	432	-515
1608	DUMMY	468	-515
1609	DUMMY	504	-515
1610	DUMMY	540	-515
1611	DUMMY	576	-515
1612	DUMMY	612	-515
1613	DUMMY	648	-515
1614	DUMMY	684	-515
1615	DUMMY	720	-515
1616	DUMMY	756	-515
1617	DUMMY	792	-515
1618	DUMMY	828	-515
1619	DUMMY	864	-515
1620	DUMMY	900	-515
1621	DUMMY	936	-515
1622	DUMMY	972	-515
1623	DUMMY	1008	-515
1624	DUMMY	1044	-515
1625	S[961]	1056	-325
1626	S[962]	1068	-420
1627	S[963]	1080	-515
1628	S[964]	1092	-325
1629	S[965]	1104	-420
1630	S[966]	1116	-515
1631	S[967]	1128	-325
1632	S[968]	1140	-420

Pad	Name	X	Y
1633	S[969]	1152	-515
1634	S[970]	1164	-325
1635	S[971]	1176	-420
1636	S[972]	1188	-515
1637	S[973]	1200	-325
1638	S[974]	1212	-420
1639	S[975]	1224	-515
1640	S[976]	1236	-325
1641	S[977]	1248	-420
1642	S[978]	1260	-515
1643	S[979]	1272	-325
1644	S[980]	1284	-420
1645	S[981]	1296	-515
1646	S[982]	1308	-325
1647	S[983]	1320	-420
1648	S[984]	1332	-515
1649	S[985]	1344	-325
1650	S[986]	1356	-420
1651	S[987]	1368	-515
1652	S[988]	1380	-325
1653	S[989]	1392	-420
1654	S[990]	1404	-515
1655	S[991]	1416	-325
1656	S[992]	1428	-420
1657	S[993]	1440	-515
1658	S[994]	1452	-325
1659	S[995]	1464	-420
1660	S[996]	1476	-515
1661	S[997]	1488	-325
1662	S[998]	1500	-420
1663	S[999]	1512	-515
1664	S[1000]	1524	-325
1665	S[1001]	1536	-420
1666	S[1002]	1548	-515
1667	S[1003]	1560	-325
1668	S[1004]	1572	-420
1669	S[1005]	1584	-515
1670	S[1006]	1596	-325

Pad	Name	X	Y
1671	S[1007]	1608	-420
1672	S[1008]	1620	-515
1673	S[1009]	1632	-325
1674	S[1010]	1644	-420
1675	S[1011]	1656	-515
1676	S[1012]	1668	-325
1677	S[1013]	1680	-420
1678	S[1014]	1692	-515
1679	S[1015]	1704	-325
1680	S[1016]	1716	-420
1681	S[1017]	1728	-515
1682	S[1018]	1740	-325
1683	S[1019]	1752	-420
1684	S[1020]	1764	-515
1685	S[1021]	1776	-325
1686	S[1022]	1788	-420
1687	S[1023]	1800	-515
1688	S[1024]	1812	-325
1689	S[1025]	1824	-420
1690	S[1026]	1836	-515
1691	S[1027]	1848	-325
1692	S[1028]	1860	-420
1693	S[1029]	1872	-515
1694	S[1030]	1884	-325
1695	S[1031]	1896	-420
1696	S[1032]	1908	-515
1697	S[1033]	1920	-325
1698	S[1034]	1932	-420
1699	S[1035]	1944	-515
1700	S[1036]	1956	-325
1701	S[1037]	1968	-420
1702	S[1038]	1980	-515
1703	S[1039]	1992	-325
1704	S[1040]	2004	-420
1705	S[1041]	2016	-515
1706	S[1042]	2028	-325
1707	S[1043]	2040	-420
1708	S[1044]	2052	-515

Pad	Name	X	Y
1709	S[1045]	2064	-325
1710	S[1046]	2076	-420
1711	S[1047]	2088	-515
1712	S[1048]	2100	-325
1713	S[1049]	2112	-420
1714	S[1050]	2124	-515
1715	S[1051]	2136	-325
1716	S[1052]	2148	-420
1717	S[1053]	2160	-515
1718	S[1054]	2172	-325
1719	S[1055]	2184	-420
1720	S[1056]	2196	-515
1721	S[1057]	2208	-325
1722	S[1058]	2220	-420
1723	S[1059]	2232	-515
1724	S[1060]	2244	-325
1725	S[1061]	2256	-420
1726	S[1062]	2268	-515
1727	S[1063]	2280	-325
1728	S[1064]	2292	-420
1729	S[1065]	2304	-515
1730	S[1066]	2316	-325
1731	S[1067]	2328	-420
1732	S[1068]	2340	-515
1733	S[1069]	2352	-325
1734	S[1070]	2364	-420
1735	S[1071]	2376	-515
1736	S[1072]	2388	-325
1737	S[1073]	2400	-420
1738	S[1074]	2412	-515
1739	S[1075]	2424	-325
1740	S[1076]	2436	-420
1741	S[1077]	2448	-515
1742	S[1078]	2460	-325
1743	S[1079]	2472	-420
1744	S[1080]	2484	-515
1745	S[1081]	2496	-325
1746	S[1082]	2508	-420

Pad	Name	X	Y
1747	S[1083]	2520	-515
1748	S[1084]	2532	-325
1749	S[1085]	2544	-420
1750	S[1086]	2556	-515
1751	S[1087]	2568	-325
1752	S[1088]	2580	-420
1753	S[1089]	2592	-515
1754	S[1090]	2604	-325
1755	S[1091]	2616	-420
1756	S[1092]	2628	-515
1757	S[1093]	2640	-325
1758	S[1094]	2652	-420
1759	S[1095]	2664	-515
1760	S[1096]	2676	-325
1761	S[1097]	2688	-420
1762	S[1098]	2700	-515
1763	S[1099]	2712	-325
1764	S[1100]	2724	-420
1765	S[1101]	2736	-515
1766	S[1102]	2748	-325
1767	S[1103]	2760	-420
1768	S[1104]	2772	-515
1769	S[1105]	2784	-325
1770	S[1106]	2796	-420
1771	S[1107]	2808	-515
1772	S[1108]	2820	-325
1773	S[1109]	2832	-420
1774	S[1110]	2844	-515
1775	S[1111]	2856	-325
1776	S[1112]	2868	-420
1777	S[1113]	2880	-515
1778	S[1114]	2892	-325
1779	S[1115]	2904	-420
1780	S[1116]	2916	-515
1781	S[1117]	2928	-325
1782	S[1118]	2940	-420
1783	S[1119]	2952	-515
1784	S[1120]	2964	-325

Pad	Name	X	Y
1785	S[1121]	2976	-420
1786	S[1122]	2988	-515
1787	S[1123]	3000	-325
1788	S[1124]	3012	-420
1789	S[1125]	3024	-515
1790	S[1126]	3036	-325
1791	S[1127]	3048	-420
1792	S[1128]	3060	-515
1793	S[1129]	3072	-325
1794	S[1130]	3084	-420
1795	S[1131]	3096	-515
1796	S[1132]	3108	-325
1797	S[1133]	3120	-420
1798	S[1134]	3132	-515
1799	S[1135]	3144	-325
1800	S[1136]	3156	-420
1801	S[1137]	3168	-515
1802	S[1138]	3180	-325
1803	S[1139]	3192	-420
1804	S[1140]	3204	-515
1805	S[1141]	3216	-325
1806	S[1142]	3228	-420
1807	S[1143]	3240	-515
1808	S[1144]	3252	-325
1809	S[1145]	3264	-420
1810	S[1146]	3276	-515
1811	S[1147]	3288	-325
1812	S[1148]	3300	-420
1813	S[1149]	3312	-515
1814	S[1150]	3324	-325
1815	S[1151]	3336	-420
1816	S[1152]	3348	-515
1817	S[1153]	3360	-325
1818	S[1154]	3372	-420
1819	S[1155]	3384	-515
1820	S[1156]	3396	-325
1821	S[1157]	3408	-420
1822	S[1158]	3420	-515

Pad	Name	X	Y
1823	S[1159]	3432	-325
1824	S[1160]	3444	-420
1825	S[1161]	3456	-515
1826	S[1162]	3468	-325
1827	S[1163]	3480	-420
1828	S[1164]	3492	-515
1829	S[1165]	3504	-325
1830	S[1166]	3516	-420
1831	S[1167]	3528	-515
1832	S[1168]	3540	-325
1833	S[1169]	3552	-420
1834	S[1170]	3564	-515
1835	S[1171]	3576	-325
1836	S[1172]	3588	-420
1837	S[1173]	3600	-515
1838	S[1174]	3612	-325
1839	S[1175]	3624	-420
1840	S[1176]	3636	-515
1841	S[1177]	3648	-325
1842	S[1178]	3660	-420
1843	S[1179]	3672	-515
1844	S[1180]	3684	-325
1845	S[1181]	3696	-420
1846	S[1182]	3708	-515
1847	S[1183]	3720	-325
1848	S[1184]	3732	-420
1849	S[1185]	3744	-515
1850	S[1186]	3756	-325
1851	S[1187]	3768	-420
1852	S[1188]	3780	-515
1853	S[1189]	3792	-325
1854	S[1190]	3804	-420
1855	S[1191]	3816	-515
1856	S[1192]	3828	-325
1857	S[1193]	3840	-420
1858	S[1194]	3852	-515
1859	S[1195]	3864	-325
1860	S[1196]	3876	-420

Pad	Name	X	Y
1861	S[1197]	3888	-515
1862	S[1198]	3900	-325
1863	S[1199]	3912	-420
1864	S[1200]	3924	-515
1865	S[1201]	3936	-325
1866	S[1202]	3948	-420
1867	S[1203]	3960	-515
1868	S[1204]	3972	-325
1869	S[1205]	3984	-420
1870	S[1206]	3996	-515
1871	S[1207]	4008	-325
1872	S[1208]	4020	-420
1873	S[1209]	4032	-515
1874	S[1210]	4044	-325
1875	S[1211]	4056	-420
1876	S[1212]	4068	-515
1877	S[1213]	4080	-325
1878	S[1214]	4092	-420
1879	S[1215]	4104	-515
1880	S[1216]	4116	-325
1881	S[1217]	4128	-420
1882	S[1218]	4140	-515
1883	S[1219]	4152	-325
1884	S[1220]	4164	-420
1885	S[1221]	4176	-515
1886	S[1222]	4188	-325
1887	S[1223]	4200	-420
1888	S[1224]	4212	-515
1889	S[1225]	4224	-325
1890	S[1226]	4236	-420
1891	S[1227]	4248	-515
1892	S[1228]	4260	-325
1893	S[1229]	4272	-420
1894	S[1230]	4284	-515
1895	S[1231]	4296	-325
1896	S[1232]	4308	-420
1897	S[1233]	4320	-515
1898	S[1234]	4332	-325

Pad	Name	X	Y
1899	S[1235]	4344	-420
1900	S[1236]	4356	-515
1901	S[1237]	4368	-325
1902	S[1238]	4380	-420
1903	S[1239]	4392	-515
1904	S[1240]	4404	-325
1905	S[1241]	4416	-420
1906	S[1242]	4428	-515
1907	S[1243]	4440	-325
1908	S[1244]	4452	-420
1909	S[1245]	4464	-515
1910	S[1246]	4476	-325
1911	S[1247]	4488	-420
1912	S[1248]	4500	-515
1913	S[1249]	4512	-325
1914	S[1250]	4524	-420
1915	S[1251]	4536	-515
1916	S[1252]	4548	-325
1917	S[1253]	4560	-420
1918	S[1254]	4572	-515
1919	S[1255]	4584	-325
1920	S[1256]	4596	-420
1921	S[1257]	4608	-515
1922	S[1258]	4620	-325
1923	S[1259]	4632	-420
1924	S[1260]	4644	-515
1925	S[1261]	4656	-325
1926	S[1262]	4668	-420
1927	S[1263]	4680	-515
1928	S[1264]	4692	-325
1929	S[1265]	4704	-420
1930	S[1266]	4716	-515
1931	S[1267]	4728	-325
1932	S[1268]	4740	-420
1933	S[1269]	4752	-515
1934	S[1270]	4764	-325
1935	S[1271]	4776	-420
1936	S[1272]	4788	-515

Pad	Name	X	Y
1937	S[1273]	4800	-325
1938	S[1274]	4812	-420
1939	S[1275]	4824	-515
1940	S[1276]	4836	-325
1941	S[1277]	4848	-420
1942	S[1278]	4860	-515
1943	S[1279]	4872	-325
1944	S[1280]	4884	-420
1945	S[1281]	4896	-515
1946	S[1282]	4908	-325
1947	S[1283]	4920	-420
1948	S[1284]	4932	-515
1949	S[1285]	4944	-325
1950	S[1286]	4956	-420
1951	S[1287]	4968	-515
1952	S[1288]	4980	-325
1953	S[1289]	4992	-420
1954	S[1290]	5004	-515
1955	S[1291]	5016	-325
1956	S[1292]	5028	-420
1957	S[1293]	5040	-515
1958	S[1294]	5052	-325
1959	S[1295]	5064	-420
1960	S[1296]	5076	-515
1961	S[1297]	5088	-325
1962	S[1298]	5100	-420
1963	S[1299]	5112	-515
1964	S[1300]	5124	-325
1965	S[1301]	5136	-420
1966	S[1302]	5148	-515
1967	S[1303]	5160	-325
1968	S[1304]	5172	-420
1969	S[1305]	5184	-515
1970	S[1306]	5196	-325
1971	S[1307]	5208	-420
1972	S[1308]	5220	-515
1973	S[1309]	5232	-325
1974	S[1310]	5244	-420

Pad	Name	X	Y
1975	S[1311]	5256	-515
1976	S[1312]	5268	-325
1977	S[1313]	5280	-420
1978	S[1314]	5292	-515
1979	S[1315]	5304	-325
1980	S[1316]	5316	-420
1981	S[1317]	5328	-515
1982	S[1318]	5340	-325
1983	S[1319]	5352	-420
1984	S[1320]	5364	-515
1985	S[1321]	5376	-325
1986	S[1322]	5388	-420
1987	S[1323]	5400	-515
1988	S[1324]	5412	-325
1989	S[1325]	5424	-420
1990	S[1326]	5436	-515
1991	S[1327]	5448	-325
1992	S[1328]	5460	-420
1993	S[1329]	5472	-515
1994	S[1330]	5484	-325
1995	S[1331]	5496	-420
1996	S[1332]	5508	-515
1997	S[1333]	5520	-325
1998	S[1334]	5532	-420
1999	S[1335]	5544	-515
2000	S[1336]	5556	-325
2001	S[1337]	5568	-420
2002	S[1338]	5580	-515
2003	S[1339]	5592	-325
2004	S[1340]	5604	-420
2005	S[1341]	5616	-515
2006	S[1342]	5628	-325
2007	S[1343]	5640	-420
2008	S[1344]	5652	-515
2009	S[1345]	5664	-325
2010	S[1346]	5676	-420
2011	S[1347]	5688	-515
2012	S[1348]	5700	-325

Pad	Name	X	Y
2013	S[1349]	5712	-420
2014	S[1350]	5724	-515
2015	S[1351]	5736	-325
2016	S[1352]	5748	-420
2017	S[1353]	5760	-515
2018	S[1354]	5772	-325
2019	S[1355]	5784	-420
2020	S[1356]	5796	-515
2021	S[1357]	5808	-325
2022	S[1358]	5820	-420
2023	S[1359]	5832	-515
2024	S[1360]	5844	-325
2025	S[1361]	5856	-420
2026	S[1362]	5868	-515
2027	S[1363]	5880	-325
2028	S[1364]	5892	-420
2029	S[1365]	5904	-515
2030	S[1366]	5916	-325
2031	S[1367]	5928	-420
2032	S[1368]	5940	-515
2033	S[1369]	5952	-325
2034	S[1370]	5964	-420
2035	S[1371]	5976	-515
2036	S[1372]	5988	-325
2037	S[1373]	6000	-420
2038	S[1374]	6012	-515
2039	S[1375]	6024	-325
2040	S[1376]	6036	-420
2041	S[1377]	6048	-515
2042	S[1378]	6060	-325
2043	S[1379]	6072	-420
2044	S[1380]	6084	-515
2045	S[1381]	6096	-325
2046	S[1382]	6108	-420
2047	S[1383]	6120	-515
2048	S[1384]	6132	-325
2049	S[1385]	6144	-420
2050	S[1386]	6156	-515

Pad	Name	X	Y
2051	S[1387]	6168	-325
2052	S[1388]	6180	-420
2053	S[1389]	6192	-515
2054	S[1390]	6204	-325
2055	S[1391]	6216	-420
2056	S[1392]	6228	-515
2057	S[1393]	6240	-325
2058	S[1394]	6252	-420
2059	S[1395]	6264	-515
2060	S[1396]	6276	-325
2061	S[1397]	6288	-420
2062	S[1398]	6300	-515
2063	S[1399]	6312	-325
2064	S[1400]	6324	-420
2065	S[1401]	6336	-515
2066	S[1402]	6348	-325
2067	S[1403]	6360	-420
2068	S[1404]	6372	-515
2069	S[1405]	6384	-325
2070	S[1406]	6396	-420
2071	S[1407]	6408	-515
2072	S[1408]	6420	-325
2073	S[1409]	6432	-420
2074	S[1410]	6444	-515
2075	S[1411]	6456	-325
2076	S[1412]	6468	-420
2077	S[1413]	6480	-515
2078	S[1414]	6492	-325
2079	S[1415]	6504	-420
2080	S[1416]	6516	-515
2081	S[1417]	6528	-325
2082	S[1418]	6540	-420
2083	S[1419]	6552	-515
2084	S[1420]	6564	-325
2085	S[1421]	6576	-420
2086	S[1422]	6588	-515
2087	S[1423]	6600	-325
2088	S[1424]	6612	-420

Pad	Name	X	Y
2089	S[1425]	6624	-515
2090	S[1426]	6636	-325
2091	S[1427]	6648	-420
2092	S[1428]	6660	-515
2093	S[1429]	6672	-325
2094	S[1430]	6684	-420
2095	S[1431]	6696	-515
2096	S[1432]	6708	-325
2097	S[1433]	6720	-420
2098	S[1434]	6732	-515
2099	S[1435]	6744	-325
2100	S[1436]	6756	-420
2101	S[1437]	6768	-515
2102	S[1438]	6780	-325
2103	S[1439]	6792	-420
2104	S[1440]	6804	-515
2105	S[1441]	6816	-325
2106	S[1442]	6828	-420
2107	S[1443]	6840	-515
2108	S[1444]	6852	-325
2109	S[1445]	6864	-420
2110	S[1446]	6876	-515
2111	S[1447]	6888	-325
2112	S[1448]	6900	-420
2113	S[1449]	6912	-515
2114	S[1450]	6924	-325
2115	S[1451]	6936	-420
2116	S[1452]	6948	-515
2117	S[1453]	6960	-325
2118	S[1454]	6972	-420
2119	S[1455]	6984	-515
2120	S[1456]	6996	-325
2121	S[1457]	7008	-420
2122	S[1458]	7020	-515
2123	S[1459]	7032	-325
2124	S[1460]	7044	-420
2125	S[1461]	7056	-515
2126	S[1462]	7068	-325

Pad	Name	X	Y
2127	S[1463]	7080	-420
2128	S[1464]	7092	-515
2129	S[1465]	7104	-325
2130	S[1466]	7116	-420
2131	S[1467]	7128	-515
2132	S[1468]	7140	-325
2133	S[1469]	7152	-420
2134	S[1470]	7164	-515
2135	S[1471]	7176	-325
2136	S[1472]	7188	-420
2137	S[1473]	7200	-515
2138	S[1474]	7212	-325
2139	S[1475]	7224	-420
2140	S[1476]	7236	-515
2141	S[1477]	7248	-325
2142	S[1478]	7260	-420
2143	S[1479]	7272	-515
2144	S[1480]	7284	-325
2145	S[1481]	7296	-420
2146	S[1482]	7308	-515
2147	S[1483]	7320	-325
2148	S[1484]	7332	-420
2149	S[1485]	7344	-515
2150	S[1486]	7356	-325
2151	S[1487]	7368	-420
2152	S[1488]	7380	-515
2153	S[1489]	7392	-325
2154	S[1490]	7404	-420
2155	S[1491]	7416	-515
2156	S[1492]	7428	-325
2157	S[1493]	7440	-420
2158	S[1494]	7452	-515
2159	S[1495]	7464	-325
2160	S[1496]	7476	-420
2161	S[1497]	7488	-515
2162	S[1498]	7500	-325
2163	S[1499]	7512	-420
2164	S[1500]	7524	-515

Pad	Name	X	Y
2165	S[1501]	7536	-325
2166	S[1502]	7548	-420
2167	S[1503]	7560	-515
2168	S[1504]	7572	-325
2169	S[1505]	7584	-420
2170	S[1506]	7596	-515
2171	S[1507]	7608	-325
2172	S[1508]	7620	-420
2173	S[1509]	7632	-515
2174	S[1510]	7644	-325
2175	S[1511]	7656	-420
2176	S[1512]	7668	-515
2177	S[1513]	7680	-325
2178	S[1514]	7692	-420
2179	S[1515]	7704	-515
2180	S[1516]	7716	-325
2181	S[1517]	7728	-420
2182	S[1518]	7740	-515
2183	S[1519]	7752	-325
2184	S[1520]	7764	-420
2185	S[1521]	7776	-515
2186	S[1522]	7788	-325
2187	S[1523]	7800	-420
2188	S[1524]	7812	-515
2189	S[1525]	7824	-325
2190	S[1526]	7836	-420
2191	S[1527]	7848	-515
2192	S[1528]	7860	-325
2193	S[1529]	7872	-420
2194	S[1530]	7884	-515
2195	S[1531]	7896	-325
2196	S[1532]	7908	-420
2197	S[1533]	7920	-515
2198	S[1534]	7932	-325
2199	S[1535]	7944	-420
2200	S[1536]	7956	-515
2201	S[1537]	7968	-325
2202	S[1538]	7980	-420

Pad	Name	X	Y
2203	S[1539]	7992	-515
2204	S[1540]	8004	-325
2205	S[1541]	8016	-420
2206	S[1542]	8028	-515
2207	S[1543]	8040	-325
2208	S[1544]	8052	-420
2209	S[1545]	8064	-515
2210	S[1546]	8076	-325
2211	S[1547]	8088	-420
2212	S[1548]	8100	-515
2213	S[1549]	8112	-325
2214	S[1550]	8124	-420
2215	S[1551]	8136	-515
2216	S[1552]	8148	-325
2217	S[1553]	8160	-420
2218	S[1554]	8172	-515
2219	S[1555]	8184	-325
2220	S[1556]	8196	-420
2221	S[1557]	8208	-515
2222	S[1558]	8220	-325
2223	S[1559]	8232	-420
2224	S[1560]	8244	-515
2225	S[1561]	8256	-325
2226	S[1562]	8268	-420
2227	S[1563]	8280	-515
2228	S[1564]	8292	-325
2229	S[1565]	8304	-420
2230	S[1566]	8316	-515
2231	S[1567]	8328	-325
2232	S[1568]	8340	-420
2233	S[1569]	8352	-515
2234	S[1570]	8364	-325
2235	S[1571]	8376	-420
2236	S[1572]	8388	-515
2237	S[1573]	8400	-325
2238	S[1574]	8412	-420
2239	S[1575]	8424	-515
2240	S[1576]	8436	-325

Pad	Name	X	Y
2241	S[1577]	8448	-420
2242	S[1578]	8460	-515
2243	S[1579]	8472	-325
2244	S[1580]	8484	-420
2245	S[1581]	8496	-515
2246	S[1582]	8508	-325
2247	S[1583]	8520	-420
2248	S[1584]	8532	-515
2249	S[1585]	8544	-325
2250	S[1586]	8556	-420
2251	S[1587]	8568	-515
2252	S[1588]	8580	-325
2253	S[1589]	8592	-420
2254	S[1590]	8604	-515
2255	S[1591]	8616	-325
2256	S[1592]	8628	-420
2257	S[1593]	8640	-515
2258	S[1594]	8652	-325
2259	S[1595]	8664	-420
2260	S[1596]	8676	-515
2261	S[1597]	8688	-325
2262	S[1598]	8700	-420
2263	S[1599]	8712	-515
2264	S[1600]	8724	-325
2265	S[1601]	8736	-420
2266	S[1602]	8748	-515
2267	S[1603]	8760	-325
2268	S[1604]	8772	-420
2269	S[1605]	8784	-515
2270	S[1606]	8796	-325
2271	S[1607]	8808	-420
2272	S[1608]	8820	-515
2273	S[1609]	8832	-325
2274	S[1610]	8844	-420
2275	S[1611]	8856	-515
2276	S[1612]	8868	-325
2277	S[1613]	8880	-420
2278	S[1614]	8892	-515

Pad	Name	X	Y
2279	S[1615]	8904	-325
2280	S[1616]	8916	-420
2281	S[1617]	8928	-515
2282	S[1618]	8940	-325
2283	S[1619]	8952	-420
2284	S[1620]	8964	-515
2285	S[1621]	8976	-325
2286	S[1622]	8988	-420
2287	S[1623]	9000	-515
2288	S[1624]	9012	-325
2289	S[1625]	9024	-420
2290	S[1626]	9036	-515
2291	S[1627]	9048	-325
2292	S[1628]	9060	-420
2293	S[1629]	9072	-515
2294	S[1630]	9084	-325
2295	S[1631]	9096	-420
2296	S[1632]	9108	-515
2297	S[1633]	9120	-325
2298	S[1634]	9132	-420
2299	S[1635]	9144	-515
2300	S[1636]	9156	-325
2301	S[1637]	9168	-420
2302	S[1638]	9180	-515
2303	S[1639]	9192	-325
2304	S[1640]	9204	-420
2305	S[1641]	9216	-515
2306	S[1642]	9228	-325
2307	S[1643]	9240	-420
2308	S[1644]	9252	-515
2309	S[1645]	9264	-325
2310	S[1646]	9276	-420
2311	S[1647]	9288	-515
2312	S[1648]	9300	-325
2313	S[1649]	9312	-420
2314	S[1650]	9324	-515
2315	S[1651]	9336	-325
2316	S[1652]	9348	-420

Pad	Name	X	Y
2317	S[1653]	9360	-515
2318	S[1654]	9372	-325
2319	S[1655]	9384	-420
2320	S[1656]	9396	-515
2321	S[1657]	9408	-325
2322	S[1658]	9420	-420
2323	S[1659]	9432	-515
2324	S[1660]	9444	-325
2325	S[1661]	9456	-420
2326	S[1662]	9468	-515
2327	S[1663]	9480	-325
2328	S[1664]	9492	-420
2329	S[1665]	9504	-515
2330	S[1666]	9516	-325
2331	S[1667]	9528	-420
2332	S[1668]	9540	-515
2333	S[1669]	9552	-325
2334	S[1670]	9564	-420
2335	S[1671]	9576	-515
2336	S[1672]	9588	-325
2337	S[1673]	9600	-420
2338	S[1674]	9612	-515
2339	S[1675]	9624	-325
2340	S[1676]	9636	-420
2341	S[1677]	9648	-515
2342	S[1678]	9660	-325
2343	S[1679]	9672	-420
2344	S[1680]	9684	-515
2345	S[1681]	9696	-325
2346	S[1682]	9708	-420
2347	S[1683]	9720	-515
2348	S[1684]	9732	-325
2349	S[1685]	9744	-420
2350	S[1686]	9756	-515
2351	S[1687]	9768	-325
2352	S[1688]	9780	-420
2353	S[1689]	9792	-515
2354	S[1690]	9804	-325

Pad	Name	X	Y
2355	S[1691]	9816	-420
2356	S[1692]	9828	-515
2357	S[1693]	9840	-325
2358	S[1694]	9852	-420
2359	S[1695]	9864	-515
2360	S[1696]	9876	-325
2361	S[1697]	9888	-420
2362	S[1698]	9900	-515
2363	S[1699]	9912	-325
2364	S[1700]	9924	-420
2365	S[1701]	9936	-515
2366	S[1702]	9948	-325
2367	S[1703]	9960	-420
2368	S[1704]	9972	-515
2369	S[1705]	9984	-325
2370	S[1706]	9996	-420
2371	S[1707]	10008	-515
2372	S[1708]	10020	-325
2373	S[1709]	10032	-420
2374	S[1710]	10044	-515
2375	S[1711]	10056	-325
2376	S[1712]	10068	-420
2377	S[1713]	10080	-515
2378	S[1714]	10092	-325
2379	S[1715]	10104	-420
2380	S[1716]	10116	-515
2381	S[1717]	10128	-325
2382	S[1718]	10140	-420
2383	S[1719]	10152	-515
2384	S[1720]	10164	-325
2385	S[1721]	10176	-420
2386	S[1722]	10188	-515
2387	S[1723]	10200	-325
2388	S[1724]	10212	-420
2389	S[1725]	10224	-515
2390	S[1726]	10236	-325
2391	S[1727]	10248	-420
2392	S[1728]	10260	-515

Pad	Name	X	Y
2393	S[1729]	10272	-325
2394	S[1730]	10284	-420
2395	S[1731]	10296	-515
2396	S[1732]	10308	-325
2397	S[1733]	10320	-420
2398	S[1734]	10332	-515
2399	S[1735]	10344	-325
2400	S[1736]	10356	-420
2401	S[1737]	10368	-515
2402	S[1738]	10380	-325
2403	S[1739]	10392	-420
2404	S[1740]	10404	-515
2405	S[1741]	10416	-325
2406	S[1742]	10428	-420
2407	S[1743]	10440	-515
2408	S[1744]	10452	-325
2409	S[1745]	10464	-420
2410	S[1746]	10476	-515
2411	S[1747]	10488	-325
2412	S[1748]	10500	-420
2413	S[1749]	10512	-515
2414	S[1750]	10524	-325
2415	S[1751]	10536	-420
2416	S[1752]	10548	-515
2417	S[1753]	10560	-325
2418	S[1754]	10572	-420
2419	S[1755]	10584	-515
2420	S[1756]	10596	-325
2421	S[1757]	10608	-420
2422	S[1758]	10620	-515
2423	S[1759]	10632	-325
2424	S[1760]	10644	-420
2425	S[1761]	10656	-515
2426	S[1762]	10668	-325
2427	S[1763]	10680	-420
2428	S[1764]	10692	-515
2429	S[1765]	10704	-325
2430	S[1766]	10716	-420

Pad	Name	X	Y
2431	S[1767]	10728	-515
2432	S[1768]	10740	-325
2433	S[1769]	10752	-420
2434	S[1770]	10764	-515
2435	S[1771]	10776	-325
2436	S[1772]	10788	-420
2437	S[1773]	10800	-515
2438	S[1774]	10812	-325
2439	S[1775]	10824	-420
2440	S[1776]	10836	-515
2441	S[1777]	10848	-325
2442	S[1778]	10860	-420
2443	S[1779]	10872	-515
2444	S[1780]	10884	-325
2445	S[1781]	10896	-420
2446	S[1782]	10908	-515
2447	S[1783]	10920	-325
2448	S[1784]	10932	-420
2449	S[1785]	10944	-515
2450	S[1786]	10956	-325
2451	S[1787]	10968	-420
2452	S[1788]	10980	-515
2453	S[1789]	10992	-325
2454	S[1790]	11004	-420
2455	S[1791]	11016	-515
2456	S[1792]	11028	-325
2457	S[1793]	11040	-420
2458	S[1794]	11052	-515
2459	S[1795]	11064	-325
2460	S[1796]	11076	-420
2461	S[1797]	11088	-515
2462	S[1798]	11100	-325
2463	S[1799]	11112	-420
2464	S[1800]	11124	-515
2465	S[1801]	11136	-325
2466	S[1802]	11148	-420
2467	S[1803]	11160	-515
2468	S[1804]	11172	-325

Pad	Name	X	Y
2469	S[1805]	11184	-420
2470	S[1806]	11196	-515
2471	S[1807]	11208	-325
2472	S[1808]	11220	-420
2473	S[1809]	11232	-515
2474	S[1810]	11244	-325
2475	S[1811]	11256	-420
2476	S[1812]	11268	-515
2477	S[1813]	11280	-325
2478	S[1814]	11292	-420
2479	S[1815]	11304	-515
2480	S[1816]	11316	-325
2481	S[1817]	11328	-420
2482	S[1818]	11340	-515
2483	S[1819]	11352	-325
2484	S[1820]	11364	-420
2485	S[1821]	11376	-515
2486	S[1822]	11388	-325
2487	S[1823]	11400	-420
2488	S[1824]	11412	-515
2489	S[1825]	11424	-325
2490	S[1826]	11436	-420
2491	S[1827]	11448	-515
2492	S[1828]	11460	-325
2493	S[1829]	11472	-420
2494	S[1830]	11484	-515
2495	S[1831]	11496	-325
2496	S[1832]	11508	-420
2497	S[1833]	11520	-515
2498	S[1834]	11532	-325
2499	S[1835]	11544	-420
2500	S[1836]	11556	-515
2501	S[1837]	11568	-325
2502	S[1838]	11580	-420
2503	S[1839]	11592	-515
2504	S[1840]	11604	-325
2505	S[1841]	11616	-420
2506	S[1842]	11628	-515

Pad	Name	X	Y
2507	S[1843]	11640	-325
2508	S[1844]	11652	-420
2509	S[1845]	11664	-515
2510	S[1846]	11676	-325
2511	S[1847]	11688	-420
2512	S[1848]	11700	-515
2513	S[1849]	11712	-325
2514	S[1850]	11724	-420
2515	S[1851]	11736	-515
2516	S[1852]	11748	-325
2517	S[1853]	11760	-420
2518	S[1854]	11772	-515
2519	S[1855]	11784	-325
2520	S[1856]	11796	-420
2521	S[1857]	11808	-515
2522	S[1858]	11820	-325
2523	S[1859]	11832	-420
2524	S[1860]	11844	-515
2525	S[1861]	11856	-325
2526	S[1862]	11868	-420
2527	S[1863]	11880	-515
2528	S[1864]	11892	-325
2529	S[1865]	11904	-420
2530	S[1866]	11916	-515
2531	S[1867]	11928	-325
2532	S[1868]	11940	-420
2533	S[1869]	11952	-515
2534	S[1870]	11964	-325
2535	S[1871]	11976	-420
2536	S[1872]	11988	-515
2537	S[1873]	12000	-325
2538	S[1874]	12012	-420
2539	S[1875]	12024	-515
2540	S[1876]	12036	-325
2541	S[1877]	12048	-420
2542	S[1878]	12060	-515
2543	S[1879]	12072	-325
2544	S[1880]	12084	-420

Pad	Name	X	Y
2545	S[1881]	12096	-515
2546	S[1882]	12108	-325
2547	S[1883]	12120	-420
2548	S[1884]	12132	-515
2549	S[1885]	12144	-325
2550	S[1886]	12156	-420
2551	S[1887]	12168	-515
2552	S[1888]	12180	-325
2553	S[1889]	12192	-420
2554	S[1890]	12204	-515
2555	S[1891]	12216	-325
2556	S[1892]	12228	-420
2557	S[1893]	12240	-515
2558	S[1894]	12252	-325
2559	S[1895]	12264	-420
2560	S[1896]	12276	-515
2561	S[1897]	12288	-325
2562	S[1898]	12300	-420
2563	S[1899]	12312	-515
2564	S[1900]	12324	-325
2565	S[1901]	12336	-420
2566	S[1902]	12348	-515
2567	S[1903]	12360	-325
2568	S[1904]	12372	-420
2569	S[1905]	12384	-515
2570	S[1906]	12396	-325
2571	S[1907]	12408	-420
2572	S[1908]	12420	-515
2573	S[1909]	12432	-325
2574	S[1910]	12444	-420
2575	S[1911]	12456	-515
2576	S[1912]	12468	-325
2577	S[1913]	12480	-420
2578	S[1914]	12492	-515
2579	S[1915]	12504	-325
2580	S[1916]	12516	-420
2581	S[1917]	12528	-515
2582	S[1918]	12540	-325

Pad	Name	X	Y
2583	S[1919]	12552	-420
2584	S[1920]	12564	-515
2585	S[1921]	12576	-325
2586	S[1922]	12588	-420
2587	VSSA	12600	-515
2588	VSSA	12612	-325
2589	VSSA	12624	-420
2590	VSSA	12636	-515
2591	VCOM_R	12648	-325
2592	VCOM_R	12660	-420
2593	VCOM_R	12672	-515
2594	VCOM_R	12684	-325
2595	VCOM_R	12696	-420
2596	VCOM_R	12708	-515
2597	VSSA	12720	-325
2598	VSSA	12732	-420
2599	VSSA	12744	-515
2600	VSSA	12756	-325
2601	VSSA	12768	-420
2602	VSSA	12780	-515
2603	VGH	12792	-325
2604	VGH	12804	-420
2605	VGH	12816	-515
2606	VGH	12828	-325
2607	VGH	12840	-420
2608	VGH	12852	-515
2609	GHV_R[20]	12864	-325
2610	GHV_R[20]	12876	-420
2611	GHV_R[20]	12888	-515
2612	GHV_R[19]	12900	-325
2613	GHV_R[19]	12912	-420
2614	GHV_R[19]	12924	-515
2615	GHV_R[18]	12936	-325
2616	GHV_R[18]	12948	-420
2617	GHV_R[18]	12960	-515
2618	GHV_R[17]	12972	-325
2619	GHV_R[17]	12984	-420
2620	GHV_R[17]	12996	-515

Pad	Name	X	Y
2621	GHV_R[16]	13008	-325
2622	GHV_R[16]	13020	-420
2623	GHV_R[16]	13032	-515
2624	GHV_R[15]	13044	-325
2625	GHV_R[15]	13056	-420
2626	GHV_R[15]	13068	-515
2627	GHV_R[14]	13080	-325
2628	GHV_R[14]	13092	-420
2629	GHV_R[14]	13104	-515
2630	GHV_R[13]	13116	-325
2631	GHV_R[13]	13128	-420
2632	GHV_R[13]	13140	-515
2633	GHV_R[12]	13152	-325
2634	GHV_R[12]	13164	-420
2635	GHV_R[12]	13176	-515
2636	GHV_R[11]	13188	-325
2637	GHV_R[11]	13200	-420
2638	GHV_R[11]	13212	-515
2639	GHV_R[10]	13224	-325
2640	GHV_R[10]	13236	-420
2641	GHV_R[10]	13248	-515
2642	GHV_R[9]	13260	-325
2643	GHV_R[9]	13272	-420
2644	GHV_R[9]	13284	-515
2645	VGL	13296	-325
2646	VGL	13308	-420
2647	VGL	13320	-515
2648	VGL	13332	-325
2649	VGL	13344	-420
2650	VGL	13356	-515
2651	GHV_R[8]	13368	-325
2652	GHV_R[8]	13380	-420
2653	GHV_R[8]	13392	-515
2654	GHV_R[7]	13404	-325
2655	GHV_R[7]	13416	-420
2656	GHV_R[7]	13428	-515
2657	GHV_R[6]	13440	-325
2658	GHV_R[6]	13452	-420

Pad	Name	X	Y
2659	GHV_R[6]	13464	-515
2660	GHV_R[5]	13476	-325
2661	GHV_R[5]	13488	-420
2662	GHV_R[5]	13500	-515
2663	GHV_R[4]	13512	-325
2664	GHV_R[4]	13524	-420
2665	GHV_R[4]	13536	-515
2666	GHV_R[3]	13548	-325
2667	GHV_R[3]	13560	-420
2668	GHV_R[3]	13572	-515
2669	GHV_R[2]	13584	-325
2670	GHV_R[2]	13596	-420
2671	GHV_R[2]	13608	-515
2672	GHV_R[1]	13620	-325
2673	GHV_R[1]	13632	-420
2674	GHV_R[1]	13644	-515
2675	DUMMY	13656	-325
2676	DUMMY	13668	-420
2677	DUMMY	13680	-515
2678	Dummy	13825	-480
2679	TEST_VR	13825	-420
2680	GPO_R[13]	13825	-360
2681	GPO_R[12]	13825	-300
2682	GPO_R[11]	13825	-240
2683	GPO_R[10]	13825	-180
2684	GPO_R[9]	13825	-120
2685	GPO_R[8]	13825	-60
2686	GPO_R[7]	13825	0
2687	GPO_R[6]	13825	60
2688	GPO_R[5]	13825	120
2689	GPO_R[4]	13825	180
2690	GPO_R[3]	13825	240
2691	GPO_R[2]	13825	300
2692	GPO_R[1]	13825	360
	Alignment Mark_R	13822	497
	Alignment Mark_L	-13822	497

13. ORDERING INFORMATION

Part.No	Package
Chip Name – Gx	G: means COG x: means chip thickness 6 = 200um

14. REVISION HISTORY

Version	Date	Description
V0.1	2024/02/06	New setup
V0.2	2024/03/06	1. Update 7.1 Power on Sequence at p193-p195. 2. Update 12.1 COG Outline at p214.
V0.3	2024/05/07	1. Update 2. FEATURES at p7. 2. Update 9.1 Source Driver and LVDS at p201. 3. Update 12.1 COG Outline at p214.