FT5x26

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

The FT5X26 is single-chip capacitive touch panel controllers with built-in enhanced Micro-controller unit (MCU).It provides the benefits of full screen common mode scan technology, fast response time and high level of accuracy. It can drive capacitive type touch panel with up to 52 driving and 30 sensing lines.

FEATURES

- Mutual Capacitive Sensing Techniques
- Full Screen Common Mode Scan Techniques
- True Multi-touch up to 10 Points of absolute X and Y Coordinates
- High immunity to RF and power Interferences
- 5626 Supports up to 40TX + 27 RX
- 5726 Supports up to 42TX + 30 RX
- 5826S Supports up to 52TX + 30 RX
- Support up to 10 fingers
- High immunity to inductive power noise
- Automatic mode switching (Active, Monitor, Sleep)
- Support >100Hz sampling rate
- Auto-calibration
- Support IIC (up to 400kbits/sec) interface
- Power
  - 2.7 to 3.6V Operating Voltage
  - IOVCC supports from 1.71V to 3.6V
- Built-in 64KB(000)/128KB(003) Flash
- Single Channel(TX or RX)resistance: Up to100K Ω
- Single Channel (transmit / receive) Capacitance: 40pF
- Features “short I/O ” testing for sense pins
- 12-Bit ADC Accuracy
- 3 Operating Modes
  - Active
  - Monitor
  - Hibernation
- Operating Temperature Range: -40°C to +85°C
- Package:
  - QFN88L 10x10x0.8mm, 0.4mm/pitch
  - BGA100 5x9x0.6mm, 0.6mm/pitch

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1 OVERVIEW

1.1 Typical Applications

FT5X26 accommodates a wide range of applications with a set of buttons up to a 2D touch sensing device; their typical applications are listed below.

- Tablet
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices

FT5X26 support Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended for Smart Phone TP Size (16:9)	Flash Size
FT5626	QFN 88L 10x10x0.8mm Pitch =0.4mm	40	27	67	≦10.1", Sensor Pitch:6mm	64KB
FT5726	QFN 88L 10x10x0.8mm Pitch =0.4mm	42	30	72	≦ 11.6", Sensor Pitch:6mm	64KB(-000) 128KB(-003)
FT5826S	BGA 100 5x9x0.6mm Pitch =0.6mm	52	30	82	≦ 13.3", Sensor Pitch:6mm	64KB

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT5X26.

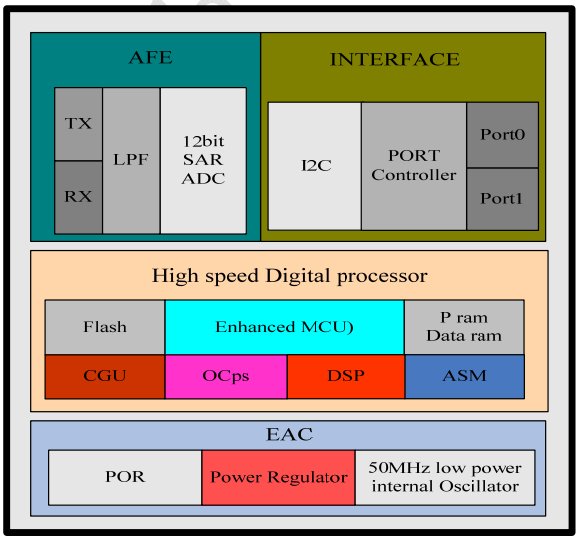


Figure 2-1 System Architecture Diagram

The FT5X26 is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit

(TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU with DSP accelerator

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is implemented to store programs and some key parameters.
Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches reliably and efficiently. Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip. The port is also use to wake up the FT5X26 from the Hibernate mode.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply
- Power On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.

2.2 MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

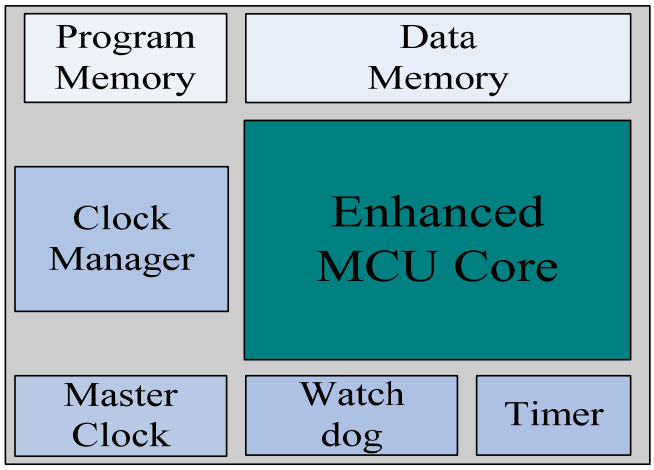


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT5X26 offers following three modes:

- **Active Mode**

When in this mode, FT5X26 actively scans the panel. The default scan rate is 100 frames per second. The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In this mode, FT5X26 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5X26 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Hibernate Mode**

In this mode, the chip is set in a power down mode. It shall only respond to the “RESET” signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.4 Host Interface

Figure 2-3 shows the interface between a host processor and FT5X26. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5X26 to the Host
- Reset Signal from the Host to FT5X26

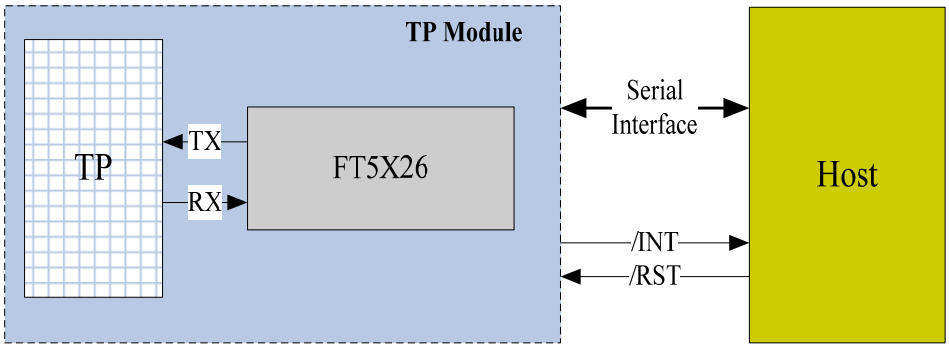


Figure 2-3 Host Interface Diagram

The serial interface of FT5X26 is I2C. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5X26 to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT5X26 from the Hibernate mode. After resetting, FT5X26 shall enter the Active mode.

2.5 Serial Interface

FT5X26 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

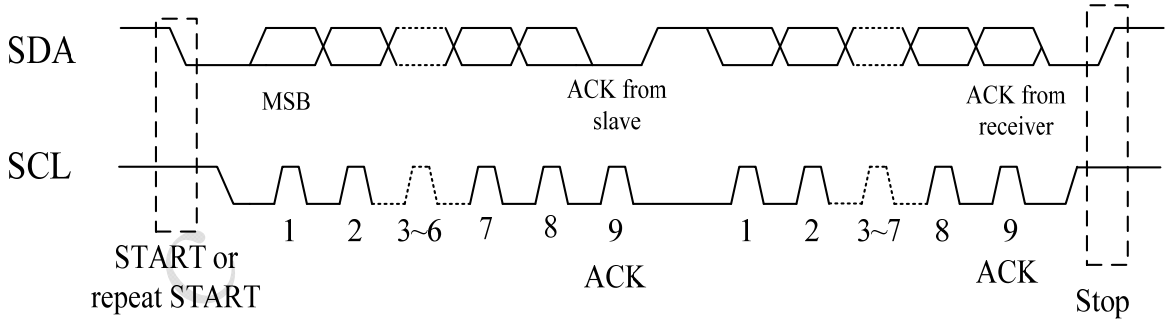


Figure 2-4 I2C Serial Data Transfer Format

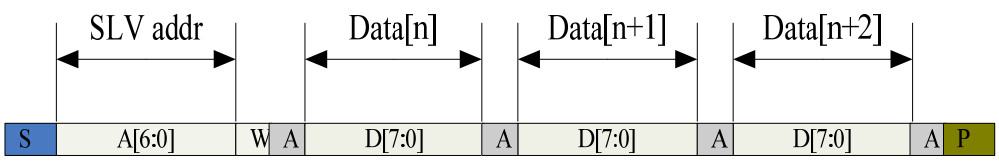


Figure 2-5 I2C master write, slave read

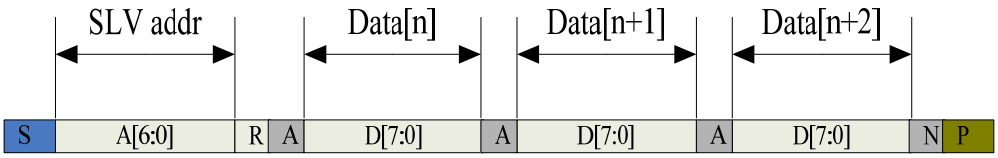


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDD3 – VSS	2.7 ~ +3.6	V	1, 3
I/O Digital Voltage	IOVCC	1.71~ +3.6	V	1
Operating Temperature	Topr	-40 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

Notes

1. If used beyond the absolute maximum ratings, FT5X26 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDD (high) ≥VSS (low)

3.2 DC Characteristics

Table 3-2 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC+0.3	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=3mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOL=4.5mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA	Vin=0~VDD3	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDD3 = 3V Ta=25℃	--	25	--	
Current consumption （Monitor mode）	Imon	mA	VDD3 = 3V Ta=25℃	--	0.54	--	
Current consumption （Sleep mode）	Islp	uA	VDD3 = 3V Ta=25℃	--	37	--	
Step-up output voltage	VDD5	V	VDD3= 2.8V		0.25		
Power Supply voltage	VDD3	V		2.7	--	3.6	

Notes: This sample data is intended for design guidance only. Values shown are typical for a 40Tx × 27Rx sensor configured at 80 Hz report rate. Actual current will depend on the particular sensor design and firmware options.

3.3 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V; Ta=25℃	49	50	51	

Table 3-3 AC Characteristics of TX & RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	
TX output rise time	Ttxr		--	210	--	nS	
TX output fall time	Ttxf		--	210	--	nS	
RX input voltage	Trxi		1.2	--	1.6	V	

3.4 I/O Ports Circuits

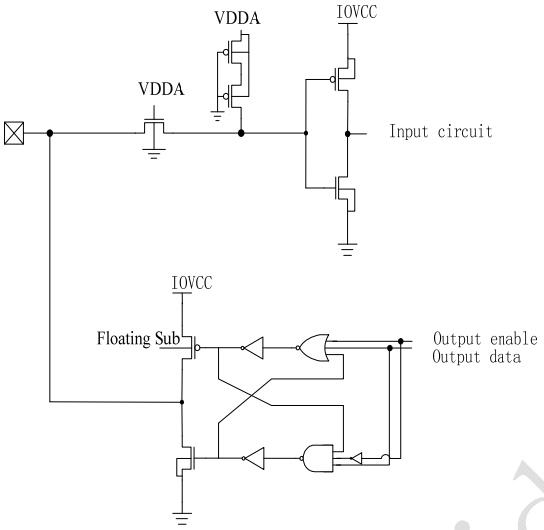


Figure 3-1 General Purpose *In/Out Port Circuit*.

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

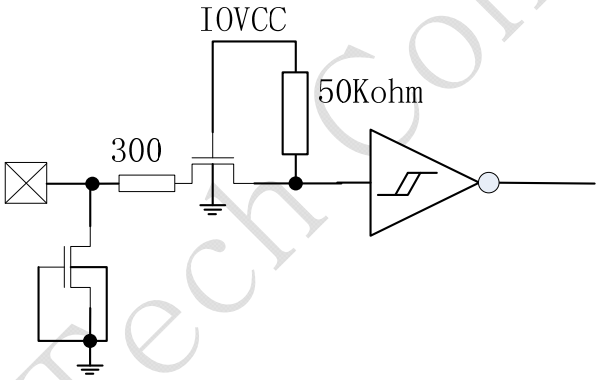


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

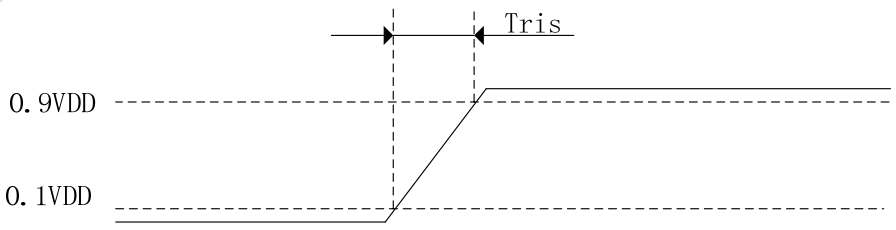


Figure 3-3 Power on time

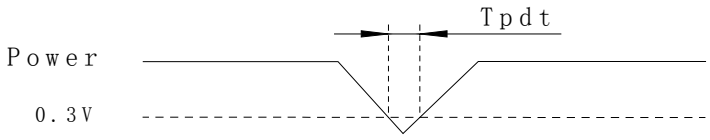


Figure 3-4 Power Cycle requirement

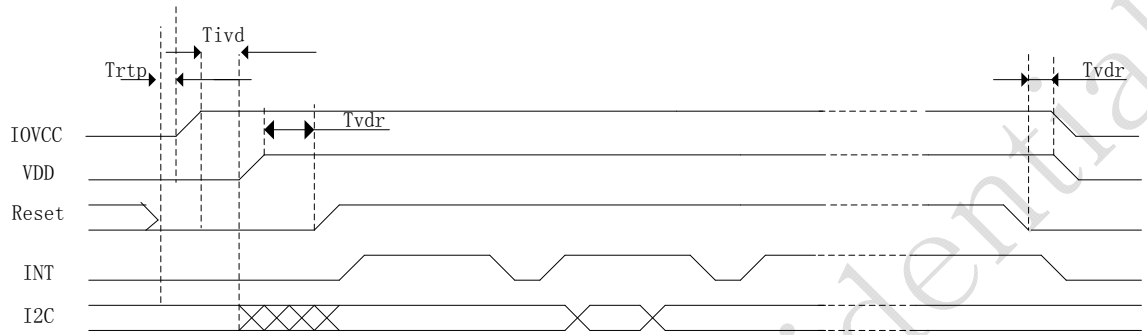


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

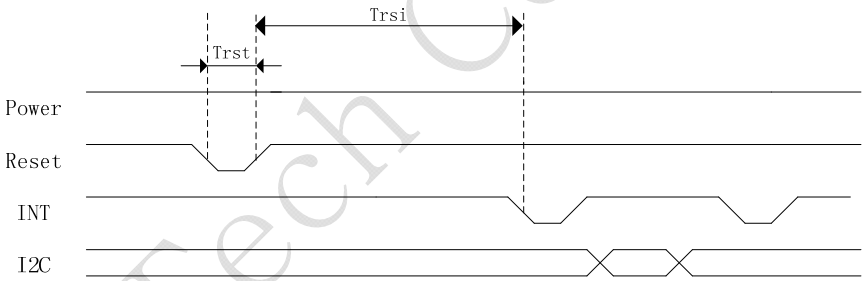


Figure 3-6 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tivd	Delay time of VDD powering on after IOVCC	10		μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

4 PIN CONFIGURATIONS

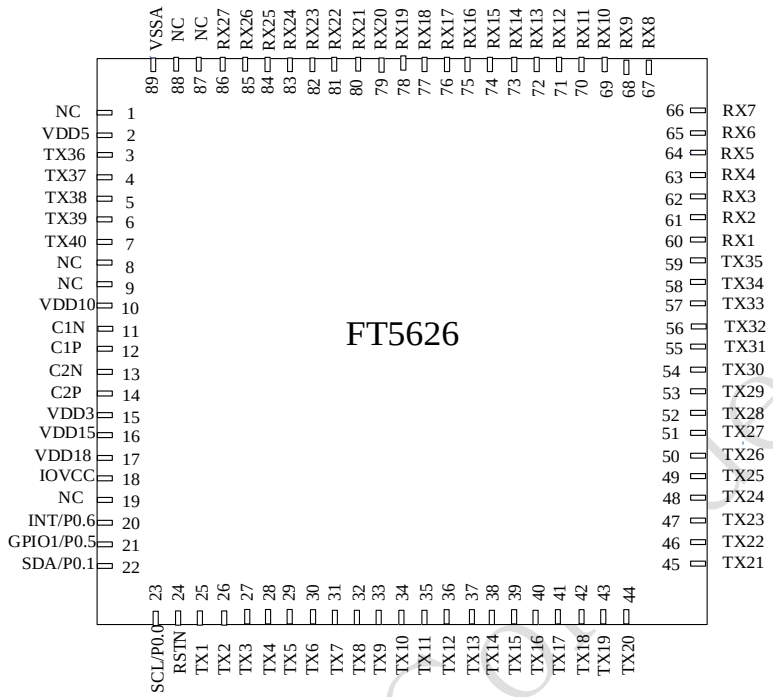
Pin List of FT5X26

Table 4-1 Pin Definition

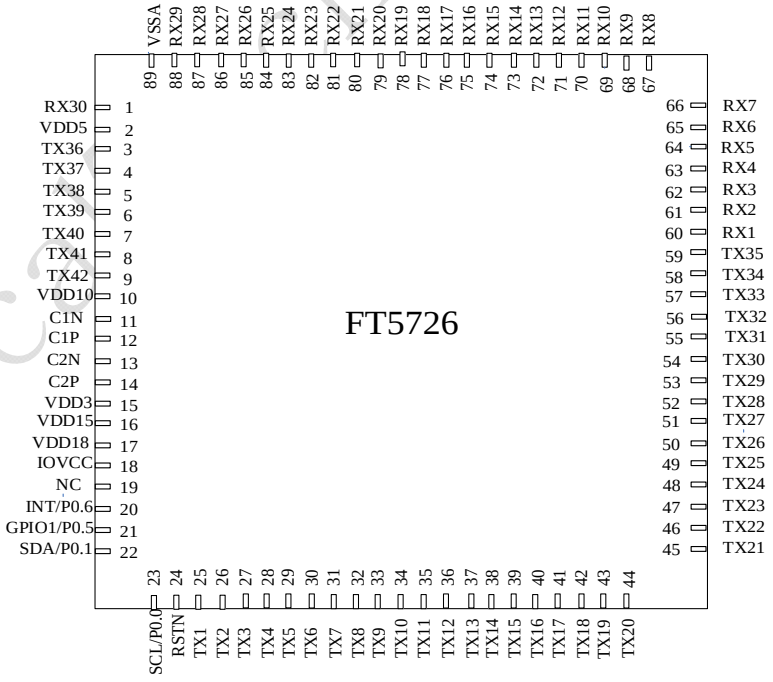
Name	Pin/Ball No.			Type	Description
	5626	5726	5826		
RX30		1	D3	I	Receiver input pins
RX29		88	D2	I	Receiver input pins
RX28		87	D1	I	Receiver input pins
RX27	86	86	E3	I	Receiver input pins
RX26	85	85	E2	I	Receiver input pins
RX25	84	84	E1	I	Receiver input pins
RX24	83	83	F3	I	Receiver input pins
RX23	82	82	F2	I	Receiver input pins
RX22	81	81	F1	I	Receiver input pins
RX21	80	80	G3	I	Receiver input pins
RX20	79	79	G2	I	Receiver input pins
RX19	78	78	G1	I	Receiver input pins
RX18	77	77	H3	I	Receiver input pins
RX17	76	76	H2	I	Receiver input pins
RX16	75	75	H1	I	Receiver input pins
RX15	74	74	J3	I	Receiver input pins
RX14	73	73	J2	I	Receiver input pins
RX13	72	72	J1	I	Receiver input pins
RX12	71	71	K3	I	Receiver input pins
RX11	70	70	K2	I	Receiver input pins
RX10	69	69	K1	I	Receiver input pins
RX9	68	68	L3	I	Receiver input pins
RX8	67	67	L2	I	Receiver input pins
RX7	66	66	L1	I	Receiver input pins
RX6	65	65	M3	I	Receiver input pins
RX5	64	64	M2	I	Receiver input pins
RX4	63	63	M1	I	Receiver input pins
RX3	62	62	N3	I	Receiver input pins
RX2	61	61	N2	I	Receiver input pins
RX1	60	60	N1	I	Receiver input pins
TX52			A8	O	Transmit output pin
TX51			A7	O	Transmit output pin
TX50			A6	O	Transmit output pin
TX49			A5	O	Transmit output pin
TX48			A4	O	Transmit output pin
TX47			A3	O	Transmit output pin

TX46			A2	O	Transmit output pin
TX45			A1	O	Transmit output pin
TX44			B8	O	Transmit output pin
TX43			B7	O	Transmit output pin
TX42	7	9	B6	O	Transmit output pin
TX41	7	8	B5	O	Transmit output pin
TX40	7	7	B4	O	Transmit output pin
TX39	6	6	B3	O	Transmit output pin
TX38	5	5	B2	O	Transmit output pin
TX37	4	4	B1	O	Transmit output pin
TX36	3	3	C8	O	Transmit output pin
TX35	59	59	C7	O	Transmit output pin
TX34	58	58	C6	O	Transmit output pin
TX33	57	57	C5	O	Transmit output pin
TX32	56	56	C4	O	Transmit output pin
TX31	55	55	C3	O	Transmit output pin
TX30	54	54	C2	O	Transmit output pin
TX29	53	53	C1	O	Transmit output pin
TX28	52	52	D8	O	Transmit output pin
TX27	51	51	D7	O	Transmit output pin
TX26	50	50	D6	O	Transmit output pin
TX25	49	49	D5	O	Transmit output pin
TX24	48	48	D4	O	Transmit output pin
TX23	47	47	E8	O	Transmit output pin
TX22	46	46	E7	O	Transmit output pin
TX21	45	45	E6	O	Transmit output pin
TX20	44	44	E5	O	Transmit output pin
TX19	43	43	E4	O	Transmit output pin
TX18	42	42	F8	O	Transmit output pin
TX17	41	41	F7	O	Transmit output pin
TX16	40	40	F6	O	Transmit output pin
TX15	39	39	F5	O	Transmit output pin
TX14	38	38	F4	O	Transmit output pin
TX13	37	37	G8	O	Transmit output pin
TX12	36	36	G7	O	Transmit output pin
TX11	35	35	G6	O	Transmit output pin
TX10	34	34	H8	O	Transmit output pin
TX9	33	33	H7	O	Transmit output pin
TX8	32	32	H6	O	Transmit output pin
TX7	31	31	J8	O	Transmit output pin
TX6	30	30	J7	O	Transmit output pin
TX5	29	29	J6	O	Transmit output pin
TX4	28	28	J5	O	Transmit output pin
TX3	27	27	J4	O	Transmit output pin
TX2	26	26	K4	O	Transmit output pin
TX1	25	25	L4	O	Transmit output pin

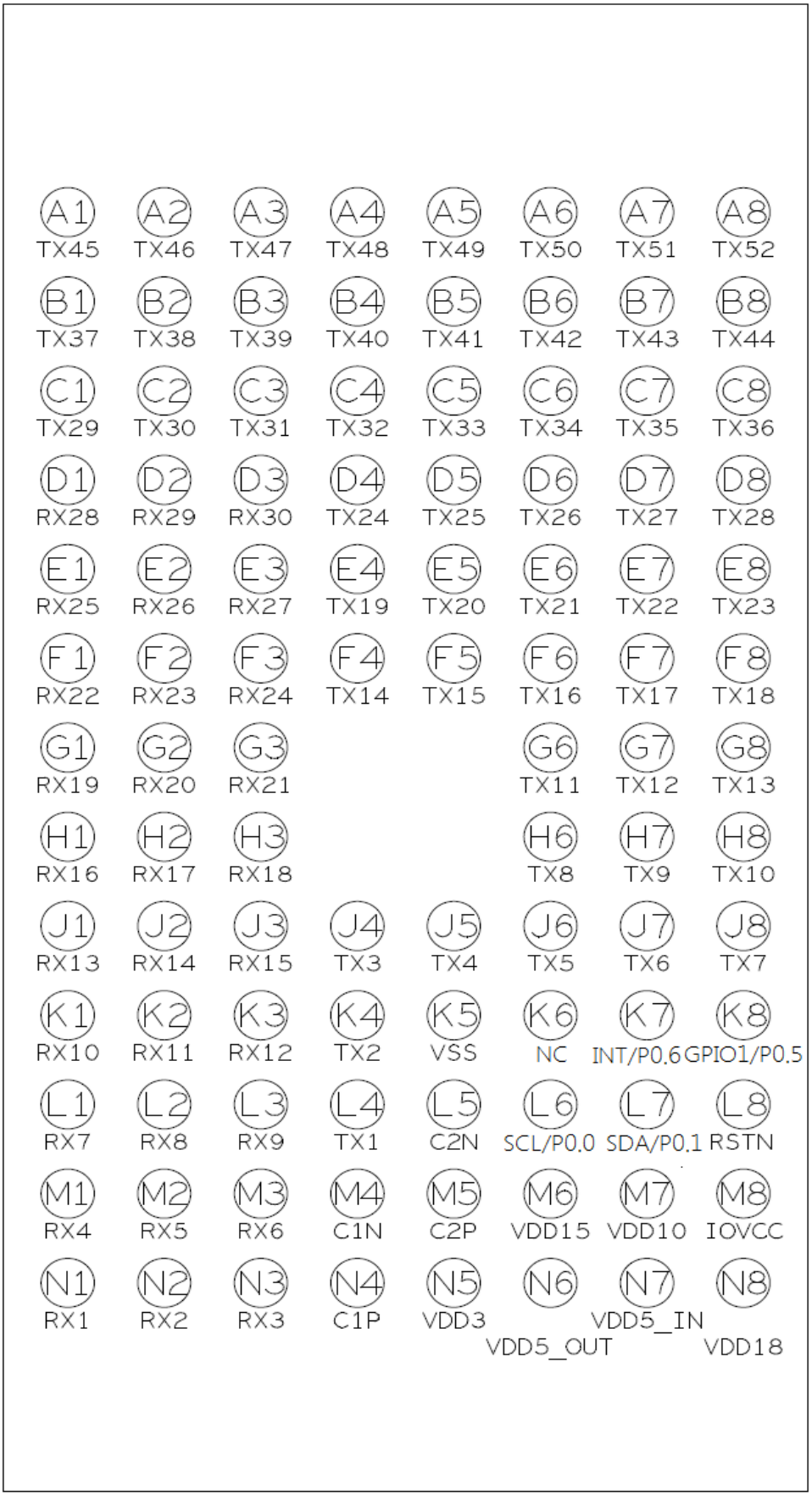
RSTN	24	24	L8	I	External Reset, Low is active
SCL/P0.0	23	23	L6	I/O	I2C clock input / General Purpose Input/Output port
SDA/P0.1	22	22	L7	I/O	I2C data input and output / General Purpose Input/Output port
GPIO1/P0.5	21	21	K8	I/O	General Purpose Input/Output port, Or EXT Interrupt
INT/P0.6	20	20	K7	I/O	Interrupt request to the host, Or Wakeup request from the host / General Purpose Input/Output port
NC	19	19	K6	NC	
IOVCC	18	18	M8	PWR	I/O power supply
VDD18	17	17	N8	PWR	digital power supply, requires external decoupling capacitor
VDD15	16	16	M6	PWR	digital power supply, requires external decoupling capacitor
VDD3	15	15	N5	PWR	chip power supply, requires external decoupling capacitor
C2P	14	14	M5		Positive terminal of CHP5 Flying CAP
C2N	13	13	L5		Negative terminal of CHP5 Flying CAP
C1P	12	12	N4		Positive terminal of CHP10 Flying CAP
C1N	11	11	M4		Negative terminal of CHP10 Flying CAP
VDD10	10	10	M7	PWR	charge pump 10V power supply, requires external decoupling capacitor
NC	9			NC	
NC	8			NC	
VDD5	2	2		PWR	charge pump 5V power supply, requires external decoupling capacitor
NC	1			NC	
VSS	89	89	K5	PWR	Analog ground
NC	88			NC	
NC	87			NC	
VDD5_IN			N7	PWR	charge pump 5V power supply, requires external decoupling capacitor
VDD5_OUT			N6	PWR	charge pump 5V power supply, requires external decoupling capacitor



FT5626 Package Diagram



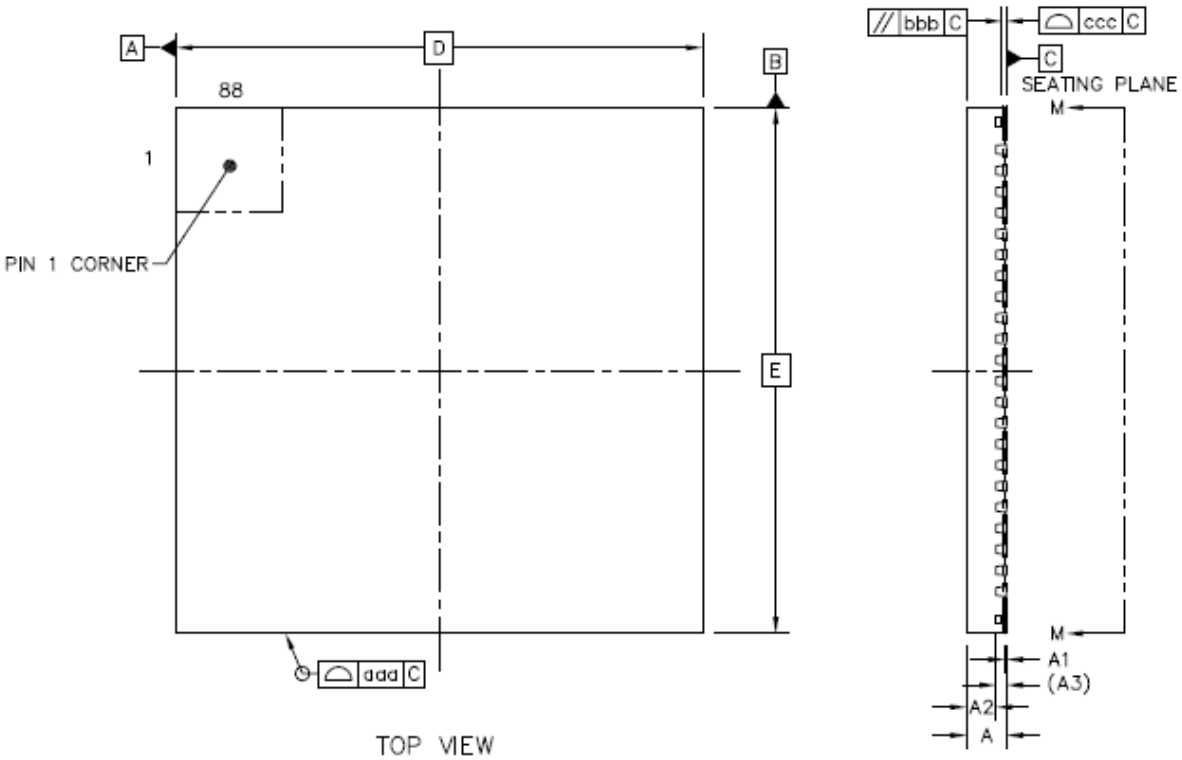
FT5726 Package Diagram

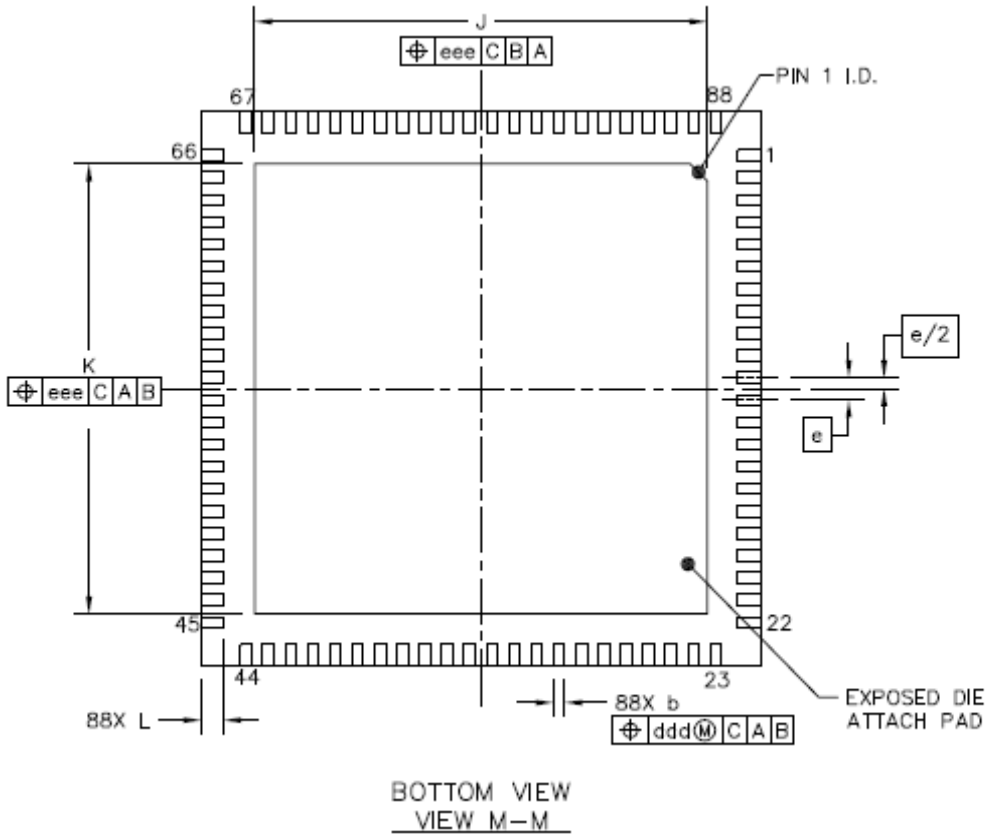


FT5826S Package Diagram

5 PACKAGE INFORMATION

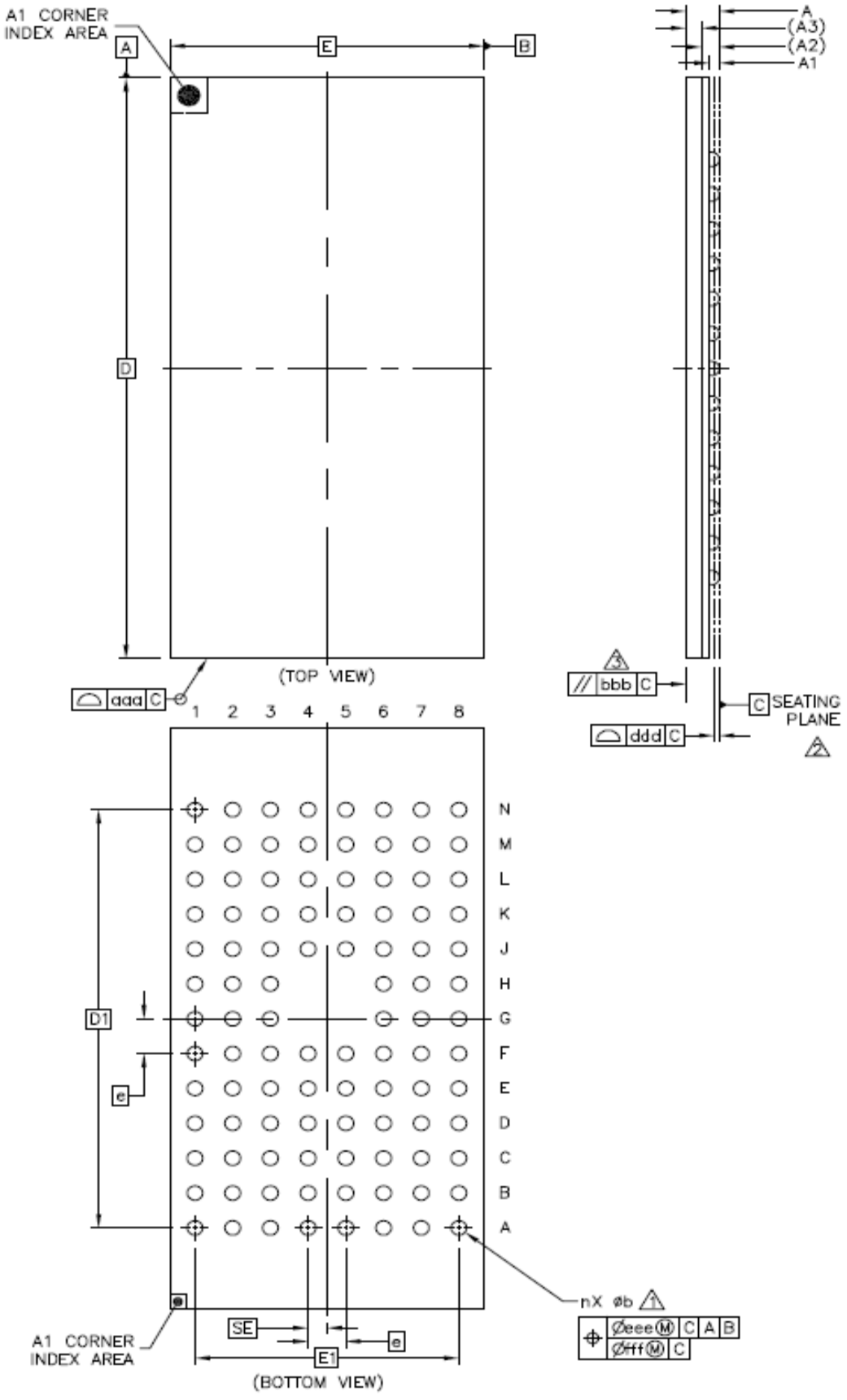
5.1 Package Information of QFN-10x10-88L Package





Item		Symbol	Millimeter		
			Min	Type	Max
Total Thickness		A	0.7	0.75	0.8
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	----	0.55	----
L/F Thickness		A3		0.203 REF	
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		10 BSC	
	Y	E		10 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	J	8	8.1	8.2
	Y	K	8	8.1	8.2
Lead Length		L	0.35	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Co Planarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

5.2 Package Information of BGA-5x9-100 Package



Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	---	---	0.6
Stand Off	A1	0.12	---	0.2
Substrate Thickness	A2	0.125 REF		
Mold Thickness	A3	0.25 REF		
Body Size	D	9 BSC		
	E	5 BSC		
Ball Diameter		0.25		
Ball Opening		0.25		
Ball width	b	0.2		0.3
Ball pitch	e	0.6 BSC		
Ball count	n	100		
Edge Ball Center to Center	D1	7.2 BSC		
	E1	4.2 BSC		
Body Center to Contact Ball	SD	---		
	SE	0.3 BSC		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Co Planarity	ddd	0.08		
Ball Offset(Package)	eee	0.15		
Ball Offset(Ball)	fff	0.08		

5.3 Order Information

Product Name	Package Type	# TX Pins	# RX Pins
FT5626	**QFN-88L**	**40**	**27**
FT5726-000/003	**QFN-88L**	**42**	**30**
FT5826S	**BGA-100**	**52**	**30**

Appendix: IC Revision history of FT5X26 Specification

Version	Change Items	Effective Date
1.0	1st Preliminary	21-Aug-15
1.1	Update Pin Description Update Table 4-1	9-Oct-15
1.2	Update Table 4-1	1-Nov-15
1.3	Update Table 3-2	31-Aug-16
1.4	Update FT5726-003	5-Aug-18

END OF DATASHEET