ILI2132

Single Chip Capacitive Touch Panel Controller

Data Sheet

(Preliminary)

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1. Introduction

ILI2132 is a high performance capacitive touch panel controller. It integrates USB, I2C, SPI interfaces and Flash memory into a BGA-90 package. ILI2132 has 57 touch sensor channels, it can support out-cell and on-cell touch sensors.

With ILITEK's unique driving technology and algorithm, ILI2132 has excellent noise immunity ability and acheave high signal to noise ratio. For noise immunity, ILI2132 can support IEC-61000-4-6 CS 10Vrms requirement. ILI2132 is an optimal touch solution for Tablet, Appliance, HMI, POS kind of applications.

2. Features

2.1 Driving and Sensing Channels for Capacitive Touch Panel

- 12 TX driving channels
- 29 RX sensing channels
- 16 TRX channels
- 1 Guarding (GR) channel
- Multiple virtual key and extra HW key (Mutual type, 1Tx and 3Rx)
- Integrated x5 AVDD_CP charge pump controller and support 10V driving voltage for driving heavy RC loading touch panel.
- Support mutual-cap and self-cap driving/sensing technology
- Support G/G (DITO), G/G (SITO), OGS, GFF, GF2, FFF and On-Cell touch panel stack up (approved by ILITEK or ILITEK qualified touch panel maker)
- Support both of direct bonding and air bonding with TFT and IPS LCD module (LCM)
- Support Ag nano wire (AgNW), metal mesh (copper or Ag), printing copper and ITO conductive material
- Support Diamond and proprietary sensor patterns (approved by ILITEK or ILITEK qualified touch panel maker)
- Support PET and glass cover lens
  - Plastic 0.2mm to 4mm, depends on panel size, touch size, panel stack up and performance requirements
  - Glass 0.4mm to 8mm, depends on panel size, touch size, panel stack up and performance requirements

2.2 Host Interface

- I2C
  - Support 100kHz standard mode and 400kHz fast mode clock rate
  - I2C slave clock stretching function
  - Support Windows HID over I2C protocol

- USB
  - Support USB 2.0/1.1 specification
  - Up to 12Mbps Full Speed and 1.5Mbps Low Speed data transfer rate
  - Support Windows HID over USB protocol (both Bootloader and Application mode)

2.3 Reset
- Support chip enable/disable input
- Support power on reset (POR) function
- Support low voltage detection (LVD) function

2.4 Power Supply
- Input voltage for Analog (AVDD_CP) and Digital (PVDD), nominal 3.3V
- On-chip 1.2V regulator output for Digital core (VDD12), nominal 1.2V
- On-chip X2 charge pump controller output (PVDD_MVCP), nominal 2*AVDD_CP
- On-chip X7 charge pump controller output (PVDD_HVCP)
- On-chip programmingable MV regulator output for internal Analog circuit (AVDD)
- On-chip X5 charge pump controller and regulator output (HVDD), nominal 10V

2.5 General Purpose I/O (GPIO)
- 4.9V general purpose I/O, up to 30 pin (Multi-function with Rx channel and GR)

2.6 Package
- 90-pin, BGA-90, 6 × 6 × 1.2 mm, pitch 0.5 mm

2.7 Operating Temperature
- -40℃ to +85℃

2.8 Storage temperature
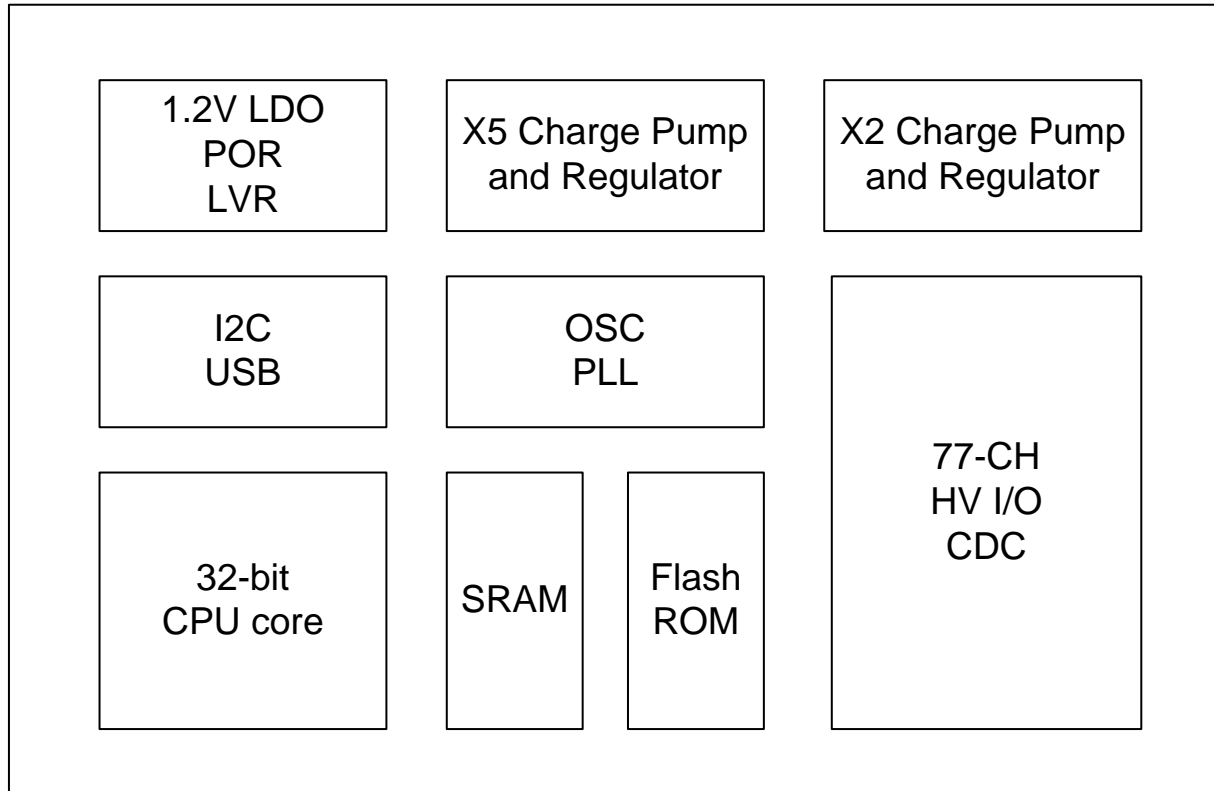- -55~125°C

3. Device Overview

3.1. Block Diagram

Figure 1. ILI2132 Block Diagram

3.2. Ball Configuration

3.2.1. BGA-90 (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	CN_MV	AVDD_CP	HVDD	PVDD	DP	XIN		GPIO2	GPIO0	TX0	TX2
B	CP_MV	PVSS_HVCP	PVDD_HVCP	VDD12	DM	XOUT		GPIO3	GOIP1	TX1	TX4
C	PVDD_MVCP	PVSS_MVCP			VBUS	VSS	SDA/RXD	SCL	AVSS	TX3	TX6
D	AVDD		CHIPEN	INT/TXD					TX11	TX5	TX8
E	GR	AVSS			RX_KEY0		TX_KEY		TX7	TX9	TX10
F	RX0	RX1			RX_KEY1	RX_KEY2				TRX1	TRX0
G	RX2	RX3	RX4							TRX3	TRX2
H	RX5	RX6	RX7				AVSS		TRX15	TRX5	TRX4
J	RX8	RX9	RX13	RX17	RX20	RX23	RX26		TRX14	TRX7	TRX6
K	RX10	RX11	RX15	RX18	RX21	RX24	RX27		TRX13	TRX8	TRX9
L	RX12	RX14	RX16	RX19	RX22	RX25	RX28		TRX12	TRX11	TRX10

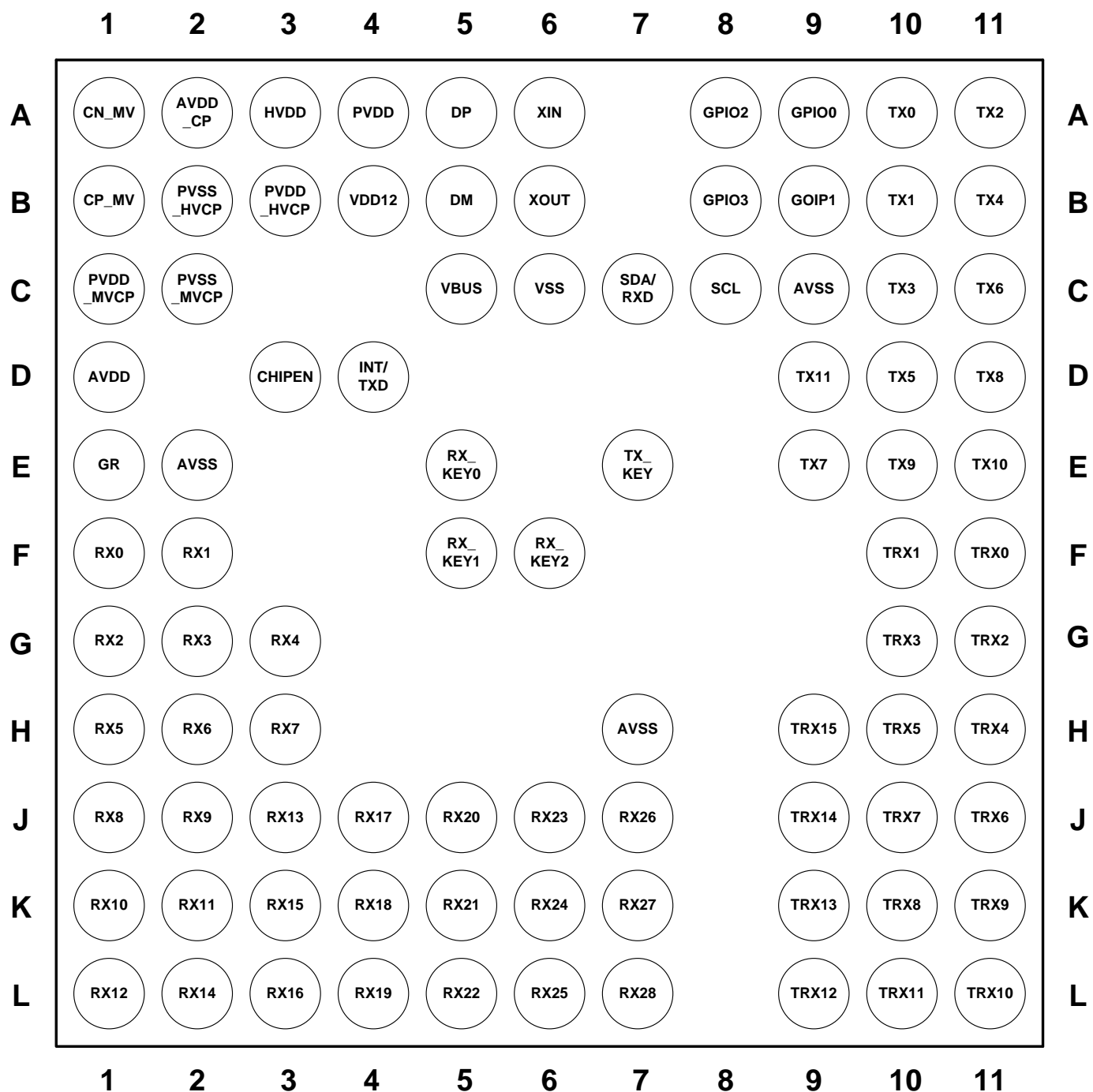**Figure 2. ILI2132 Schematic Symbol**

3.2.2. Pin Definition

Ball No.	Pin Name.	Type	Description	If Unused...
A1	CN_MV	P	Fly capacitor output of On-chip AVDD_CP x2 charge pump controller. Connect a 2.2uF/10V/X5R fly capacitor to CP_MV.	--
A2	AVDD_CP	I	Input power supply, typical 3.3V. Connect to a 1uF/10V/X5R bypass capacitor.	--
A3	HVDD	P	Input power supply for TX driving channel. Connect to a 2.2uF/25V/X5R bypass capacitor. HVDD internal mode: On-chip programmingable HV regulator output. Output Level : 8V to 10 V External mode : Input Level : 10V to 25V	--
A4	PVDD	P	Input power supply, typical 3.3V. Connect to a 1uF/10V/X5R bypass capacitor.	--
A5	DP	I/O	USB Mode: Data plus.	Leave open
A6	XIN	I/O	Sync 12 MHz clock input	Leave open
A8	GPIO2	I/O	It can be programming PAD_GPIO02 and SPI DI.	Leave open
A9	GPIO0	I/O	It can be programming PAD_GPIO00 and SPI CLK.	Leave open
A10	TX0	I/O	TX driving channel	Leave open
A11	TX2	I/O	TX driving channel	Leave open
B1	CP_MV	P	Fly capacitor output of On-chip AVDD_CP x2 charge pump controller. Connect a 2.2uF/10V/X5R fly capacitor to CN_MV.	--
B2	PVSS_HVCP	P	HV charge pump ground	--
B3	PVDD_HVCP	P	On-chip X7 charge pump controller output. Connect to a 2.2uF/25V/X5R bypass capacitor.	--
B4	VDD12	P	On-chip 1.2V regulator output, typical 1.2V. Connect to a 1uF/10V/X5R bypass capacitor.	--
B5	DM	I/O	USB Mode: Data minus.	Leave open
B6	XOUT	I/O	NC	Leave open
B8	GPIO3	I/O	It can be programming PAD_GPIO03 and SPI DO.	Leave open
B9	GPIO1	I/O	It can be programming PAD_GPIO01 and SPI CS.	Leave open
B10	TX1	I/O	TX driving channel	Leave open
B11	TX4	I/O	TX driving channel	Leave open
C1	PVDD_MVCP	P	On-chip AVDD_CP x2 charge pump controller output. Connect to a 2.2uF/10V/X5R bypass capacitor.	--
C2	PVSS_MVCP	P	MV charge pump ground	--

Ball No.	Pin Name.	Type	Description	If Unused...
C5	VBUS	P	5V VBUS detection	Leave open
C6	VSS	P	Digital ground	--
C7	SDA	I/O	I2C Mode: Serial Clock.	--
C8	SCL	I	I2C Mode: Serial Data.	--
C9	AVSS	P	Analog ground	--
C10	TX3	I/O	TX driving channel	Leave open
C11	TX6	I/O	TX driving channel	Leave open
D1	AVDD	P	On-chip programmingable MV regulator output. Connect to a 2.2uF/10V/X5R bypass capacitor.	--
D3	CHIPEN	I	Chip reset signal. Normal: High, Active Reset: Low	--
D4	INT	I/O	Multi-function I/O. It can be programming as INT signal or UART TXD signal. INT: Interrupt signal to Host. Normal: High, Active: Low UART TXD: UART transmit data channel	--
D9	TX11	I/O	TX driving channel	Leave open
D10	Tx5	I/O	TX driving channel	Leave open
D11	TX8	I/O	TX driving channel	Leave open
E1	GR	I/O	Multi-function I/O. It can be programming as Guarding (GR) channel or INT signal. INT: Interrupt signal to Host. Normal: High, Active: Low GR: Guarding (GR) signal for TX and RX channels.	--
E2	AVSS	P	Analog ground	--
E5	RX_KEY0	I	RX Touch key	Leave open
E7	TX_KEY	I	TX Touch key	Leave open
E9	TX7	I/O	TX driving channel	Leave open
E10	TX9	I/O	TX driving channel	Leave open
E11	TX10	I/O	TX driving channel	Leave open
F1	RX0	I/O	RX driving channel	Leave open
F2	RX1	I/O	RX driving channel	Leave open
F5	RX_KEY1	I	RX Touch key	Leave open
F6	RX_KEY2	I	RX Touch key	Leave open
F10	TRX1	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
F11	TRX0	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
G1	RX2	I/O	RX driving channel	Leave open
G2	RX3	I/O	RX driving channel	Leave open
G3	RX4	I/O	RX driving channel	Leave open

Ball No.	Pin Name.	Type	Description	If Unused...
G10	TRX3	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
G11	TRX2	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
H1	RX5	I/O	RX driving channel	Leave open
H2	RX6	I/O	RX driving channel	Leave open
H3	RX7	I/O	RX driving channel	Leave open
H7	AVSS	P	Analog ground	--
H9	TRX15	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
H10	TRX5	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
H11	TRX4	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
J1	RX8	I/O	RX driving channel	Leave open
J2	RX9	I/O	RX driving channel	Leave open
J3	RX13	I/O	RX driving channel	Leave open
J4	RX17	I/O	RX driving channel	Leave open
J5	RX20	I/O	RX driving channel	Leave open
J6	RX23	I/O	RX driving channel	Leave open
J7	RX26	I/O	RX driving channel	Leave open
J9	TRX14	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
J10	TRX7	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
J11	TRX6	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
K1	RX10	I/O	RX driving channel	Leave open
K2	RX11	I/O	RX driving channel	Leave open
K3	RX15	I/O	RX driving channel	Leave open
K4	RX18	I/O	RX driving channel	Leave open
K5	RX21	I/O	RX driving channel	Leave open
K6	RX24	I/O	RX driving channel	Leave open
K7	RX27	I/O	RX driving channel	Leave open
K9	TRX13	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
K10	TRX8	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open

Ball No.	Pin Name.	Type	Description	If Unused...
K11	TRX9	I/O	Multi-function channels. It can be programming as TX or RX channel.driving and RX sensing function.	Leave open
L1	RX12	I/O	RX driving channel	Leave open
L2	RX14	I/O	RX driving channel	Leave open
L3	RX16	I/O	RX driving channel	Leave open
L4	RX19	I/O	RX driving channel	Leave open
L5	RX22	I/O	RX driving channel	Leave open
L6	RX25	I/O	RX driving channel	Leave open
L7	RX28	I/O	RX driving channel	Leave open
L9	TRX12	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
L10	TRX11	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open
L11	TRX10	I/O	Multi-function channels. It can be programming as TX or RX channel.	Leave open

Pin Type:

P: Power or Ground

I: Input only

O: Output only

I/O: Input or Output

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Item	Symbol	Unit	Value
Input Power Supply 1	PVDD	V	-0.3 ~ +3.4
Input Power Supply 2	AVDD_CP	V	-0.3 ~ +3.4
Input Power Supply 3 (For External mode only)	HVDD	V	-0.3 ~ +25
Parameters maximum writes		Cycle	10,000
ESD target for Human Body Model	HBM	V	4000
ESD target for Machine Model	MM	V	400
Maximum junction temperature	Tj	℃	125
Operating temperature	Topr	℃	-40 ~ +85
Storage temperature	Tstg	℃	-55 ~ +125

External mode : Customer supply HVDD Voltage for TP IC

CAUTION:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanently damage to the device. These are stresses ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability of the device.

4.2. Recommended Operating Conditions

Item	Symbol	Unit	Recommended Value
Input Power Supply 1	PVDD	V	3.3 ± 3%
Input Power Supply 2	AVDD_CP	V	3.3 ± 3%
Input Power Supply 3	HVDD	V	10 (For Internal mode) 20 (For External mode)
Operating Temperature	Topr	℃	-40 ~ +85
Storage Temperature	Tstg	℃	-55 ~ +125
Temperature Slew Rate			10℃/min

4.3. Input Power Supply and GPIO Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Power Supply 1	PVDD	2.97	3.3	3.4	V	
Input Power Supply 2	AVDD_CP	2.97	3.3	3.4	V	
Input Power Supply 3	HVDD	-	8	10	V	Internal mode
		10	20	25	V	External mode
On-Chip 1.2V Regulator	VDD12	1.08	1.2	1.32	V	
Operating Current	PVDD		90		mA	1
Idle Current	PVDD		20		mA	1
Low Input Logic Level	VIL			0.3* PVDD	V	
High Input Logic Level	VIH	0.7* PVDD			V	

Note 1: The configuration values listed below table were used in the ILITEK's Bench Board to validate the interfaces and derive the operating current.

Test Configuration Table

| Item	Typical Value	Note
HVDD	10V	HVDD Internal mode.
Active Mode Report Rate	120Hz	ILI2132 report touch ID to ILITEK's I2C to USB bridge board.
Report Touch ID Number	10	
I2C SCL Clock Rate	400kHz	Fast mode.
Idle Mode	Idle time: 30ms	Support touch wake up function and it depends on self scan rate.
USB Suspend Mode	Suspend time: 300ms	Support Touch wake up function and it depends on host setting

4.4. USB DC Characteristics

| Item	Symbol	Min.	Typ.	Max.	Unit	Note
Low Input Logic Level	V_{IL}			0.8	V	
High Input Logic Level	V_{IH}	2.0			V	
Differential input sensitivity	V_{DI}	0.2			V	
Differential common-mode range	V_{CM}	0.8		2.5	V	
Single-ended receiver threshold	V_{SE}	0.8		2.0	V	
Receiver hysteresis	V_{RH}		200		mV	
Low Output Voltage	V_{OL}	0		0.3		
High Output Voltage	V_{OH}	2.9		3.4		
Output signal cross voltage	V_{CRS}	1.3		2.0		
Pull-up resistor	R_{PU}	1.425		1.575	Ω	
Pull-down resistor	R_{PD}	14.25		15.75	Ω	
Termination Voltage for upstream port pull up (RPU)	V_{TRM}	2.9		3.4	V	

4.5. I2C AC Characteristics
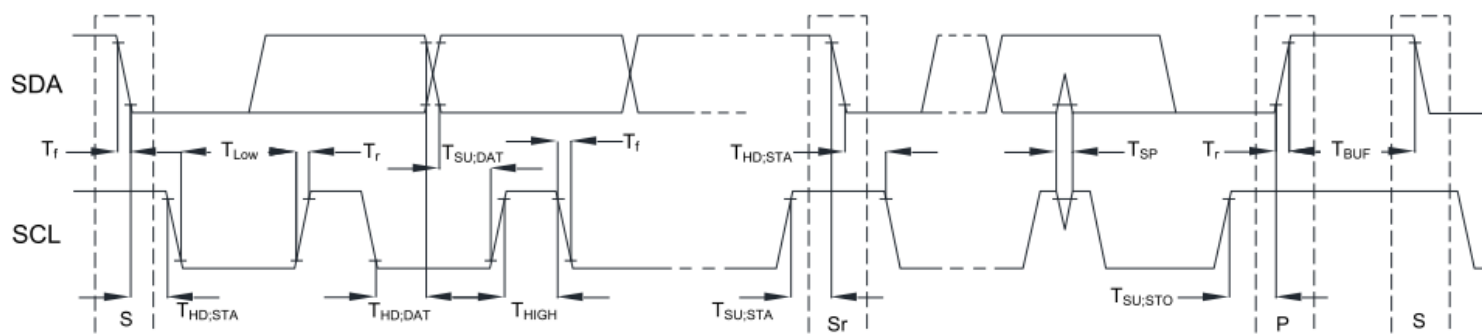
Item	Symbol	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
SCL standard mode clock frequency	F_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock is generated.	$T_{HD;STA}$	4	--	0.6	--	us
LOW period of the SCL clock	T_{LOW}	4.7	--	1.3	--	us
HIGH period of the SCL clock	T_{HIGH}	4	--	0.6	--	us
Setup time for a repeat START condition.	$T_{SU;STA}$	4.7	--	0.6	--	us
Data hold time	$T_{HD;DAT}$	0	--	0	--	us
Data setup time	$T_{SU;DAT}$	250	--	100	--	ns
Rising time of both SDA and SCL signals	Tr	--	1000	--	300	ns
Falling time of both SDA and SCL signals	Tf	--	300	--	300	ns
Setup time for STOP condition.	$T_{SU;STO}$	4	--	0.6	--	us
Free time between STOP and START condition	T_{BUF}	4.7	--	1.3	--	us
Pulse width of spikes which must be suppressed by input filter	T_{SP}	--	--	0	50	ns

4.6. Power Sequence
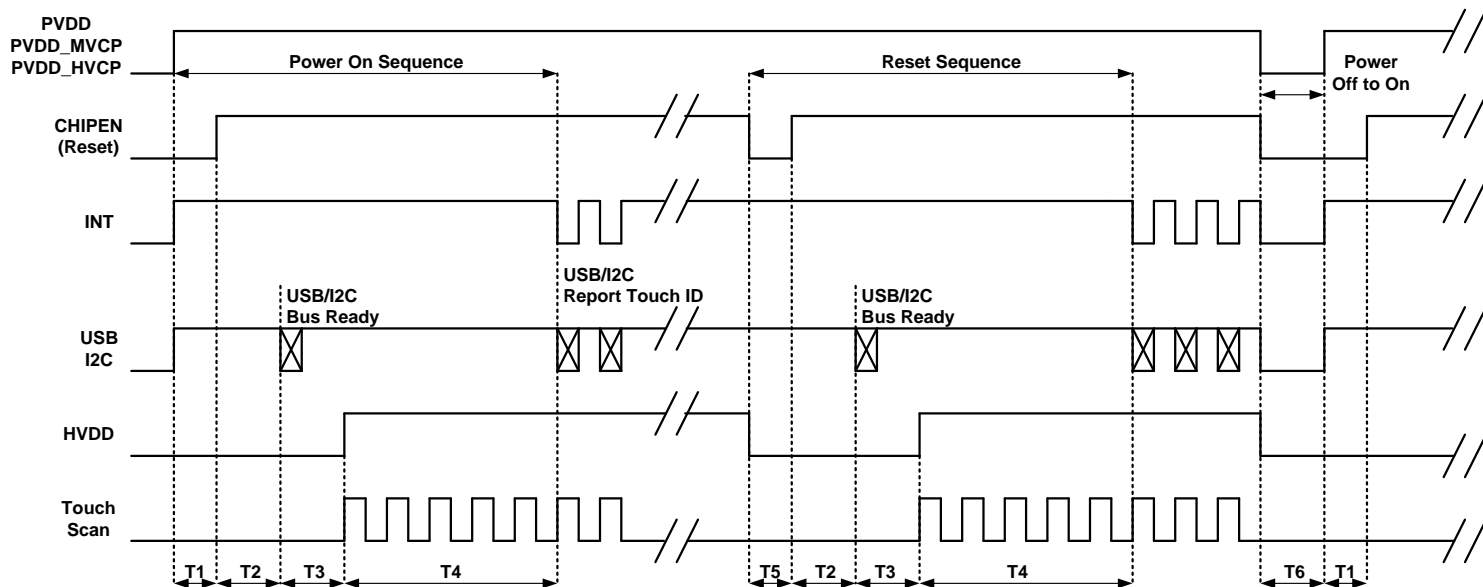
| Symbol	Description	Min.	Max.	Unit.
T1	Input Power Supply PVDD, PVDD_MVCP, Power on Reset time. Host need to control Reset time to be larger than 10ms.	10	--	ms
T2	Chip initial time		400	ms
T3	HVDD start up time		300	ms
T4	Chip report Touch ID preparation time		400	ms
T5	Chip Reset and HVDD discharge time. Host need to control Reset time to be larger than 10ms.	10		ms
T6	Input Power Supply PVDD, PVDD_MVCP, and HVDD Power off discharge time. Host need to control discharge time to be larger than 100ms.	100		ms

5. SMT IR Reflow Profile
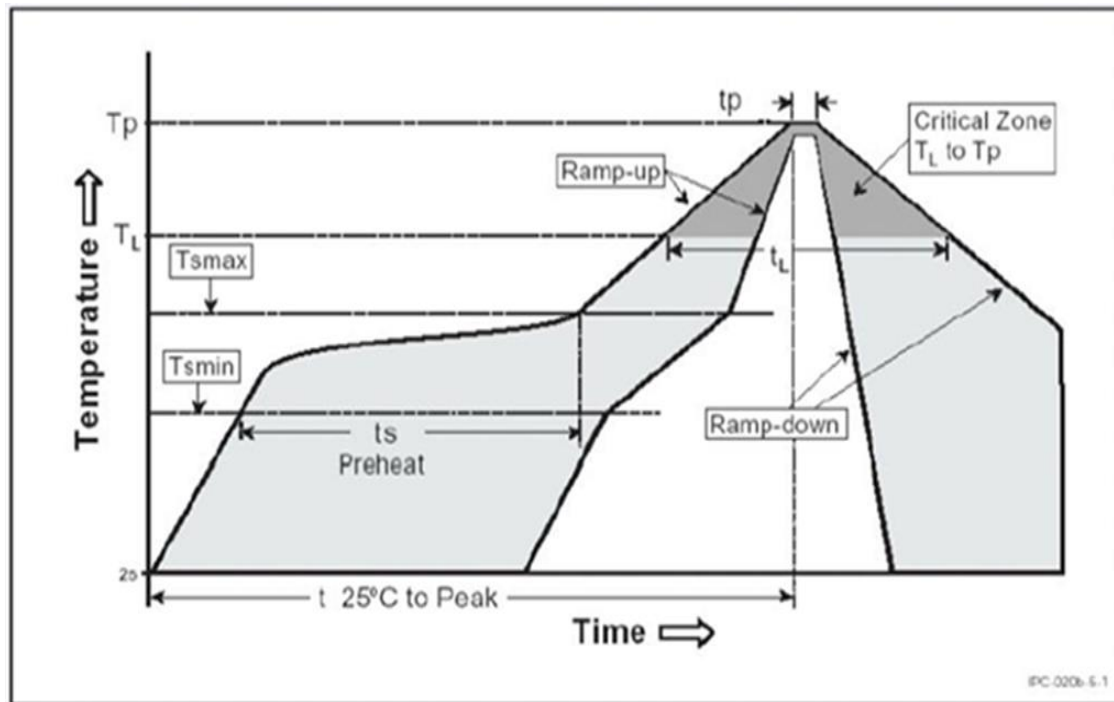
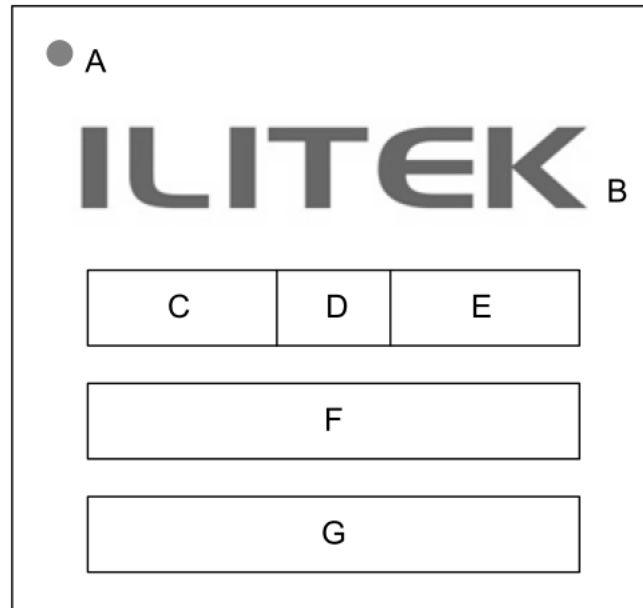| Profile Feature	Pb-Free Assemble
Average ramp-up rate (TL to Tp)	3℃/Second max
Preheat -Temperature Min (Tsmim) -Temperature Max(Tsmax) -Time (min to max)(ts)	 150℃ 200℃ 60-120 Seconds
Time maintained above -Temperature(TL) -Time(tL)	 217℃ 60-150 Seconds
Peak Temperature(Tp)	245 +0/-5℃
Time within 5℃ of actual Peak Temperature(tp)	20-40 Seconds

6. Package Information

6.1. BGA-90 Package Dimension
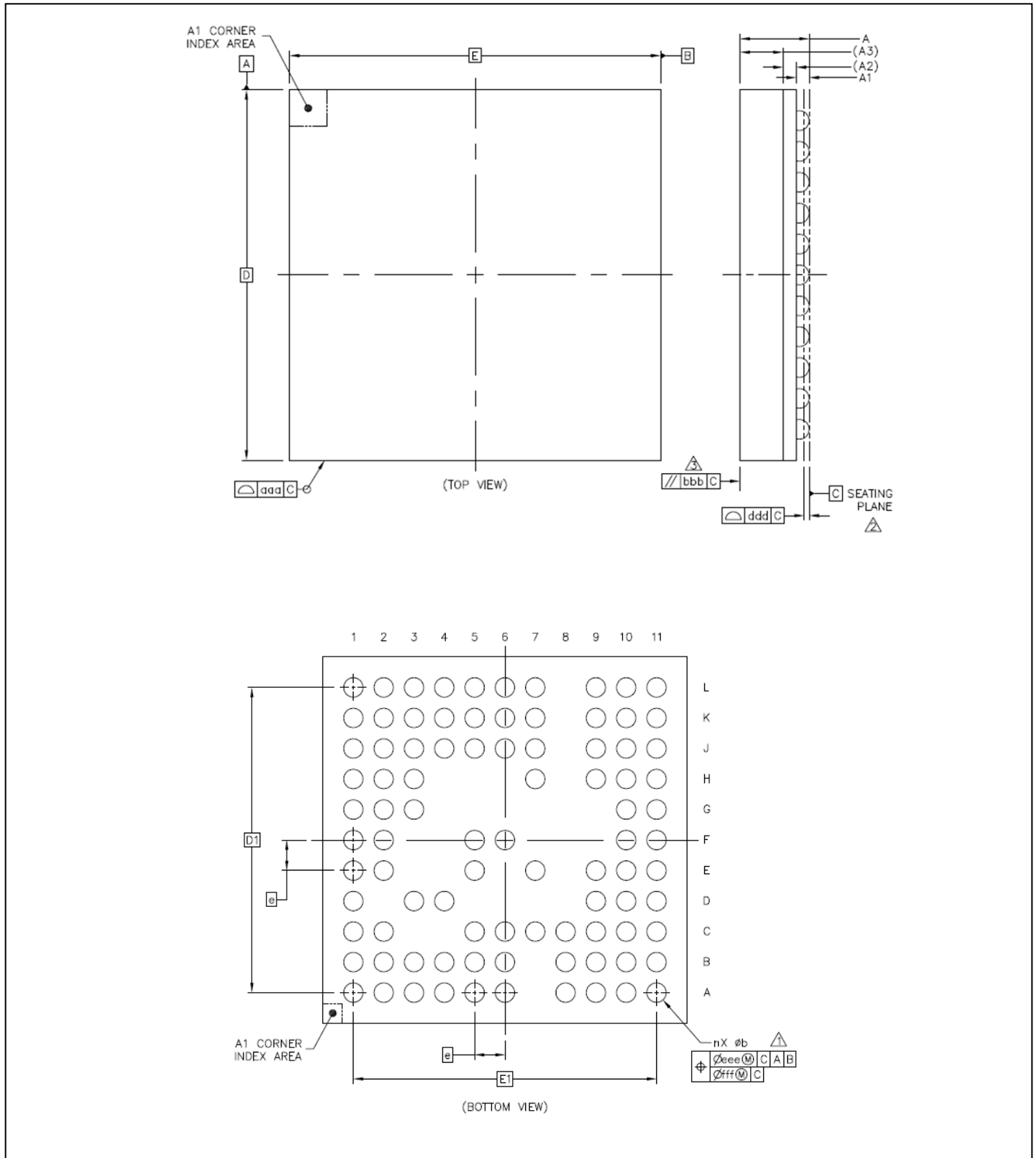
SYMBOL	COMMON DIMENSIONS		
	MIN.	NOR.	MAX.

|	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.2
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		6	BSC
	E		6	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.5	BSC
BALL COUNT	n		90	
EDGE BALL CENTER TO CENTER	D1		5	BSC
	E1		5	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

6.2. Marking Information

Item	Description
A	Pin 1 Indication
B	ILITEK logo
C	IC Model Name: ILI2132
D	Blank
E	Blank
F	Assembly Lot No.: The code will be updated by production control (1st code is A)
G	Wafer Lot No.: The code will be updated by production control (1st code is A)

7. Typical Application Circuit

7.1. USB Typical Application Circuit
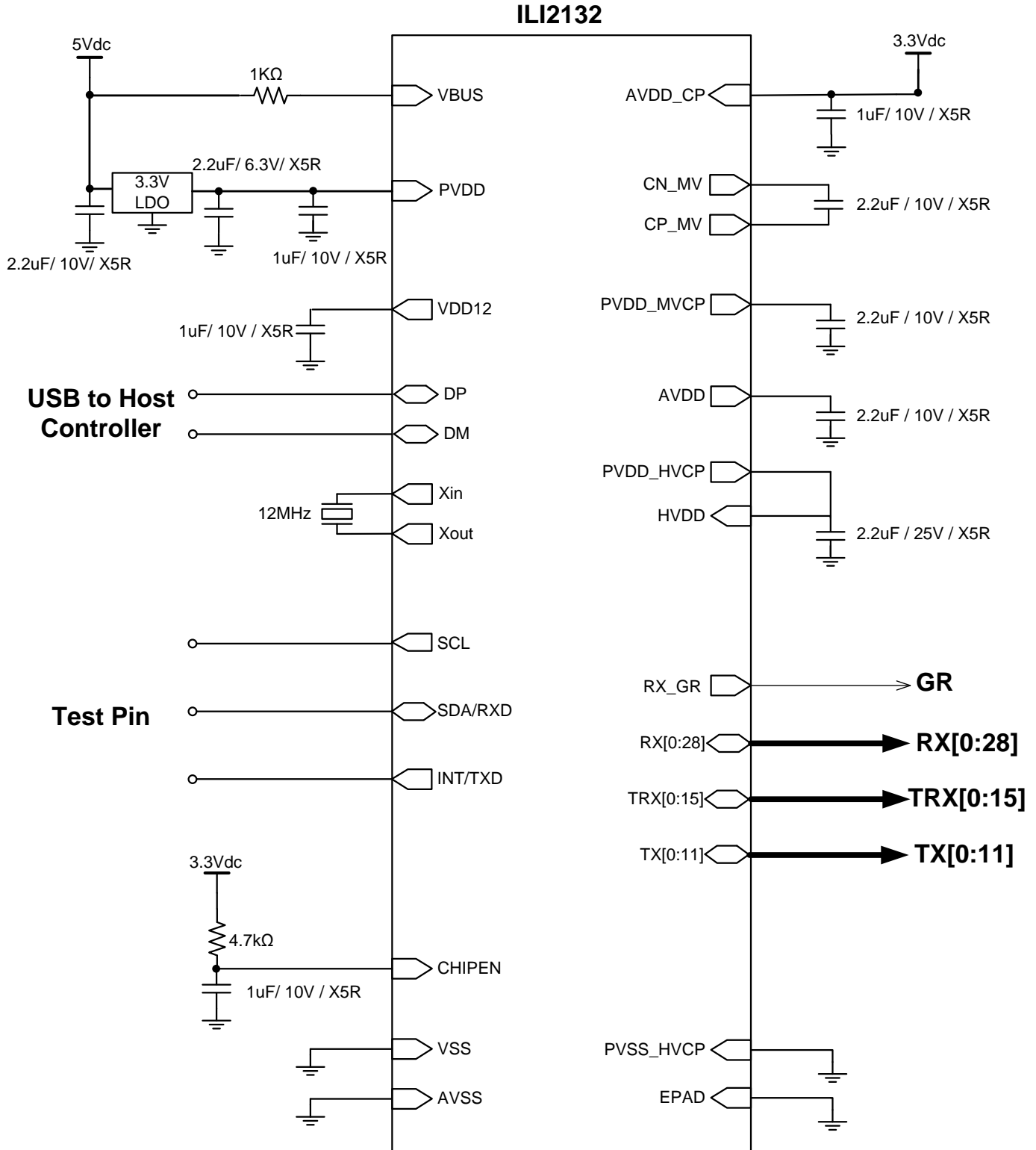
7.2. I2C Typical Application Circuit
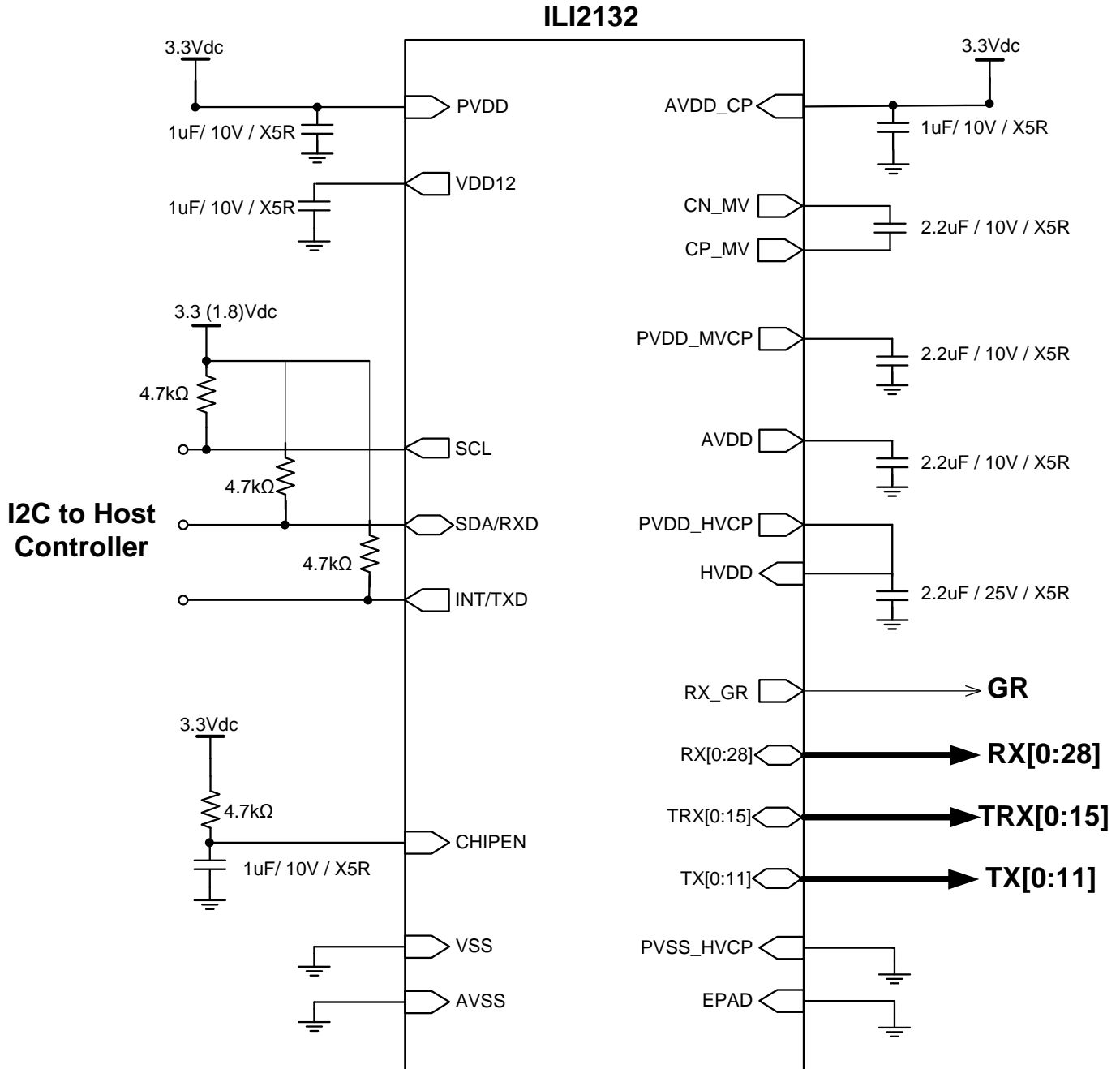
8. Revision History

Version No.	Date	Page	Description
V001	2020/04/8	All	Initial release
V001.1	2020/04/9	3, 13	1. Add multiple virtual key and extra HW key (Mutual type, 1Tx & 3Rx) 2. Modify Test Configuration Table
V002	2020/05/14	8	Recommand Input Voltage
V003	2020/06/16	5 6 7-15 16 20-21	Modify Block Diagram Modify Pin Configuration Figure, Re-edit page 7-15 Add SMT IR Reflow Profile Add Typical Application Circuit