CDTech(H.K.)Electronics Limited

Product Specification

Model Name	S035CQ35NS
Description	TFT LCD Module 3.5" QVGA 320(RGB)x240 Dots
Date	2018/02/05
Version	6.0

Approved by/Date	**Check by/Date**	**Prepared by/Date**
	ZHP 2018/02/05	Yigui.Han 2018/02/05

Customer Approval	
Date	

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1. Record of Revision

Rev	Issued Date	Description	Editor
1.0	2017.08.02	First Release.	Jack Guo
2.0	2015.07.29	Update FPC	Rich Liang
3.0	2015.09.20	Update FPC	Rich Liang
4.0	2015.10.24	Update spec	Rich Liang
5.0	2016.10.20	Update P&N	Jack Guo
6.0	2018.02.05	Update Absolute Maximum Rating &Interface Timing.	Jack Guo

2. General Specifications

Feature		Spec
Characteristics	Size	3.5 inch
	Resolution	320(horizontal)*240(Vertical)
	Interface	24bit-RGB
	Connect type	Connector
	Color Depth	16.7M
	Technology type	a-Si
	Pixel pitch (mm)	0.219*0.219
	Pixel Configuration	R.G.B.Stripe
	Display Mode	Normally White
	Driver IC	HX8238D
	Viewing Direction	12 O'clock
	Gray Inversion Direction	6 O'clock
Mechanical	LCM (W x H x D) (mm)	76.90*63.90*3.26
	Active Area(mm)	70.08*52.56
	Weight (g)	TBD
	LED Numbers	6 LEDs

Note 1: Requirements on Environmental Protection: RoHs
Note 2: LCM weight tolerance: +/- 5%

3. Input/Output Terminals

No.	Symbol	Description
1-2	VBL-	Backlight LED Cathode
3-4	VBL+	Backlight LED Anode.
5	Y1	Touch panel up side
6	X1	Touch panel right side
7	NC	-
8	RESET	Reset Signal pin (“Low” is enable)
9	SPENB	Chip select
10	SPCK	Serial Clock.
11	SPDA	Serial Data
12-19	B0~B7	Data bus
20-27	G0~G7	Data bus
28-35	R0~R7	Data bus
36	HSYNC	Line Synchronous Signal
37	VSYNC	Frame Synchronous Signal
38	DOTCLK	Dot-clock signal and oscillator source
39-40	NC	-
41-42	VCI	Power supply for logic operation
43	Y2	Touch panel bottom side
44	X2	Touch panel left side
45-47	NC	-
48	IF2	Control the input data format
49	IF1	Control the input data format
50	IF0	Control the input data format
51	NC	-
52	DEN	Display enable signal
53-54	GND	System Ground

4. Absolute Maximum Rating

Item	Symbol	MIN	Typ	MAX	Unit	Remark
Supply Voltage	VCI	-0.3	-	3.6	V	-
Current Drain Per Pin Excluding VDD and VSS	I	-	25	-	mA	-
Operating Temperature	T_{OPR}	-20	-	70	℃	-
Storage Temperature	T_{STG}	-30	-	80	℃	

5. Timing characteristics

5.1 ELECTRICAL CHARACTERISTICS

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		V_{CI}	2.5	3.3	3.6	V	
Input Signal Voltage	Low Leve	V_{IL}	GND	-	0.1x VCI	V	
	High Level	V_{IH}	0.8x VCI	-	VCI	V	
Output Signal Voltage	Low Leve	V_{OL}	0	-	0.2*VCI	V	
	High Level	V_{OH}	0.8*VCI	-	VCI	V	

5.2 LED Driving Conditions

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	-	mA	
Forward Voltage	V_F	18.6	19.2	19.8	V	
Backlight Power consumption	W_{BL}	-	0.384	-	W	
LED Lifetime		-	30000	-	Hrs	

Note 1: Each LED: IF =20 mA, VF =3.2+/0.2V.

Note 2: Optical performance should be evaluated at Ta=25℃ only.

Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life Time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

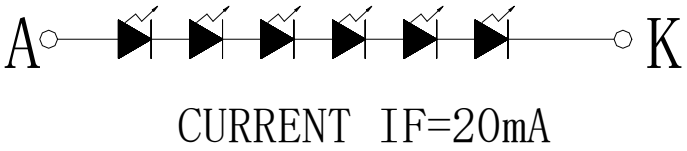
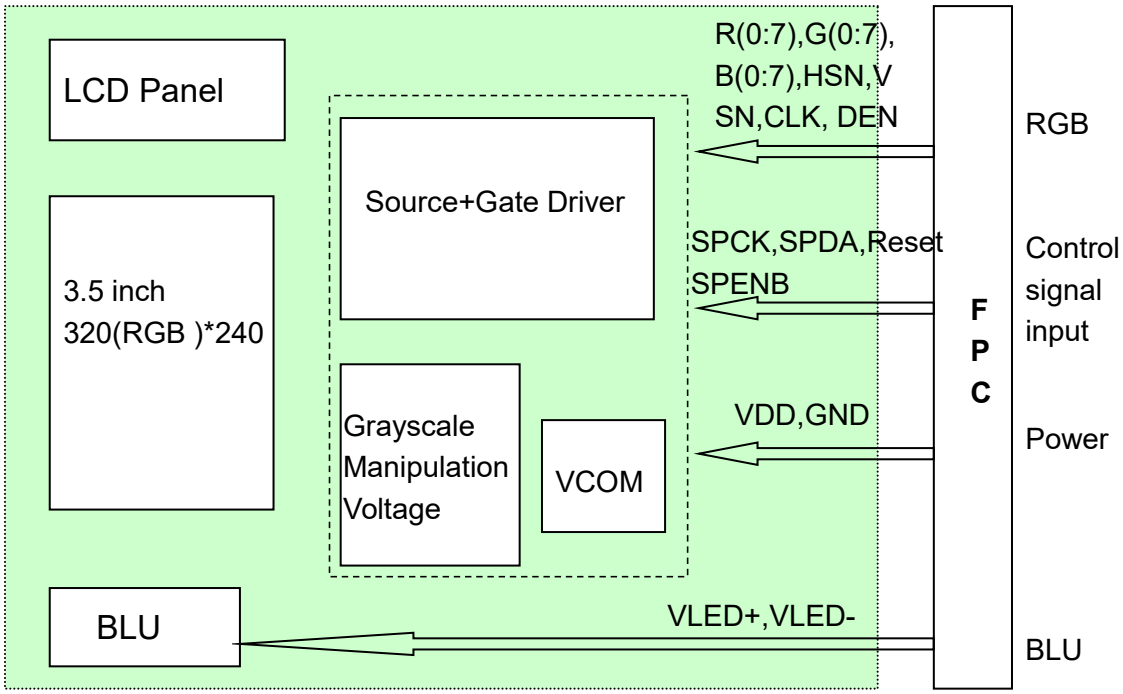


Figure: LED connection of backlight(Constant Current)

5.3 Block Diagram



6 Interface Timing

6.1 AC Electrical Characteristics

AC characteristics

(Unless otherwise specified, Voltage Referenced to Vss, V_{DDIO} = 2.2V, T_A = 25℃)

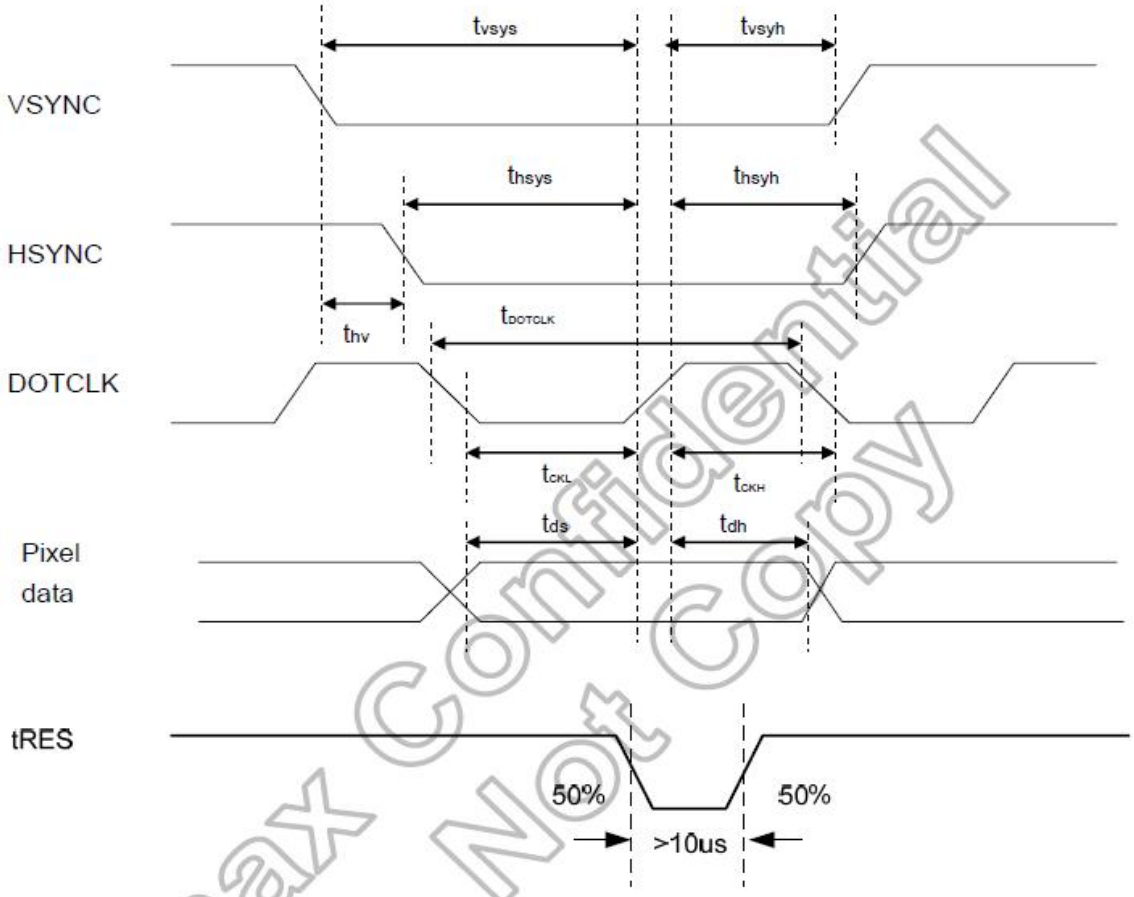


Figure 12. 1: Pixel timing

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Vertical Sync Setup Time	tvsys	20	10	-	-	-	-	ns
Vertical Sync Hold Time	tvsyh	20	10	-	-	-	-	ns
Horizontal Sync Setup Time	thsys	20	10	-	-	-	-	ns
Horizontal Sync Hold Time	thsyh	20	10	-	-	-	-	ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-	-	-	-	ns
DOTCLK High Period	tCKH	50	15	-	-	-	-	ns
Data Setup Time	tds	12	10	-	-	-	-	ns
Data hold Time	tdh	12	10	-	-	-	-	ns
Reset pulse width	tRES	10		-		-		µs

Note: External clock source must be provided to DOTCLK pin of HX8238-D. The driver will not operate if absent of the clocking signal.

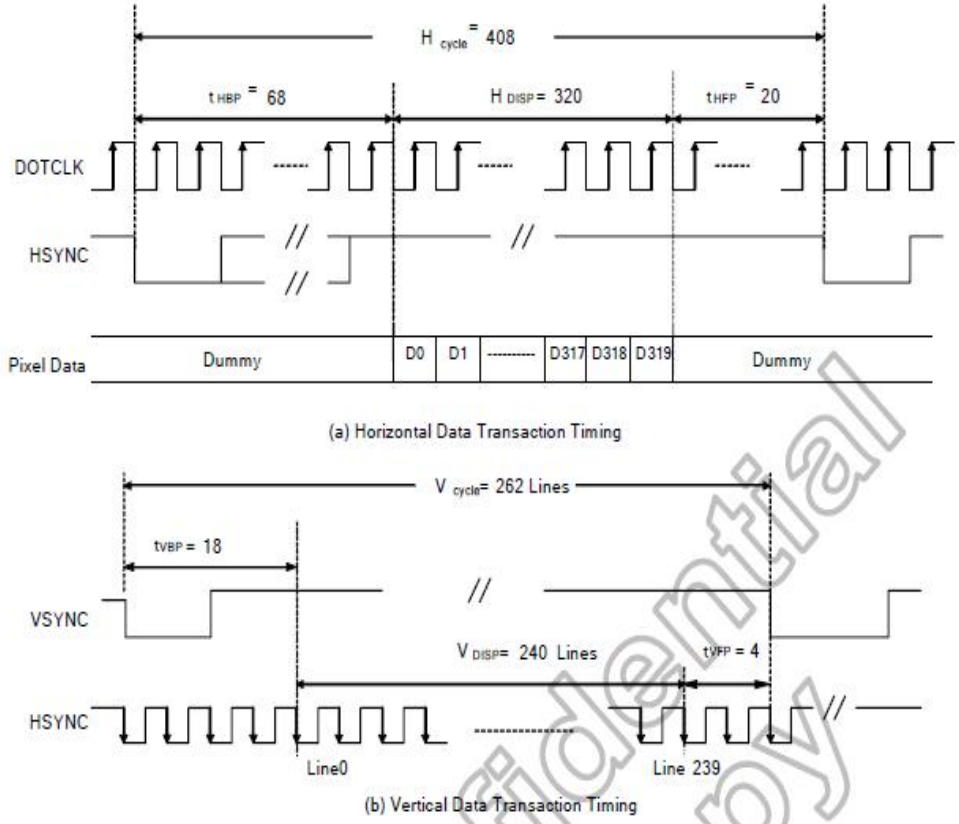


Figure 12. 2: Data transaction timing in parallel RGB (24-bit) interface (SYNC mode)

Characteristics		Symbol	Min.		Typ.		Max.		Unit
			24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency		fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period		tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)		fH	-		14.9		22.35		KHz
Vertical Frequency (Refresh)		fV	-		60		90		Hz
Horizontal Back Porch		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch		tHFP	-	-	20	60	-	-	tDOTCLK
Horizontal Data Start Point		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Blanking Period		tHBP + tHFP	52	146	88	264	180	960	tDOTCLK
Horizontal Display Area		HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle		Hcycle	372	1106	408	1224	500	1920	tDOTCLK
Vertical Back Porch		tVBP	-		18		-		Lines
Vertical Front Porch		tVFP	-		4		-		Lines
Vertical Data Start Point		tVBP	-		18		-		Lines
Vertical Blanking Period	NTSC	tVBP + tVFP	10		22		47		Lines
	PAL		20		33		120		
	PAL		12		25		112		
Vertical Display Area	NTSC	VDISP	-		240		-		Lines
	PAL				280(PALM=0)				
	PAL				288(PALM=1)				
Vertical Cycle	NTSC	Vcycle	250		262		287		Lines
	PAL		300		313		400		

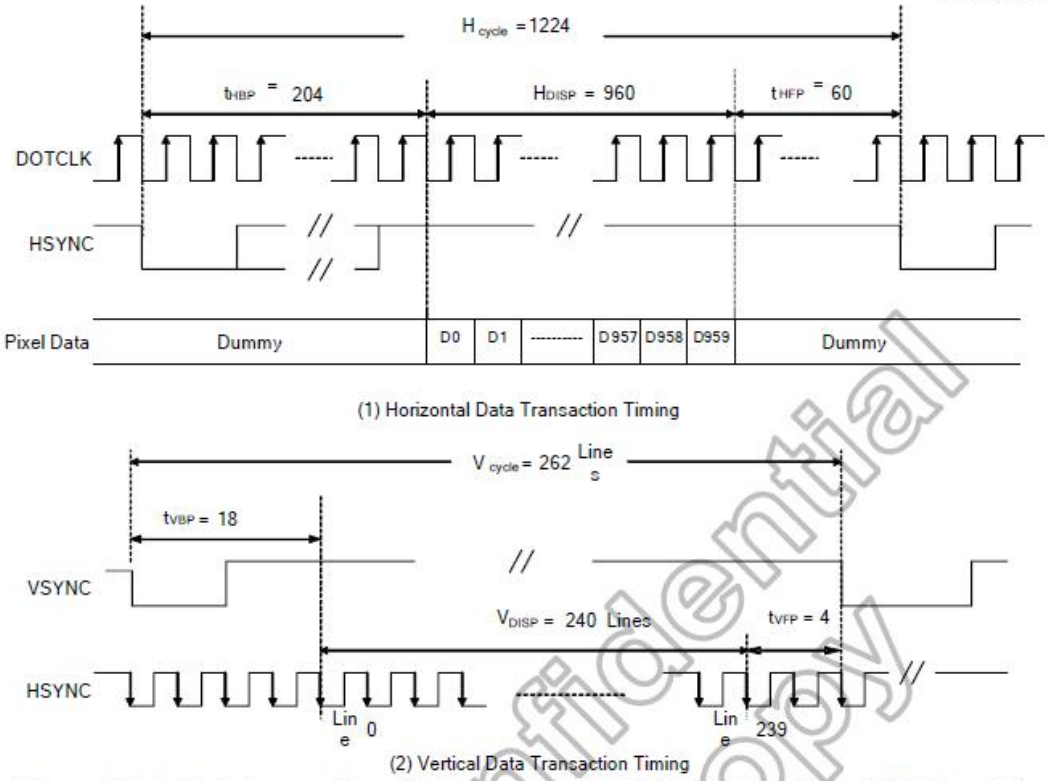


Figure 12. 3: Data transaction timing in serial RGB (8-bit) interface (SYNC mode)

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Blanking Period	tHBP + tHFP	52	146	88	264	180	960	tDOTCLK
Horizontal Display Area	HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle	Hcycle	372	1106	408	1224	500	1920	tDOTCLK
Vertical Blanking Period	tVBP + tVFP	2		-		47		Lines
Vertical Display Area	VDISP	-		240		-		Lines
Vertical Cycle	Vcycle	242		-		287		Lines

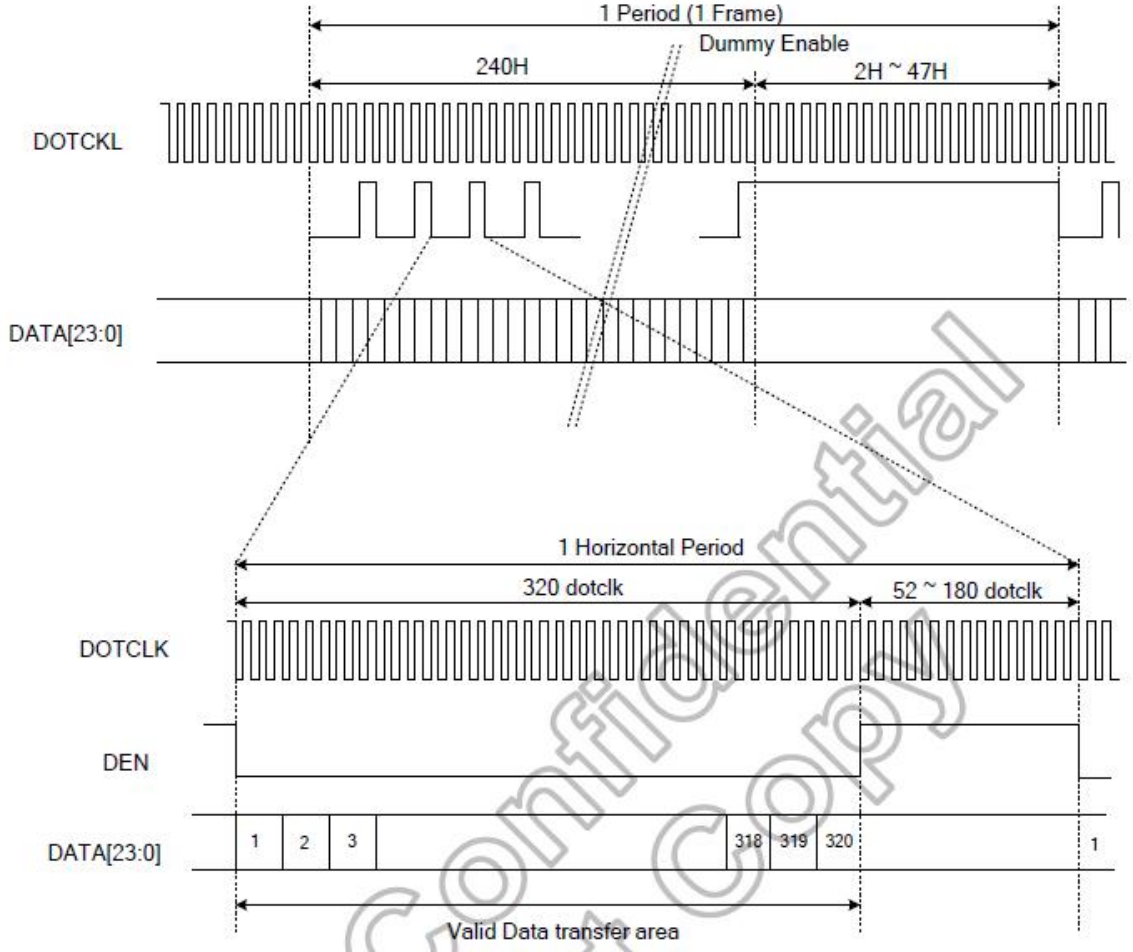
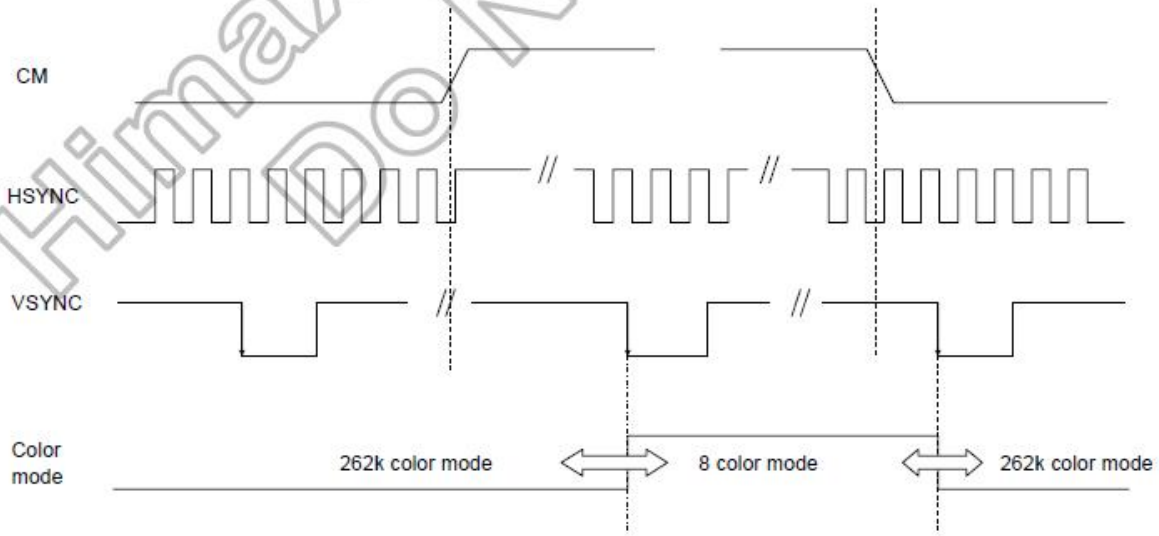
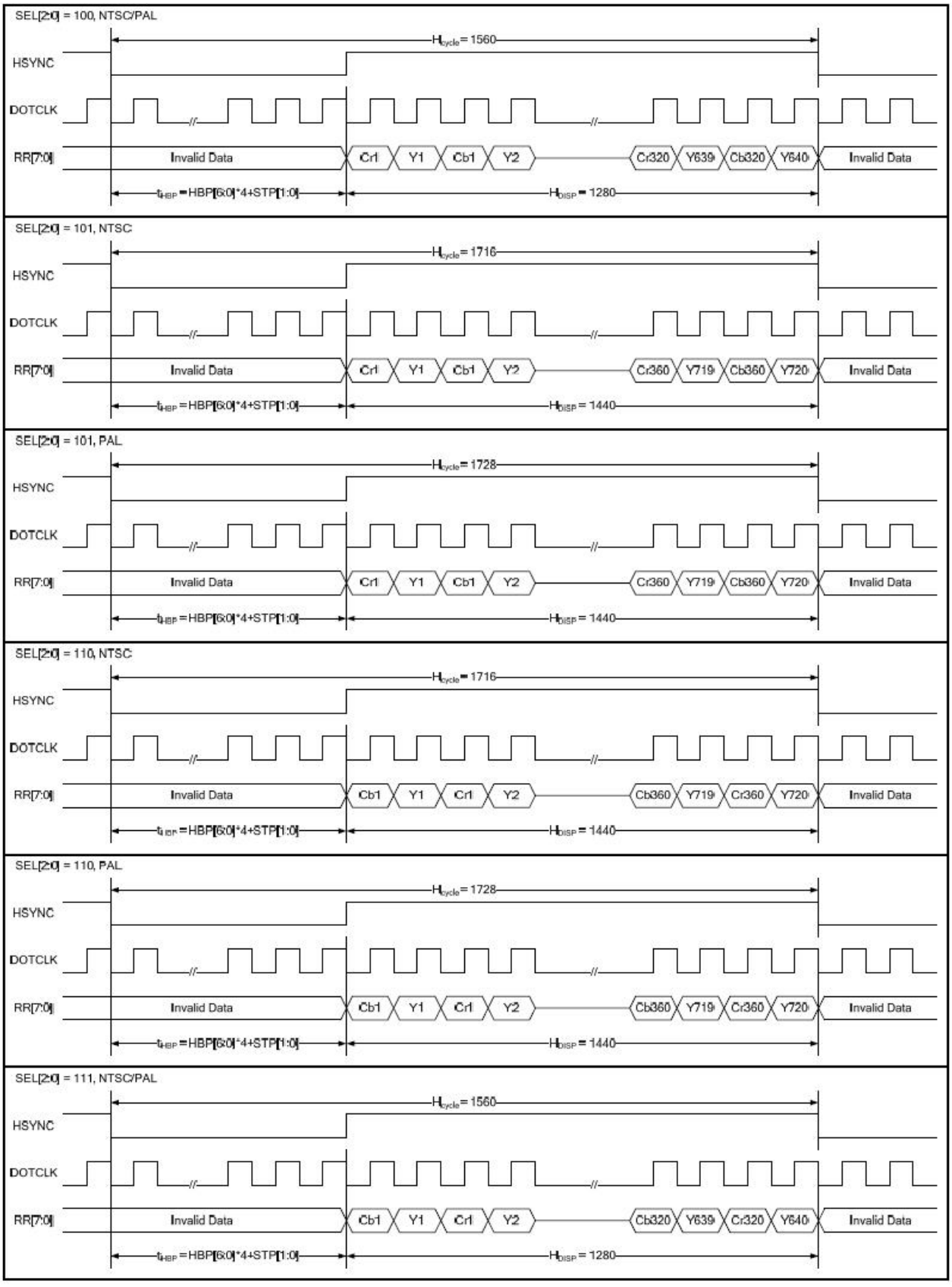
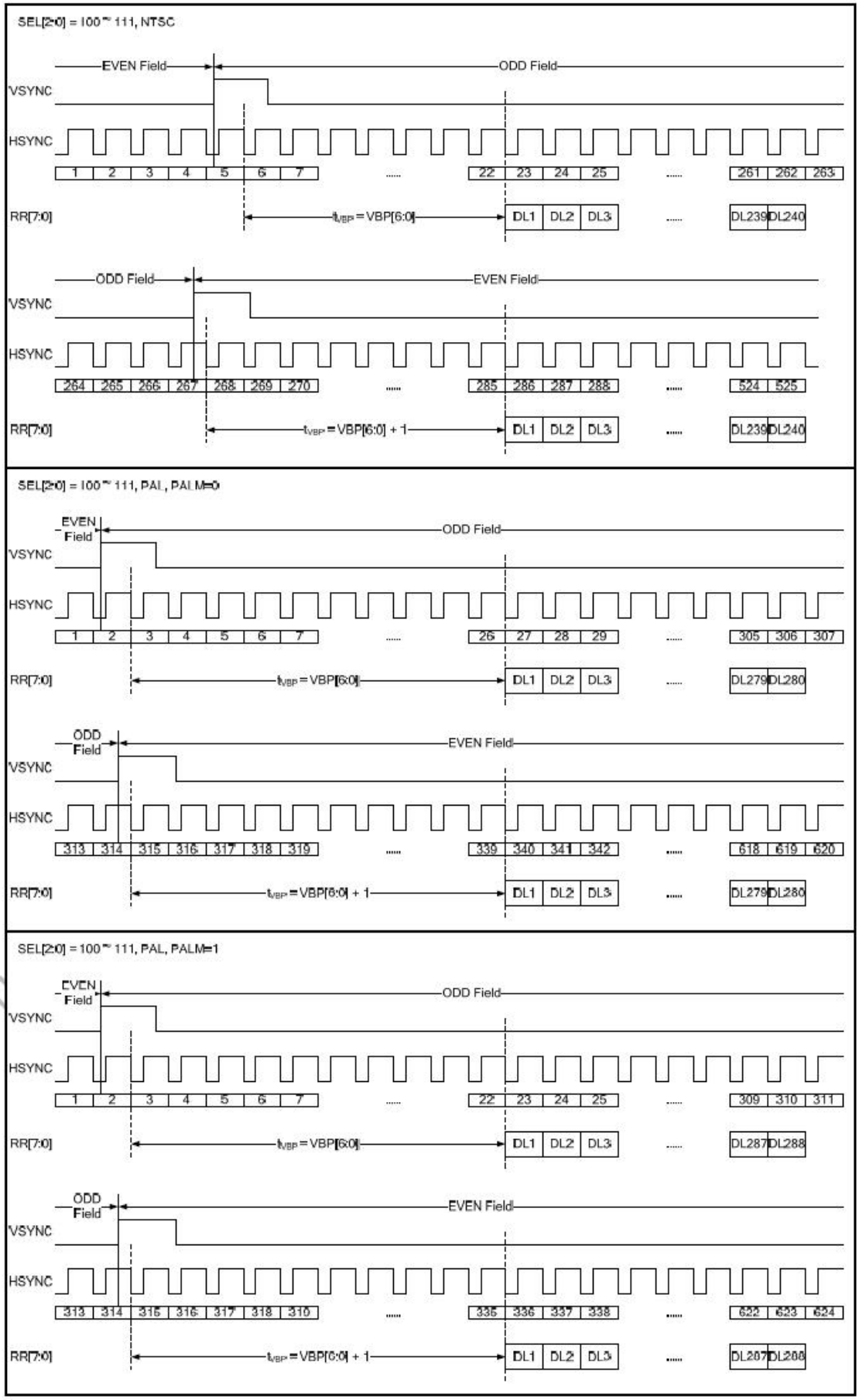


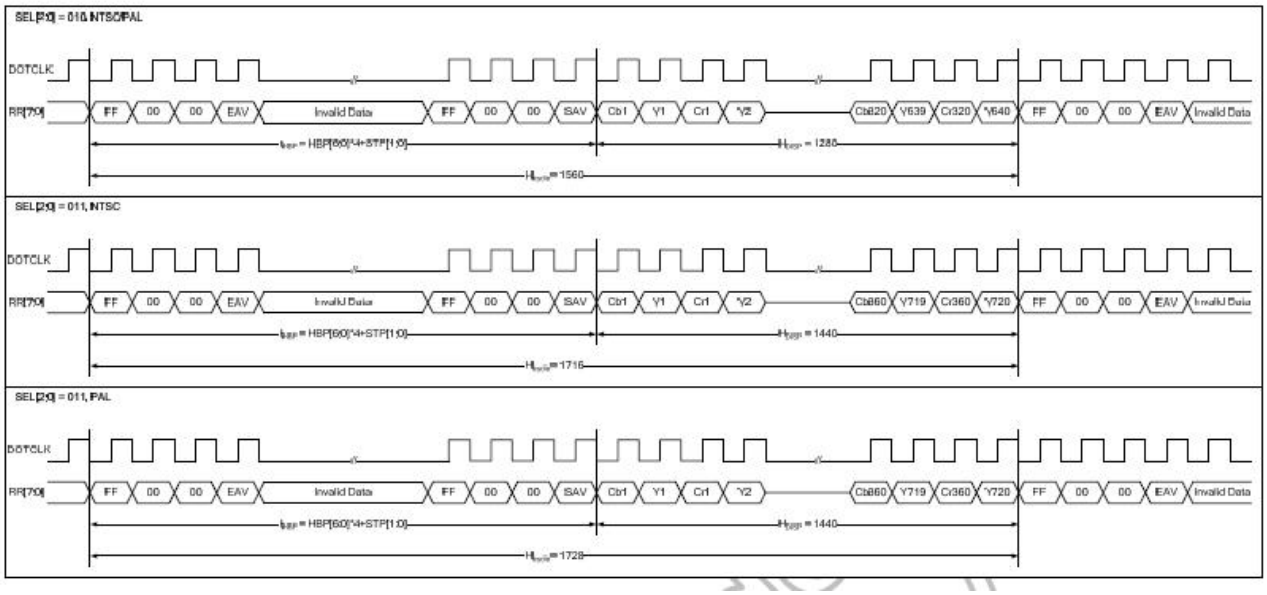
Figure 12. 4: Signal timing in DE only mode

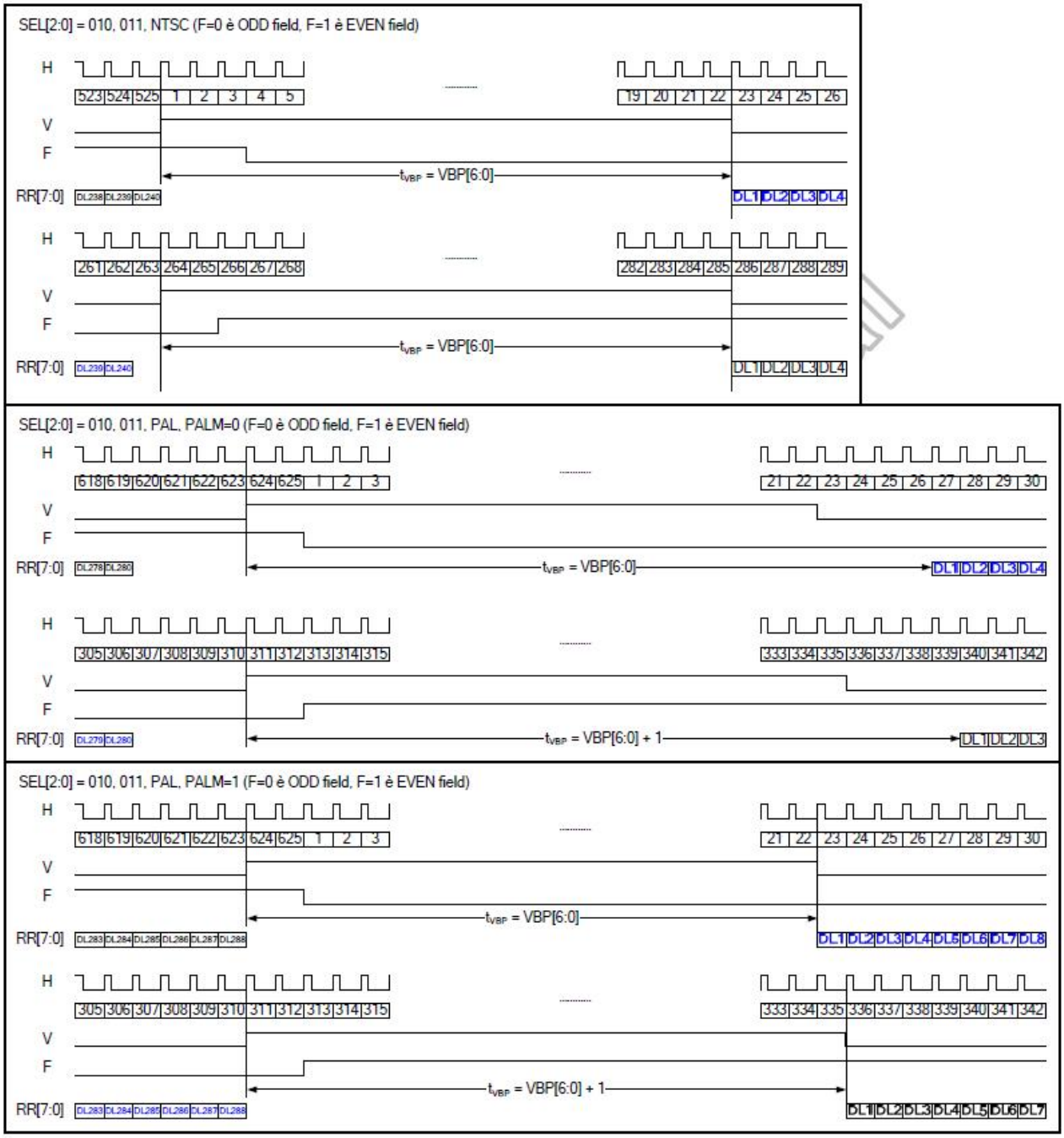


Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.


SEL[2:0] = 100, NTSC/PAL
Hcycle = 1560
HSYNC
DOTCLK
RR[7:0]
Invalid Data
Cr1
Y1
Cb1
Y2
Cr320
Y639
Cb320
Y640
Invalid Data
tHBP = HBP[6:0]*4+STP[1:0]
HDISP = 1280
SEL[2:0] = 101, NTSC
Hcycle = 1716
Cr360
Y719
Cb360
Y720
HDISP = 1440
SEL[2:0] = 101, PAL
Hcycle = 1728
SEL[2:0] = 110, NTSC
SEL[2:0] = 110, PAL
SEL[2:0] = 111, NTSC/PAL


SEL[2:0] = 100 ~ 111, NTSC
EVEN Field
ODD Field
VSYNC
HSYNC
1 2 3 4 5 6 7 ..... 22 23 24 25 ..... 261 262 263
RR[7:0]
tVBP = VBP[6:0]
DL1 DL2 DL3 ..... DL239 DL240
ODD Field
EVEN Field
VSYNC
HSYNC
264 265 266 267 268 269 270 ..... 285 286 287 288 ..... 524 525
RR[7:0]
tVBP = VBP[6:0] + 1
DL1 DL2 DL3 ..... DL239 DL240
SEL[2:0] = 100 ~ 111, PAL , PALM=0
EVEN Field
ODD Field
VSYNC
HSYNC
1 2 3 4 5 6 7 ..... 26 27 28 29 ..... 305 306 307
RR[7:0]
tVBP = VBP[6:0]
DL1 DL2 DL3 ..... DL279 DL280
ODD Field
EVEN Field
VSYNC
HSYNC
313 314 315 316 317 318 319 ..... 339 340 341 342 ..... 618 619 620
RR[7:0]
tVBP = VBP[6:0] + 1
DL1 DL2 DL3 ..... DL279 DL280
SEL[2:0] = 100 ~ 111, PAL, PALM=1
EVEN Field
ODD Field
VSYNC
HSYNC
1 2 3 4 5 6 7 ..... 22 23 24 25 ..... 309 310 311
RR[7:0]
tVBP = VBP[6:0]
DL1 DL2 DL3 ..... DL287 DL288
ODD Field
EVEN Field
VSYNC
HSYNC
313 314 315 316 317 318 319 ..... 335 336 337 338 ..... 622 623 624
RR[7:0]
tVBP = VBP[6:0] + 1
DL1 DL2 DL3 ..... DL287 DL288


SEL[2:0] = 010, NTSC/PAL
DOTCLK
RR[7:0]
FF
00
00
EAV
Invalid Data
FF
00
00
SAV
Cb1
Y1
Cr1
Y2
Cb639
Y639
Cr319
Y640
FF
00
00
EAV
Invalid Data
= HBP[6:0]*4+STP[1:0]
= 1280
= 1560
SEL[2:0] = 011, NTSC
DOTCLK
RR[7:0]
FF
00
00
EAV
Invalid Data
FF
00
00
SAV
Cb1
Y1
Cr1
Y2
Cb859
Y719
Cr359
Y720
FF
00
00
EAV
Invalid Data
= HBP[6:0]*4+STP[1:0]
= 1440
= 1716
SEL[2:0] = 011, PAL
DOTCLK
RR[7:0]
FF
00
00
EAV
Invalid Data
FF
00
00
SAV
Cb1
Y1
Cr1
Y2
Cb859
Y719
Cr359
Y720
FF
00
00
EAV
Invalid Data
= HBP[6:0]*4+STP[1:0]
= 1440
= 1728


SEL[2:0] = 010, 011, NTSC (F=0 è ODD field, F=1 è EVEN field)
H
V
F
RR[7:0]
tVBP = VBP[6:0]
SEL[2:0] = 010, 011, PAL, PALM=0 (F=0 è ODD field, F=1 è EVEN field)
tVBP = VBP[6:0] + 1
SEL[2:0] = 010, 011, PAL, PALM=1 (F=0 è ODD field, F=1 è EVEN field)

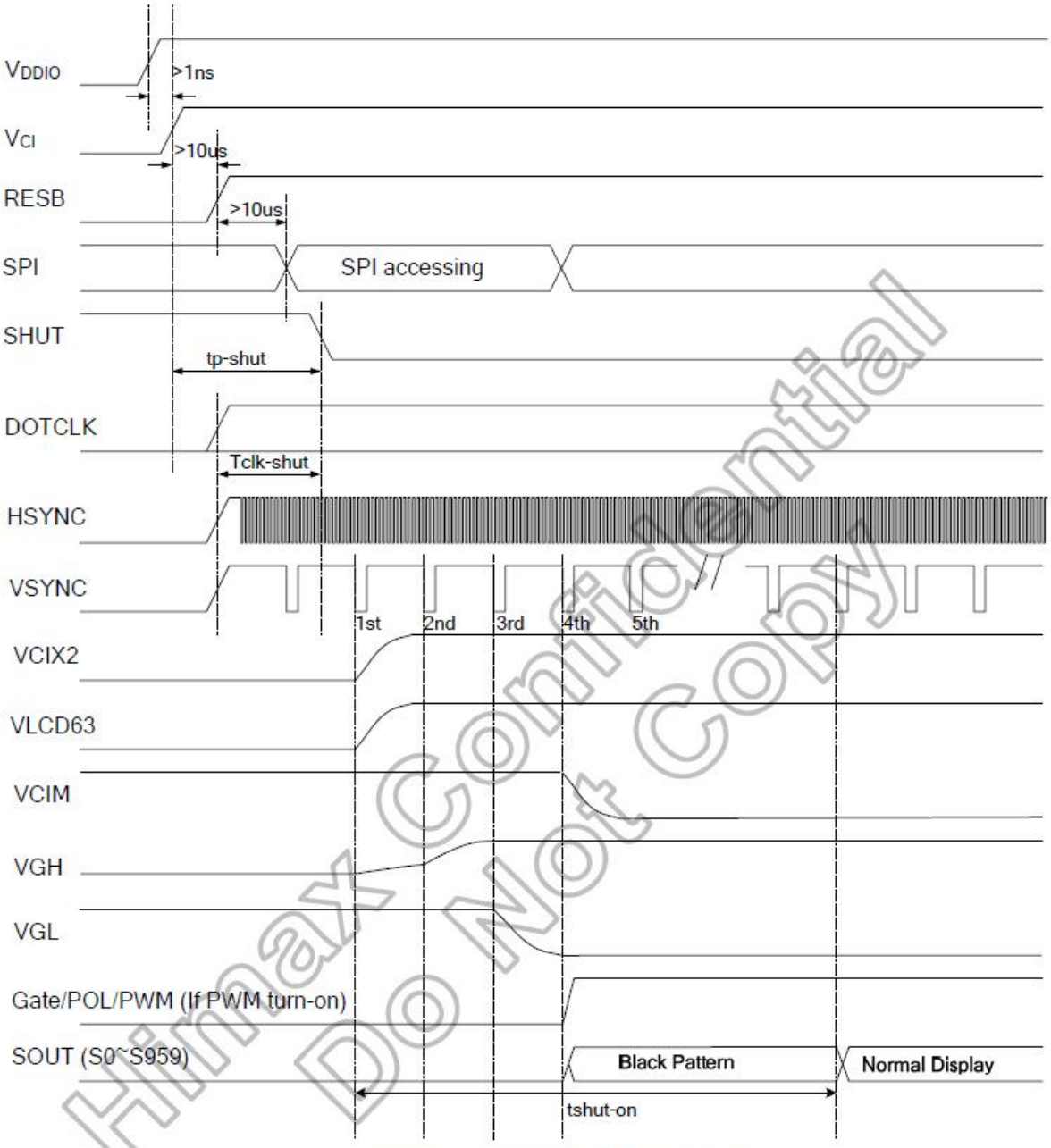
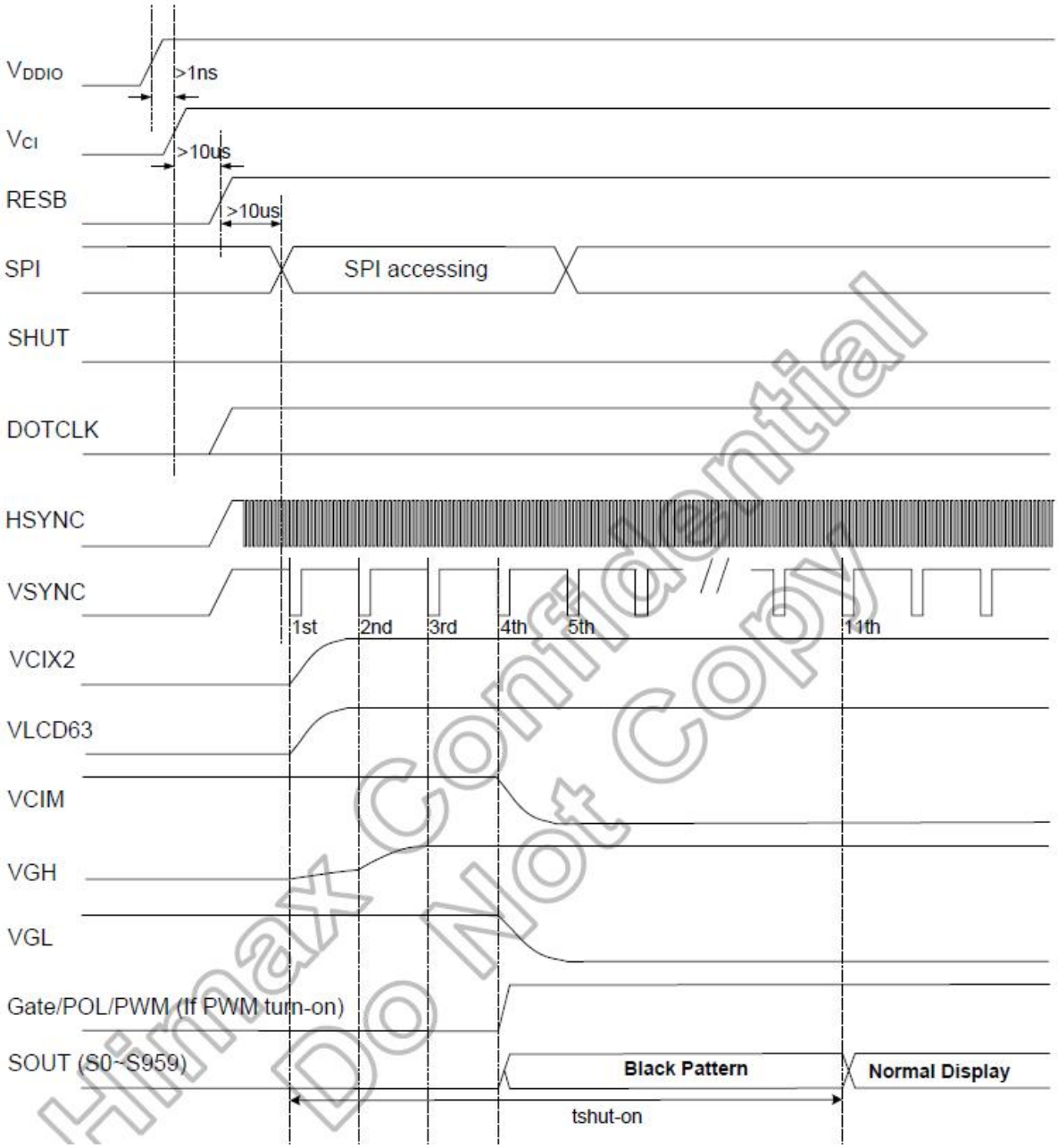


Figure 12. 10: Power up sequence

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
VCI / VDDIO on to falling edge of SHUT	tp-shut	1	-	-	µs
DOTCLK to falling edge of SHUT	tclk-shut (Note 1)	1	-	-	clk
Falling edge of SHUT to display start -1 line: 408 clk -1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on (Note 2)	-	-	14	frame

Note: (1) It is necessary to input DOTCLK before the falling edge of SHUT.
(2) Display starts at 14th falling edge of VSTNC after the falling edge of SHUT. The display starts at the falling edge of VSYNC which is determined by BLT[1:0] of R04h.



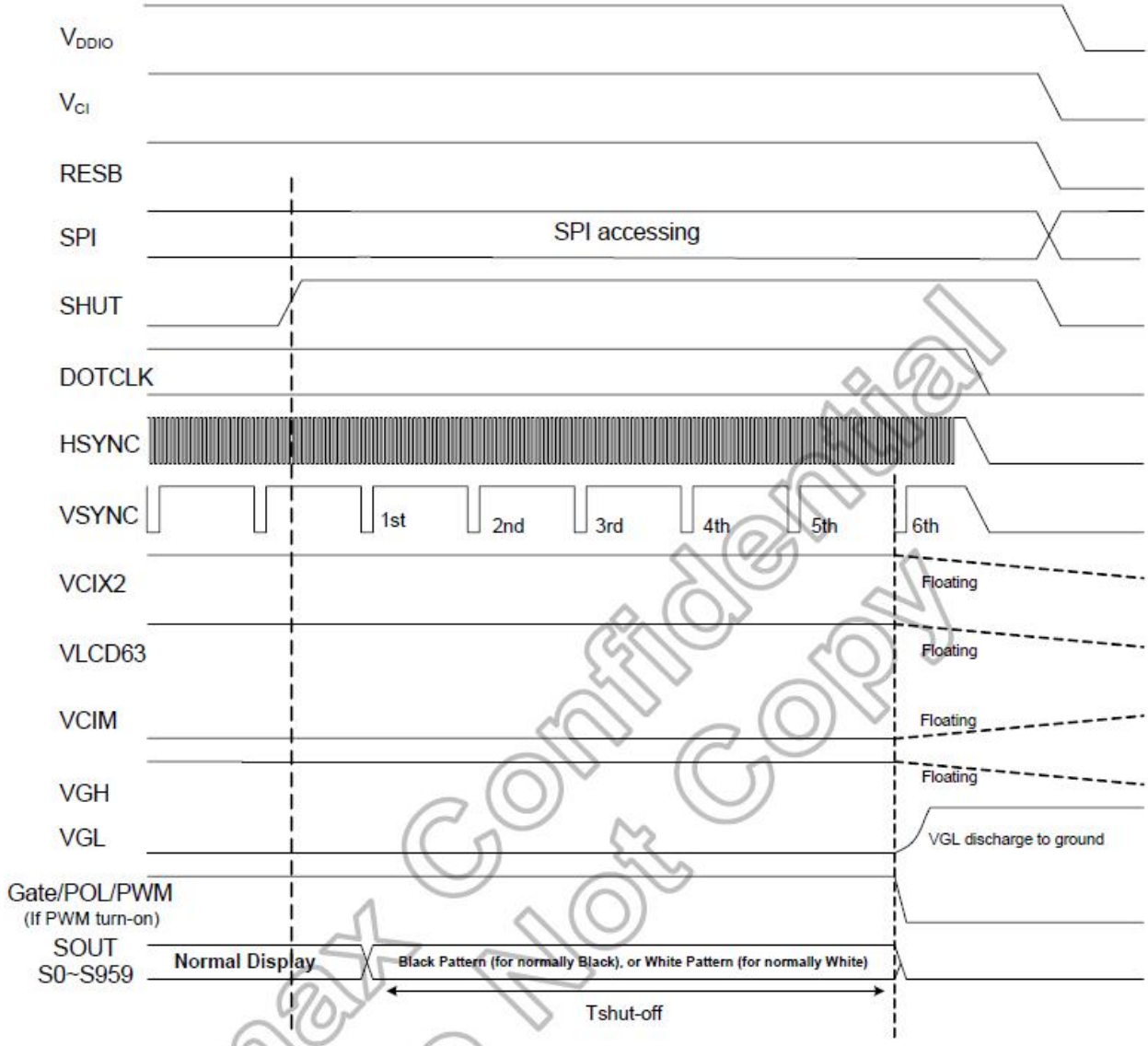
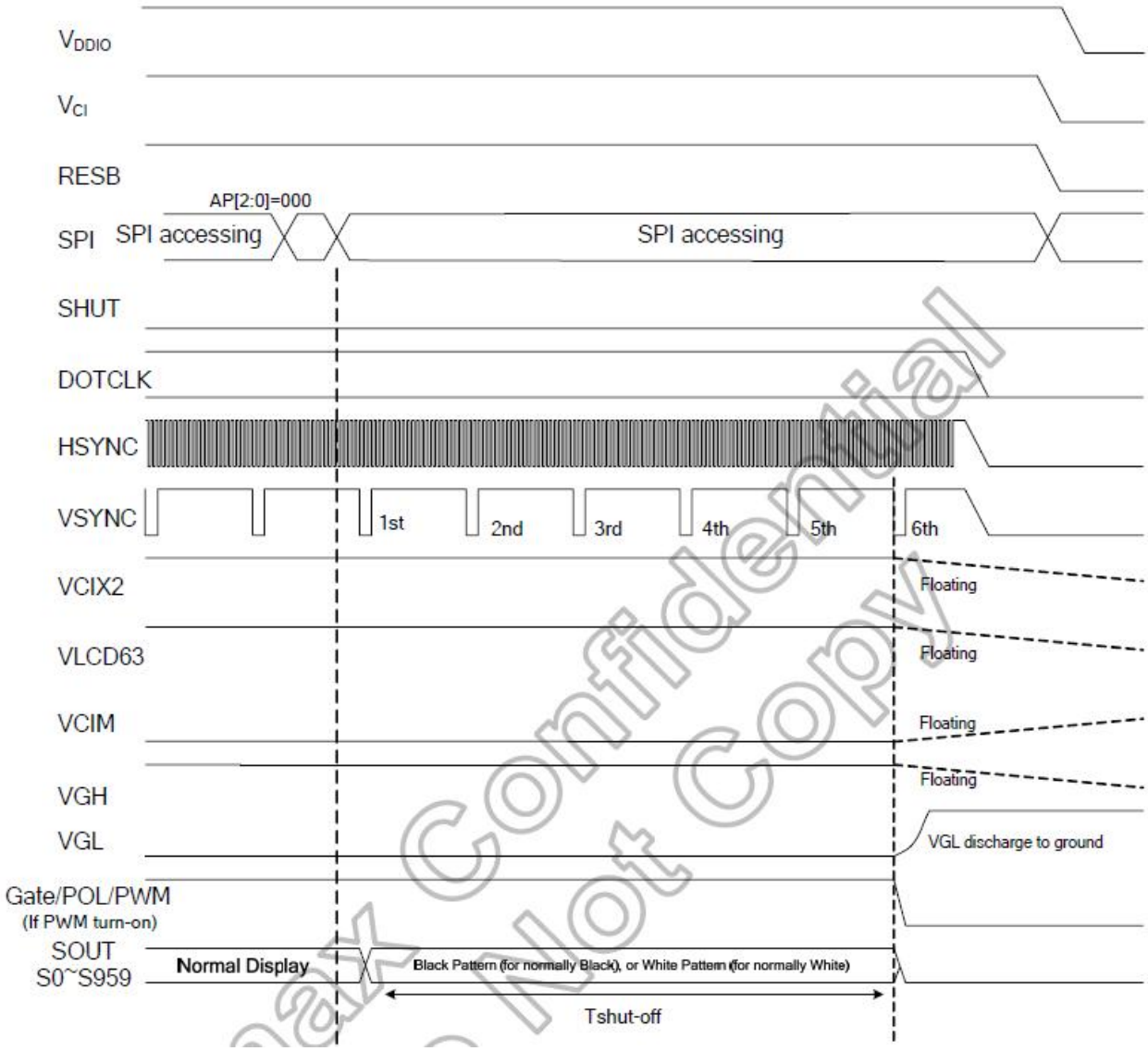


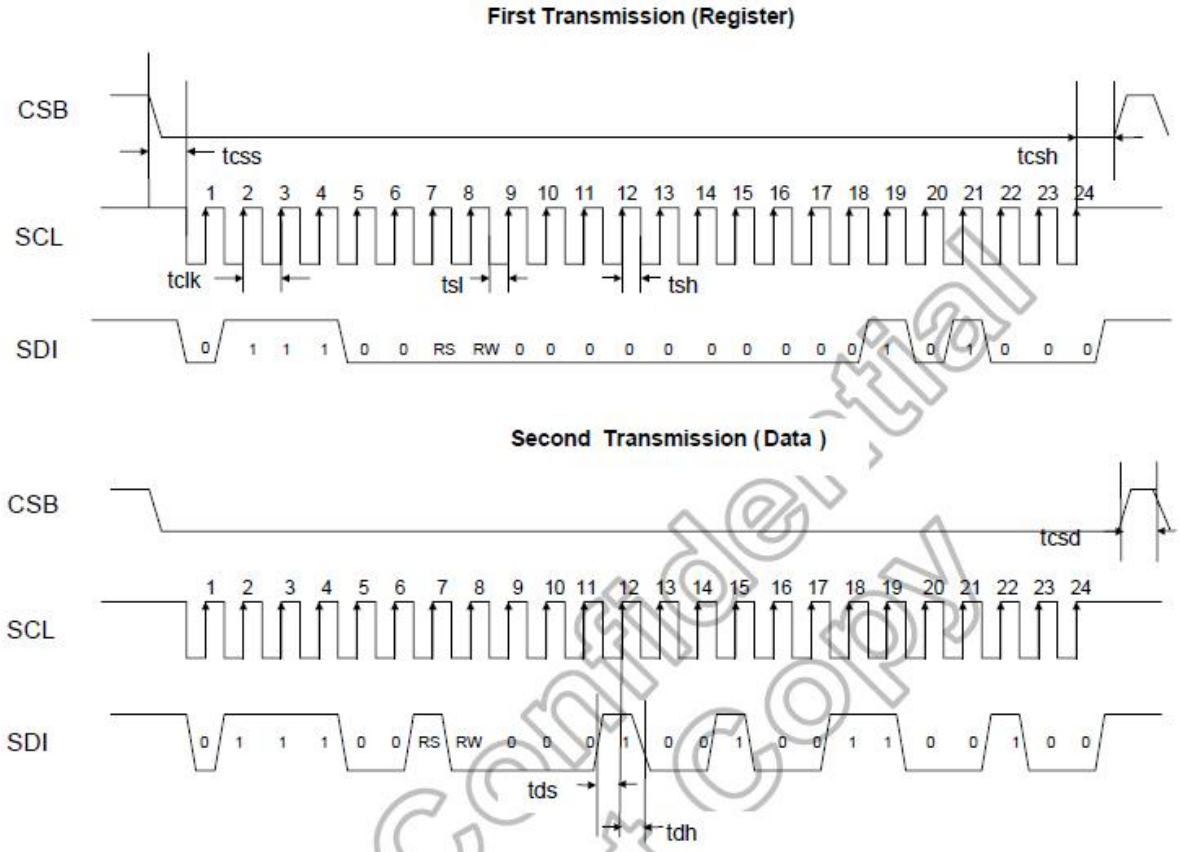
Figure 12. 12: Power down sequence

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Rising edge of SHUT to display off -1 line: 408 clk -1 frame: 262 line -DOTCLK=6.5MHz	tshut-off	-	-	6	frame

Note: DOTCLK must be maintained at lease 6 frames after the rising edge of SHUT.
Display become off at the 6th falling edge of VSYNC after the rising edge of SHUT.
If RESET signal is necessary for power down, provide it after the 6-frames-cycle of the SHUT period.



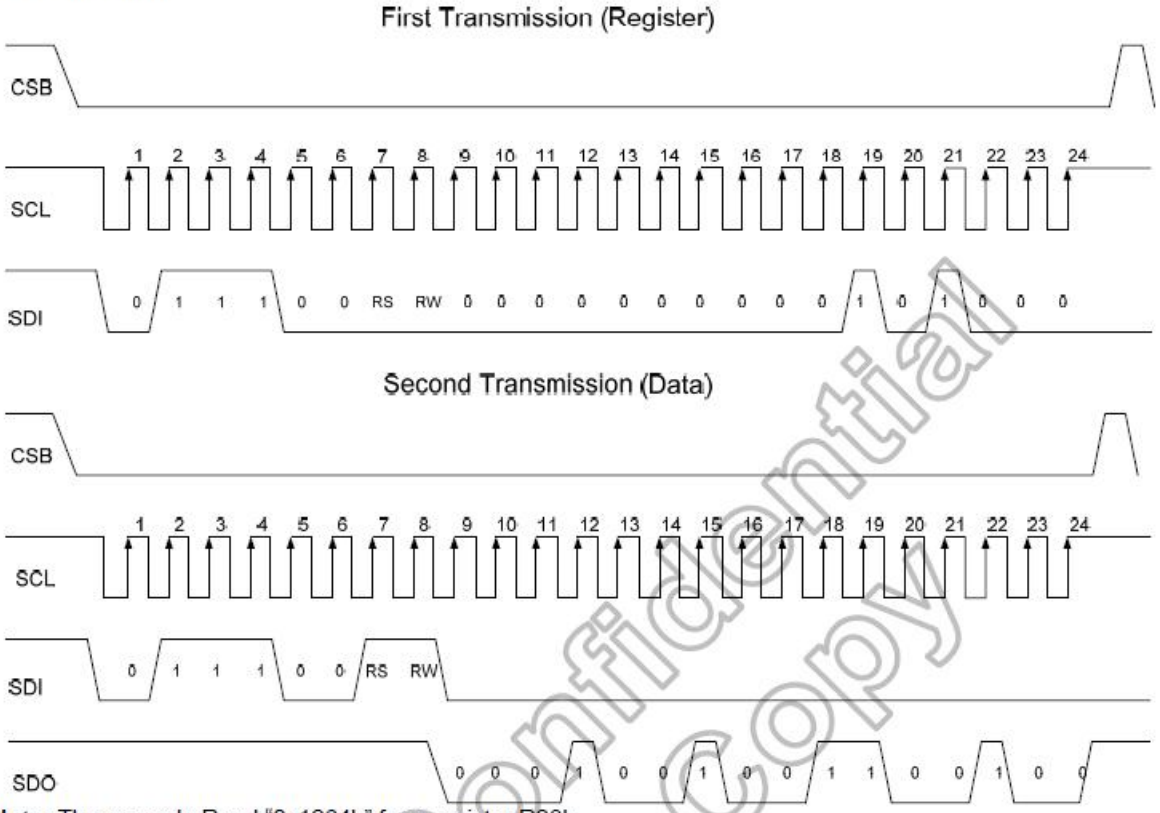
- Write SPI



Note: The example writes "0x1264h" to register R28h.
SPID connected to VSS.

Figure 12. 14: (a) SPI interface timing diagram & write SPI example

- Read SPI



Note: The example Read "0x1264h" from register R28h.

Figure 12. 15: (b) SPI interface timing diagram & read SPI example

Figure 12. 16: Rising/Falling time

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Clock Rising Time	trs	-	-	30	ns
Clock Falling Time	tfl	-	-	30	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

6.2 DC Electrical Characteristics

DC characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.2V, T_A = 25℃)

Symbol	Parameter	Test condition	Spec.			Unit
			Min.	Typ.	Max.	
V_{DD}	System power supply pins of the logic block	Recommend Operating Voltage Possible Operating Voltage	1.8	-	2.50	V
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.8	-	3.6	V
V_{CI}	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO	-	3.6	V
I_{sleep}	Sleep mode current	-	-	50	-	μA
I_{dp}	Operating mode current	VCI=3.3V	-	10	12	mA
V_{CIM}	Negative V_{CI} Output Voltage	No panel loading	- VCI	-	- VCI+0.7	V
V_{CIX2}	V_{CIX2} primary booster efficiency(1)	No panel loading, ITO for V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	83	90	-	%
V_{GH}	Gate driver High Output Voltage Booster efficiency(2)	No panel loading; 4x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	84	89.5	-	%
		No panel loading; 5x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	80	88.5	-	%
		No panel loading; 6x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	72	80	-	%
V_{GL}	Gate driver Low Output Voltage	-	- V_{GH}		-5.1	V
V_{COMH}	VCOM High Output Voltage	-	-	-	5.54	V
V_{COML}	VCOM Low Output Voltage	-	V_{CIM}+0.5	-	-	V
V_{COMA}	VCOM Amplitude	-	-	-	6	V
V_{LCD63}	V_{LCD63} Output Voltage	-	-	-	5.57	V
△V_{LCD63}	Max. Source Voltage Variation	-	-2	-	2	%
V_{OH1}	Logic High Output Voltage	Iout = -100μA	0.9V_{DDIO}	-	V_{DD}	V
V_{VD}	Source Output Voltage Deviation	-	-	±20	-	mV
V_{OS}	Source Output Voltage Offset	-	-	-	±30	mV
V_{OL1}	Logic Low Output Voltage	Iout = 100μA	0	-	0.1V_{DDIO}	V
V_{IH1}	Logic High Input voltage	-	0.8V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage	-	0	-	0.2V_{DDIO}	V
I_{OH}	Logic High Output Current Source	V out = VDD – 0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	V out = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source	-	-1	-	1	μA
$I_{IL/I\ IH}$	Logic Input Current	-	-1	-	1	μA
C_{IN}	Logic Pins Input Capacitance	-	-	5	7.5	pF
R_{SON}	Source drivers output resistance	-	-	1	-	kΩ
R_{GON}	Gate drivers output resistance	-	-	500	-	Ω
R_{COM}	VCOM output resistance	-	-	200	-	Ω

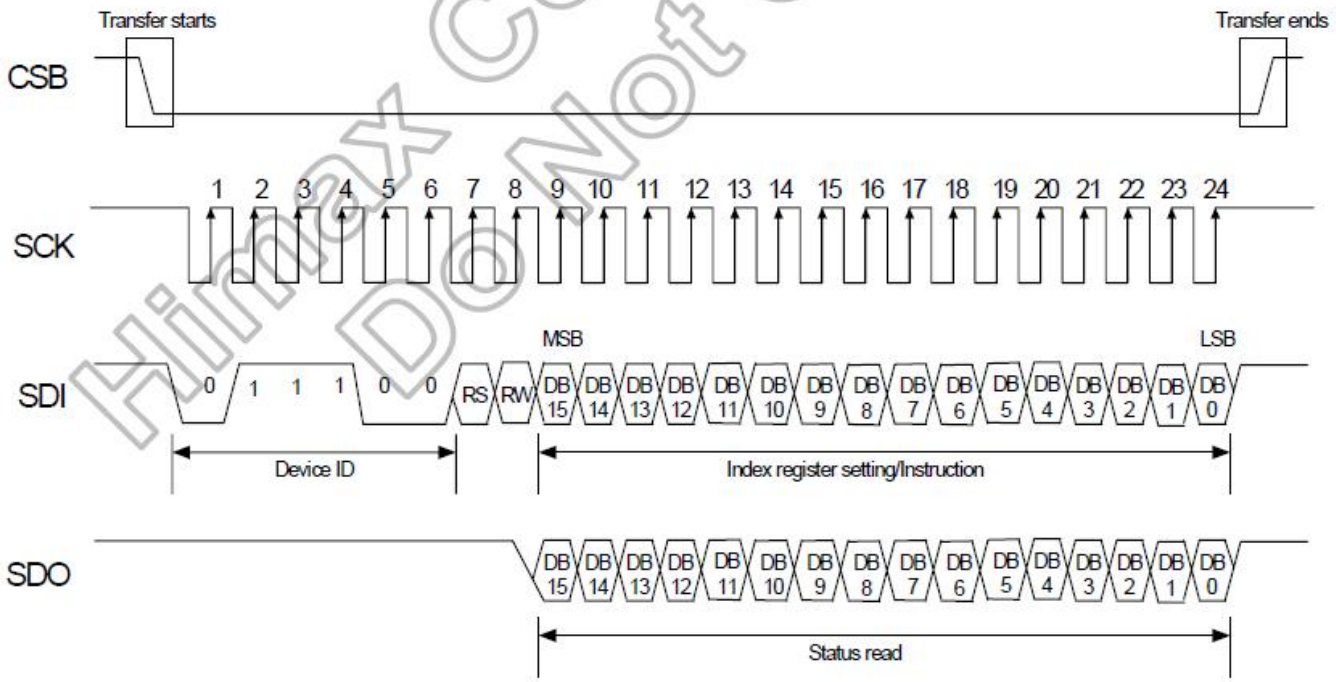
Note : (1) VCIX2 efficiency=VCIX2 / (2 x VCI) x 100%
(2) VGH efficiency=VGH / (VCI x n) x 100% (where n=booster factor)

6.3 Serial interface

The SPI is available through the chip select line (CSB), serial transfer clock line (SCK), serial data input (SDI), and serial data output (SDO).

The Driver IC recognizes the start of data transfer at the falling edge of CSB input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CSB input. The Driver IC is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the Driver IC are compared and both 6-bit data correspond. The identification code must be 011100(Primary SPI Register) or 011101(Secondary SPI Register). Two different chip addresses must be assigned to the Driver IC because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When the RS=1, instruction write. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

After receiving the start byte, the Driver IC starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted (9th SCK started). All Driver IC instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (IB15 to 0---9th ~24th SCK).



7 Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	-	-	50	80	ms	FIG.1	Note4
Contrast Ratio		CR		-	350	-	-	FIG.2	Note1
Surface luminance		LV	θ =0°	-	350	-	cd/m2	FIG.2	Note2
Luminance uniformity		Yu	θ =0°	75	80	-	%	FIG.2	Note3
NTSC		-	θ =0°	-	50	-	%	FIG.2	Note5
Viewing angle		θ Cr>10	θ_T	-	65	-	deg	FIG.3	Note6
			θ_B	-	55	-	deg	FIG.3	
			θ_L	-	65	-	deg	FIG.3	
			θ_R	-	65	-	deg	FIG.3	
Chromaticity	Red	R_X	θ =0° ∅ =0° Ta=25°	0.609	0.639	0.669	-	FIG.2 CIE1931	Note5
		R_Y		0.314	0.344	0.374	-		
	Green	G_X		0.264	0.294	0.324	-		
		G_Y		0.557	0.587	0.617	-		
	Blue	B_X		0.102	0.132	0.162	-		
		B_Y		0.106	0.136	0.166	-		
	White	W_X		0.282	0.312	0.342	-		
		W_Y		0.319	0.349	0.379	-		

Note1. Definition of contrast ratio

Contrast ratio(Cr) is defined mathematically by the following formula. For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the “White” state}}{\text{Luminance measured when LCD on the “Black” state}}$$

For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON’s BM-5 or BM-7 photo detector or compatible.

Note2. Definition of surface luminance.

Surface luminance is the luminance with all pixels displaying white. For more information see FIG.2.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note3. Definition of luminance uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$YU = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note4. Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state.Rise time (Tr) is the time between photo detector output intensity changed from 90% to 10%. And fall time (Tf) is the time between photo detector output intensity changed from 10% to 90%.

For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)

CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10. Angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG.3.

For viewing angle and response time testing, the testing data is base on Autronic-Melchers’s ConoScope or DMS series Instruments or compatible.

FIG.1.The definition of response Time

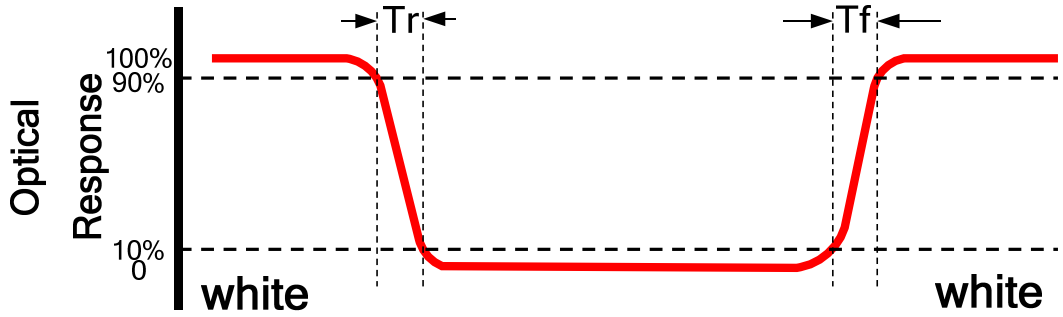


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

Size : S≤5”(see Figure a) A : 5 mm B : 5 mm
H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure a.
measurement instrument : TOPCON’s luminance meter BM-5 or BM-7 or compatible (see Figure c).

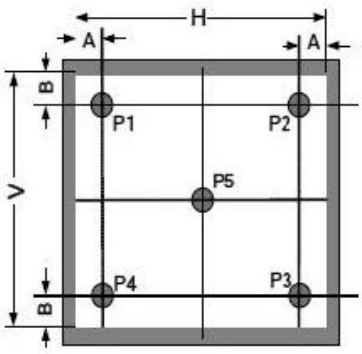
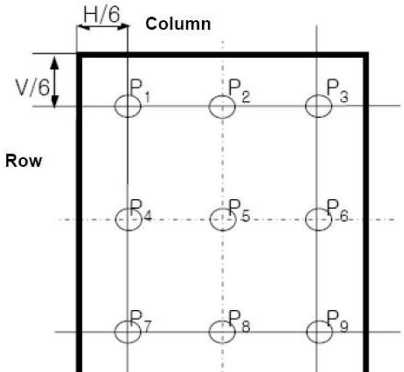


Figure a

Size : 5”＜S≤12.3”(see Figure b) H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure b.
measurement instrument : TOPCON’s luminance meter BM-5 or



BM-7 or compatible (see Figure c).

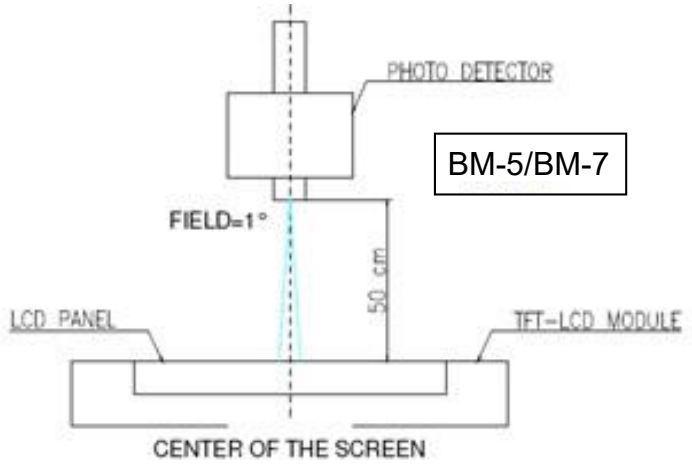
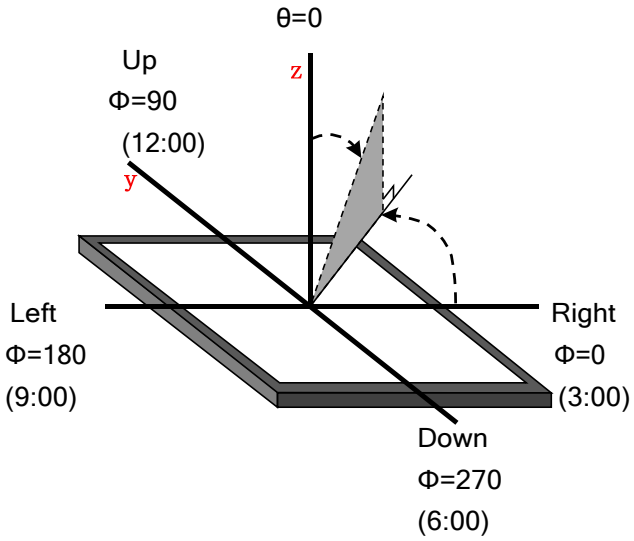


Figure b

Figure c

FIG.3.The definition of viewing angle

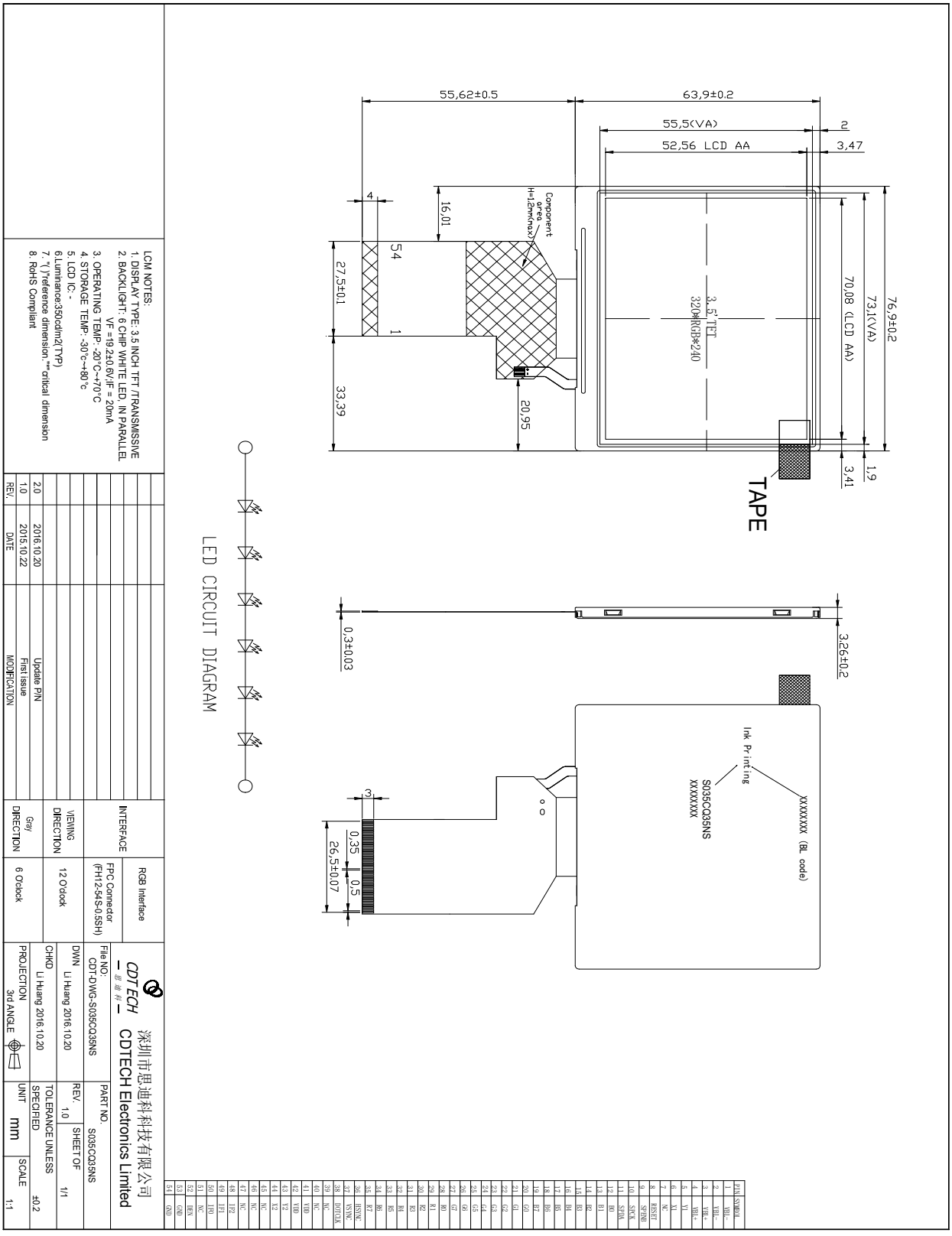


8 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts= +70℃, 96hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Operation	Ta= -20℃, 96hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 120hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 120hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max,120 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-20℃ 30 min ~ +70℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Operation)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y , ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note:1. Ts is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.
3. The size of sample is 5pcs.

9 Mechanical Drawing



10 Packing

Packing Method

TBD

11.Precautions for Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

11.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.