PRODUCT SPECIFICATION

CDTECH Model: **S035GQ94ES-DC37**

CUSTOMER Model: -

Description: **3.5” TFT-LCD Module with CTP**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2023.3.9	2023.3.9	2023.3.9

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
1.0	2023-3-9	First Release	-

Contents

1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	3.5	inch
Number of Pixels	320 (H) RGB x 240 (V)	pixels
Display Mode	Normally White	-
Viewing Direction	12 o' clock	o' clock
Interface	MCU	-
Display Colors	65K	colors
Outline Dimension	76.90 (H) x 63.90 (V) x 4.89 (D)	mm
Active Area	70.08 (H) x 52.58 (V)	mm
Pixel Pitch	0.219 (H) x 0.219 (V)	mm
Driver IC	D2119MIZF	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃

1.2 Touch Panel Information

Item	Specification
Touch Structure	G+G
Bonding Type with LCM	Perimeter Bonding
Driver IC	GT911
Interface	I²C
Touch Count Max	5 Points
Surface treatment	-
Surface hardness	6H
I2C slave address	0x28
Origin of coordinate	Top Left Corner

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VDD	-0.3	5.0	V	Note 1
Digital supply voltage	VDDIO	-0.3	3.6	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

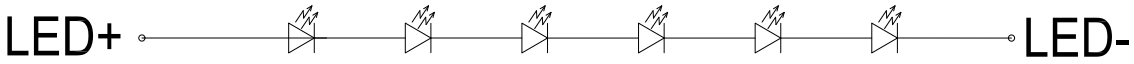
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VCI	3.0	3.3	3.6	V	
Analog supply current	I_{VCI}	-	TBD	-	mA	VCI=3.3V
Logic supply voltage	VDDIO	1.65	1.8	3.3	V	
Logic supply current	I_{VDDIO}	-	TBD	-	mA	VDDIO=1.8V
Logic input voltage	VIH	0.7*VDDIO	-	VDDIO	V	
	VIL	GND	-	0.3*VDDIO	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	20	-	mA	
Driving Voltage	V_F	18.0	19.2	20.4	V	
Power consumption	W_{BL}	0.360	0.384	0.408	W	
LED Life-Time	N/A	-	50,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



3.3 Touch Panel

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply voltage	VDD	-	3.3	-	V	
Analog supply current	I_{VDD}	-	TBD	-	mA	VDD=3.3V
Input high-level voltage	VIH	0.7*VDD	-	VDD	V	
Input low -level voltage	VIL	GND	-	0.3*VDD	V	

4. Interface Pin Assignment

4.1 LCM Pin Assignment

Recommended connector：FH12-20S-0.5SH manufactured by HIROSE

No.	Symbol	Description
1	VCI	Power supply
2	VDDIO	Voltage input pin for logic
3	VSS	Ground
4	RESET	Global reset pin
5	CS	Chip select
6	RS	Data or Command select PIN
7	RD	Serve as a read signal
8	WR	Write signal
9-16	D7-D0	Data bus
17	VSS	Ground
18	LEDK	Power for LED backlight (Cathode)
19	NC	No connection
20	LEDA	Power for LED backlight (Anode)

4.2 Touch FPC Pin Assignment

No.	Symbol	Description
1	GND	Ground
2	VDD	Power supply
3	INT	Interrupt signal from CTP
4	SDA	I2C data input and output
5	SCL	I2C clock input
6	RST	Reset pin

5. Interface Characteristics

5.1 AC Electrical Characteristics

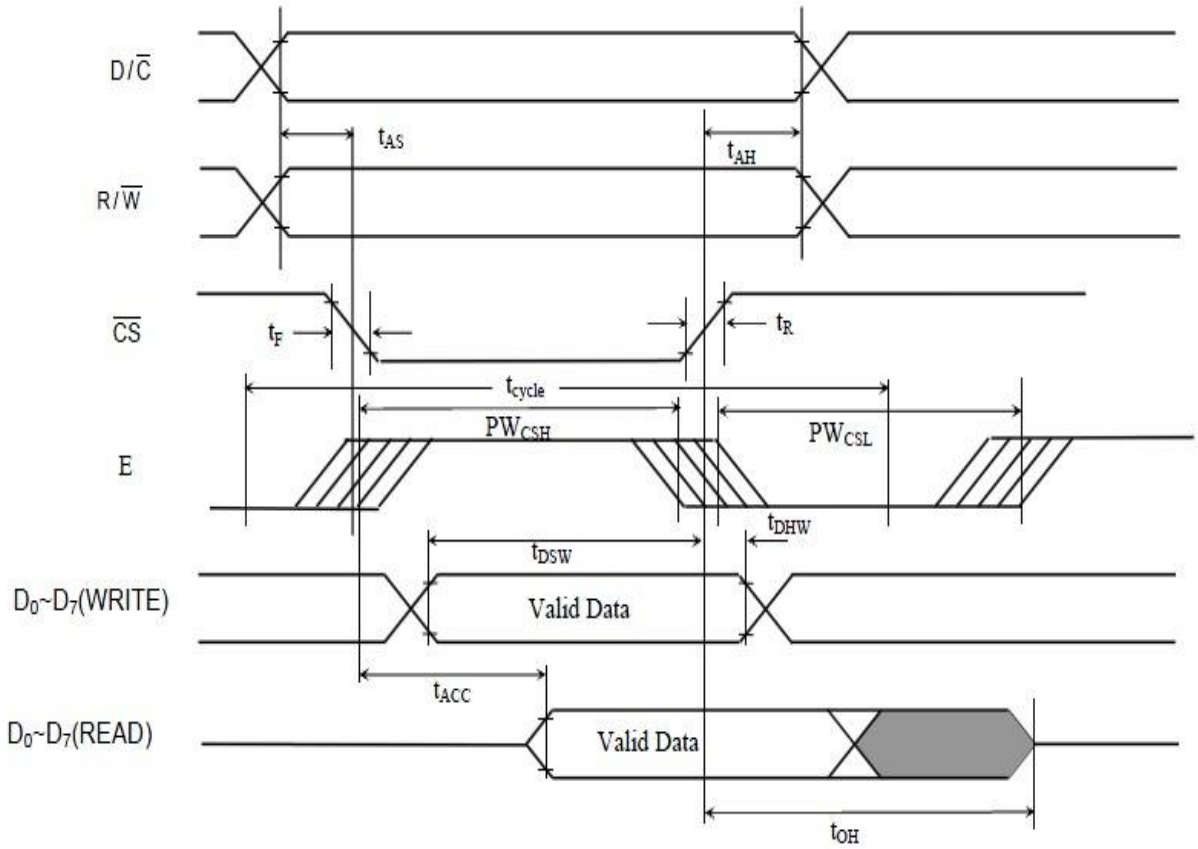
5.1.1 Parallel 6800-series Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS}	Address Setup Time (R/$\overline{W}$)	0	-	-	ns
t_{AH}	Address Hold Time (R/$\overline{W}$)	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time (/CS)	-	-	4	ns
t_F	Fall time (/CS)	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Figure 13-1: Parallel 6800-series Interface Timing Characteristics



5.1.2 Parallel 8080 Timing Characteristics

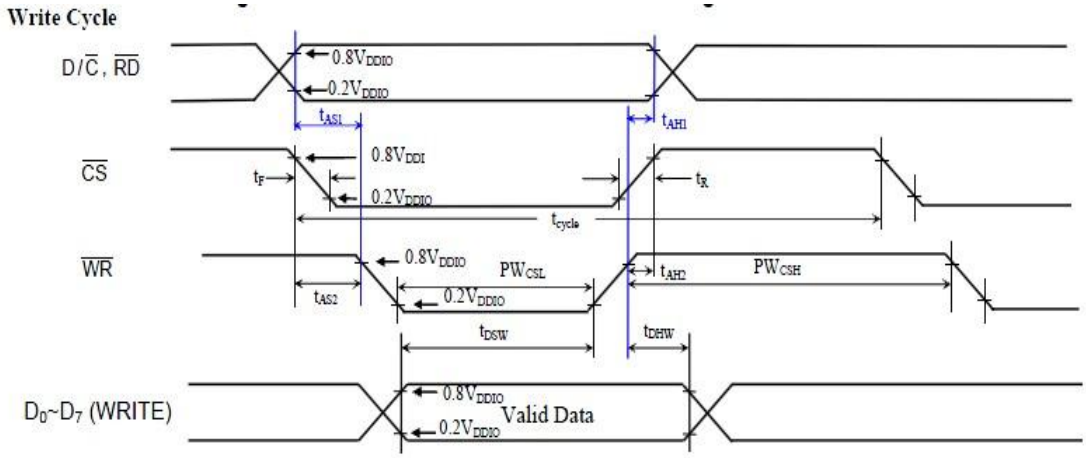
Table 13-2: Parallel 8080 Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS1}	Address Setup Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AH1}	Address Hold Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AS2}	Address Setup Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{AH2}	Address Hold Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time (/CS)	-	-	4	ns
t_F	Fall time (/CS)	-	-	4	ns

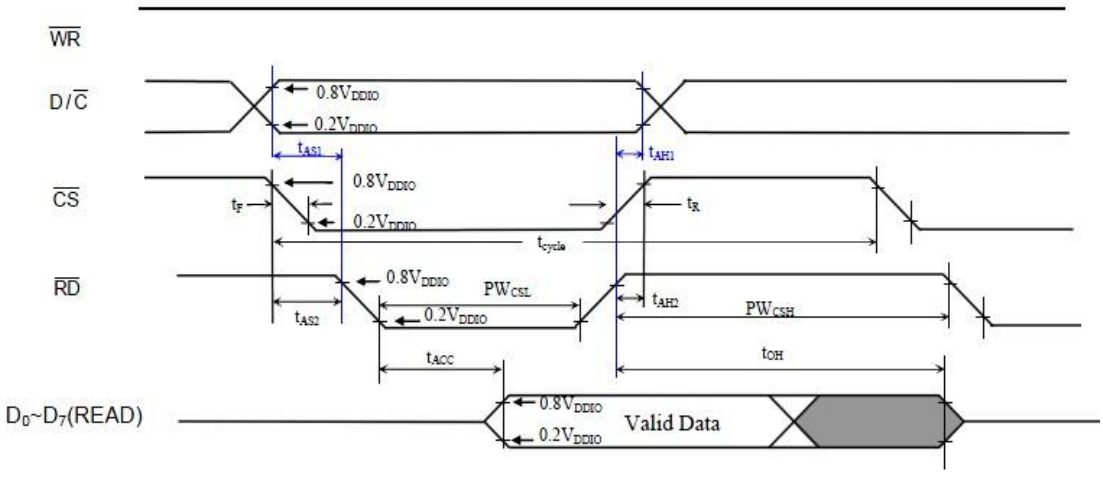
Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Write Cycle



Remark: It's highly recommended that $\overline{RD}$ remains high for the whole write cycle

Read Cycle



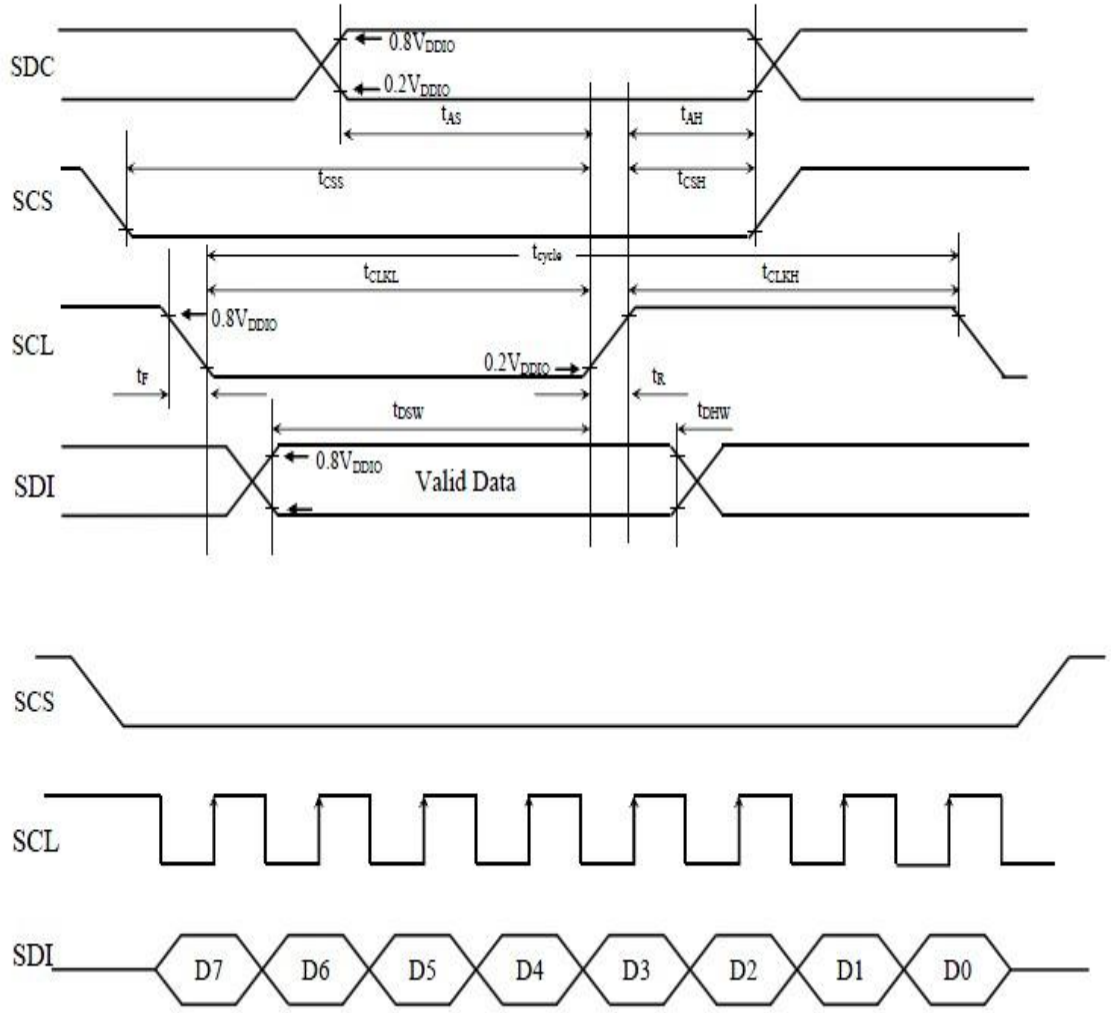
5.1.3 Serial Timing Characteristics

Table 13-3: Serial Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

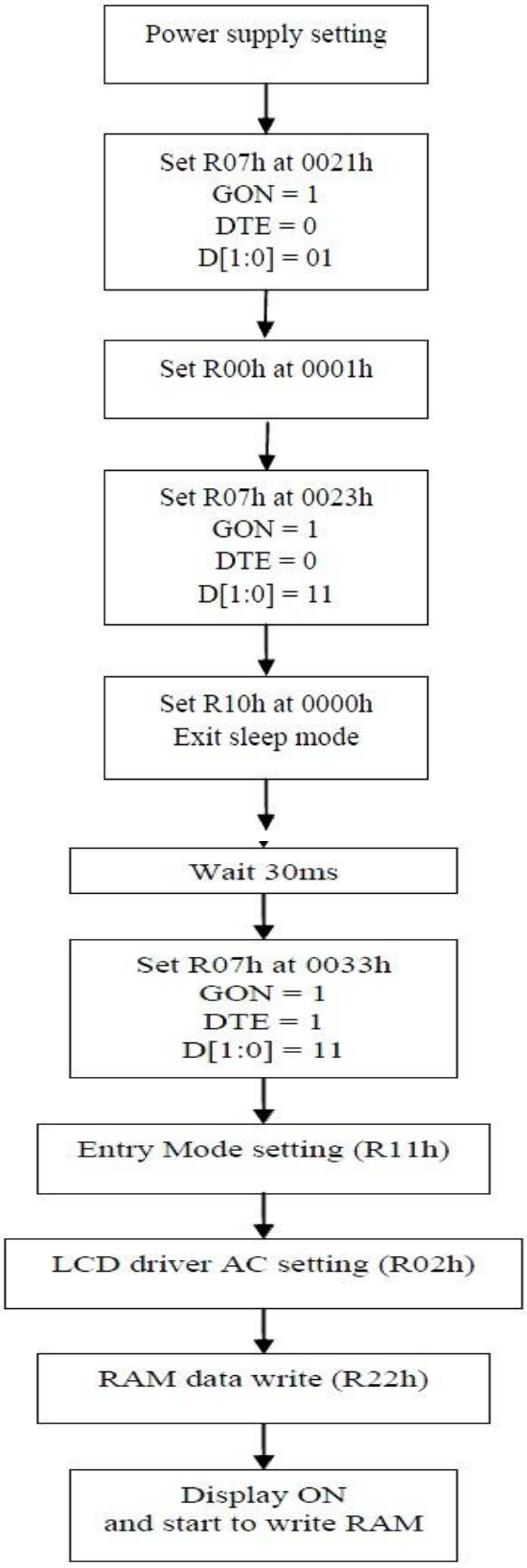
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Figure 13-3: 4 wire Serial Timing Characteristics

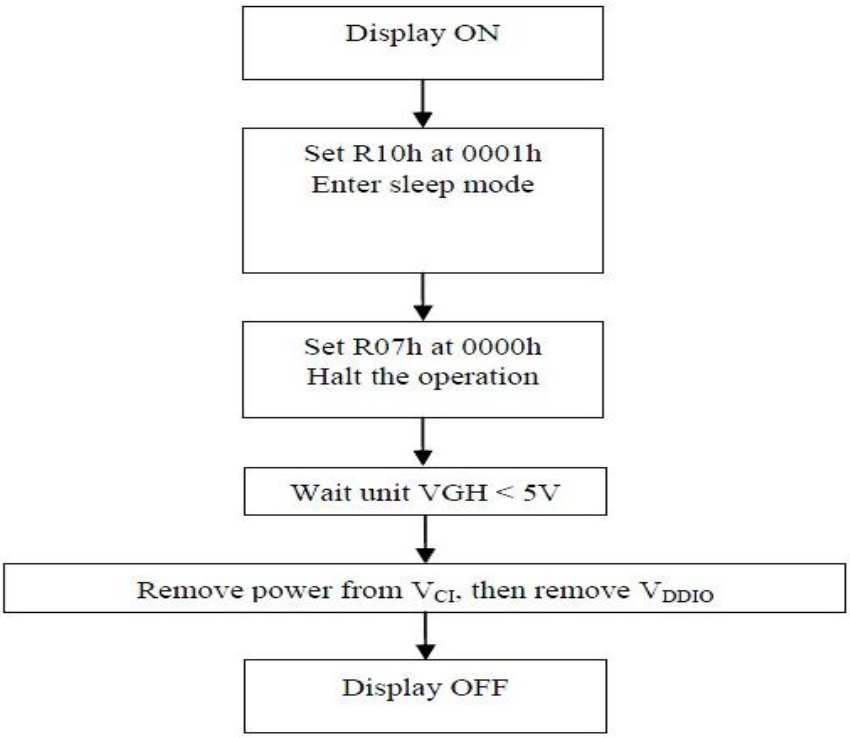


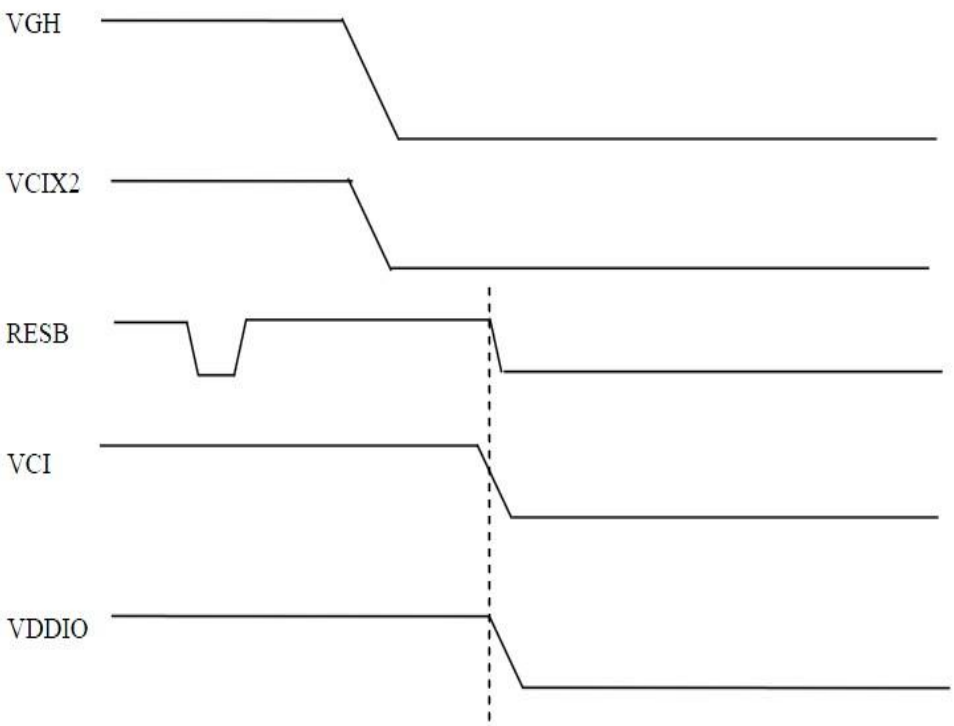
5.2 Power on/off sequence

5.2.1 Power On Sequence:



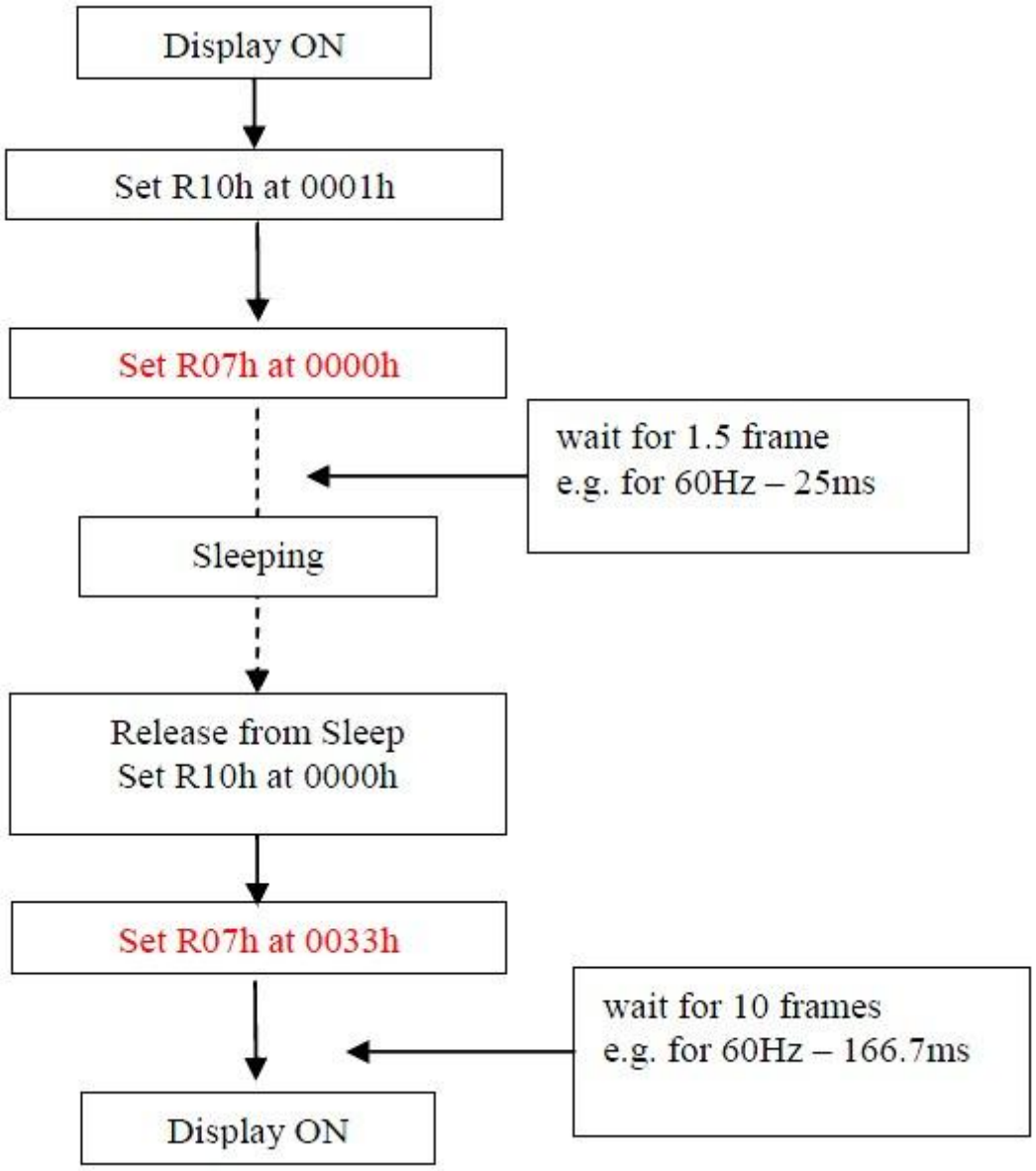
5.2.2 Display Off Sequence:



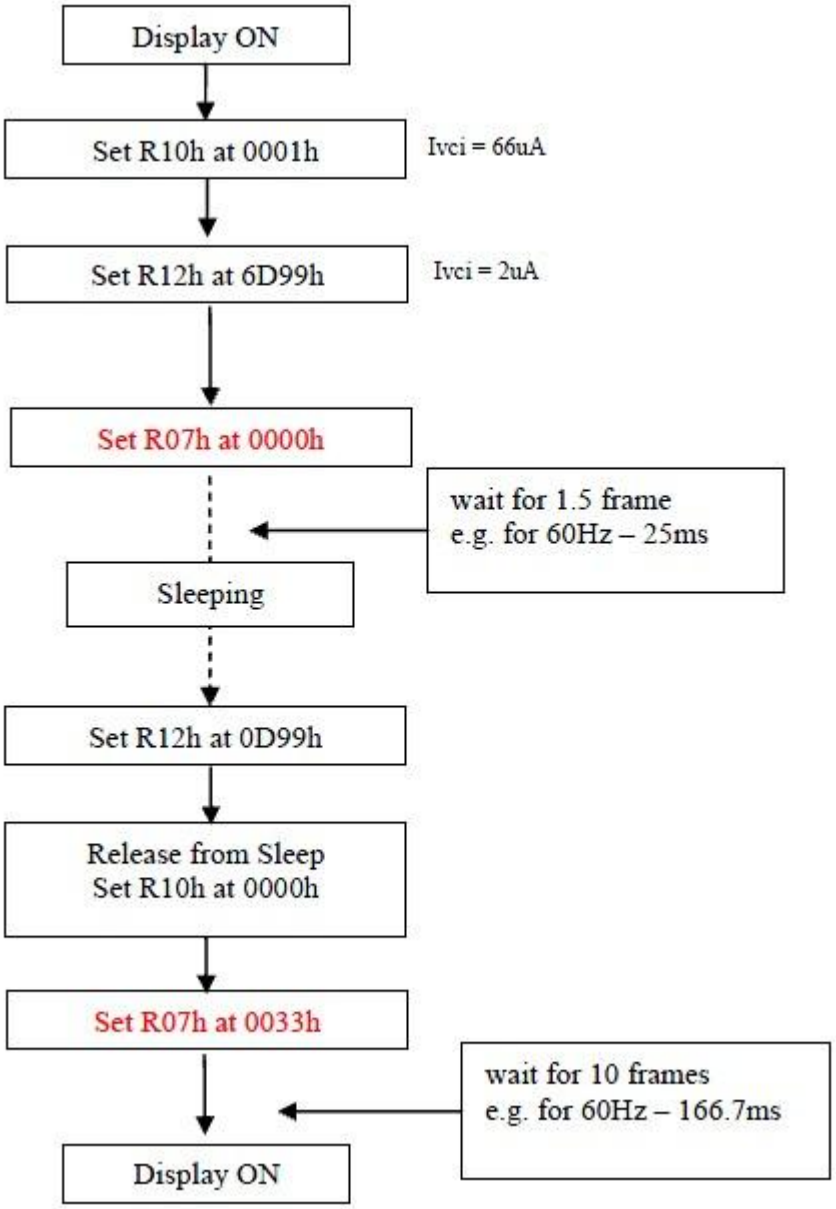


Note:
1. VDDIO should be the last to fall, or VCI/VDDIO could be power off at the same time
2. If OTP is active in the application, the OTP programming voltage should be turned off and cap discharged before VCI/VDDIO are turned off.

5.2.3 Sleep Mode Display Sequence:



5.2.4 Deep Sleep Mode Display Sequence:



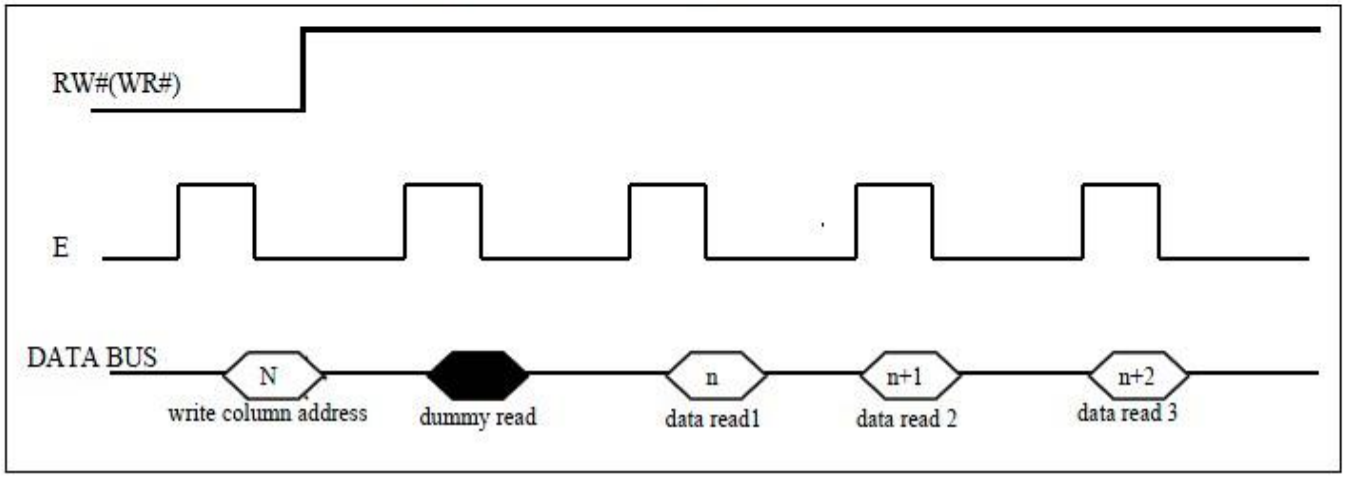
5.3 Interface

5.3.1 System Interface

MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins D[17:0], RW, DC, E and CS.
RW input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or status register. RW input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of DC input.
The E input served as data latch signal (clock) when high provided that CS is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

Figure 7-1: Read Display Data



MPU Parallel 8080-series Interface

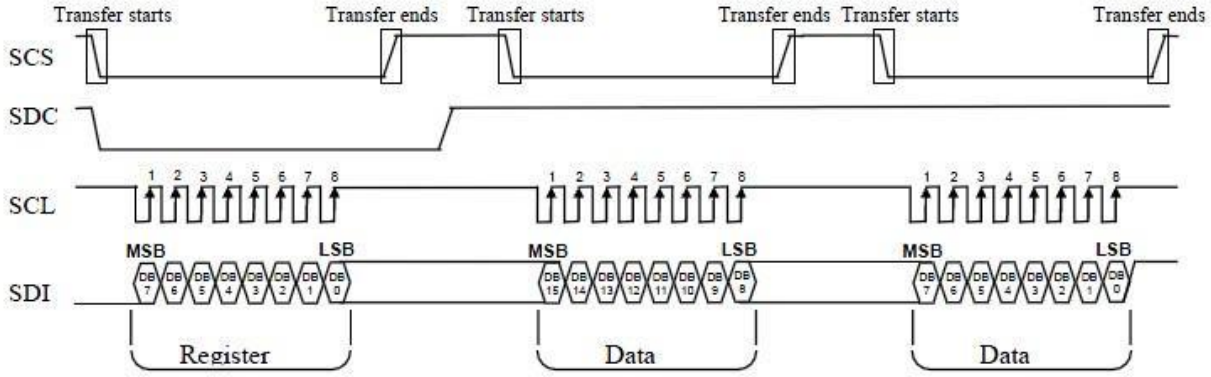
The parallel interface consists of 18 bi-directional data pins D[17:0], WR, DC, and CS.
RD input served as data read latch signal (clock) when low provided that CS is low. Weather reading the display data from GDDRAM or reading the status from the status register is controlled by DC.
WR input served as data write latch signal (clock) when low provided that CS is low. Weather writing the display data to the GDDRAM or writing the command to the command register is controlled by DC. A dummy read is also required before the first actual display data read for 8080-series interface.
Please refer to .

5.3.2 Serial Interface

4-wire Serial Peripheral Interface (8 bits)

The clock synchronized serial peripheral interface (SPI) using the chip select line (SCS), serial transfer clock line (SCL), serial input data (SDI). The serial data transfer starts at the falling edge of SCS input and ends at the rising edge of SCS.
SDC determinates the data of SDI which is register or data.

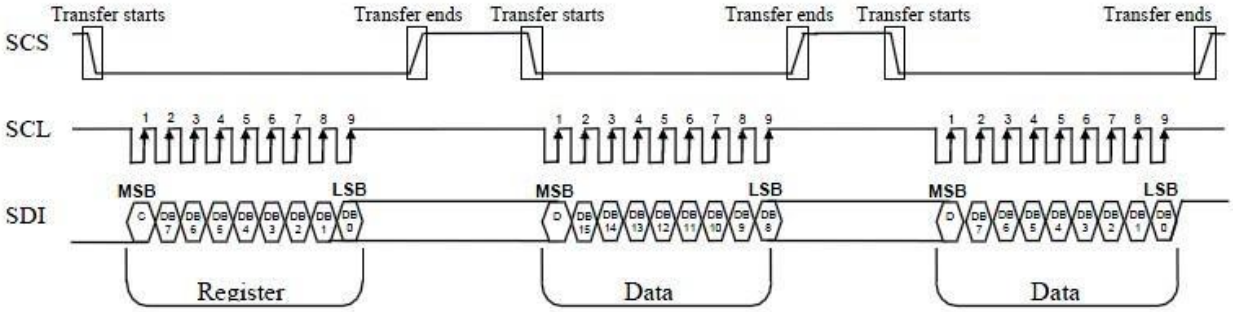
Figure 7-2: 4-wire SPI interface (8 bits)



3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while SDC is not use. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).

Figure 7-3: 3-wire SPI interface (9 bits)



5.4 Command List

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	GD	BGR	SM	TB	0	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	(3AEFh)			0	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6A64h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5308h)			0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R26h	Analogue Setting	0	1	0	RW_T	VCB	RLTM	ENN	0	0	0	0	0	0	0	0	0	0	0
	(3800h)			0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
R28h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

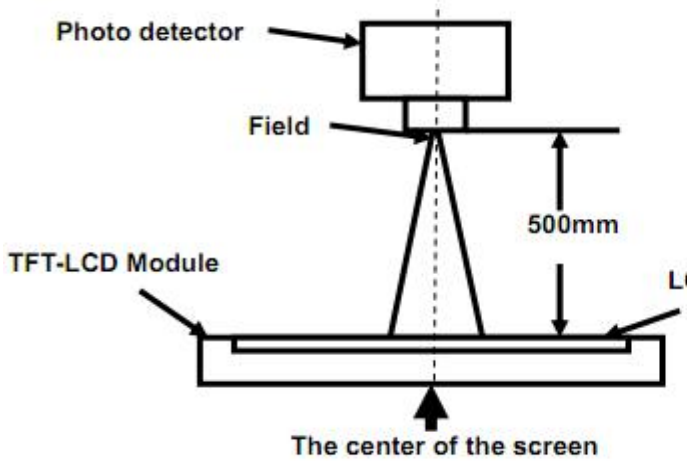
R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Horizontal RAM address start position	0	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Horizontal RAM address end position	0	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	XAD8	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	0	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	45	60	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	60	70	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	60	70	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	60	70	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	25	-	msec	Note4
	T_{OFF}		-	25	-	msec	Note4
Contrast Ratio	CR		320	400	-	-	Note1 Note3
Color Chromaticity	W_X		0.280	0.330	0.380	-	Note1 Note5
	W_Y		0.300	0.350	0.400	-	Note1 Note5
Luminance	L		580	680	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		-	50	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2:Definition of viewing angle range and measurement system
Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

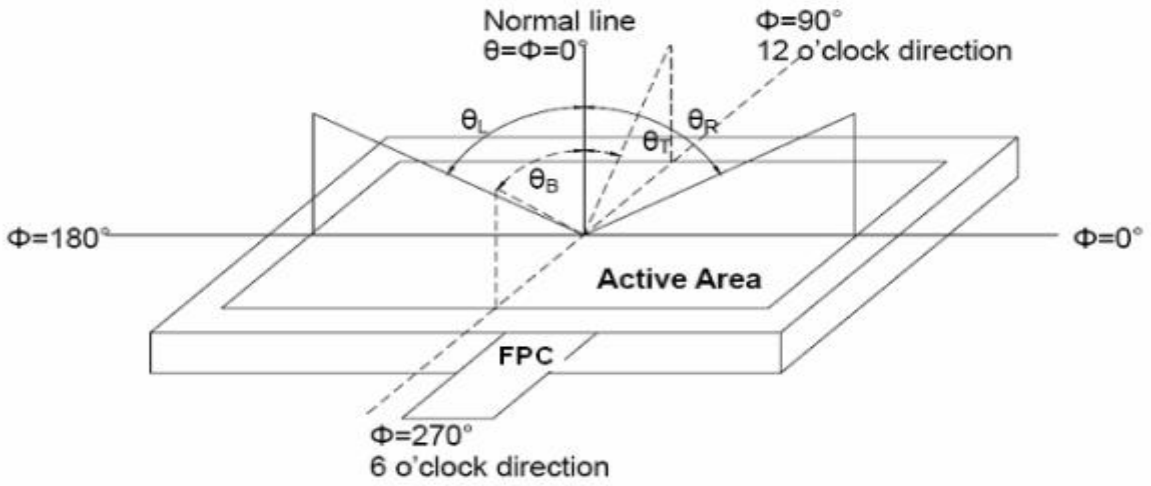


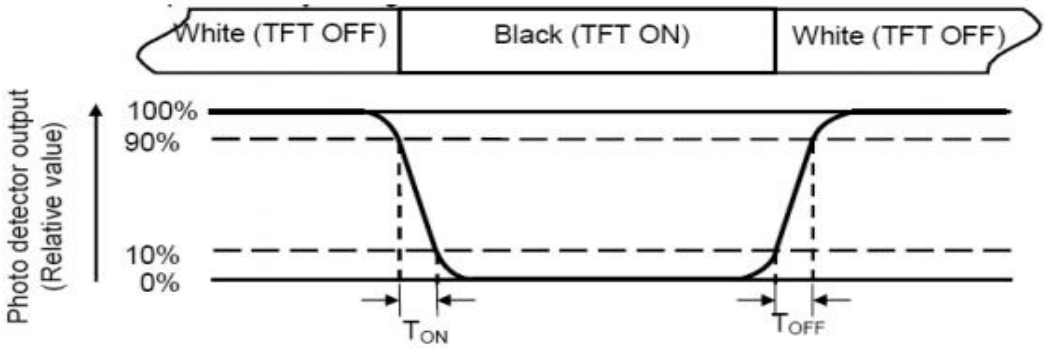
Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black”state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5:Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6:Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.2.

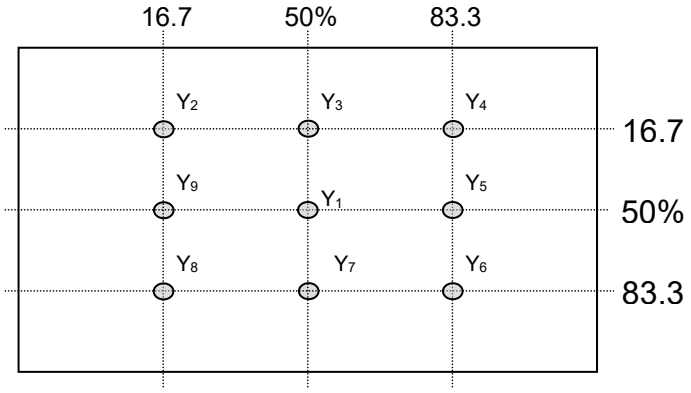


Fig. 2 Definition of points

Note 7:Definition of Luminance (Refer Fig. 2)

Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn).

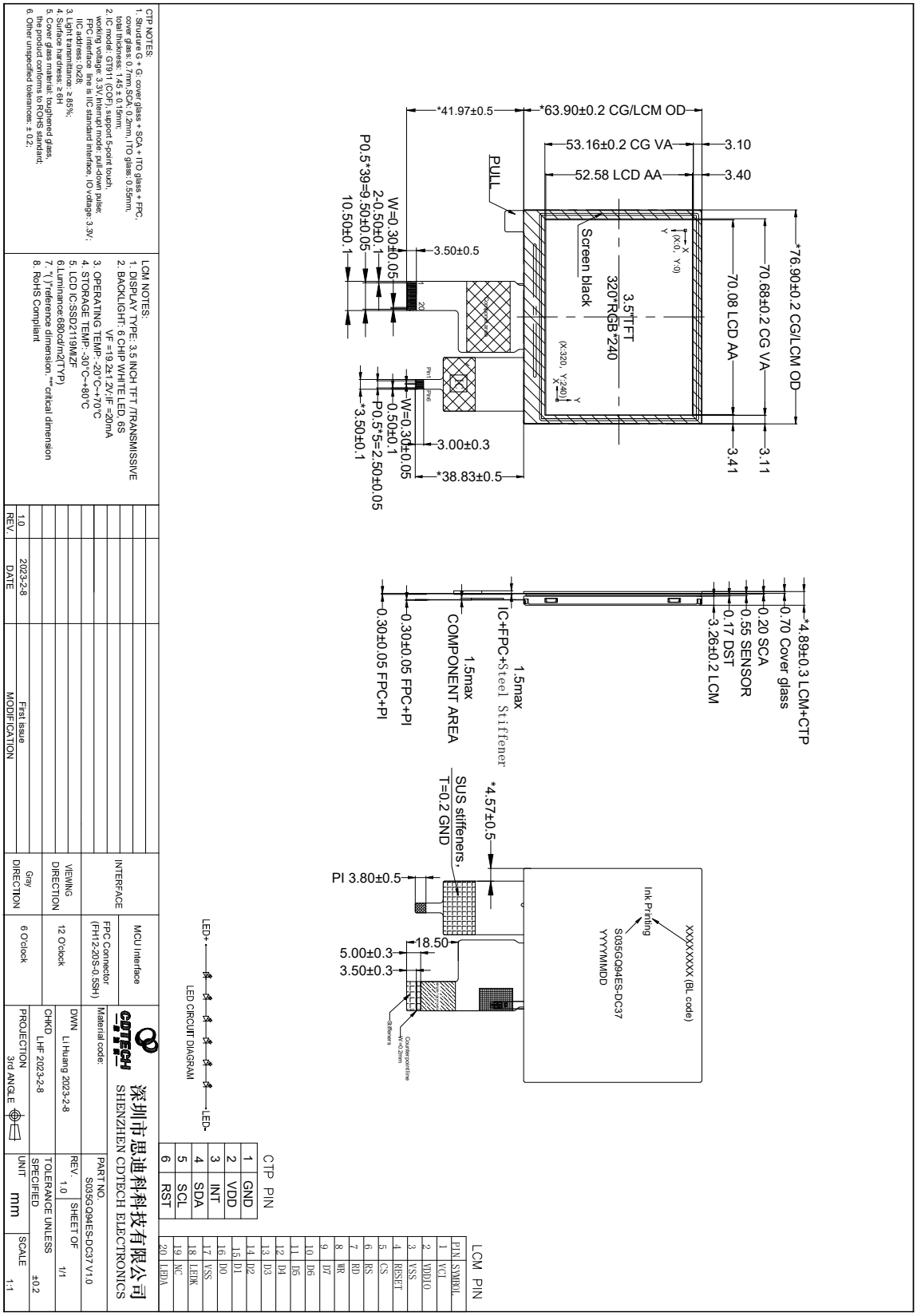
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +80℃	96hrs
Low Temperature Storage	Ta= -30℃	96hrs
High Temperature Operation	Ta= +70℃	96hrs
Low Temperature Operation	Ta= -20℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-30℃/30 min ~ +80℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



CTP NOTES:
1. Structure G + G: cover glass + SCA + ITO glass + FPC;
cover glass: 0.7mm SCA: 0.2mm; ITO glass: 0.55mm;
total thickness: 1.45 ± 0.15mm;
2. IC model: GT911 (OGF); support 5-point touch;
working voltage: 3.3V; communication mode: standard I2C;
FPC interface: line is IIC standard interface, IO voltage: 3.3V;
IIC address: 0x28;
3. Light transmittance: ≥ 85%;
4. Surface hardness: ≥ 6H
5. Cover glass material: toughened glass,
the product conforms to ROHS standard;
6. Other unspecified tolerances: ± 0.2;

LCM NOTES:
1. DISPLAY TYPE: 3.5 INCH TFT /TRANSMISSIVE
2. BACKLIGHT: 6 CHIP WHITE LED, 6S
VF = 19.2± 1.2V/ IF =20mA
3. OPERATING TEMP: -20°C~+70°C
4. STORAGE TEMP: -30°C~+80°C
5. LCD IC:SSD2119MZF
6.Luminance:680cd/m2(TYP)
7. *():reference dimension, ***:critical dimension
8. RoHS Compliant

REV.	DATE	MODIFICATION
1.0	2023-2-8	First issue

INTERFACE	MCU Interface
	FPC Connector (FH12-20S-0.5SH)
VIEWING DIRECTION	12 O'clock
	6 O'clock
Gray DIRECTION	

深圳市思迪科科技有限公司
SHENZHEN CDTECH ELECTRONICS

Material code:	PART NO. S035GQ94ES-DC37 V1.0
DWN Li Huang 2023-2-8	REV. 1.0 SHEET OF 1/1
CHKD LHF 2023-2-8	TOLERANCE UNLESS SPECIFIED ±0.2
PROJECTION 3rd ANGLE	UNIT mm SCALE 1:1

CTP PIN

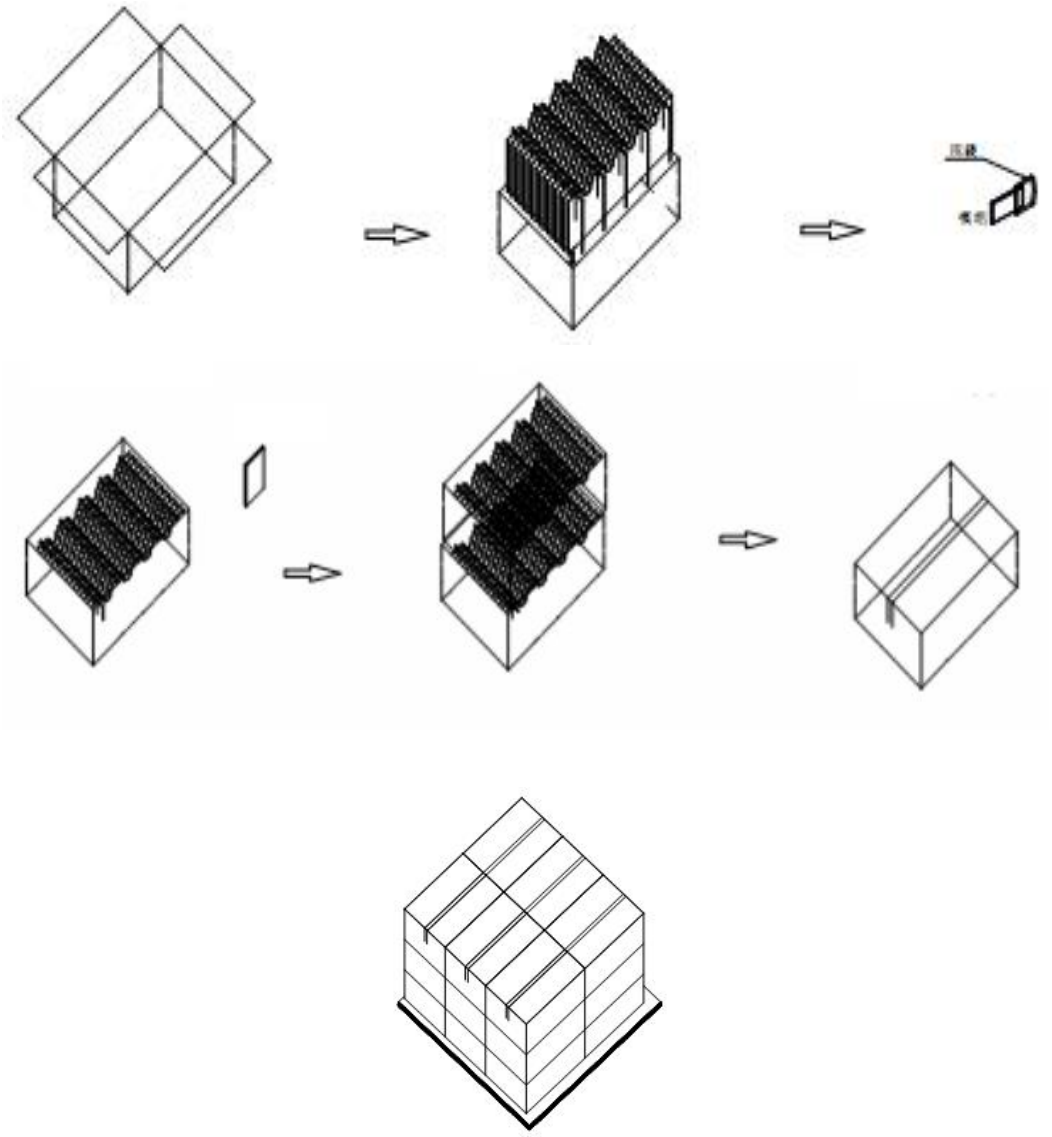
1	GND
2	VDD
3	INT
4	SDA
5	SCL
6	RST

LCM PIN

PIN	SYMBOL
1	VCI
2	VDDIO
3	VSS
4	RESET
5	CS
6	RS
7	RD
8	WR
9	D7
10	D6
11	D5
12	D4
13	D3
14	D2
15	D1
16	D0
17	VSS
18	LEDK
19	NC
20	LEDA

9. Packing

Packing Method



Steps:
1. Put module into tray cavity
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above
4. Fix the cardboard to the tray stack with adhesive tape
5. Put the tray stack into carton
6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.