PRODUCT SPECIFICATION

CDTECH Model: **S035BV108HN-DC49-D**

CUSTOMER Model: -

Description: **3.5 ” TFT-LCD Module with CTP**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2025.9.5	2025.9.5	2025.9.5

CUSTOMER APPROVAL	SIGNATURE	DATE

Record of Revisions

Version	Revise Date	Description	Page
1.0	2025-9-5	First Release	-

Contents

1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	3.5	inch
Number of Pixels	640 (H) RGB x 480 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	85/85/85/85	-
Interface	RGB	-
Display Colors	16.7M	colors
Outline Dimension	86.40 (H) x 72.15 (V) x 5.07 (D)	mm
Active Area	70.08 (H) x 52.56 (V)	mm
Pixel Pitch	0.1095 (H) x 0.1095 (V)	mm
Driver IC	NV3052C	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃

1.2 Touch Panel Information

Item	Specification
Touch Structure	G+G
Bonding Type with LCM	Perimeter Bonding
Driver IC	GT911
Interface	I²C
Touch Count Max	5 Points
Surface treatment	-
Surface hardness	6H
I2C slave address	0x28
Origin of coordinate	Down Right Corner

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	VDD	-0.3	4.5	V	Note 1

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

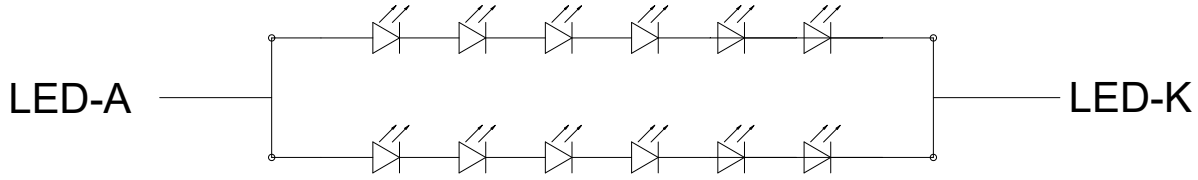
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VDD	3.0	3.3	3.6	V	
Analog supply current	I_{VDD}	-	30	40	mA	VDD=3.3V（PHOTO）
Logic input voltage	VIH	0.7*VDD	-	VDD	V	
	VIL	GND	-	0.3*VDD	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	40	-	mA	
Driving Voltage	V_F	16.2	-	20.4	V	
Power consumption	W_{BL}	0.648	-	0.816	W	
LED Life-Time	N/A	-	30,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



3.3 Touch Panel

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply voltage	CTP_VDD	-	3.3	-	V	
Analog supply current	I_{VCC}	-	15	-	mA	CTP_VDD=3.3V
Input high-level voltage	VIH	0.7*CTP_VDD	-	CTP_VDD	V	
Input low -level voltage	VIL	GND	-	0.3*CTP_VDD	V	

4. Interface Pin Assignment

4.1 LCM Pin Assignment

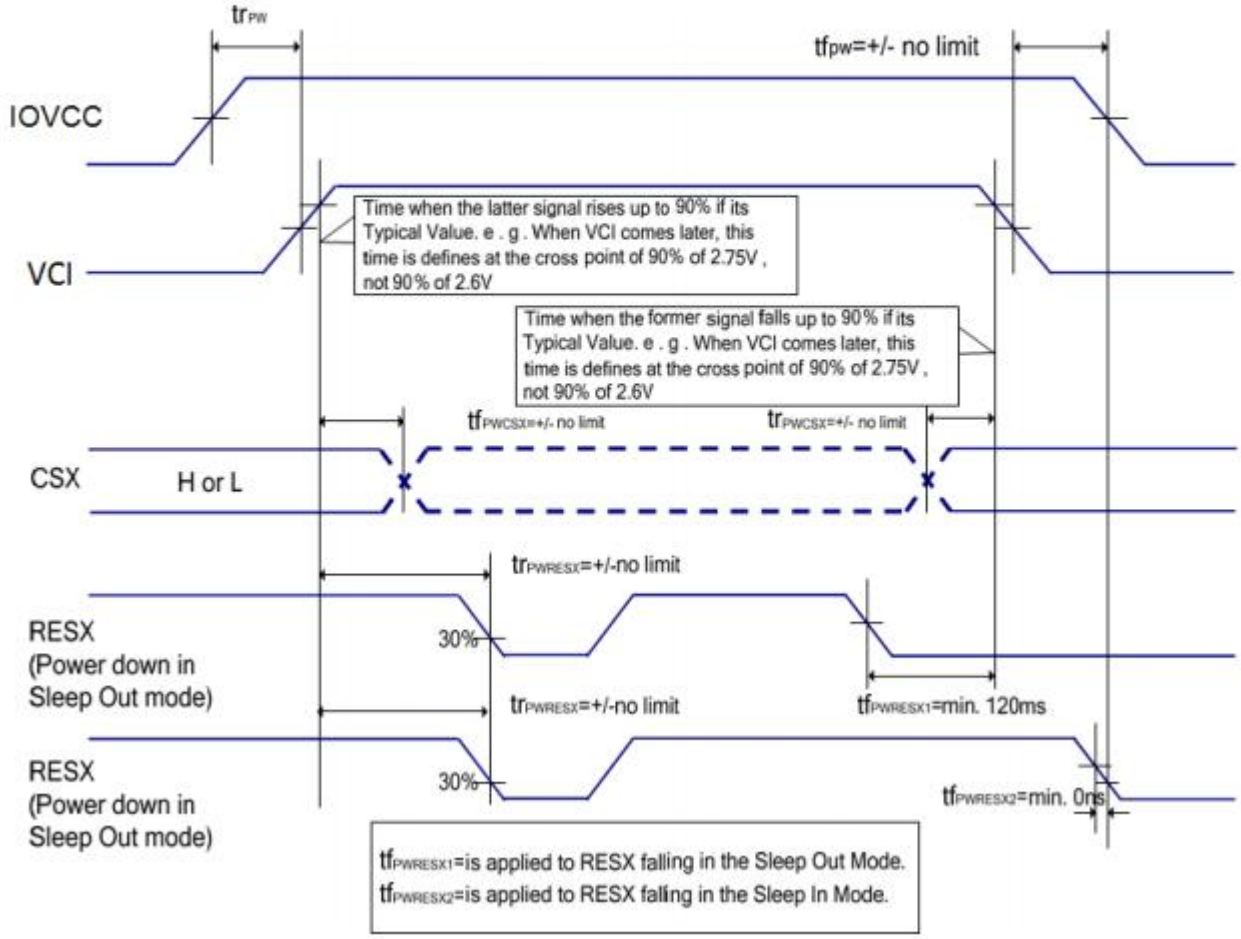
No.	Symbol	Description
1	LEDK	Power for LED backlight (Cathode)
2	LEDK	Power for LED backlight (Cathode)
3	LEDA	Power for LED backlight (Anode)
4	LEDA	Power for LED backlight (Anode)
5	NC(YU)	No connection
6	NC(XR)	No connection
7	NC	No connection
8	RESET	Global reset pin
9	CS/SPENA	Chip select signal for SPI interface operation.
10	SCL/SPCLK	Serial interface Clock Input.
11	SDA/SPDAT	Serial interface DATA Input/Output.
12-19	B0-B7	Data bus
20-27	G0-G7	Data bus
28-35	R0-R7	Data bus
36	HSYNC	Horizontal synchronizing input signal.
37	VSYNC	Vertical synchronizing input signal.
38	DCLK	Dot clock signal.
39	GND	Ground
40	GND	Ground
41	VDD 3.3V	Power supply(3.3V)
42	VDD 3.3V	Power supply(3.3V)
43	NC(YD)	No connection
44	NC(XL)	No connection
45	NC	No connection
46	CTP_VDD	Power supply for CTP
47	CTP_SCL	I2C clock input for CTP
48	CTP_SDA	I2C data input and output for CTP
49	CTP_INT	Interrupt signal for CTP
50	CTP_RST	Reset Pin for CTP
51	NC	No connection
52	DEN	Data enable pin.
53	GND	Ground
54	GND	Ground

5. Interface Characteristics

5.1 Power Sequence

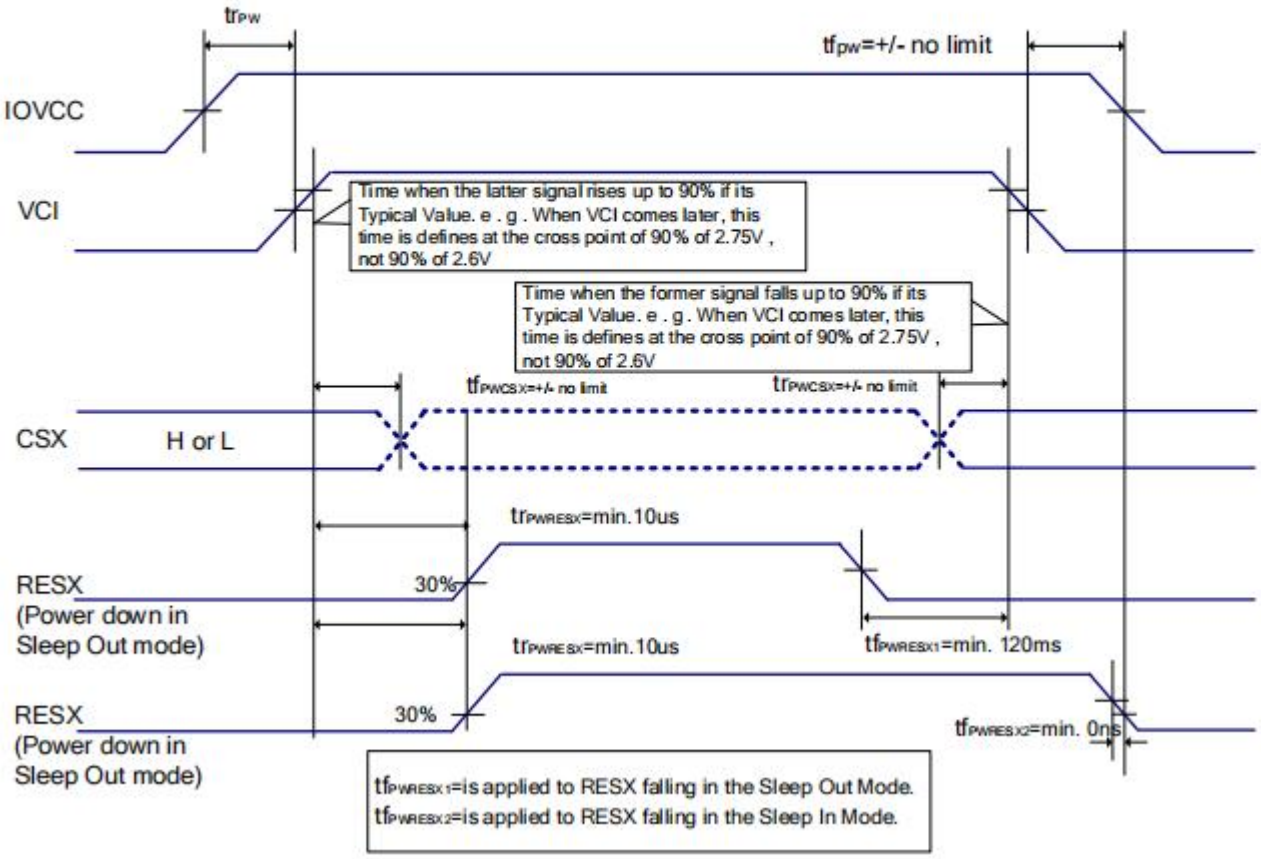
Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Case 2 – RESX line is held low or unstable by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10sec after both VCI and IOVCC have been applied.



5.2 DC Characteristics

Basic DC characteristic

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.5	2.8	6.0	V	
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.6	V	
Input/Output							
Logic High level input voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3*IOVCC	V	
Logic High level output voltage	VOH	IOH = -0.1mA	0.8*IOVCC	-	IOVCC	V	
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2*IOVCC	V	
Logic Input leakage current	IIL	Vin=IOVCC or VSSI	-0.1	-	+0.1	uA	
VCOM Operation							
VCOM voltage	VCOM	-	-3.375	-1.0	0	V	
Source Driver							
Source output range	Vsout	-	VGMN+0.1	-	VGMP-0.1	V	
Gamma positive reference voltage	VGMP	-	2.62	-	5.68	V	
Gamma negative reference voltage	VGMN	-	-5.68	-	-2.62	V	
Source output settling time	Tr	Below with 99% precision	-	TBD	-	us	
Output deviation voltage (Source positive output channel)	V,dev	Sout >=+4.2V, Sout<=+0.8V	-	-	TBD	mV	
		+4.2V>Sout>+0.8V	-	-	TBD	mV	
Output deviation voltage (Source negative output channel)	V,dev	Sout <=-4.2V, Sout>=-0.8V	-	-	TBD	mV	
		-4.2V<Sout<-0.8V	-	-	TBD	mV	

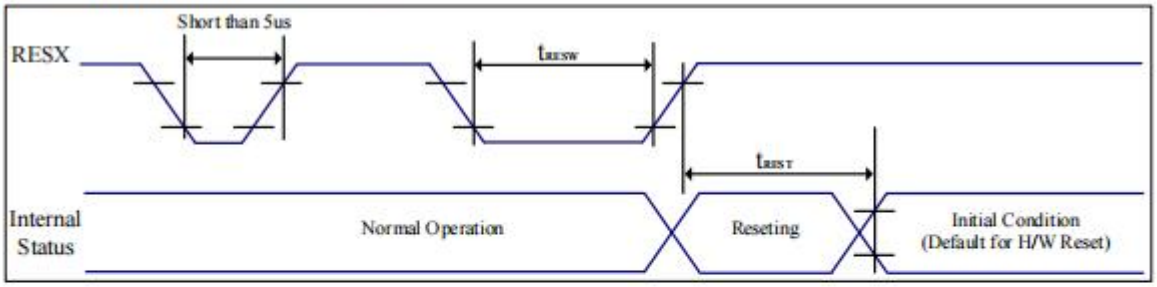
Output offset voltage	VOFFSET	-	-	-	TBD	mV	
Reference Voltage							
Internal reference voltage	VREF		1.876	2.00	2.125	V	
Booster operation							
1st booster output voltage	VSP		4.5		6	V	
	VSN		-6		-4.5	V	
2ndbooster output voltage	VGH		11.0		20.5	V	
	VGL		-15.5		-7.0	V	
Current Consumption							
Sleep-IN mode	IIOVCC	RESX=High		TBD	TBD	uA	Note2
	IVCI			TBD	TBD	uA	
Deep standby mode	IIOVCC	RESX=High		TBD	TBD	uA	
	IVCI			TBD	TBD	uA	

Note1. The power/temperature conditions for Current consumption (Sleep-IN) part is VCI=3.0V, IOVCC=1.8V@25℃

(These values might be updated after further evaluation.)

5.3 AC Characteristics

Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30℃ to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

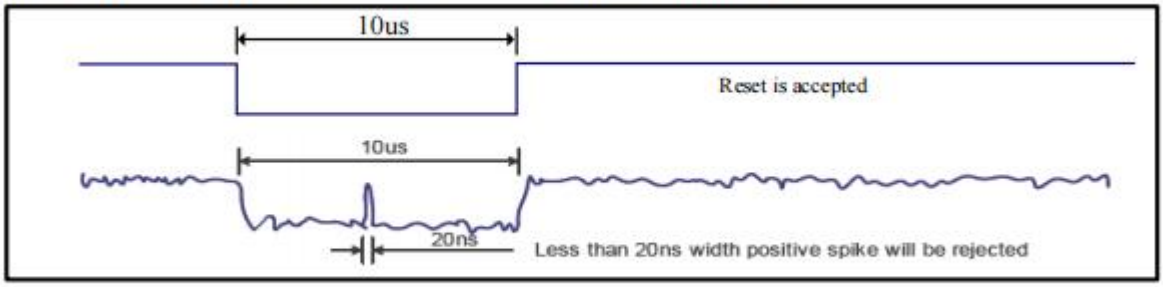
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

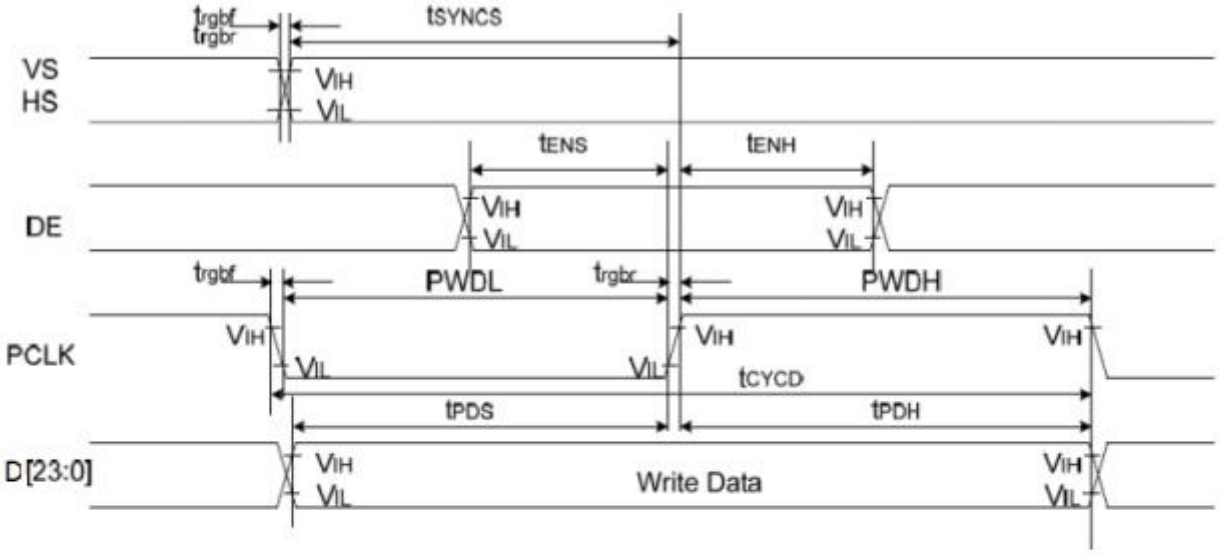
Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms..The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/HS	tSYNCS	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	tSYNCH	VS/HS hold time	5	-	ns	
DE	tENS	DE setup time	5	-	ns	
	tENH	DE hold time	5	-	ns	
D[23:0]	tPDS	Data setup time	5	-	ns	
	tPDH	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	7	-	ns	
	PWDL	PCLK low-level period	7	-	ns	
	tCYCD	PCLK cycle time	14	-	ns	
	trgbr,trgbf	PCLK,HS,VS rise/fall time	-	15	ns	

Serial interface characteristics (SPI)

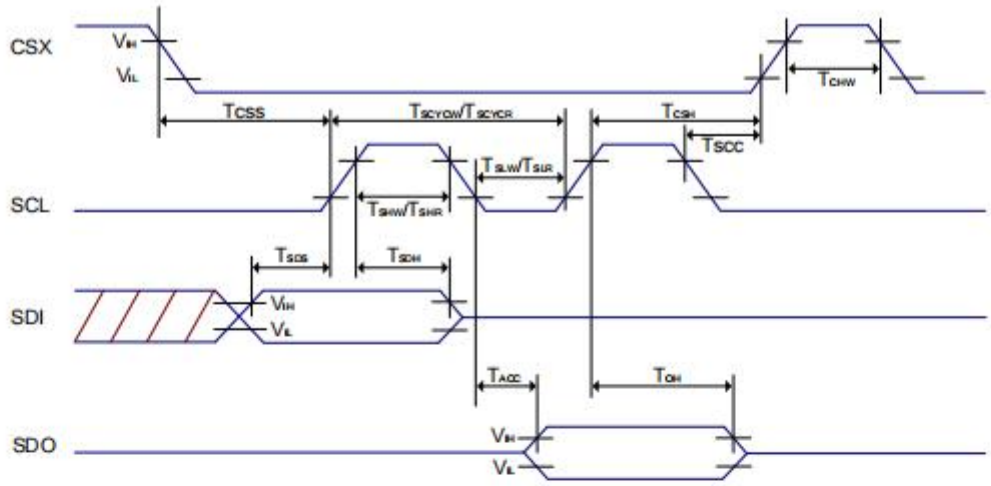


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

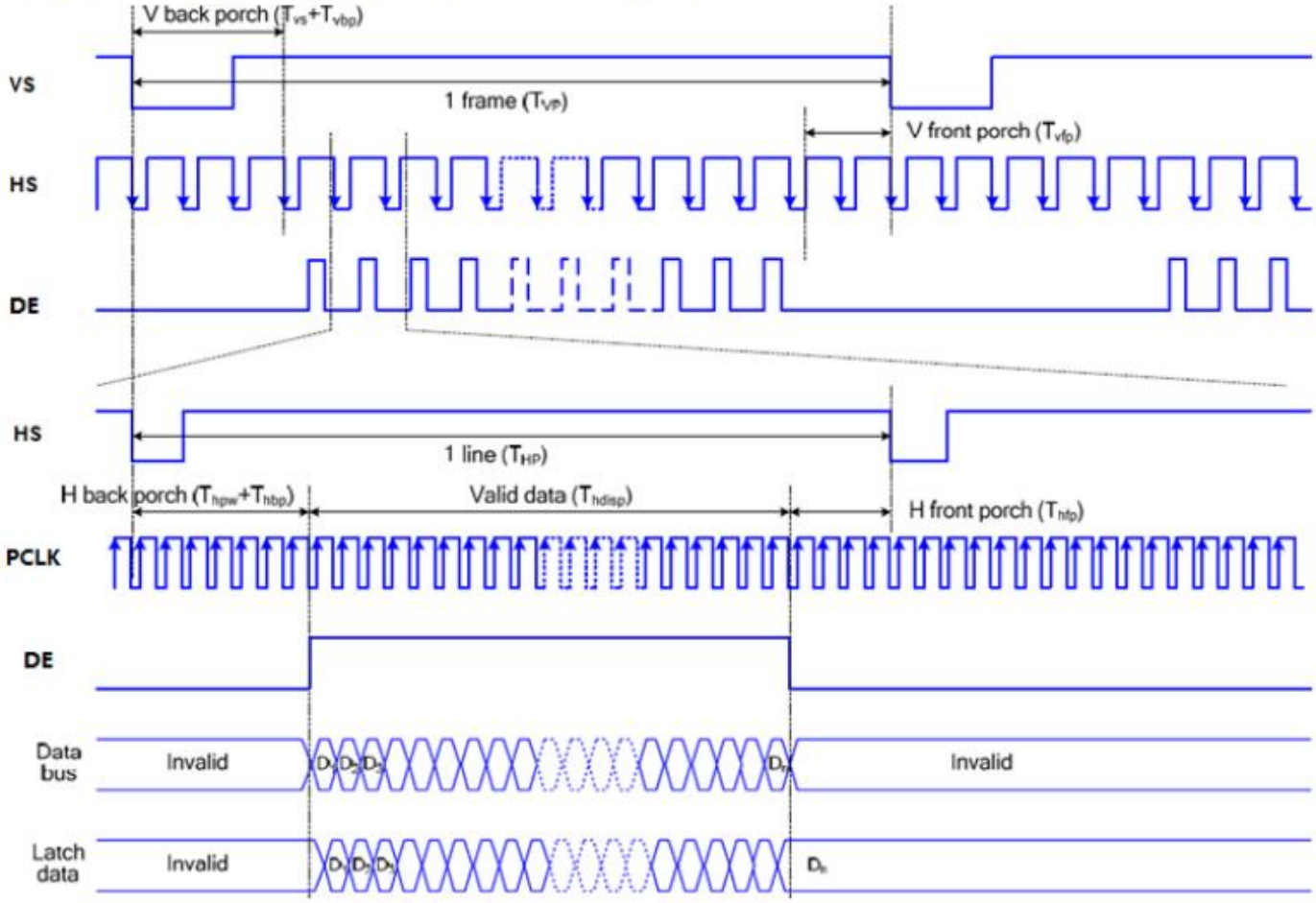
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	15	-	ns	-
	T_{CSH}	Chip select hold time	15	-	ns	
	T_{SCC}	Chip select setup time	20	-	ns	
	T_{CHW}	Chip "H" pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66	-	ns	-
	T_{SHW}	SCL "H" pulse width (Write)	10	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	10	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	150	-	ns	-
	T_{SHR}	SCL"H" pulse width (Read)	60	-	ns	
	T_{SLR}	SCL"L" pulse width (Read)	60	-	ns	
SDI	TSDS	Data setup time	10	-	ns	-
	T_{SDH}	Data hold time	10	-	ns	
	T_{ACC}	Access time	10	50	ns	For maximum C_L=30pF For minimum C_L=8pF
	T_{OH}	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSA=VSS=0V, Ta=-30 to 85℃

Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

5.4 RGB Interface Timing

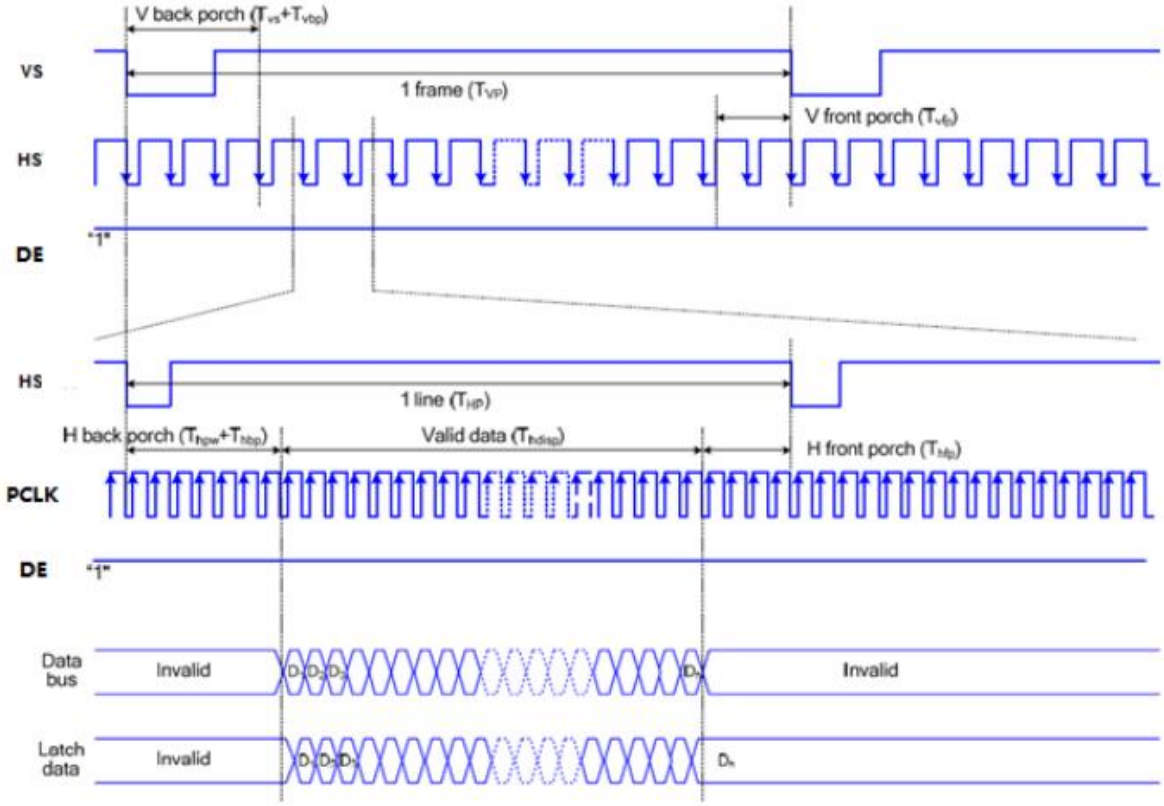
The timing chart of RGB interface DE mode is shown as follows.



Timing Chart of Signals in RGB Interface DE Mode

Note: The setting of front porch and back porch in host must match that in IC as this mode.

The timing chart of RGB interface SYNC mode is shown as follows.



Timing chart of RGB interface SYNC mode

Below Table provide the timing parameter by external Vertical-cycle

(Resolution for 720/640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
Horizontal Synchronization	hpw	-	2	-	PCLK
Horizontal Back Porch	hbp	-	42	-	PCLK
Horizontal Front Porch	hfp	-	44	-	PCLK
Hsync+ HBP+ HFP	-	-	88*Note1	-	PCLK
Horizontal Address (Display area)	hdisp	-	720	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	VS	-	2	-	Line
Vertical Back Porch	vbp	-	14	-	Line
Vertical Front Porch	vfp	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	vdisp	-	1280	-	Line
Vertical cycle	-	-	16.66	16.181	ms
Frame-Rate	-	-	60	61.8	Hz

"-" means no limit.

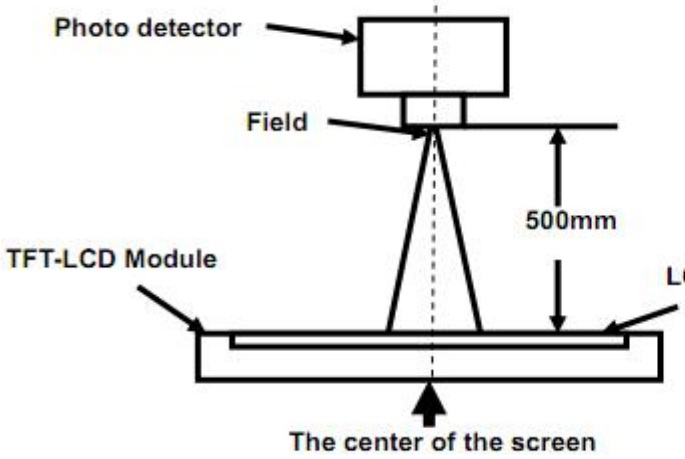
Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	80	85	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	80	85	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	80	85	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	80	85	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	12	17	msec	Note4
	T_{OFF}		-	12	17	msec	Note4
Contrast Ratio	CR		800	1100	-	-	Note1 Note3
Color Chromaticity	W_X		TBD	TBD	TBD	-	Note1 Note5
	W_Y		TBD	TBD	TBD	-	Note1 Note5
Luminance	L		450	550	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		55	60	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Fig 1

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

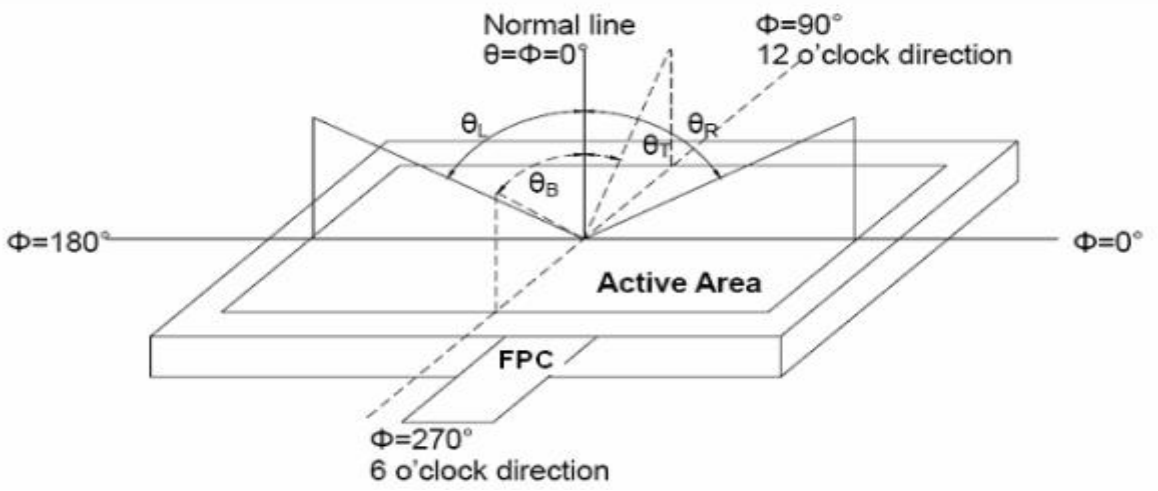


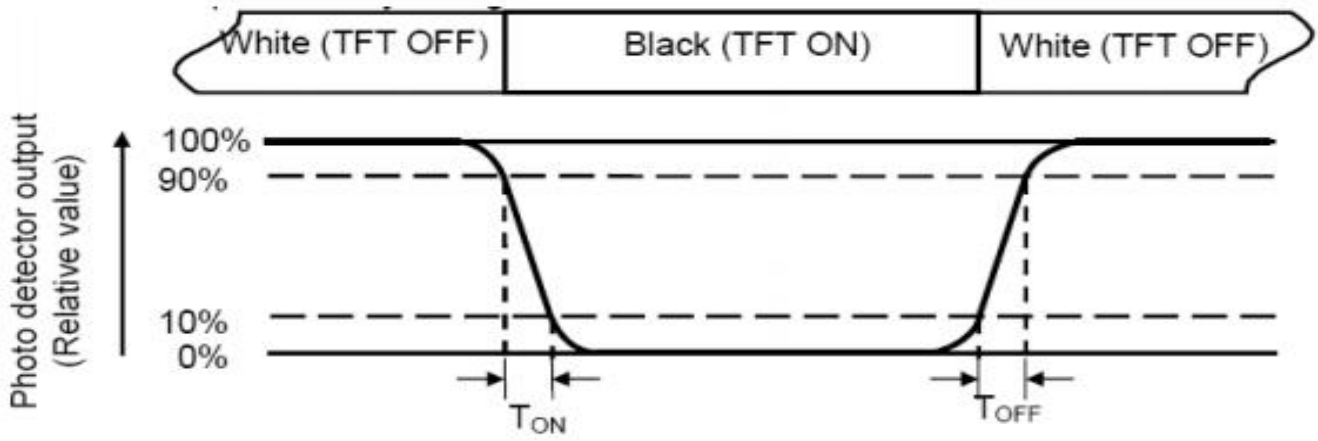
Fig 2 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.3-a/b

Note 7:Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

For more information see FIG.3-a/b

Note 8:

H,V : Active area(see Figure a)

Light spot size ⌀ =5mm(BM-5) or ⌀ =7.7mm (BM-7)50cm distance or test spot position : see Figure a.

measurement instrument : TOPCON's luminance meter SR-3A or BM-7 or compatible (see Figure 1).

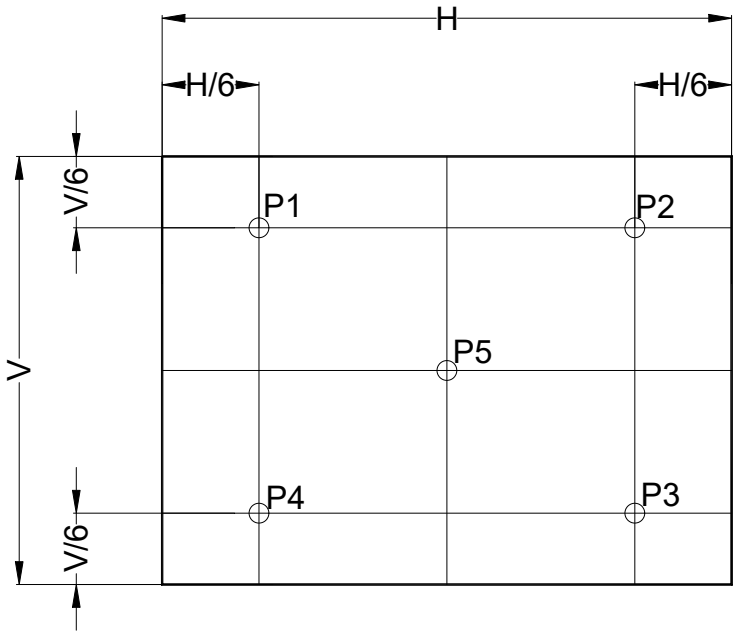


Fig. 3-a Definition of points

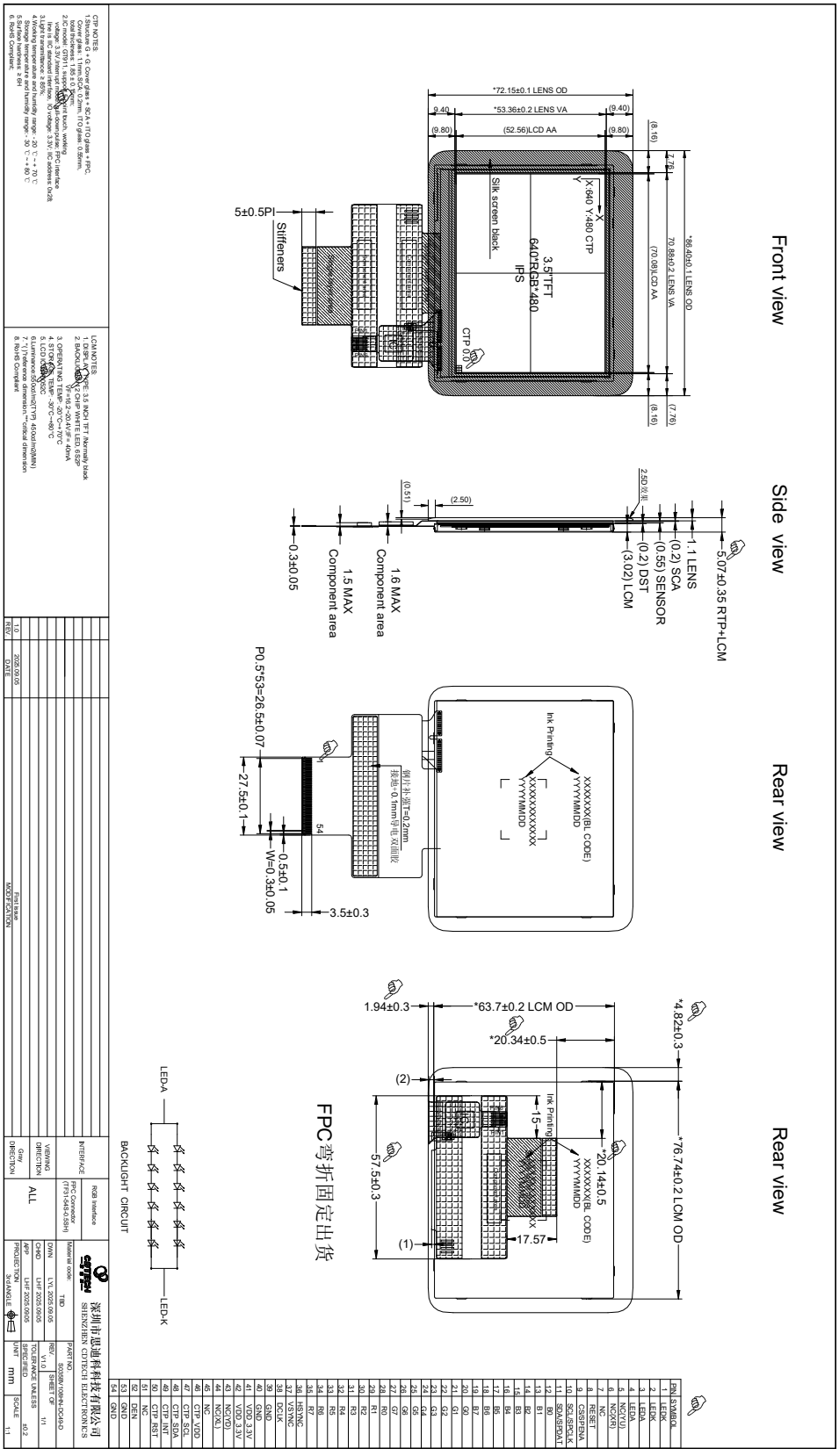
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +80℃	96hrs
Low Temperature Storage	Ta= -30℃	96hrs
High Temperature Operation	Ta= +70℃	96hrs
Low Temperature Operation	Ta= -20℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-30℃/30 min ~ +80℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

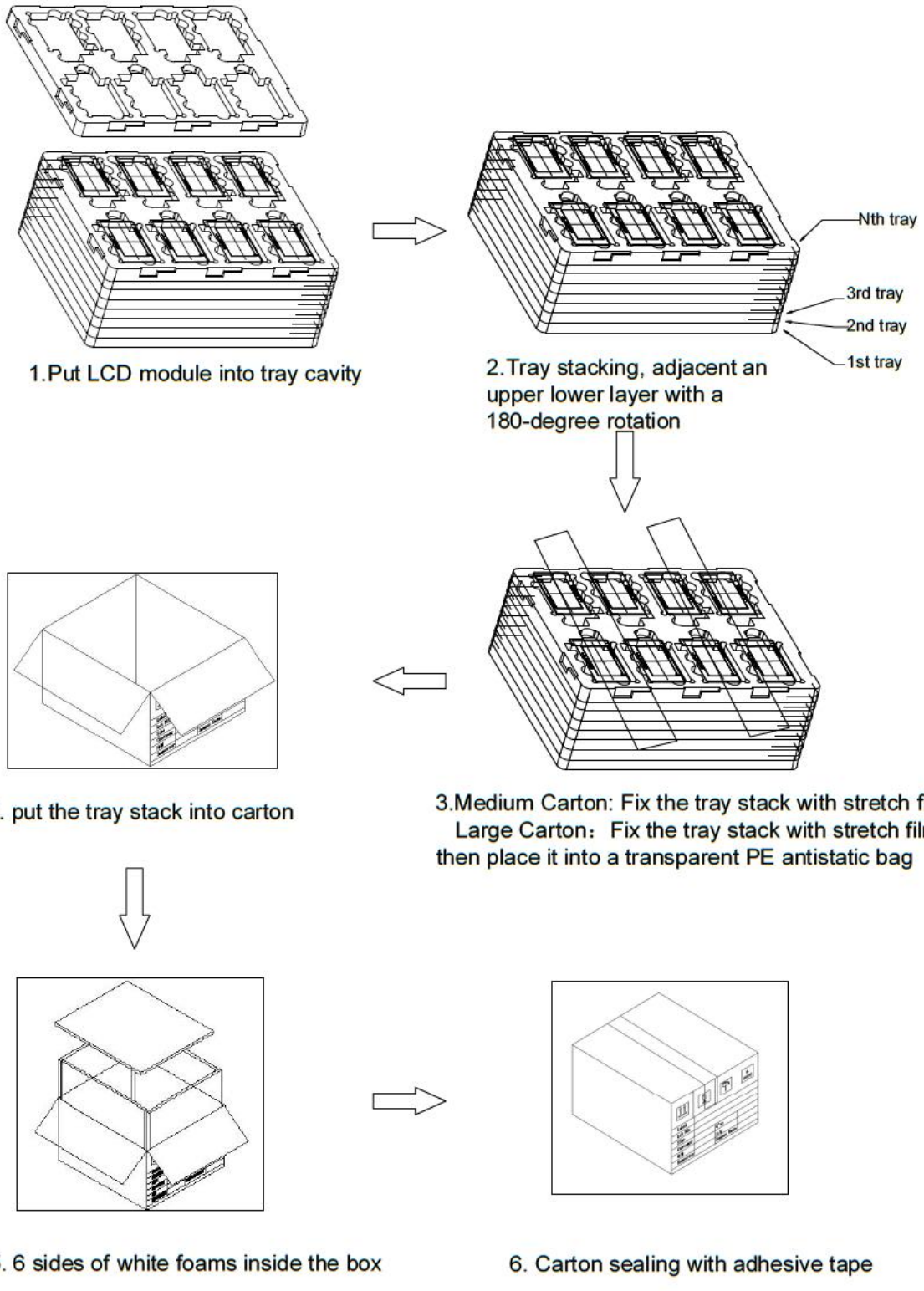
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



9. Packing

Packing Method



10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

10.4 Packaging instructions

When the customers using trays, they have to stack the adjacent trays in a 180° staggered to prevent pressure that could cause product damage.