

PRODUCT SPECIFICATION

CDTECH Model: **S057BWV02NP-FC01**

CUSTOMER Model: **-**

Description: **5.7 " TFT-LCD Module with CTP**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2025.12.22	2025.12.22	2025.12.22

CUSTOMER APPROVAL	SIGNATURE	DATE



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1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	5.7	inch
Number of Pixels	640 (H) RGB x 480 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Typ:85/85/85/85 Min:80/80/80/80	-
Interface	RGB&LVDS&MIPI	-
Display Colors	16.7M	colors
Outline Dimension	127.1 (H) x 98.53 (V) x 8.01 (D)	mm
Active Area	115.2 (H) x 86.4 (V)	mm
Pixel Pitch	0.18 (H) x 0.18 (V)	mm
Driver IC	JD9168	-
Operation Temperature	-20~70	°C
Storage Temperature	-30~80	°C

1.2 Touch Panel Information

Item	Specification
Touch Structure	G+G
Bonding Type with LCM	OCA Optical Bonding
Driver IC	GT911
Interface	I ² C
Touch Count Max	5 Points
Surface treatment	-
Surface hardness	6H
I2C slave address	0x28
Origin of coordinate	Top Left Corner

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	IOVCC	-0.3	3.6	V	Note 1
Input voltage for analog circuit	AVDD	-0.3	6.3	V	Note 1
	AVEE	-6.0	-0.3	V	

Note 1: Permanent damage may occur to the LCD module if beyond this specification.

Functional operation should be restricted to the conditions described under normal operating conditions.

3. Electrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

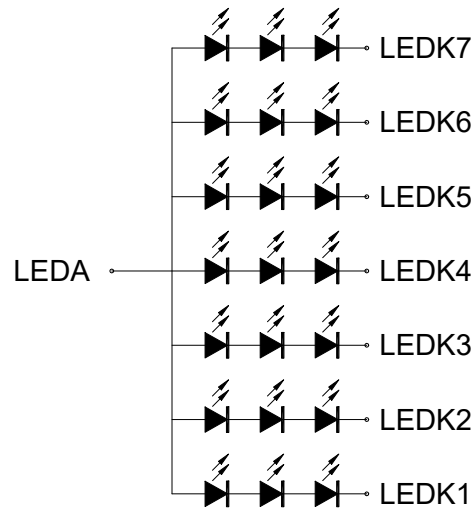
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Logic supply voltage	IOVCC	2.5	3.3	3.3	V	
Logic supply current	I_{IOVCC}	-	TBD	-	mA	IOVCC=3.3V
Power supply for LCD	AVDD	4.5	5.5	6.0	V	
	AVEE	-6.0	-5.5	-4.5	V	
Logic input voltage	VIH	0.7*IOVCC	-	IOVCC	V	
	VIL	GND	-	0.3*IOVCC	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	120	-	mA	
Driving Voltage	V_F	8.1	-	10.2	V	
Power consumption	W_{BL}	0.972	-	1.224	W	
LED Life-Time	N/A	-	30,000	-	Hours	Ta=25°C Note 1

Note 1: LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



3.3 Touch Panel

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply voltage	VDD	-	3.3	-	V	
Analog supply current	I_{VDD}	-	15	-	mA	VDD=3.3V
Input high-level voltage	V_{IH}	$0.7 \cdot VDD$	-	VDD	V	
Input low -level voltage	V_{IL}	GND	-	$0.3 \cdot VDD$	V	

4. Interface Pin Assignment

4.1 DISPLAY Pin Assignment

No.	Symbol	Description																				
1	SDA	SPI data																				
2	CSX	Chip select																				
3	SCL	SPI clock																				
4	RESX	Reset Pin																				
5-12	B0-B7	RGB data																				
13-20	G0-G7	RGB data																				
21-28	R0-R7	RGB data																				
29	GS	gate scan																				
30	SS	source scan																				
31	LAN0	Select the lane mode as listed below: <table border="1" data-bbox="483 913 1241 1128"> <thead> <tr> <th colspan="2">LAN[1:0]</th> <th>DSI IF</th> <th>LVDS IF</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Not used</td> <td>Not used</td> </tr> <tr> <td>0</td> <td>1</td> <td>2 Lane</td> <td>Not used</td> </tr> <tr> <td>1</td> <td>0</td> <td>3 Lane</td> <td>6 Bit</td> </tr> <tr> <td>1</td> <td>1</td> <td>4 Lane</td> <td>8 Bit</td> </tr> </tbody> </table>	LAN[1:0]		DSI IF	LVDS IF	0	0	Not used	Not used	0	1	2 Lane	Not used	1	0	3 Lane	6 Bit	1	1	4 Lane	8 Bit
LAN[1:0]		DSI IF	LVDS IF																			
0	0	Not used	Not used																			
0	1	2 Lane	Not used																			
1	0	3 Lane	6 Bit																			
1	1	4 Lane	8 Bit																			
32	LAN1																					
33	LVFMT	Data format select for LVDS mode LVFMT=0,VESA LVFMT=1,JEIDA																				
34	STBYB	Standby mode STBYB=0,Standby Mode STBYB=1,Normal Mode																				
35	IM1	Select the interface mode as listed below: <table border="1" data-bbox="483 1435 1015 1650"> <thead> <tr> <th colspan="2">IM[1:0]</th> <th>Interface</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>DSI</td> </tr> <tr> <td>0</td> <td>1</td> <td>LVDS</td> </tr> <tr> <td>1</td> <td>0</td> <td>RGB</td> </tr> <tr> <td>1</td> <td>1</td> <td>Not used</td> </tr> </tbody> </table>	IM[1:0]		Interface	0	0	DSI	0	1	LVDS	1	0	RGB	1	1	Not used					
IM[1:0]		Interface																				
0	0	DSI																				
0	1	LVDS																				
1	0	RGB																				
1	1	Not used																				
36	IM0																					
37	DCLK	RGB clock																				
38	DE	RGB data enable																				
39	VS	RGB V-sync																				
40	HS	RGB H-sync																				
41	DS2	Select for DSI or LVDS data lane sequence and polarity Select for DSI Interface,PS=1,DS[2:0]=100 Select for LVDS Interface,PS=1,DS[2:0]=000																				
42	DS1																					
43	DS0																					
44	PS																					

45	GND	Ground
46	D0N	LVDS D0N
47	D0P	LVDS D0P
48	D1N	LVDS D1N
49	D1P	LVDS D1P
50	CKN	LVDS CKN
51	CKP	LVDS CKP
52	D2N	LVDS D2N
53	D2P	LVDS D2P
54	D3N	LVDS D3N
55	D3P	LVDS D3P
56	IOVCC	Power
57	AVDD	Power
58	AVEE	Power
59	VPP	OTP power
60	GND	Ground

4.2 Touch FPC Pin Assignment

No.	Symbol	Description
1	GND	Ground
2	INT	Interrupt signal for CTP
3	RST	Reset Pin for CTP
4	SDA	I2C data input and output for CTP
5	SCL	I2C clock input for CTP
6	VDD	Power supply for CTP
7	VDD	Power supply for CTP
8	GND	Ground

4.3 Backlight LED FPC Pin Assignment

No.	Symbol	Description
1	NC	No connection
2	LEDA	Power for LED backlight (Anode)
3	LEDK1	Power for LED backlight (Cathode)
4	LEDK2	Power for LED backlight (Cathode)
5	LEDK3	Power for LED backlight (Cathode)
6	LEDK4	Power for LED backlight (Cathode)
7	LEDK5	Power for LED backlight (Cathode)
8	LEDK6	Power for LED backlight (Cathode)
9	LEDK7	Power for LED backlight (Cathode)
10	NC	No connection

5. Interface Characteristics

5.1 Power Sequence

Power on sequence

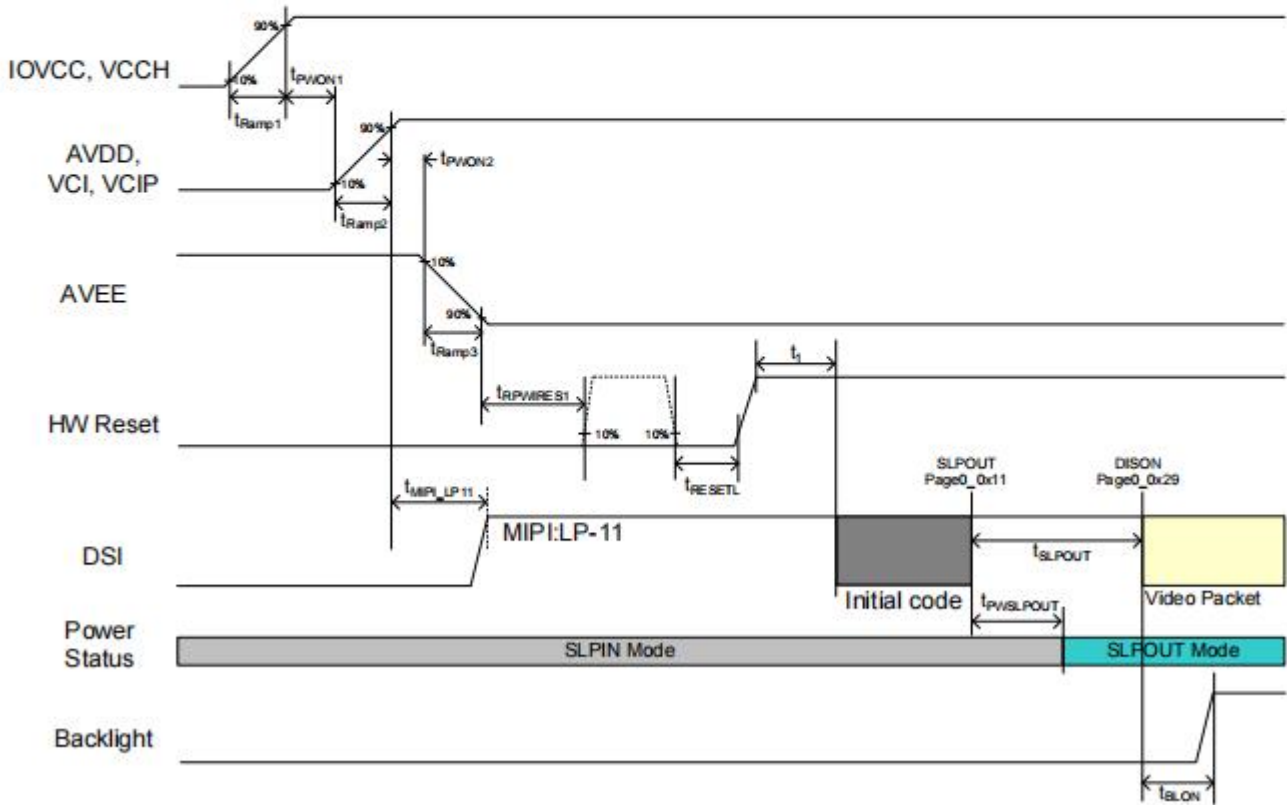
The power on sequence timing for different power input modes and interfaces are shown as below table.

Symbol	Value			Unit	Remark
	Min	Typ	Max		
t_{PWON1}	0	5	-	ms	
t_{PWON2}	0	5	-	ms	
t_{PWON3}	0	5		ms	
t_{PWON4}	0	5		ms	
t_{ramp1}	0.2	-	20	ms	IOVCC, VCCH
t_{ramp2}	0.2	-	20	ms	VCI, VCIP, AVDD
t_{ramp3}	0.2	-	20	ms	AVEE
t_{ramp4}	0.2	-	-	ms	VGL
t_{ramp5}	0.2	-	-	ms	VGH
$t_{RPWIRES1}$	10	-	-	ms	
$t_{RPWIRES2}$	1	-	-	ms	
t_{MIPI_LP11}	-	-	$t_{RPWIRES1}$	ms	
t_{RESETL}	20	-	-	μ s	
t_1	5	-	-	ms	
t_{SLP_OUT}	120	-	-	ms	
t_{PWSL_OUT}	-	45	-	ms	
t_{BLON}	2	-	-	VS	

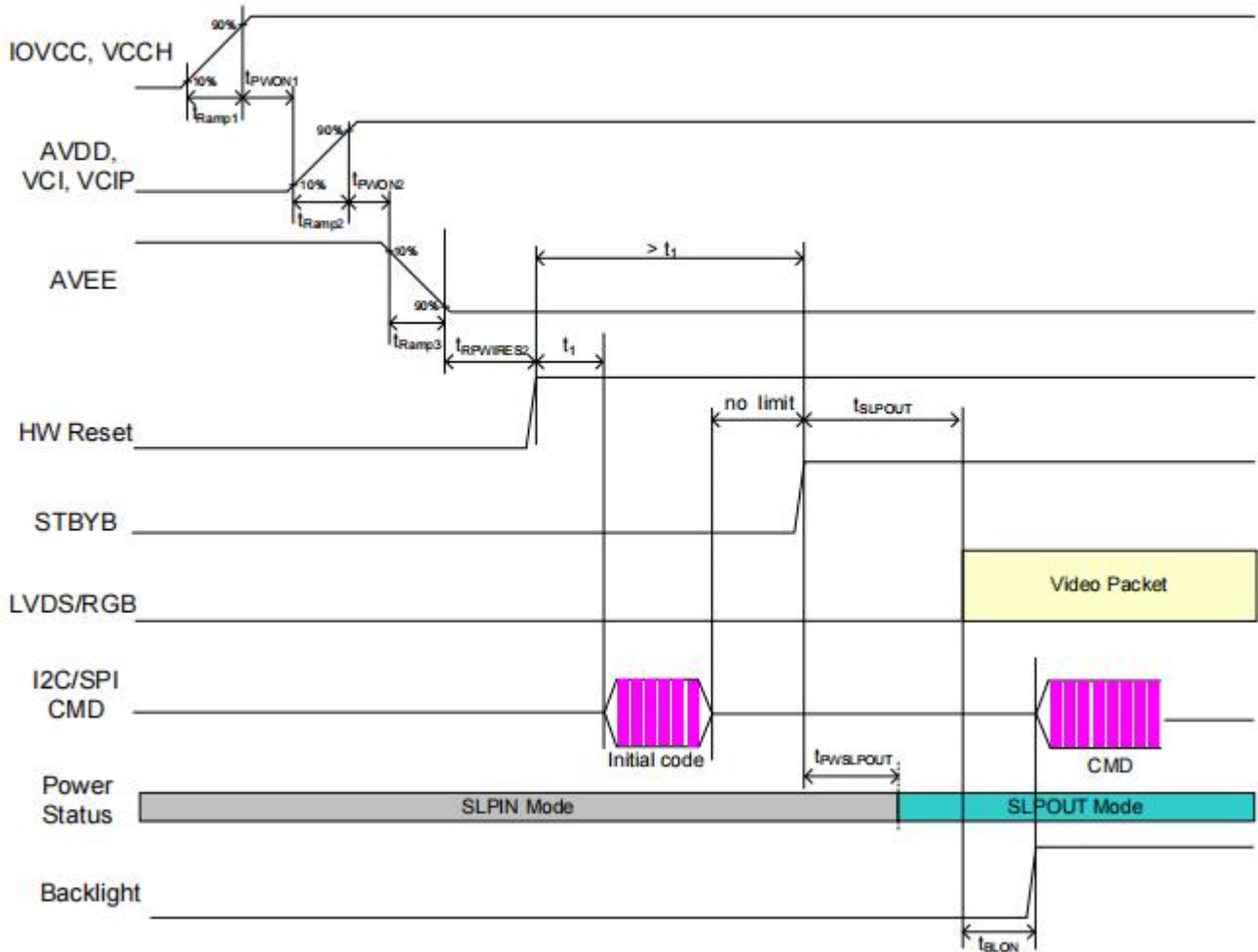
3 input power mode (EXT_VGL=0, BOOSTM [1:0]=01)

- External IOVCC, AVDD, AVEE Power.
- IOVCC=VCCH=2.5~3.3V, VCI=VCIP=AVDD=4.5~5.5V, AVEE=-4.5~-5.5V.

3 power mode power on sequence – DSI:



3 power mode power on sequence – LVDS, RGB:



Power off sequence

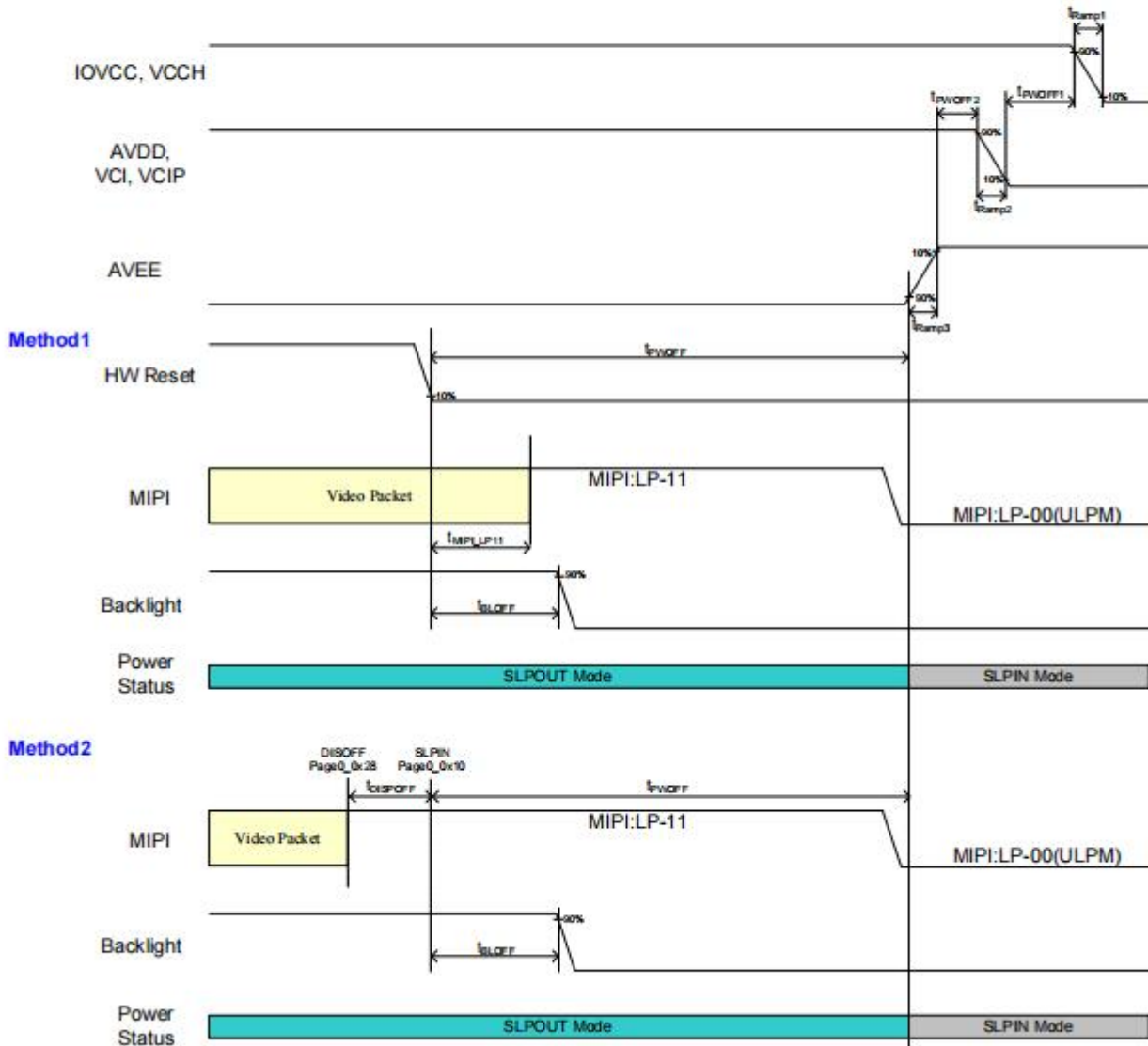
The power off sequence timing for different power input modes and interfaces are shown as below table.

Symbol	Value			Unit	Remark
	Min	Typ	Max		
$t_{PW\text{OFF}1}$	0	5	-	ms	
$t_{PW\text{OFF}2}$	0	5	-	ms	
$t_{PW\text{OFF}3}$	0	5	-	ms	
$t_{PW\text{OFF}4}$	0	5	-	ms	
$t_{\text{ramp}1}$	0.2	-	20	ms	IOVCC, VCCH
$t_{\text{ramp}2}$	0.2	-	20	ms	VCI, VCIP, AVDD
$t_{\text{ramp}3}$	0.2	-	20	ms	AVEE
$t_{\text{ramp}4}$	0.2	-	-	ms	5Power: VGL
$t_{\text{ramp}5}$	0.2	-	-	ms	5Power: VGH
$t_{PW\text{OFF}}$	120	-	-	ms	
$t_{\text{MIPI_LP}11}$	0	-	$t_{PW\text{OFF}}$	ms	
t_{DISPOFF}	50	-	$t_{PW\text{OFF}}$	ms	
t_{RSTHtoL}	50	-	$t_{PW\text{OFF}}$	ms	
$t_{\text{Video_OFF}}$	0	-	$t_{PW\text{OFF}}$	ms	
t_{BLOFF}	0	-	-	ms	

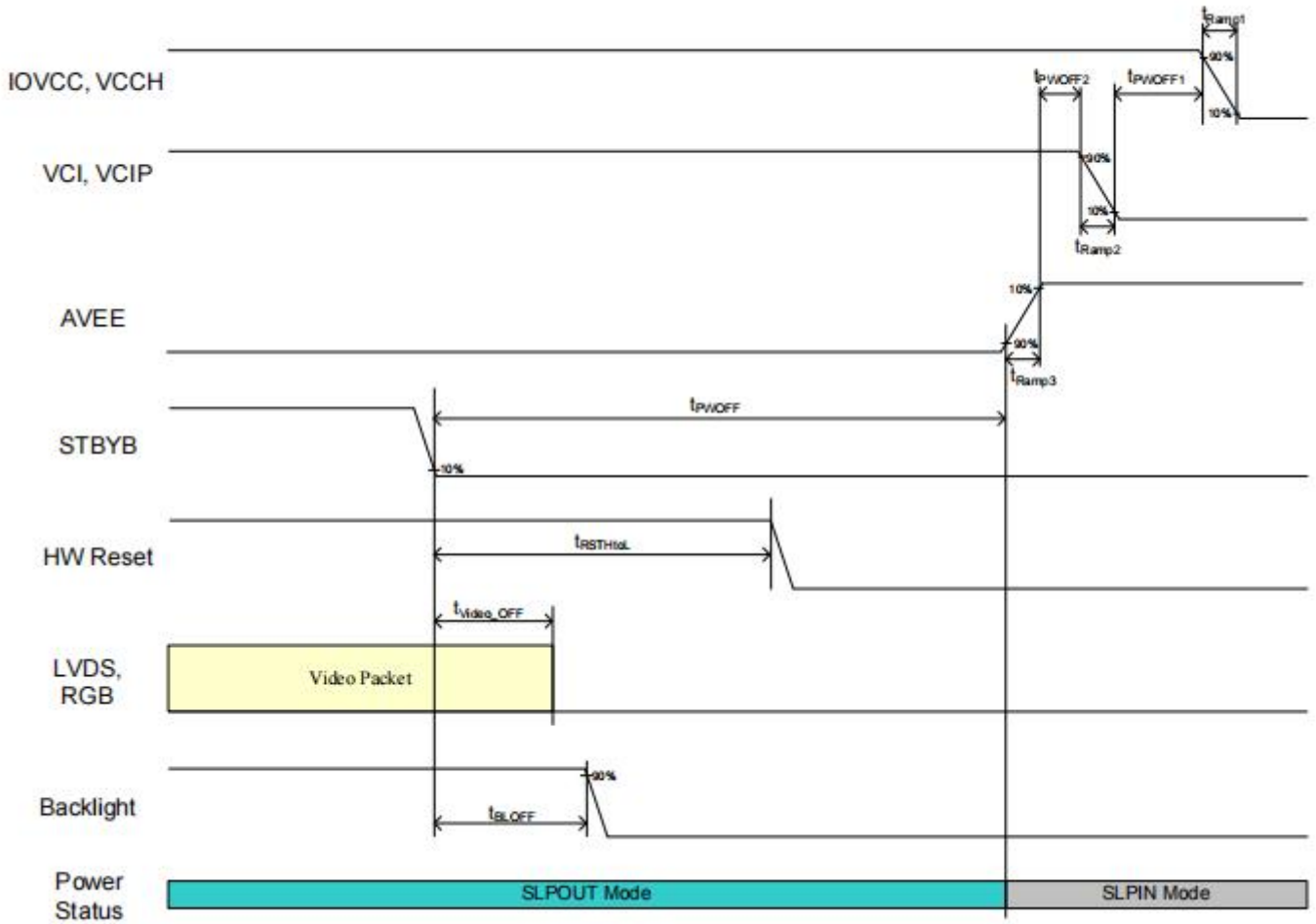
3 input power mode (EXT_VGL=0, BOOSTM [1:0]=01)

- External IOVCC, AVDD, AVEE Power.
- IOVCC=VCCH=2.5~3.3V, VCI=VCIP=AVDD=4.5~5.5V, AVEE=-4.5~-5.5V.

3 power mode power off sequence – DSI:



3 power mode power off sequence – LVDS, RGB:



5.2 DC Characteristics

RGB Interface DC electrical characteristics

Input high voltage	V_{IH}	IOVCC= 2.5 ~ 3.3V VCIP= 2.5 ~ 6.0V VCI= 2.5 ~ 6.0V	$0.7 \times$ IOVCC	-	IOVCC	V
Input low voltage	V_{IL}		0	-	$0.3 \times$ IOVCC	V
Output high voltage (SDA, GPIO)	V_{OH1}	$I_{OH} = -1.0 \text{ mA}$	$0.8 \times$ IOVCC	-	IOVCC	V
Output low voltage (SDA, GPIO)	V_{OL1}	IOVCC= 2.5 ~ 3.3V $I_{OL} = 1.0 \text{ mA}$	0	-	$0.2 \times$ IOVCC	V
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	μA
		RESX, SCL, CSX, DB[23...0], SDA	-	-	1	μA
	I_{IHD}	DB[23...0]	-	-	1	μA
		VSYNC, HSYNC	-1	-		μA
Logic Low level input current	I_{IL}	RESX, CSX, SCL	-1	-		μA
		DB[23...0], SDA	-1	-		μA
	I_{ILD}	DB[23...0]	-1	-		μA
		VCI/VCCH=3.3V, IOVCC=3.3V $T_A = 25^\circ\text{C}$	-	TBD	-	μA
Current consumption standby mode (VCI/VCI-VSSD)	$I_{ST(VDD)}$		-	TBD	-	μA
Current consumption standby mode (IOVCC- VSSD)	$I_{ST(IOVCC)}$		-	TBD	-	μA
Current consumption during Deep-standby mode (VCI/VCI-VSSD)	$I_{DP-ST(VDD)}$	VCI/VCCH=3.3V, IOVCC=3.3V $T_A = 25^\circ\text{C}$	-	TBD	-	μA
Current consumption during Deep-standby mode (IOVCC- VSSD)	$I_{DP-ST(IOVCC)}$		-	TBD	-	μA

Table 11.2: RGB Interface DC characteristic

LVDS DC electrical characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential input high threshold voltage	R_{XVTH}	$R_{XVCM}=1.2V$	+0.1	+0.2	+0.3	V
Differential input low threshold voltage	R_{XVTL}		-0.3	-0.2	-0.1	V
Input voltage range (singled-end)	R_{XVIN}		0.7	-	1.7	V
Differential input common mode voltage	R_{XVCM}	$ VID =0.2$	1	1.2	1.4	V
Differential input impedance	ZID		80	100	125	ohm
Differential input voltage	$ VID $		0.2	-	0.6	V
Differential input leakage current	I_{LCLVDS}		-10	-	+10	μA
LVDS Digital Stand-by Current	I_{STLVDS}	Clock & all Functions are stopped	-	TBD	-	μA

Table 11.3: LVDS DC characteristic

Single-End Signals

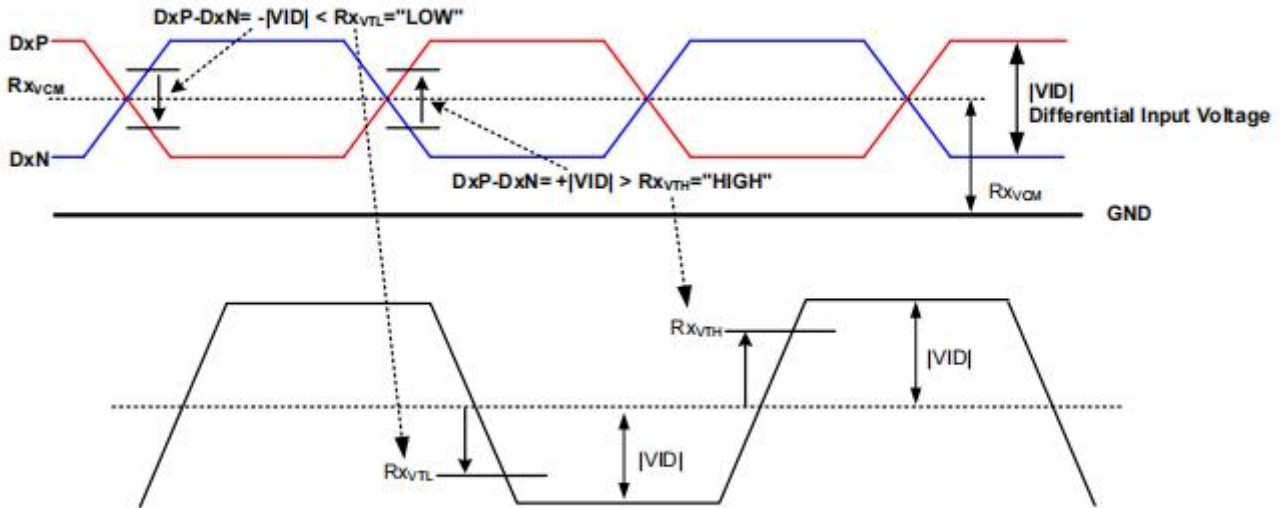


Figure 11.1: LVDS input timings

5.3 AC characteristics

Reset input timings

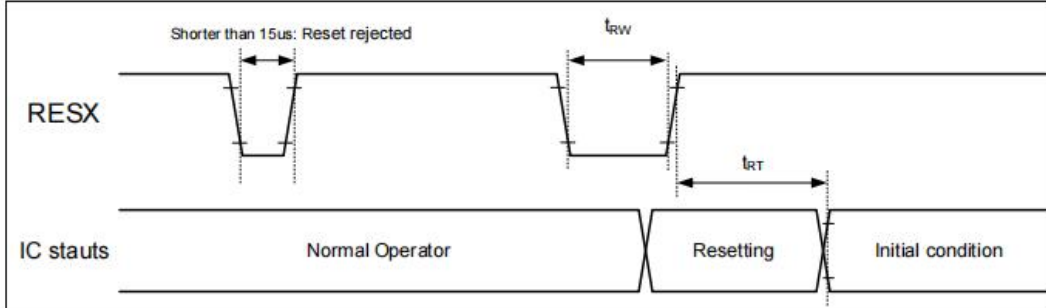


Figure 11.2: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset "L" pulse width ⁽²⁾	RESX	20	-	μs
t_{RT}	Reset complete time ⁽³⁾	-	-	5 ⁽⁵⁾	ms
		-	-	120 ^{(6) (7) (8)}	ms

Note:

- (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset complete time (t_{RT}) within 5 ms after a rising edge of RESX.
- (2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 15 μs	Reset Rejected
Longer than 20 μs	Reset
Between 15 μs and 20 μs	Reset Start

- (3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode) and then returns to Default condition for H/W reset.
- (4) Spike Rejection also applies during a valid reset pulse as shown below.

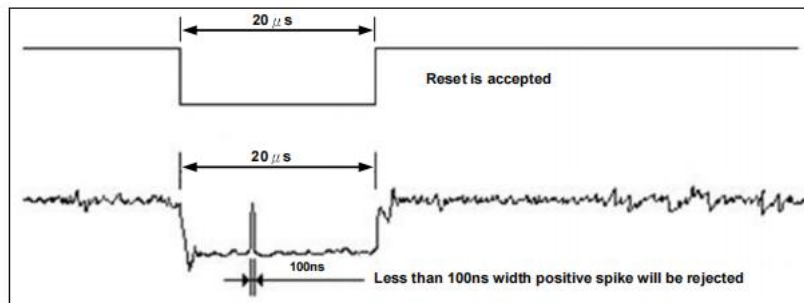


Table 11.4: Reset timings

- (5) When Reset is applied during Sleep In Mode.
- (6) When Reset is applied during Sleep Out Mode.
- (7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.
- (8) After Sleep Out command, it is necessary to wait 120msec then send RESX.

LVDS electronic characteristics

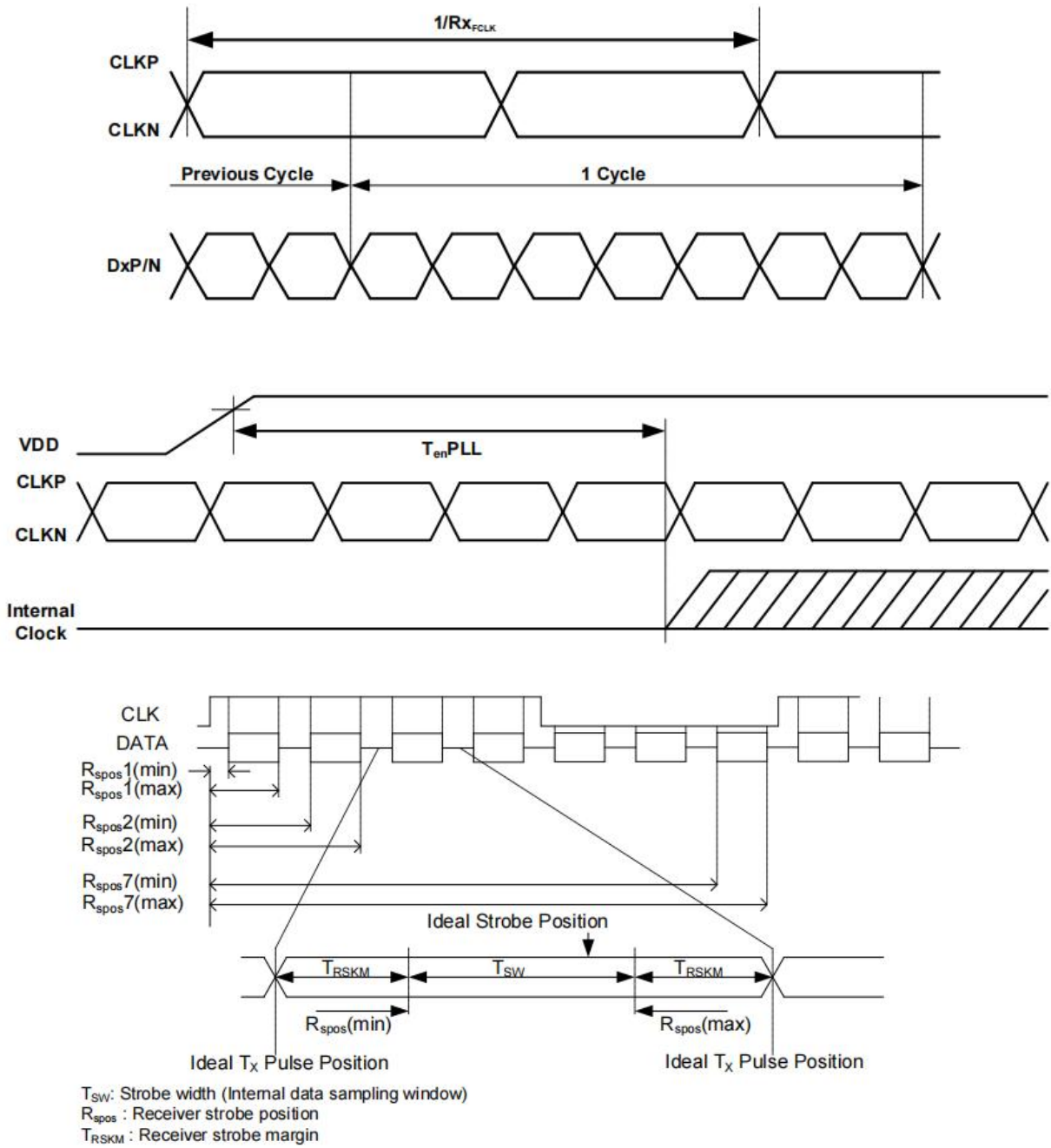


Figure 11.4: LVDS AC characteristics

Signal	Symbol	Min.	Typ	Max.	Unit	Description
Clock frequency	Rx_{FCLK}	30	-	75	MHz	-
Input data skew margin	T_{RSKM}	500	-	-	ps	$ VID = 200mV$ $RxVCM = 1.2V$ $@Rx_{FCLK}=75MHz$
Clock high time	T_{LVCH}	-	$4/(7x Rx_{FCLK})$	-	ns	-
Clock low time	T_{LVCL}	-	$3/(7x Rx_{FCLK})$	-	ns	-
PLL wake-up time	T_{en_PLL}	-	-	150	us	-

Table 11.6: LVDS AC characteristics

DSI D-PHY electronic characteristics

The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 11.5 shows the complete set of electronic functions required for a fully featured PHY transceiver.

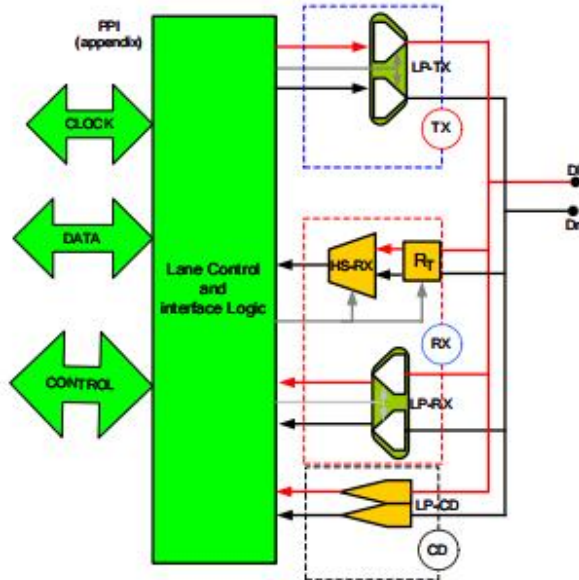


Figure 11.5: Electronic functions of a D-PHY transceiver

Figure 11.6 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

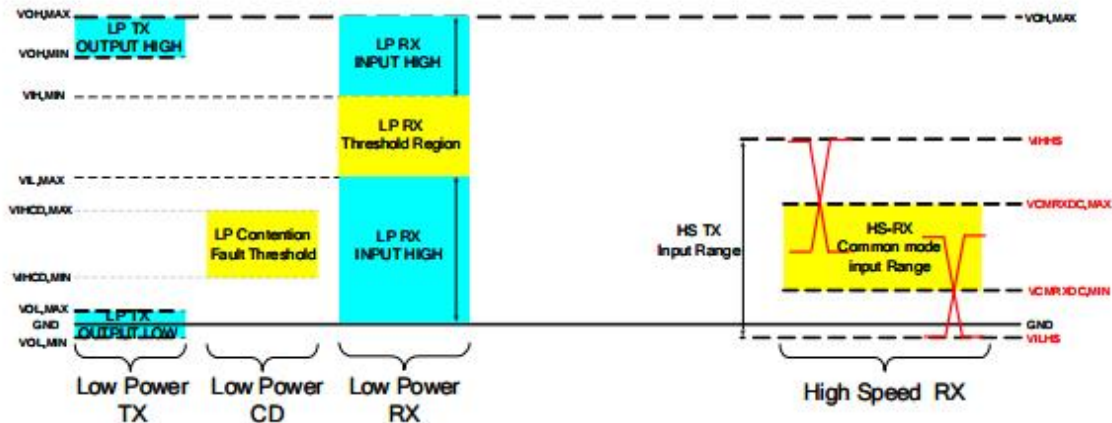


Figure 11.6: HS and LP signal levels

Timings for DSI Video mode

Vertical Timings

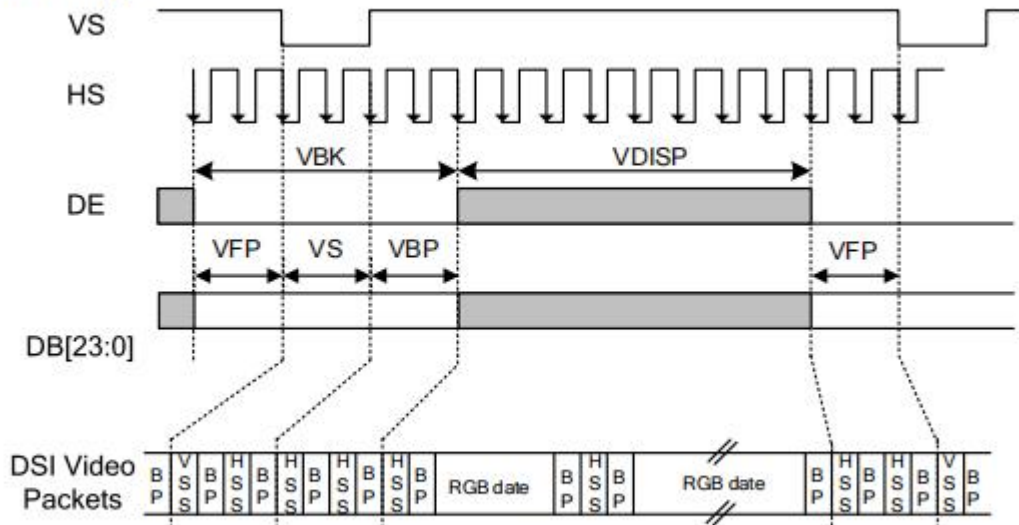


Figure 11.12: Vertical Timings for DPI I/F

5.4 RGB interface

General timing diagram

The image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). If it is returned from out of the range to in range timings, then the correct display image must be displayed automatically (by the display module) on the next frame (vertical sync.).

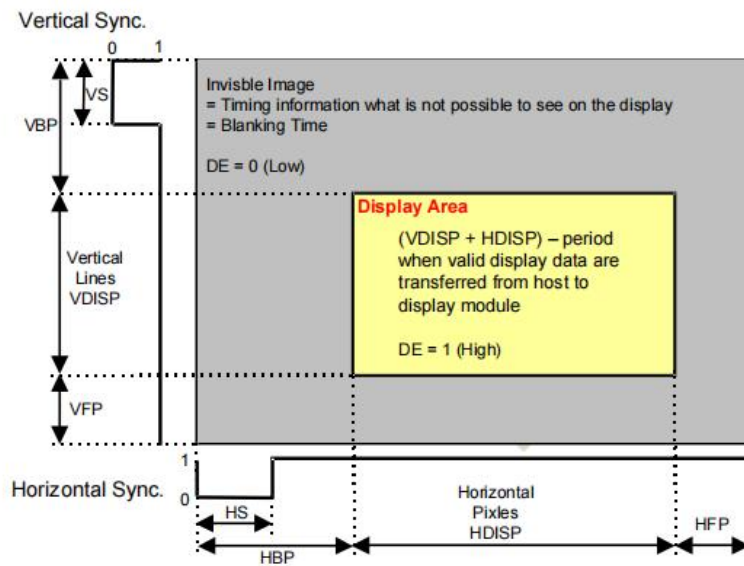


Figure 7.7: General timing diagram

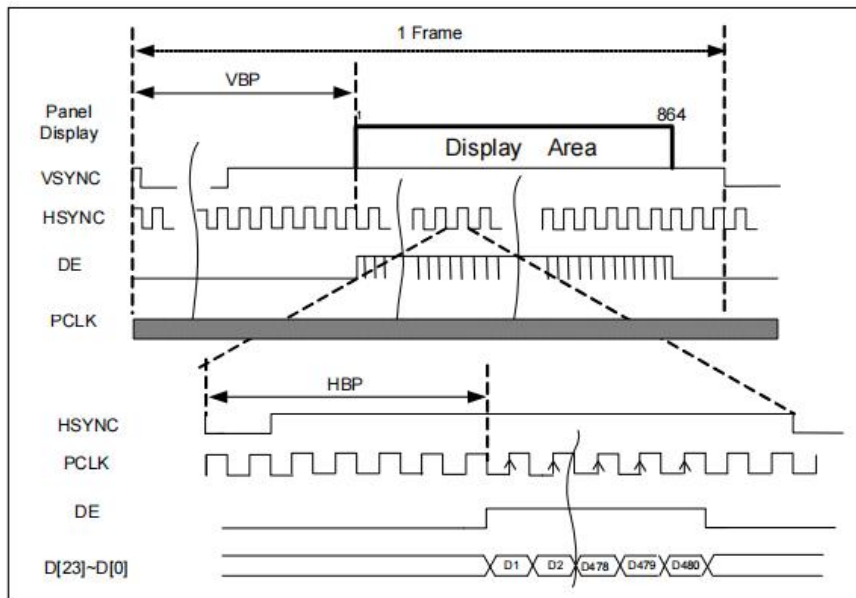
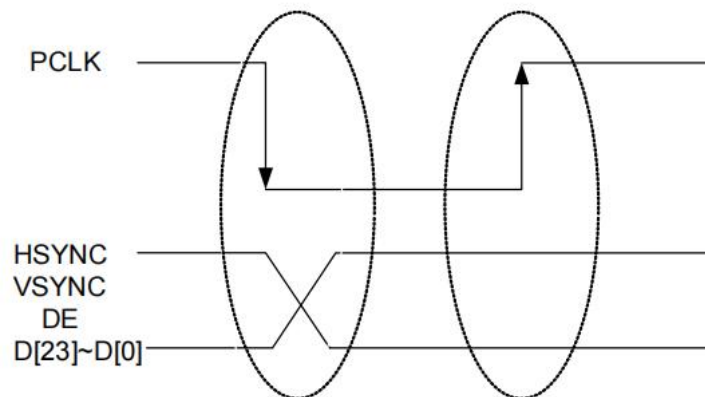


Figure 7.8: RGB (800RGB x 480) timing diagram

RGB Data format

The JD9168S supports 16-bit, 18-bit or 24-bit parallel RGB interface which includes: HSYNC, VSYNC, DE, PCLK, DB[23:0]. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HS, VS, DE and D[23:0] lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In- mode etc. Vertical synchronization (VSYNC) is start signal to receive a “new frame” of the display. This is negative (“-”, “0”, low) active by rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is start signal to receive a “new line” of the frame. This is negative (“-”, “0”, low) active by rising edge of the PCLK- line. Data enable (DE) is used to receive RGB information that should be transferred on the display. This is positive (“+”, “1”, high) active by rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.



Note: PCLK is an unsynchronized signal (It can be stopped).

Figure 7.9: PCLK cycle

Data format	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16 bit (3Ah=0x50)	R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0			
18 bit (3Ah=0x60)	R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0		
24 bit (3Ah=0x70)	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Table 7.2: RGB Interface data format

RGB interface mode select

JD9168S support RGB interface mode 1(SYNC + DE mode) and mode 2(SYNC only mode), it is select by USER command.

In RGB mode 1(SYNC + DE mode), writing data to line buffer is done by PCLK and Video Data Bus (D[23] to D[0]), when DE is high state. The external clocks (PCLK, VSYNC and HSYNC) are used for internal displaying clock. So, controller must always transfer PCLK, VSYNC and HSYNC signal to JD9168S.

In RGB mode 2(SYNC only mode), back porch of Vsync VBP is defined by VBP[7:0]. And back porch of Hsync HBP is defined by HBP[7:0]. Front porch of Vsync VFP is defined by VFP[7:0]. And front porch of Hsync HFP is defined by HFP[7:0].

RGB mode	VSYNC	HSYNC	DE	PCLK	D[23] ~ D[0]	Register VFP[7:0] ,VBP[7:0], HFP[7:0], HBP[7:0]
Mode 1	Used	Used	Used	Used	Used	Not used
Mode 2	Used	Used	Not used	Used	Used	Used

Table 7.3: Interface selection

5.5 LVDS interface

LVDS Data format

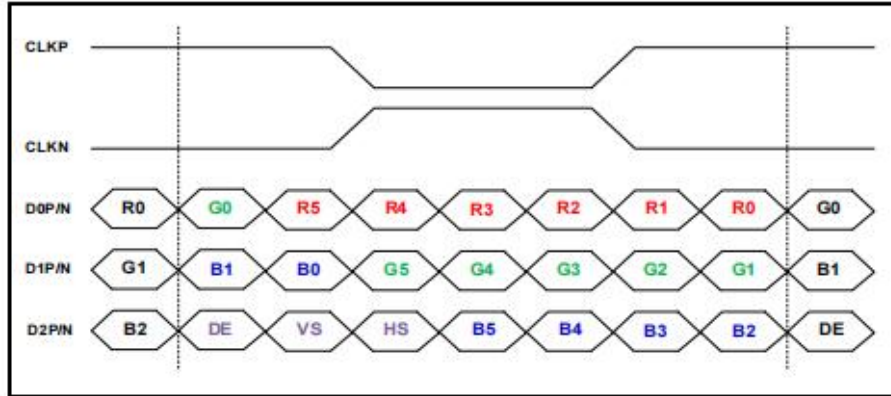


Figure 7.10: 6-bit LVDS input (IM[1:0]=01, LANSEL[1:0]=10, LVFMT=Don't care)

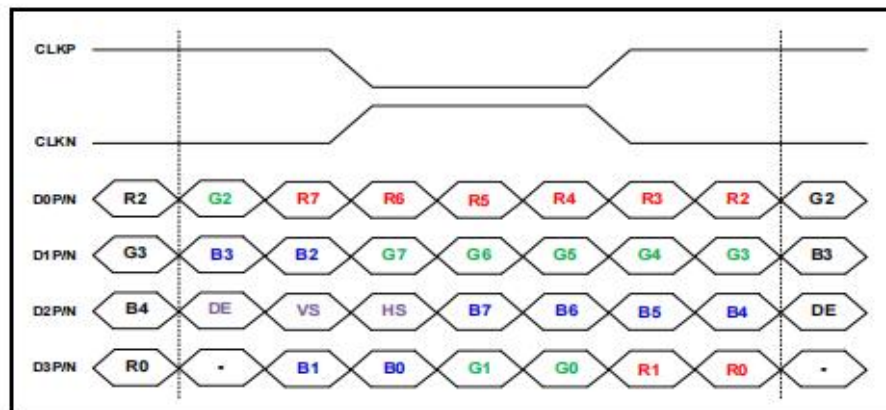


Figure 7.11: 8-bit LVDS input (IM[1:0]=01, LANSEL[1:0]=11, LVFMT=1(JEIDA))

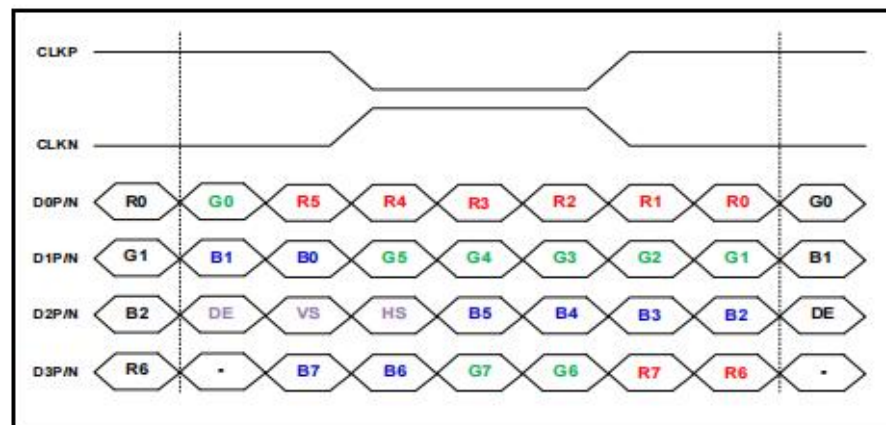


Figure 7.12: 8-bit LVDS input (IM[1:0]=01, LANSEL[1:0]=11, LVFMT=0(VESA))

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	$\Phi=90^\circ$ (12 o'clock)	80	85	-	deg	Note2
	θ_B	$\Phi=270^\circ$ (6 o'clock)	80	85	-	deg	Note2
	θ_L	$\Phi=180^\circ$ (9 o'clock)	80	85	-	deg	Note2
	θ_R	$\Phi=0^\circ$ (3 o'clock)	80	85	-	deg	Note2
Response Time	T_{ON}	Normal $\theta=\Phi=0^\circ$	-	15	17	msec	Note4
	T_{OFF}		-	15	17	msec	Note4
Contrast Ratio	CR		1000	1200	-	-	Note1 Note3
Color Chromaticity	W_X		TBD	TBD	TBD	-	Note1 Note5
	W_Y		TBD	TBD	TBD	-	Note1 Note5
Luminance	L		310	360	-	cd/m ²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		60	65	-	%	-

Note 1: Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.

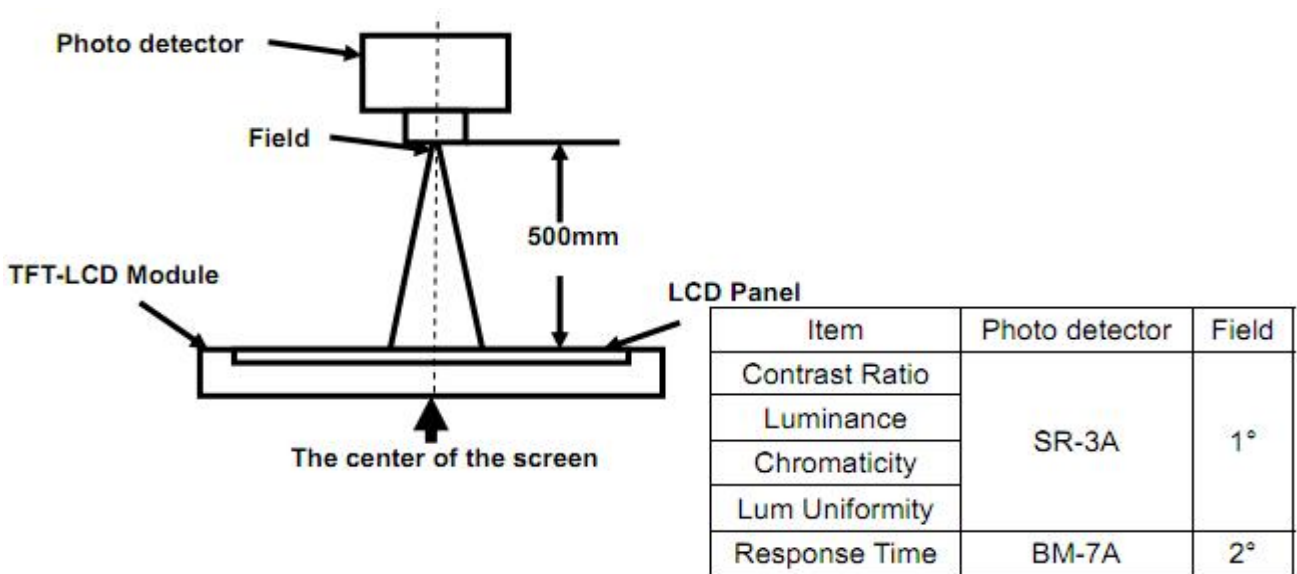


Fig 1

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

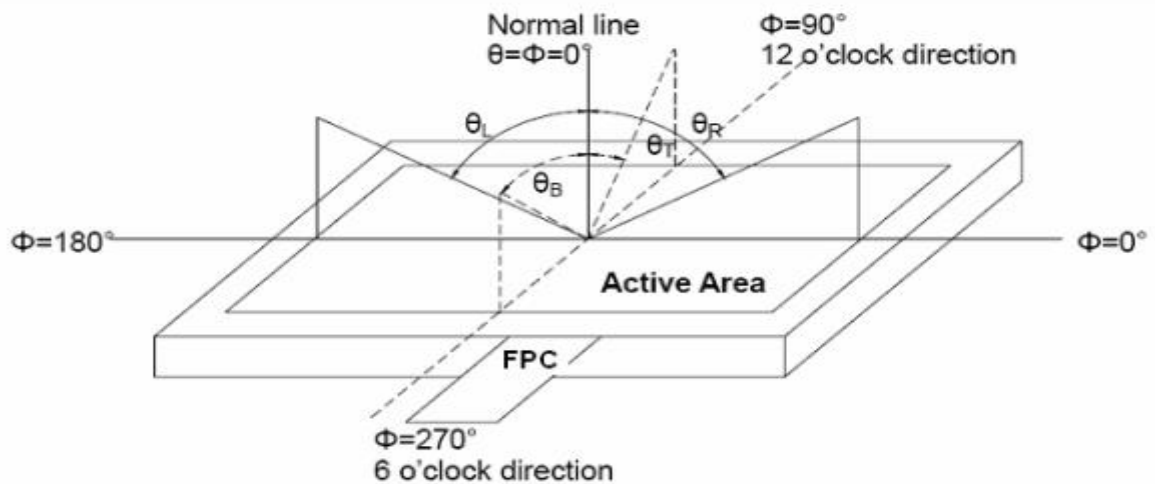


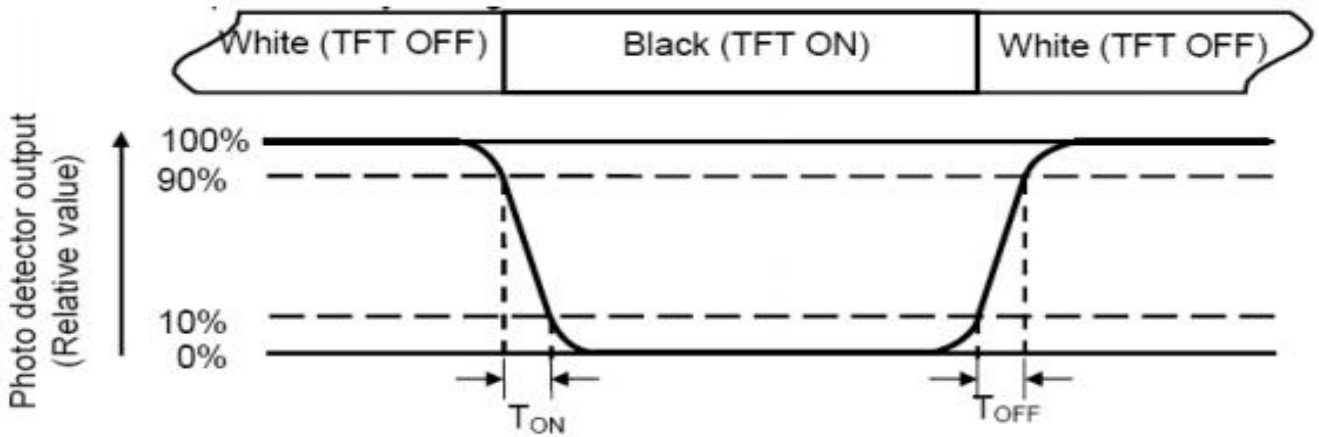
Fig 2 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance. For more information see FIG.3-a/b

Note 7: Surface luminance is the luminance with all pixels displaying white.

$L_v = \text{Average Surface Luminance with all white pixels}(P_1, P_2, P_3, \dots, P_n)$

For more information see FIG.3-a/b

Note 8:

H,V : Active area(see Figure b)

Light spot size $\varnothing = 5\text{mm}$ (BM-5) or $\varnothing = 7.7\text{mm}$ (BM-7)50cm distance or compatible distance from the LCD surface to detector lens. test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter SR-3A or BM-7 or compatible (see Figure 1).

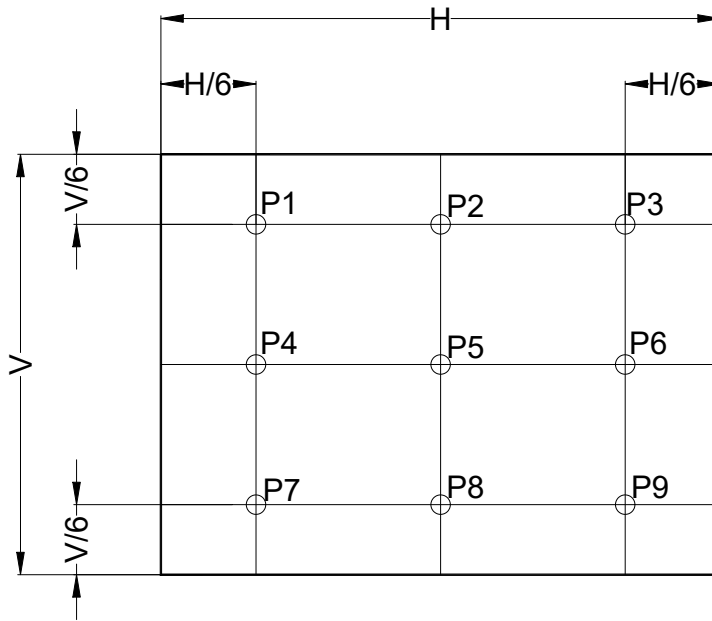


Fig. 3-b Definition of points

7. Reliability Test Items

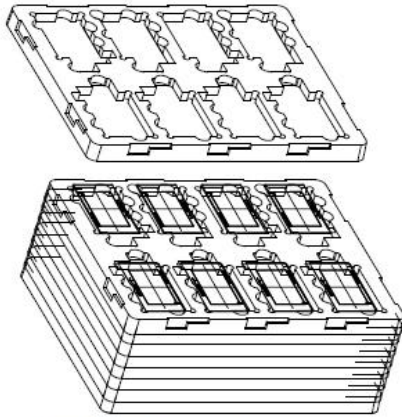
Test Item	Test Conditions
High Temperature Storage	Ta= +80°C 96hrs
Low Temperature Storage	Ta= -30°C 96hrs
High Temperature Operation	Ta= +70°C 96hrs
Low Temperature Operation	Ta= -20°C 96hrs
High Temperature and Humidity Storage	Ta= +60°C, 90% RH 96hrs
Thermal Shock (Non-operation)	-30°C/30 min ~ +80°C/30 min for 20 cycles Start with cold temperature end with high temperature
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

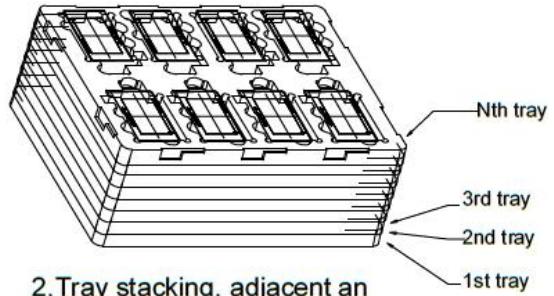
- 1). Air bubble in the LCD
- 2). Seal leak or Glass crack
- 3). Non display or abnormal display
- 4). Brightness reduction >50%

9. Packing

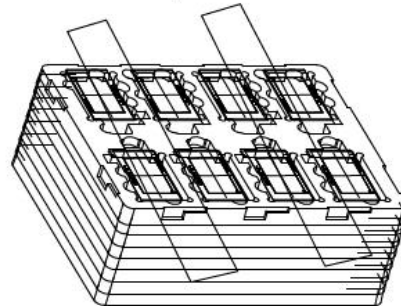
Packing Method



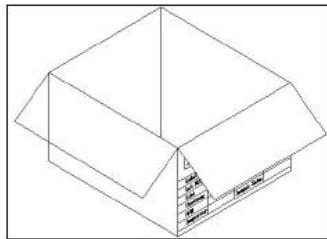
1. Put LCD module into tray cavity



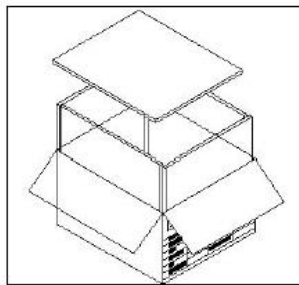
2. Tray stacking, adjacent an upper lower layer with a 180-degree rotation



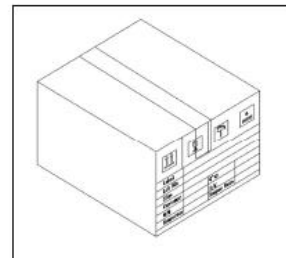
3. Medium Carton: Fix the tray stack with stretch film
Large Carton: Fix the tray stack with stretch film, then place it into a transparent PE antistatic bag



4. put the tray stack into carton



5. 6 sides of white foams inside the box



6. Carton sealing with adhesive tape

10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2. The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time, the recommend condition is :

Temperature : 0°C ~40°C Relatively humidity: ≤80%

10.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

10.4 Packaging instructions

When the customers using trays, they have to stack the adjacent trays in a 180° staggered to prevent pressure that could cause product damage.