DATA SHEET

FT7150

Super In-Cell IC Integrates TFT LCD Driver and Touch Panel Controller Into a Single Chip. Cascade Function for Amorphous TFT-LCDs and Touch Controller Support Real Multi-Touch Capability.

Preliminary

Dec. 10, 2025
Version 0.1

Table of Contents

1. GENERAL DESCRIPTION

FT7150 highly integrates TFT LCD driver and Super in-cell Touch controller. Combined with Super in-cell panel technology, FT7150 provides high performance and high-quality human-machine interactive solutions for tablet display terminals.

FT7150 also support cascade function to achieve higher resolution and smaller sensing pitch, the LCD driver in FT7150 supports 1-chip function maximum resolutions WQXGA MUX 1:1 800RGBx2560 ; MUX 1:2/Dual-gate 1280RGBx1600(DP 60Hz) resolution, and the LCD driver in FT7150 also supports 2-chip cascade function maximum resolutions WQXGA MUX 1:1 1600RGBx2560 ; MUX 1:2/Dual-gate 2560RGBx1600(DP 60Hz) resolution, provides the number of colors up to 16.7M. In addition, FT7150 uses RGB colors each with independently adjustable Gamma correction, 1-dot / 2-dot / 1+2-dot / 1-Column / 2-Column / Zigzag liquid crystal reversion mode and CABC / CE image processing technology, so that it can achieve high resolution, multi-color, high-quality display characteristics.

The touch panel controller of FT7150 uses a 32-bit high-performance single-cycle instruction-set MCU. With its built-in high-speed high-performance hardware-accelerated computing modules, it provides superior data processing capabilities. FT7150 AFE can support up to 800 channels for touch sensing. Combined with Time-Division and Area-Division scanning technology, it greatly reduces the scanning time of touch panel, so that the maximum of point reporting rate could up to 120Hz. With Focaltech's patented drive technology and algorithms, the touch controller has excellent waterproof performance, strong anti-noise-and-interference ability and high signal to noise ratio. Its touch experience can achieve up to 10 points..

In addition, the external Flash of FT7150 can store not only the firmware used for Touch controller, but also the Initial code of LCD driver. After loading the initial code through the external Flash, the HOST only needs to send out "Sleep out" and "Display on" to turn on the LCD. This will greatly simplify the operation of the HOST to LCD, making the configuration process both flexible and simple. Furthermore, when ESD occurs, HOST reloads Initial code directly from Flash, greatly improving the IC's ESD capability.

2. FEATURES

2.1. Touch Function feature list

- **32-bit embedded single-cycle instruction-set MCU**
  - Built-in hardware acceleration module
  - Program storage size: 112K Byte SRAM
  - Data storage size: 96K Byte SRAM
- **Super self-capacitance detection technology**
- **Supports up to 800 SX channels**
- **Supports up to 10pF capacitive sensing per channel**
- **10-point Real Touch**
- **Anti-floating**
- **Anti-power interference**
- **Anti-stress from external**
- **Anti-RF interference**
- **Point reporting rate up to 120Hz**
- **I2C data communication interface**
- **SPI data communication interface**
- **Support THP(Touch Host Processing)**

2.2. Display Function feature list

- **Support HD+ a-Si TFT LCD Driver without GRAM**
- **Support Flash initialization with initial code inside**
- **Support 120Hz/90Hz/60Hz/30Hz/15Hz frame rate & VESA DSC 3X decode**
- **Support Resolution :**
  - 2-chip with cascade : 2560RGBx1600(DP 60Hz, MUX 1:2/Dual-gate) ; 1600RGB x (2560, others) ; 1536RGB x (2048, others) ; 1440RGB x(2560, others) ; 1280RGB x (2048, others) ; 1200RGB x (1920, others) ; 1080RGB x (1920, others)
  - 1 chip : 1280RGBx1600(DP 60Hz, MUX 1:2/Dual-gate) ; 800RGB x (1280, others) ; 768RGB x (1366, others) ;720RGB x (1280, others) ; 600RGB x (1024, others) ; 540RGB x (960, others)

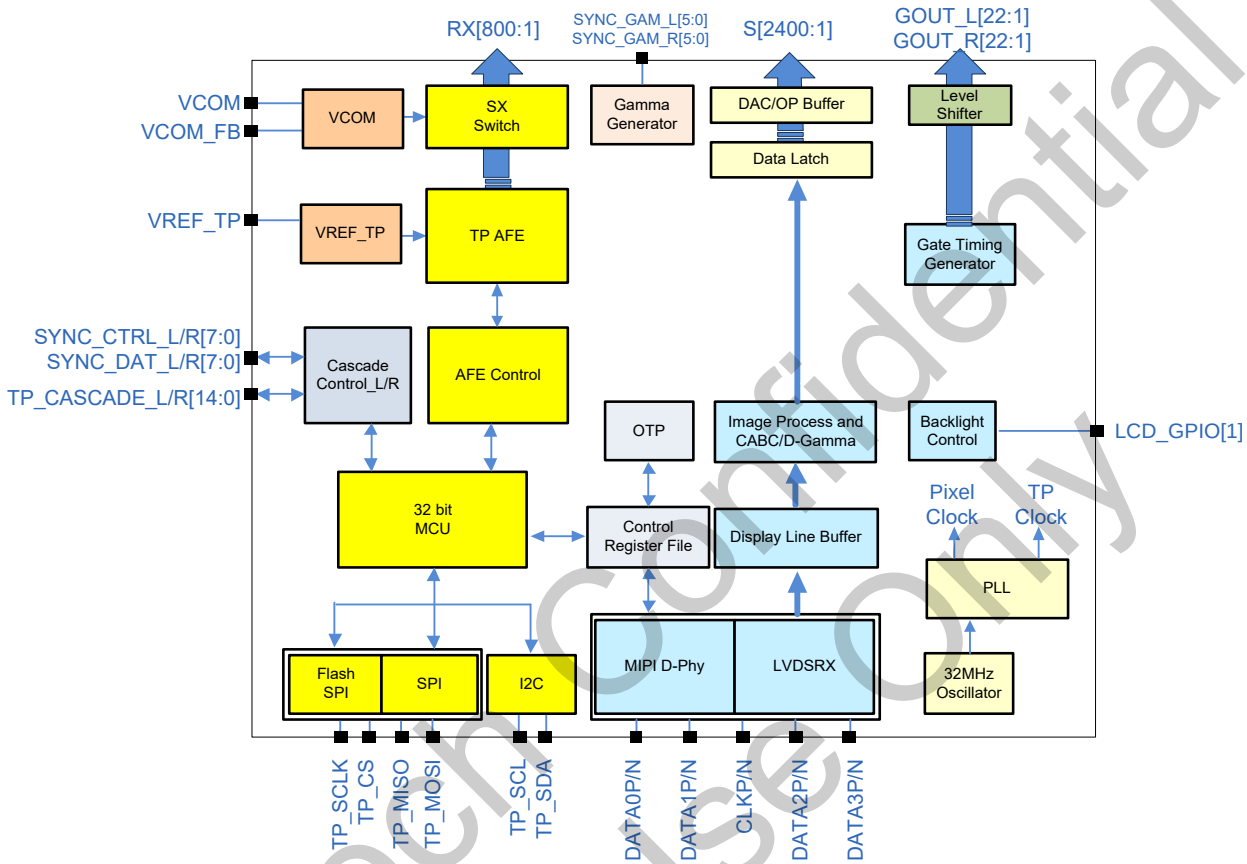
  *Note: Please contact our sales for further help if your resolution is not listed here.
- **Color Display**
  - Full color mode : 16.7M (24-bit, 8(R):8(G):8(B))
- **Support the features that refresh the display function for N-lines with an adjusted pause of 0 ~ 400us (for touch scan) and then continue to refresh the display function for N lines**
- **Display features**
  - Supports independently adjustable RGB gamma correction
  - Support 1-dot / 2-dot and 1-Column / 2-Column / Zigzag LCD reversion modes
  - Support Slew Rate control on Source driver
- **Built-in Focal CleverColor Image processing functions**
  - CleverColor – Color Enhancement$_{opt1.0}$
  - CleverColor – CABC$_{opt1.0}$
  - CleverColor – AIE$_{opt1.0}$
  - CleverColor – Digital Gamma$_{opt1.0}$
  - CleverColor – Contrast$_{opt1.0}$
  - CleverColor – WA$_{opt1.0}$
  - CleverColor – Sharpness Enhancement$_{opt1.0}$ (Not Support in Cascade Mode)
- **Interface**
  - MIPI DPHY Interface (DPHY V1.1 with 2/3/4 Lane), Max Speed 1.1Gbps
  - MIPI Display Serial Interface (DSI-2 V1.0)
  - MIPI Display Command Set (DCS V1.3)
  - LVDS interface (RGB24bit data format) , Max Speed 770 Mbps
- **On Chip function**
  - Built-in VCOM Generator
  - Provide OTP to store VCOM/ID1/ID2/ID3
  - Save command setting in external flash memory
  - Built-in Oscillator for display clock generation
  - On module checksum checking
  - Built-in 22 GOUT signals (GOUT1 ~ GOUT22) on each side of the chip, providing the drive signals to the GIP circuit on the LCD panel

- Temperature Compensation for VGHO/VGLO/VCOM

- **Output voltage levels**
  - Source output voltage level: (GVDDP~+0.1V) and (-0.1V~GVDDN)
  - Gamma voltage range: GVDDP: 3.75V ~ 6.3V, GVDDN: -3.75V~-6.3V
  - Positive gate driver output voltage range: 5.8V~6.2V;7.8V~20V
  - Negative gate driver output voltage range: -5.3V~-18V
  - Common electrode output voltage level VCOM: +0.3V ~ -3.85V
- **Supply Voltage Range**
  - I/O and logical circuit power: 1.65V ~ 1.95V (MIPI), 2.7V~3.6V(LVDS)
  - Positive Analog supply voltage range: 4.5V ~ 6.5V
  - Negative Analog supply voltage range: -4.5V ~ -6.5V
- **Support OTP Multiple Program Times**
  - ID for 5 times programmable
  - GVDD for 2 times programmable
  - Gamma for 2 times programmable
  - VCOM for 8 times programmable
  - User Info for 5 times programmable
  - Please refer to the application note to get detailed information about multiple program times.
- **Support Power Mode:**
  - 3 Power Mode: VDDI / AVDD / AVEE
  - 4 power Mode: VDDI / AVDD / AVEE / VDD

3. BLOCK DIAGRAM

3.1. Block Function



3.1.1. System interface

FT7150 supports the video data transmitted through the high-speed system interface, MIPI (Mobile Industry Processor) interface or LVDS interface, and I2C/SPI interface for the touch point-reporting function.

In normal operating mode, touch controller scans the screen, and detects the touch actions. The default setting of point-reporting rate is set as 60Hz/120Hz and can be adjusted up or down. In touch detection mode, touch controller enters low-power mode, detects and scans touch-screen body. Detection scanning frequency is 30Hz, can also be adjusted up or down. During touch detection mode, majority of the algorithm will be terminated, and only a simple detection algorithm is retained to detect if there is a touch action happened. Whenever a touch is detected, touch controller will immediately enter the normal operating mode.

In sleep mode, touch controller enters ultra low-power standby mode, HOST can only wake-up touch controller via "RESET" or "WAKEUP" signal to enter the normal operating mode. The power consumption in this mode is extremely small, can greatly extend the standby time of mobile portable devices.

3.1.2. AFE Controller

AFE controller completes the driving and scanning functions of the sensors in the touch panel, and sends the data from touch sensors after scanning to the MCU for data processing.

3.1.3. Embedded MCU

MCU and SOC subsystems complete the control, data processing, LCD operation and coordination, HOST communication and other functions of the whole touch systems. Firmware, stored in external flash memory, can be loaded into the internal SRAM by HOST via the I2C or SPI interface. Firmware can also be download from HOST through SPI interface without external FLASH required.

3.1.4. I2C/SPI Serial Interface

FT7150 can support I2C or SPI for touch communication with HOST. The control interface is consisted of two signals, INT and TP_EXT_RSTN. Whenever there is an effective touch sensed on the touch screen, touch controller will send data transfer request to the HOST via INT port, and complete the point report to the HOST. HOST can communicate with FT7150 via I2C. HOST can also reset Touch controller through TP_EXT_RSTN port.

3.1.5. LCD/TP I2C Interface

FT7150 can support LCD/TP I2C to set LCD initial code to the FT7150 IC.

3.1.6. External Flash

External Flash, used to store the Firmware, internal voltage regulator generates 1.8V power supply, which is to provide power to an external 1.8V Flash. In non-Flash application, Firmware could be downloaded from HOST through SPI interface.

3.1.7. Watch Dog

Watchdog clock is used to ensure the stability of the chip when in operation

3.1.8. Timing controller

The timing controller generates timing signals for the operations of internal circuits such as gate/source/vcom/ touch scan output timing.

3.1.9. Source driver circuit

The source driver circuit is consisted of 2400-channels source driver (S1 ~ S2400). The RGB Data from MIPI interface are latched when a single line data has been accumulated. The latched data generates the liquid crystal drive voltage from the source based on the grayscale settings in gamma correction function.

3.1.10. Gate driver circuit

The gate driver circuit outputs gate driver signals at either VGHO or VGLO level while LCD driving.

3.1.11. SX driver circuit

Supply VCOM level when LCD driving. Generates TP sensing pulse when TP driving.

3.1.12. Oscillator (OSC)

FT7150 also features an internal oscillator to generate RC oscillation with an internal resistor.

3.1.13. Grayscale voltage generating circuit

FT7150 has true 8-bit resolution D/A converter, which generates 256 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register and RGB can be adjusted separately.

3.1.14. LCD driving power supply circuit

The LCD driving power supply circuit generates the voltage levels AVDD, AVEE, VGH, VGL and VCOM for driving an LCD. All these voltages can be adjusted by register setting.

4. PIN DESCRIPTIONS

4.1. Pin Definition

Signal	I/O	PAD Type (Voltage Level)	Function
Power Supply Pad			
AVDD	I	Analog Power	4.5V~6.5V Connect a capacitor for stabilization
AVEE	I	Analog Power	-4.5V~-6.5V Connect a capacitor for stabilization
AVDDR	I	Analog Power	4.5V~6.5V for MV regulator FPC Connect together with AVDD
AVEER	I	Analog Power	-4.5V~-6.5V for MV regulator FPC Connect together with AVEE
VDDI	I	Analog Power	Power Supply for IO, 1.65V~1.95V(MIPI application) / 2.7V~3.6V(LVDS application) Connect a capacitor for stabilization
VDDAM	I	Analog Power	Power Supply for MIPI LDO, 1.65V~1.95V(MIPI application) / 2.7V~3.6V(LVDS application) FPC Connect together with VDDI
AVSS	I	Analog Ground	Ground for Analog Circuits.
VSS	I	Digital Ground	Ground for Digital Circuits.
LVDSVSS	I	Digital Ground	Ground for MIPI Circuits.
AVSSR	I	Analog Ground	Ground for MV Regulator.
DC-DC Converter Pad			
VGH_L VGH_R	O	Internal Power	Positive Charge Pump Power. FPC Connect together. Connect a capacitor for stabilization between VGH_L/VGH_R and VGHB.
VGHB	O	Internal Power	Connect a capacitor for stabilization between VGH_L/VGH_R and VGHB.
VGL	O	Internal Power	Negative Charge Pump Power. Connect a capacitor for stabilization.
C21P/C21N C22P/C22N	I/O	Step-up capacitor	Flying cap for VGH Charge Pump. Connected to a capacitor as requirement.
C31P/C31N	I/O	Step-up capacitor	Flying cap for VGL Charge Pump. Connected to a capacitor as requirement.
Regulator Pad			
VGHO_L VGHO_R	O	Internal Power	Switch output voltage for GIP circuit. FPC Connect together. Connect a capacitor for stabilization between VGHO and VGHO1B.
VGHO1B	O	Internal Power	Connect a capacitor for stabilization between VGHO and VGHO1B.
VGH1_L/R VGH2_L/R	O	Power Input	This pin is used to discharge function. FPC Connect together. If not used, please let these pins short to VGHO
VGLO_L VGLO_R	O	Internal Power	Regulator output voltage generated from VGL. FPC Connect together. Connect a capacitor for stabilization between VGLO and VGLO1B.
VGLO1B	O	Internal Power	Connect a capacitor for stabilization between VGLO and VGLO1B.
VCL	O	Internal Power	Regulator output voltage. Connect a capacitor for stabilization.
VDD	O	Internal Power	Regulator output voltage, Connect a capacitor for stabilization.
LVDSVDD	O	Internal Power	Regulator output voltage,

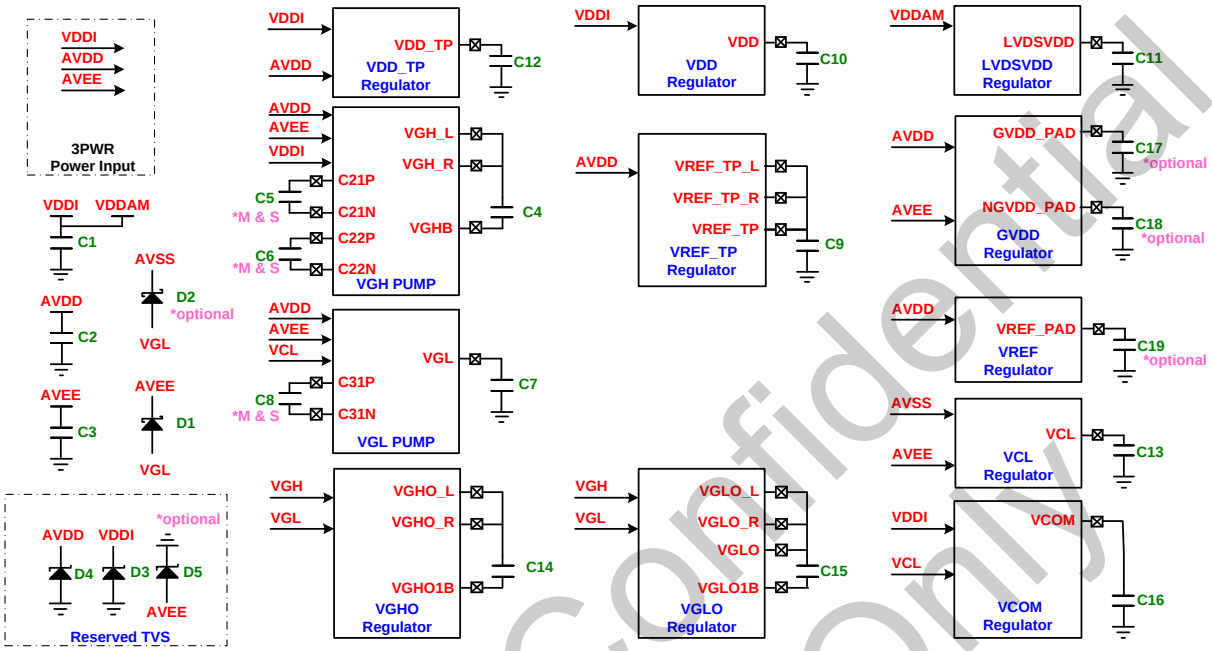
<table>
<tr><th>Signal</th><th>I/O</th><th>PAD Type
(Voltage Level)</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td>Connect a capacitor for stabilization.</td></tr>
<tr><td>VDD_TP</td><td>O</td><td>Internal Power</td><td>Regulator output voltage,
Connect a capacitor for stabilization.</td></tr>
<tr><td>VREF_TP
VREF_TP_L
VREF_TP_R</td><td>O</td><td>Internal Power</td><td>Regulator output voltage. FPC Connect together
Connect a capacitor for stabilization.</td></tr>
<tr><td>VDD5_L
VDD5_R</td><td>O</td><td>Internal Power</td><td>Regulator output voltage. FPC Connect together
Connect a capacitor for stabilization.</td></tr>
<tr><td>VCOM</td><td>O</td><td>Internal Power</td><td>Regulator output voltage.
Connect a capacitor for stabilization. Capacitor must be in the middle of FPC.</td></tr>
<tr><td>VCOM_FB</td><td>I</td><td>Internal Power</td><td>Feedback for VCOM circuit</td></tr>
<tr><td colspan="4">LCD Interface Logic Pad</td></tr>
<tr><td>RESX</td><td>I</td><td>Digital (VDDI)</td><td>Global Reset Signal. Active Low.</td></tr>
<tr><td>DSWAP[1:0]</td><td>I</td><td>Digital (VDDI)</td><td>when IM=0, please see DHPY swap table
MIPI lane swap control.
MIPI data lane swap and polarity swap table (4 Data Lane)
<table>
<tr><th>PNSWAP</th><th>DSWAP[1:0]</th><th>DSI-D2+</th><th>DSI-D2-</th><th>DSI-D1+</th><th>DSI-D1-</th><th>DSI-CLK+</th><th>DSI-CLK-</th><th>DSI-D0+</th><th>DSI-D0-</th><th>DSI-D3+</th><th>DSI-D3-</th></tr>
<tr><td rowspan="8">DPHY</td><td rowspan="4">0</td><td>00</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr>
<tr><td>01</td><td>D3-</td><td>D3+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td></tr>
<tr><td>10</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>11</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D3-</td><td>D3+</td></tr>
<tr><td rowspan="4">1</td><td>00</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>01</td><td>D3+</td><td>D3-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td></tr>
<tr><td>10</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>11</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D3+</td><td>D3-</td></tr>
</table>
WHEN IM=1, please see LVDS Lanes swap table
note: reg_lvds_dswap_M/S[2] setting by register, please see FT7150 AN “LVDS_SET”
<table>
<tr><th colspan="12">LVDS Lanes SWAP table</th></tr>
<tr><th colspan="2">SOFT controller</th><th colspan="2">HW controller</th><th colspan="8">PAD Name</th></tr>
<tr><th>register setting
(reg_lvds_dswap_M/S[2])</th><th>PSWAP</th><th>DSWAP[1:0]</th><th>DATA2P</th><th>DATA2N</th><th>DATA1P</th><th>DATA1N</th><th>CLKP</th><th>CLKN</th><th>DATA0P</th><th>DATA0N</th><th>DATA3P</th><th>DATA3N</th></tr>
<tr><td rowspan="8">0</td><td rowspan="4">0</td><td>00</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td><td>CLKN</td><td>CLKP</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td></tr>
<tr><td>01</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td><td>CLKN</td><td>CLKP</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td></tr>
<tr><td>10</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>CLKN</td><td>CLKP</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>11</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>CLKN</td><td>CLKP</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td></tr>
<tr><td rowspan="4">1</td><td>00</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>CLKP</td><td>CLKN</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>01</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>CLKP</td><td>CLKN</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr>
<tr><td>10</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>11</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr>
<tr><td rowspan="8">1</td><td rowspan="4">0</td><td>00</td><td>D0N</td><td>D0P</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>D3N</td><td>D3P</td><td>CLKN</td><td>CLKP</td></tr>
<tr><td>01</td><td>D2N</td><td>D2P</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>CLKN</td><td>CLKP</td><td>D3N</td><td>D3P</td></tr>
<tr><td>10</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td><td>CLKN</td><td>CLKP</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td></tr>
<tr><td>11</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>CLKN</td><td>CLKP</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td></tr>
<tr><td rowspan="4">1</td><td>00</td><td>D0P</td><td>D0N</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D3P</td><td>D3N</td></tr>
<tr><td>01</td><td>D2P</td><td>D2N</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D3P</td><td>D3N</td></tr>
<tr><td>10</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td><td>CLKP</td><td>CLKN</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>11</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr>
</table></td></tr>
<tr><td>PNSWAP</td><td>I</td><td>Digital (VDDI)</td><td>MIPI polarity control. IC Internal pull High.</td></tr>
<tr><td>IM</td><td>I</td><td>Digital (VDDI)</td><td>Interface selection table
0 : MIPI (D-PHY)
1: LVDSRX
IC Internal pull Low.</td></tr>
<tr><td>LANSEL[1:0]</td><td>I</td><td>Digital (VDDI)</td><td>Interface selection table
<table>
<tr><th>LANSEL[1:0]</th><th>Interface Selection</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>MIPI-2Lane</td></tr>
<tr><td>10</td><td>MIPI-3Lane</td></tr>
<tr><td>11</td><td>MIPI-4Lane</td></tr>
</table>
IC Internal pull High.</td></tr>
</table>

Signal	I/O	PAD Type (Voltage Level)	Function
			When IM =1, this is no function
BIST_EN	I/O	Digital (VDDI)	BIST mode enable, High Active. If not used, leave this pin open. IC Internal pull Low.
LCD_GPIO[2:0]	O	Digital (VDDI)	LCD_GPIO can be set as TE, LEDPWM,…etc. If not used, leave this pin open. IC Internal pull Low.
LCD_SCL	I/O	Digital (VDDI)	I2C control signal for LCD controller. IC Internal pull High. Leave it open if not used.
LCD_SDA	I/O	Digital (VDDI)	I2C control signal for LCD controller. IC Internal pull High. Leave it open if not used.
FCS	I	Digital (VDDI)	When IM =1 , Function control by Hardware / Software selection for Display Interface Pad, else "Software register setting". 0 : Software register setting. 1 : Hardware pin setting. IC Internal pull Low.
PON	I	Digital (VDDI)	When FCS = 1, PON = 0 : Sleep in mode PON = 1 : Sleep out mode When FCS = 0, Software register setting.
DISP	I	Digital (VDDI)	Display On. Display mode setting pin. Active high. When FCS = 1, 0/1 : Black display mode / Normal display mode. When FCS = 0, Software register setting.
RL	I	Digital (VDDI)	Horizontal shift direction selection for source output. When FCS = 1, 0 : Reverse (S1 → S2400) (Bump side down view) 1 : Forward (S2400 → S1) (Bump side down view) When FCS = 0, Software register setting.
MIPI-DSI / LVDS Interface input Signals			
CLKP/N	I	MIPI (LVDSVDD)	MIPI-DSI / LVDS CLOCK differential signal input pins. If not used, Please connect to LVDSVSS.
DATA0P/N	I/O	MIPI (LVDSVDD)	MIPI-DSI / LVDS Data differential signal input pins. (Data lane 0) If not used , Please connect to LVDSVSS.
DATA1P/N	I/O	MIPI (LVDSVDD)	MIPI-DSI / LVDS Data differential signal input pins. (Data lane 1) If not used , Please connect to LVDSVSS.
DATA2P/N	I/O	MIPI (LVDSVDD)	MIPI-DSI / LVDS Data differential signal input pins. (Data lane 2) If not used , Please connect to LVDSVSS.
DATA3P/N	I/O	MIPI (LVDSVDD)	MIPI-DSI / LVDS Data differential signal input pins. (Data lane 3) If not used , Please connect to LVDSVSS.
TP Interface Logic Pad			
TP_EXT_RSTN	I	Digital(VDDI)	TP External reset signal., active LOW. If not used, leave this pin open. IC Internal pull High.
TP_BOOTDEVICE	I/O	Digital(VDDI)	Interface select. "0" : I2C (boot with flash) ; "1" : SPI (boot without flash) If not used, leave this pin open.
TP_AFE_SCAN_MODE	I	Digital(VDDI)	Afe scan mode selection signal, 1 : afe scan mode ; 0 : afe normal mode If not used, leave this pin open. IC Internal pull Low.
TP_HOLD	I/O	Digital(VDDI)	HOLD signal to Flash, active LOW. If not used, leave this pin open.
TP_WP	I/O	Digital(VDDI)	write protect signal to Flash, active LOW. If not used, leave this pin open.

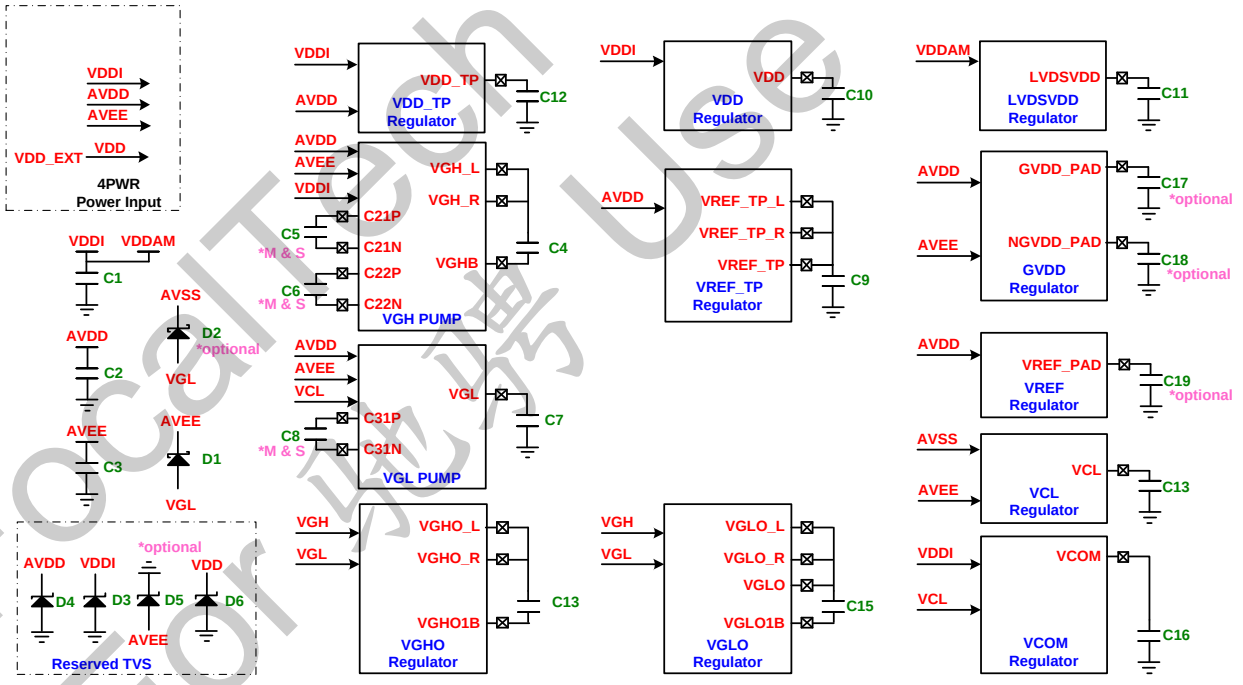
Signal	I/O	PAD Type (Voltage Level)	Function
TP_CS	I/O	Digital(VDDI)	SPI Chip select signal to Flash. If not used, leave this pin open.
TP_SCLK	I/O	Digital(VDDI)	SPI serial clock to Flash. If not used, leave this pin open.
TP_MOSI	I/O	Digital(VDDI)	SPI data output to Flash. If not used, leave this pin open.
TP_MISO	I/O	Digital(VDDI)	SPI data input from Flash. If not used, leave this pin open.
TP_WAKE	I/O	Digital(VDDI)	External wake pin, for Host wake up Touch. If not used, leave this pin open.
TP_SCL	I/O	Digital(VDDI)	I2C interface clock pin for touch. If not used, leave this pin open.
TP_SDA	I/O	Digital(VDDI)	I2C interface data pin for touch. If not used, leave this pin open.
TP_INT	I/O	Digital(VDDI)	External interrupt pin, for Touch interrupt Host. If not used, leave this pin open.
TP_GPIO[1:0]	I/O	Digital(VDDI)	Test pin or I2C master. If not used, leave this pin open.
EMR_GPIO[2:0]	I/O	Digital(VDDI)	Test pin for TP performance.
Test Pad			
VREF_PAD	O	Internal Power	Regulator output voltage. (for LCD internal reference voltage) Connect a capacitor for stabilization (option).
GVDD_PAD	O	Internal Power	Regulator output voltage (for positive gamma voltage generator). Connect a capacitor for stabilization (option).
NGVDD_PAD	O	Internal Power	Regulator output voltage (for negative gamma voltage generator). Connect a capacitor for stabilization (option).
DCHG1	O	Analog Output	For gate signal(Group1:GOUT[4:1], GOUT[22:17]) slope control usage. If user wants to use, please connect a resistor. If not used, please tie it to open.
DCHG2	O	Analog Output	For gate signal(Group2: GOUT[16:5]) slope control usage. If user wants to use, please connect a resistor. If not used, please tie it to open.
EXT_LV	I	Digital(VDDI)	Test pin for the function of external VDD(1.2V) power supply. “H” : 1.2V is generated from external power “L” : 1.2V is generated from internal regulator If not used, leave this pin open. IC Internal pull Low.
LCD_EXT_OSC	I	Digital(VDDI)	LCD test mode, external clock input. If not used, leave this pin open.
TEST[14:0]	I/O	Digital(VDDI)	LCD test pin. If not used, leave this pin open. IC Internal pull Low.
POR12_T	O	Digital(VDDI)	TP POR PAD, for test only. If not used, leave this pin open.
POR18_T	O	Digital(VDDI)	TP POR PAD, for test only. If not used, leave this pin open.
AFE_TEST_L[1:0]	O	Analog (AVDD)	TP analog test pin, not accessible to user. If not used, leave this pin open.
AFE_TEST_R[1:0]	O	Analog (AVDD)	TP analog test pin, not accessible to user. If not used, leave this pin open.
S[2400:1]	O	Analog (AVDD)	Source Output
SDUM[3:0]	O	Analog (AVDD)	Source Dummy Pin (For ZigZag Panel)
RX[800:1]	O	Analog (AVDD)	Analog touch signal pins to touch panel. (TP Sensor Pins)
SXDUM1 SXDUM2	O	Analog (AVDD)	TP Dummy Pin
VCOM_OPT0	O	Internal Power	For panel outline ring use
VCOM_OPT1	O	Internal Power	For panel outline ring use
GOUT_L[22:1] GOUT_R[22:1]	O	Analog (VGHO/ VGLO)	GOA Output. Please use GOUT[13:6] for CLK application.
Dummy Pad			
VCOM_PASS_L VCOM_PASS_R	--	--	Pass line for VCOM from ILB to OLB
TEST[16:15]	--	--	Dummy pin. Must be left open.
DUMMY_OL	--	--	Dummy pin. Must be left open.
DUMMY_OR	--	--	Dummy pin. Must be left open.
DUMMYB	--	--	Dummy pin. Must be left open.

Signal	I/O	PAD Type (Voltage Level)	Function
DUMMYPHYCK	--	--	leave it floating
DUMMYPHY0	--	--	leave it floating
DUMMYPHY1	--	--	leave it floating
DUMMYPHY2	--	--	leave it floating
DUMMYPHY3	--	--	leave it floating
Cascade Pad			
TP_MS	I	Digital(VDDI)	Master / Slave Select pin. (Internal pull high) 1 : Cascade Master IC or single chip 0 : Cascade Slave IC. IC Internal pull High.
EN_EXT_VCOM	I	Digital(VDDI)	Enable external VCOM. (Internal pull low) 1 : VCOM power form external power IC. 0 : VCOM generated by internal VCOM buffer. IC Internal pull Low.
ENB_CASCADE	I	Digital(VDDI)	Cascade enable. (Internal pull high) 0 : Single chip. 1 : Dual chip IC Internal pull High.
SYNC_CTRL_L[7:0] SYNC_CTRL_R[7:0]	I/O	Digital(VDDI)	LCD cascade signals for synchronization control
SYNC_DAT_L[7:0] SYNC_DAT_R[7:0]	I/O	Digital(VDDI)	LCD cascade signals for display data
TP_CASCADE_L[14:0] TP_CASCADE_R[14:0]	I/O	Digital(VDDI)	TP cascade signals for synchronization control and TP raw data
SYNC_GAM_L[5:0] SYNC_GAM_R[5:0]	I/O	Analog	LCD gamma cascade signals. If not used, leave this pin open.

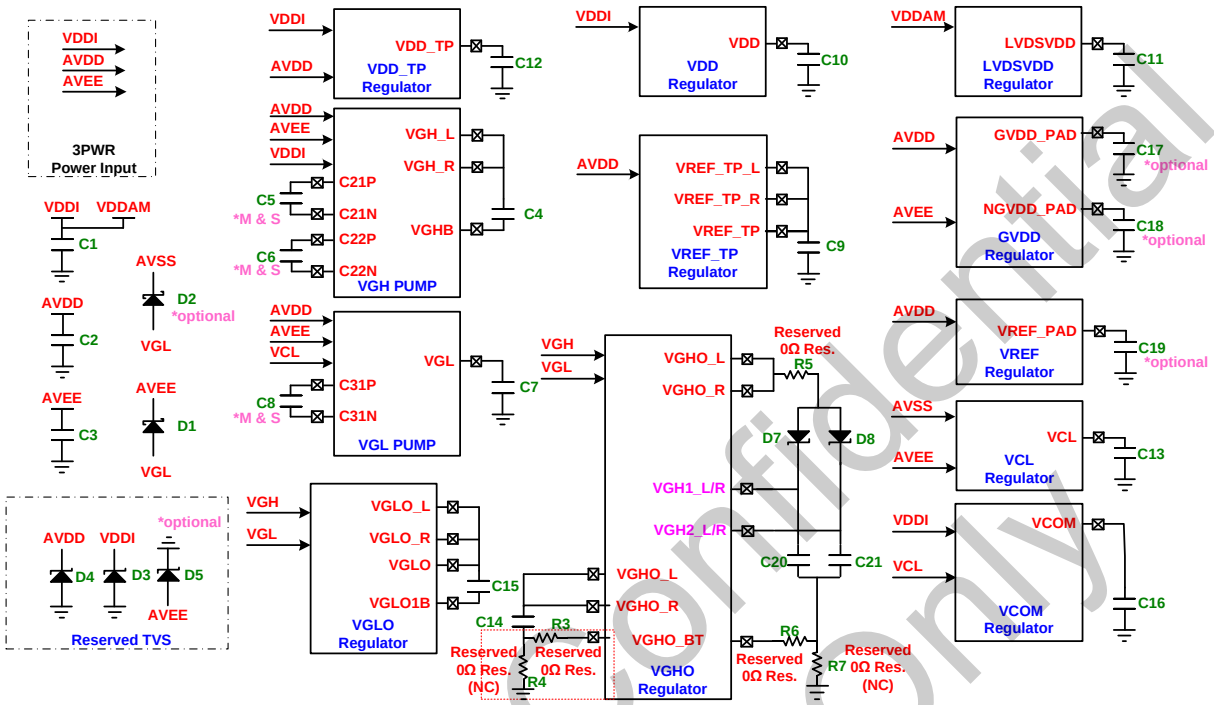
4.2. Power Block Diagram



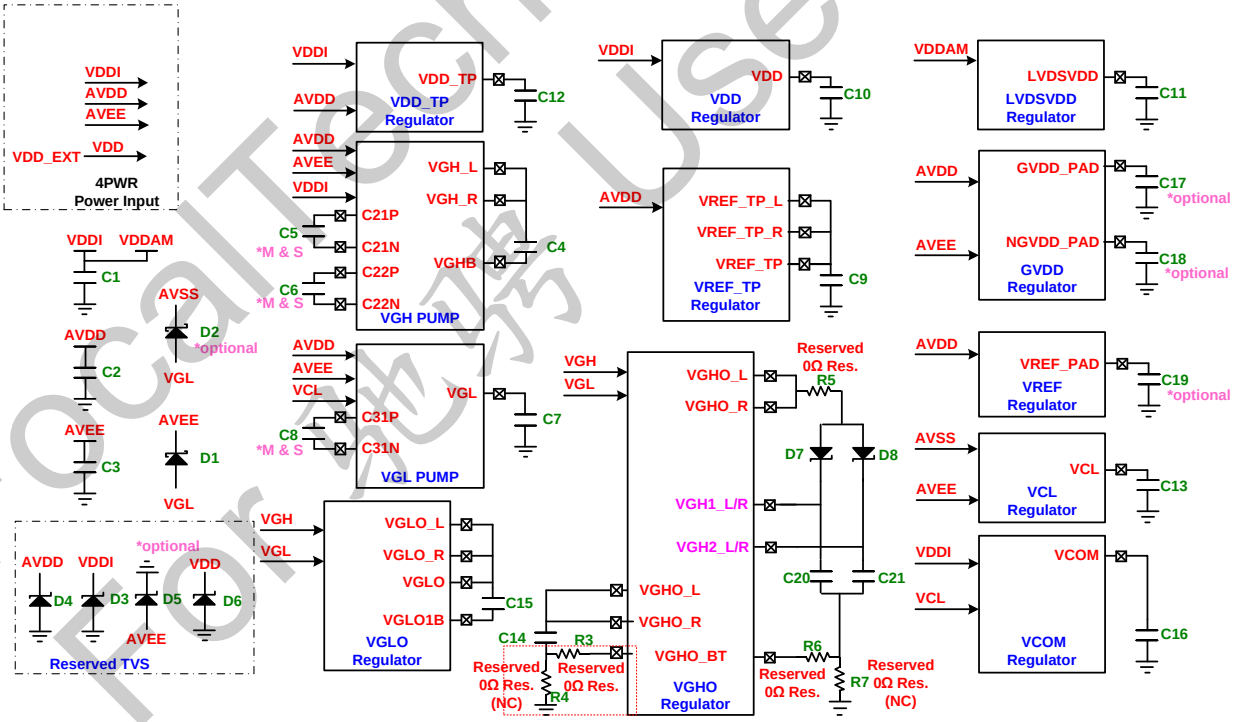
FT7150 Non IGZO



FT7150 Non IGZO

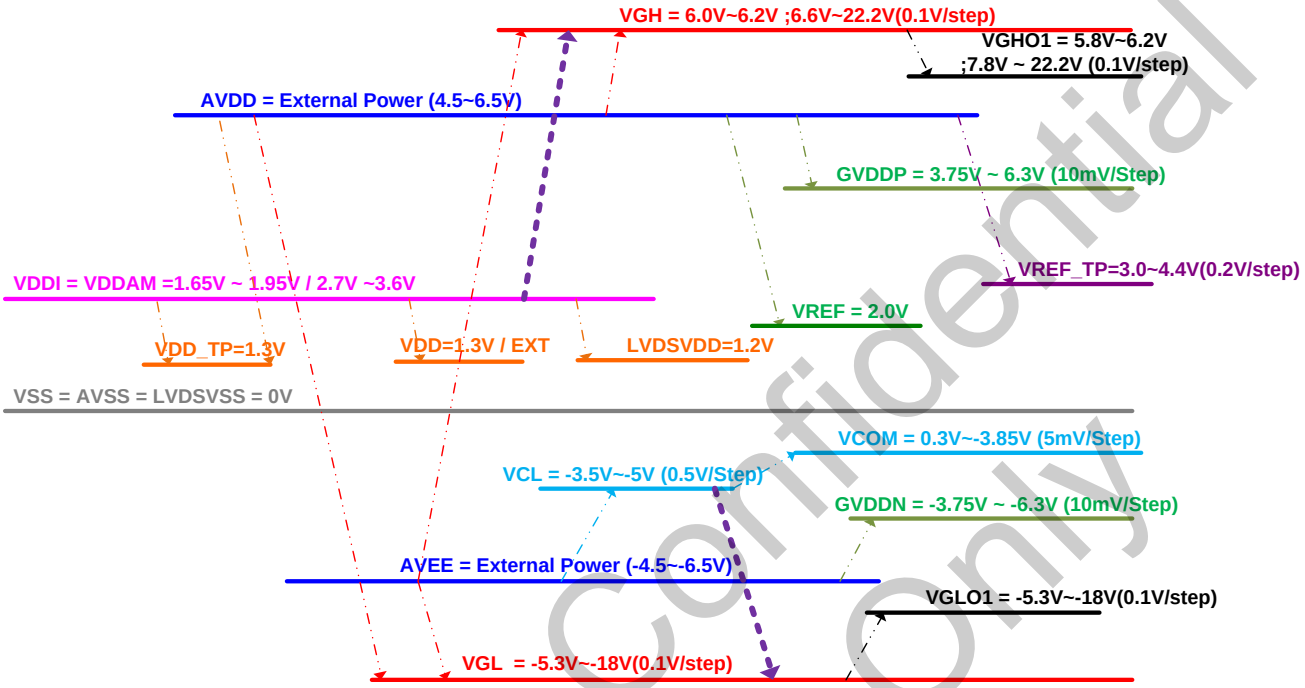


FT7150 IGZO



FT7150 IGZO

4.3. Power Supply Configuration

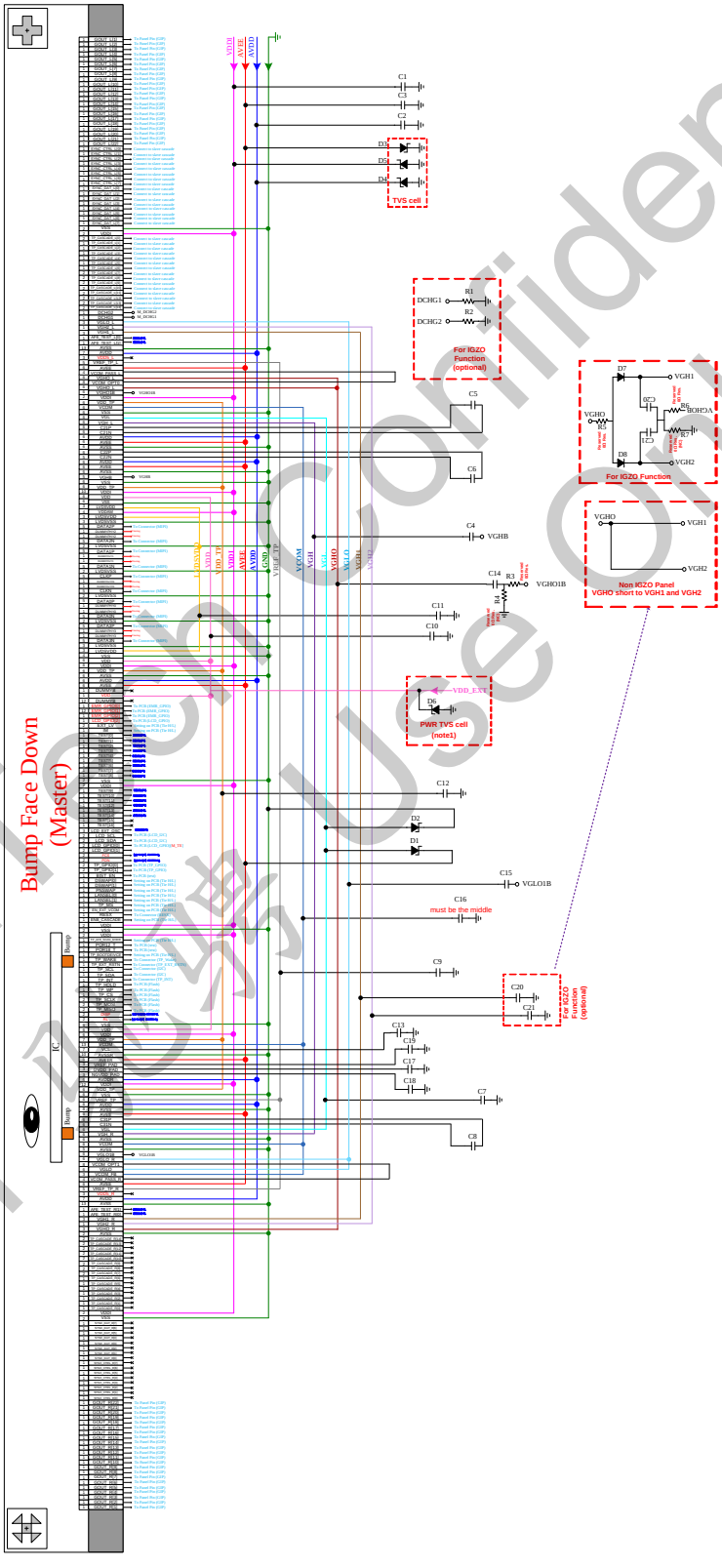


4.4. Application Circuit

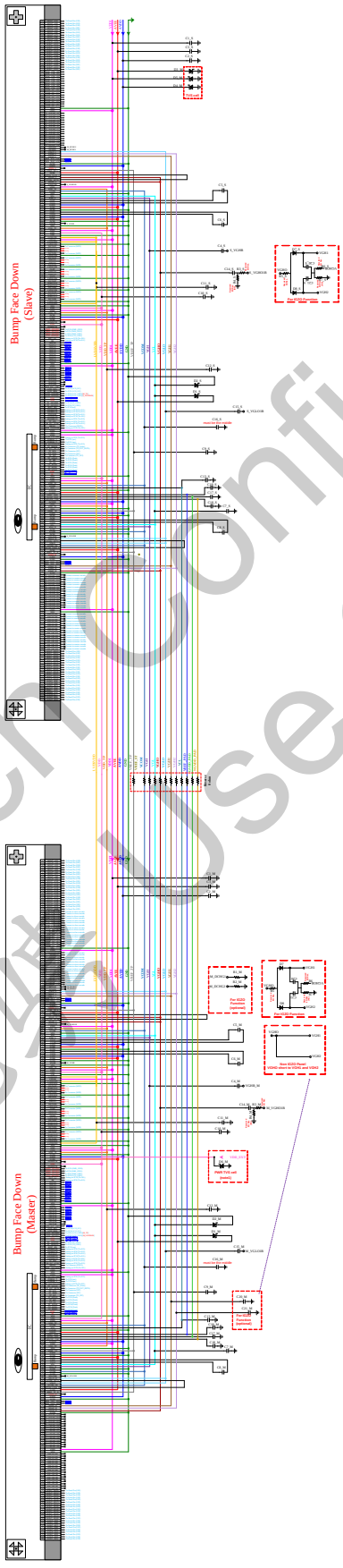
Note1 for 4-Power mode, VDD_EXT connect TVS.

Note2 It's for design reference only! User should contact our sales or FAE for suitable circuit design in actual case.

Single Chip



Dual Chip



4.5. BOM List

Please refer to application note.

4.6. Flash Select

Please refer to application note.

5. INSTRUCTION

5.1. Outline

The FT7150 supports high speed serial interface, MIPI, to configure system via accessing command register. When the command register is executed, sending the command information to specify which index register would be accessed and following the data to that control register. The MIPI interface is compliant with MIPI Alliance Standard for Display Serial Interface (DSI-2), Version 1.00, D-PHY Version 1.1, Display Command Set (DCS), Version 1.3.

The FT7150 has the following major categories of instructions:

(1). System function instructions (User Command Set).

(2). Customer Command List and Description (Manufacturer Command Set / Command 2).

These instructions are asynchronous to the FT7150 internal clock, requiring no wait cycles. Because the writing of instruction data does not interfere with the host controller processing, instructions can be handles smoothly and efficiently. The following describes details of instruction settings.

5.1.1. System function command list and description

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer “RESET TABLE” section). Commands 28h and 29h are updated during V-Blanking to avoid abnormal visual effects. By the way, all commands in master and slave side can be updated concurrently during V-Blanking via MIPI DSI v1.2 FSC function.

System function command access flow is described as following example.

Example 1: Sleep Out

Address 0x11

Example 2: Display On

Address 0x29

Example 3: Bypass Mode

Address 0x09

DATWR 0x01

System Function Command List

Command	(Hex)	Write/Read /Command	Function	Parameter Number	MIPI Transmission
SWRESET	01	**W**	Software Reset.	0	LPDT/HSDT
BISTEN	02	**WR**	BIST Mode Enable. 0x5A : Enable ; Others : Disable	1	LPDT/HSDT
DSCEN	03	**R**	Read VESA DSC Status. 0x00: VDSC Disabled; 0x01: VDSC Enabled	1	LPDT/HSDT
DSTB0	04	**WR**	Deep Standby Mode Enable 0. {DSTB0, DSTB1} = 0x5A5A Enter Deep Standby mode ; others no action.	1	LPDT/HSDT
DSTB1	05	**WR**	Deep Standby Mode Enable 1. {DSTB0, DSTB1} = 0x5A5A Enter Deep Standby mode ; others no action.	1	LPDT/HSDT
LONGH_ENB	09	**WR**	Long-H Mode Disable. 1 : Long-V Mode only ; 0 : Long-H Mode	1	LPDT/HSDT
SLPIN	10	**C**	Sleep in	0	LPDT/HSDT
SLPOUT	11	**C**	Sleep out	0	LPDT/HSDT
MA_TERMR_EN	14	**WR**	Master MIPI Termination Resistor Enable. 0xA5 : Disable Master termination. 0x5A : Force Master Termination. Others : Follow MIPI state	1	LPDT/HSDT
SL_TERMR_EN	15	**WR**	Master MIPI Termination Resistor Enable. 0xA5 : Disable Master termination. 0x5A : Force Master Termination. Others : Follow MIPI state	1	LPDT/HSDT
DISPOFF	28	**C**	Display off	0	LPDT/HSDT
DISPON	29	**C**	Display on	0	LPDT/HSDT
OTP_STOP_RELOAD	41 4E	**WR**	Both [41]/[4E] not equal to 0x5A, OTP perform self-reload periodically. [41] = 0x5A or [4E] = 0x5A, data bus is controlled by external interface and stop OTP reload.	1	LPDT/HSDT
EXT_ADR	42	**WR**	Extended address of I2C and MIPI. SysAddr = {EXT_ADR[6:0] + OFFSET[6:0]}	1	LPDT/HSDT
CMD_REPLY_EN	43	**WR**	0xC3 : Only Slave reply I2C/MIPI readout request Others : Only master reply I2C/MIPI readout request	1	LPDT/HSDT
OTP_CTRL_STS	48	**WR**	OTP Control and status.	1	LPDT/HSDT
DISBV_SET	51h	**W**	Display Brightness Value Setting	1	LPDT/HSDT
DISBV_RD	52h	**W/R**	Read Display Brightness Value	1	LPDT/HSDT
DISBV_CTRL	53h	**W/R**	Display Brightness Value Control	1	LPDT/HSDT
RDDISBV_CTRL	54h	**R**	Read Display Brightness Value Control	1	LPDT/HSDT
WRFCC_CABC	55h	**W**	Write Content Adaptive Brightness Control	1	LPDT/HSDT
RDFCC_CABC	56h	**R**	Read Content Adaptive Brightness Control	1	LPDT/HSDT
OTP_PROG	58h	**W/R**	OTP Program	1	LPDT/HSDT

Note: LPDT (Low Power Mode), HSDT (High Speed Mode)

Note: At MIPI direct mode, no matter MASTER IC or SLAVE IC, cmd need writing by each MIPI bus. Master can't pass cmd to Slave.

5.2. System Function Command Description

5.2.1. SWRESET (01h): Software Reset

Bank -									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
01H (SWRST)	No Parameter								-

Description
SWRST：Software Reset Address = '01H' - When the Software Reset command is written, it causes a software reset to display circuit only. - It resets the commands and parameters to their reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description) Restriction and notes： - It will be necessary to wait 100msec before sending new command following software reset. - The display module loads all display supplier's factory default values to the registers during 100msec. - Software Reset command cannot work during Deep Standby State.

5.2.2. BIST_MODE (02H): Enter BIST mode

Bank -									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
02H	bist_en[7:0]								A5h

Description
bist_en[7:0]： - This command is used to set BIST Mode function '5Ah' = Enter BIST Mode. 'Others' = Exit BIST Mode. Restriction and notes： - Both register software setting and I/O hardware pin can enter BIST Mode function. (Control ORed) - In CASCADE/Direct Mode application, this command should send to Master side that dominates state of both sides.

5.2.3. DSCEN (03H): VESA DSC Enable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
03H	Reserved							VDSC_EN	00h

Description
VDSC_EN： - This command is used to set VESA DSC Mode function '1' = Enable VESA DSC. '0' = Disable VESA DSC. Restriction and notes： - .

5.2.4. DEEP_STBY (04H/05H): Enter Deep Standby Mode

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
04H	DEEP_STBY0[7:0]								00h
05H	DEEP_STBY1[7:0]								00h

Description
- These two command are used to set Deep Standby Mode function. - There are 2 methods that can enter Deep Standby State： Method 1：Set DEEP_STBY0[7:0] = 5Ah and DEEP_STBY1[7:0] = 5Ah in any state. Method 2：Set DEEP_STBY0[7:0] = A5h and DEEP_STBY1[7:0] = A5h when Sleep In Mode. Restriction and notes： - In CASCADE/Direct Mode application, these commands should send to Master side that dominates state of both sides. - Only Hardware Reset can exit Deep Standby Mode, and it will be necessary to wait 100msec before sending new command following hardware reset. - The display module loads all display supplier's factory default values to the registers during 100msec.

5.2.5. LONGH_MODE (09H): Long-H mode disable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
09H	Reserved							longH_enb	00h

Description
LONGH_ENB： - This command is used to disable/enable Long-H Mode function. '1' = Long-H Mode disable.. '0' = Long-H Mode enable.(Default) Restriction： - In CASCADE application, this command should send to Master side that dominates state of both sides.

5.2.6. SLPIN (10H) & SLPOUT (11H) : Sleep-In & Sleep-Out

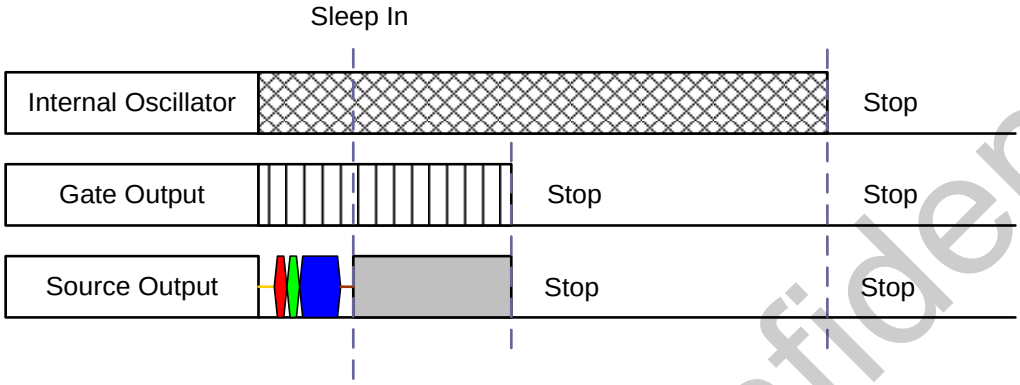
Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
10H (SLPIN)	No Parameter								-
11H (SLPOUT)	No Parameter								-

Description

SLPIN：Sleep-In (Enter Standby Mode)

Address = '10H'

- This command causes the LCD module to enter the power consumption reduced mode.
- In this mode, internal display oscillator is stopped, and panel scanning is stopped.
- Only the command path are still working to support the exit from Standby Mode.



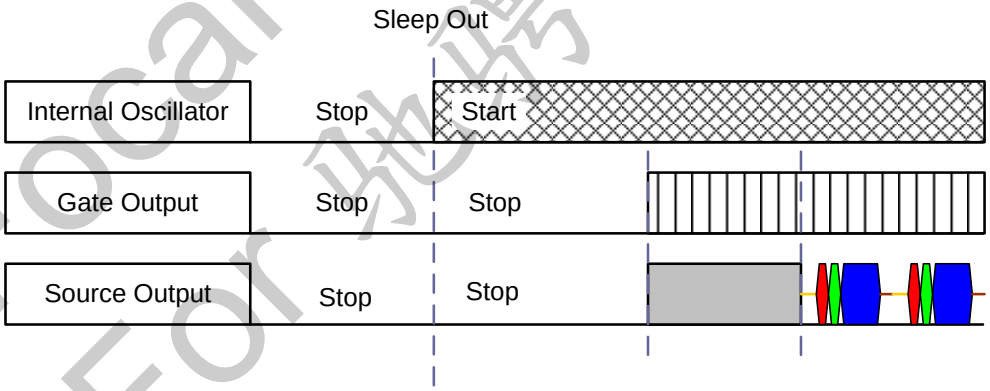
Restriction：

- This command has no effect when module is already in sleep in mode. Standby Mode can only be exit by the SLPOUT Command (11H).

SLPOUT：Sleep-Out (Exit Standby Mode)

Address = '11H'

- This command causes the LCD module to exit the power consumption reduced mode.
- In this mode, internal display oscillator is started, and panel scanning is started.



Restriction：

- This command has no effect when module is already in sleep out mode.
- Sleep Out Mode can only be exit by the SLPIN Command (10H).

5.2.7. TERMR_EN (14H~15H): MIPI TermR Enable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
14H	MA_TERMR_EN[7:0]								FFh
15H	SL_TERMR_EN[7:0]								FFh

Description

MA_TERMR_EN[7:0]：Master Side MIPI TermR Enable
- This command is used to set Master side MIPI TermR enable, disable or normal operation.
'5Ah' = Force to enable MIPI TermR
'A5h' = Force to disable MIPI TermR
'Others' = Normal operation that depends on MIPI High Speed Mode

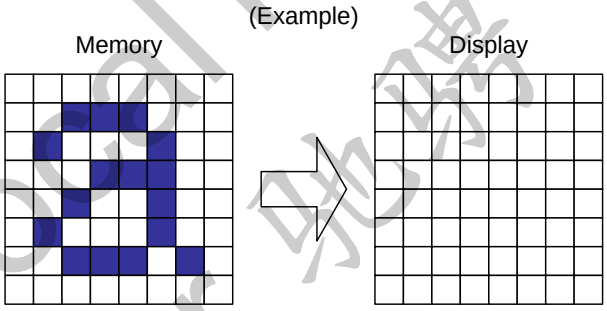
SL_TERMR_EN[7:0]：Slave Side MIPI TermR Enable
- This command is used to set Slave2 side MIPI TermR enable, disable or normal operation.
'5Ah' = Force to enable MIPI TermR
'A5h' = Force to disable MIPI TermR
'Others' = Normal operation that depends on MIPI High Speed Mode

5.2.8. DISPLAY_CTRL (28H~29H) : Display Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
28H (DISPOFF)	No Parameter								-
29H (DISPON)	No Parameter								-

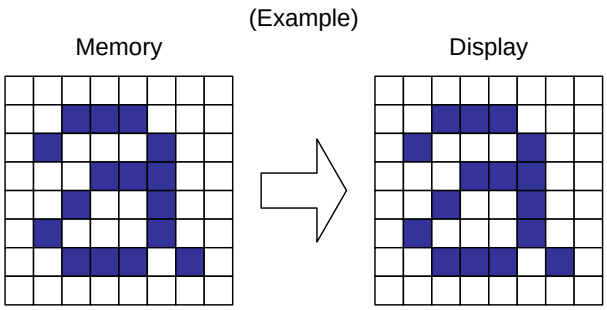
Description

DISPOFF：Display Off
Address = '28H'
- This command is used to enter into DISPLAY OFF mode. In this mode, the output from the Memory is disables and blank page is inserted.
- This command does not change any other status.
- There will be no abnormal visible effect on the display.
- Exit from this command by Display On (29H)



Restriction：
-This command has no effect when module is already in Display Off mode.

DISPON：Display On
Address = '29H'
- This command is used to recover from DISPLAY OFF mode. Output from the Memory is enabled.
- This command does not change any other status.



Restriction：
- This command has no effect when module is already in Display On mode.

5.2.9. OTP_STOP_RELOAD (41H/4EH): OTP Stop Reload Enable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
41H	OTP_STOP_RELOAD[7:0]								00h
4EH	OTP_STOP_RELOAD[7:0]								00h

Description
OTP_STOP_RELOAD：OTP Stop Reload Enable - This command is used to enable OTP stop reload function ‘REG41=5Ah or REG4E=5Ah’ : Stop OTP reload and switch bus to external interface. ‘Others’ : Enable OTP reload and switch bus to reload controller.

5.2.10. EXT_ADR (42H): Extended Address of Command Interface

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
42H		Bank_Sel[6:0]							2Fh

Description
Bank_Sel[6:0]：Bank Selection of following command groups for I2C, MIPI and SYSTEM interface. - This command is used to set extended address of I2C, MIPI and SYSTEM interface.

5.2.11. CMD_REPLY_EN (43H): Command Reply Enable

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
43H	CMD_REPLY_EN[7:0]								00h

Description
CMD_REPLY_EN[7:0]：Command Reply Enable - This command is used to set which side will reply command read data. ‘C3h’ = Slave side replies read data. ‘Others’ = Master side replies read data.

5.2.12. OTP_CTRL_STATUS (48H): OTP Control & Status

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
48H	Reserved	OTP_LOAD_FINISH	OTP_RELOAD_FINISH	SPI_LOAD_FINISH	Reserved	OTP_OP_MODE[2:0]			00h

Description
OTP_LOAD_FINISH (Read-Only)：OTP Initial Load Finish Flag '1' = OTP initial load finish OTP_RELOAD_FINISH (Read-Only)：OTP Reload Finish Flag '1' = OTP reload finish SPI_LOAD_FINISH (Read-Only)：SPI Flash Load Finish Flag '1' = SPI flash load finish OTP_OP_MODE：OTP Operation Mode '000' = Normal Mode '001' = Initial Margin Read '010' = Program Mode '100' = Program Margin Read

5.2.13. DISBV_SET (51H/52H): Display Brightness Value Setting

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
51H	DBV[11:4]								FFh
52H	Reserved				DBV[3:0]				FFh

Description
- This command is used to adjust the brightness value of the display. - It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. - In principle relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness.

5.2.14. DISBV_RD (52H/53H): Read Display Brightness Value

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
52H	DBV[11:4]								FFh
53H	Reserved				DBV[3:0]				FFh

Description
- This command returns the brightness value of the display. - This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode. - It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. - In principle the relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness. - DBV[11:0] is reset when display is in sleep-in mode. - DBV[11:0] is '0' when bit BCTRL of "Display Brightness Value Control (53H)" command is '0'. - DBV[11:0] is manual set brightness specified with "Display Brightness Value Control (53H)" command when bit BCTRL is '1'. - See command "Display Brightness Value Setting (51H)".

5.2.15. DISBV_CTRL (53H): Display Brightness Value Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
53H	Reserved		BCTRL	Reserved	DD	BL	Reserved		00h

Description
- This command is used to control ambient light, brightness and gamma settings. BCTRL：Brightness Control Block On/Off. This bit is always used to switch brightness for display and keyboard. ‘0’ = Off (Brightness registers are 00h) ‘1’ = On (Brightness registers are active, according to the other parameters.) DD：Display Dimming - Dimming function is adapted to the brightness registers for display and keyboard when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. ‘0’ = Display Dimming is off ‘1’ = Display Dimming is on BL：Backlight On/Off - When BL bit change from “On” to “Off”, backlight is turned off ‘0’ = Off (Completely turn off backlight circuit. Control lines must be low.) ‘1’ = On

5.2.16. RDDISBV_CTRL (54H): Read Display Brightness Value Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
54H	Reserved		BCTRL	Reserved	DD	BL	Reserved		00h

Description
- This command returns ambient light and brightness control values, see command “Display Brightness Value Control (53H) ”. BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display. ‘0’ = Off ‘1’ = On ... DD: Display Dimming ‘0’ = Display Dimming is off ‘1’ = Display Dimming is on ... BL: Backlight On/Off, this bit is always controlled by the user ‘0’ = Off (completely turn off backlight circuit) ‘1’ = On

5.2.17. WRFCC_CABC (55H): Write Focal CleverColor – Content Adaptive Brightness Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
55H	Reserved						CABC_MODE[1:0]		00h

Description

- This command is used to set parameters for power functionality.
- There is possible to use 3 different modes for content adaptive image functionality, which are defined on a table below.

CABC_MODE	Function	Note
0h	Power Save Off	CABC Off
1h	Power Save Low	User Interface Image(UI)
2h	Power Save Medium	Still Picture(ST)
3h	Power Save High	Moving Image(MV)

CABC = Content Adaptive Brightness Control

5.2.18. RDFCC_CABC (56H): Read Focal CleverColor – Content Adaptive Brightness Control

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
56H	Reserved						CABC_MODE[1:0]		00h

Description

- This command returns for power functionality see command “Write Focal CleverColor – Content Adaptive Brightness Control (55H) ”.

5.2.19. OTP_PROG (58H/5AH/64H/65H/66H/67H) : OTP Program

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
58H	OTP_PROG _START [7:0]								00h
5AH	OTP_PROG_UNLOCK [7:0]								00h
64H	OTP_PROG_BANK[7:0]								00h
65H	OTP_PROG_BANK[15:8]								00h
66H	OTP_PROG_BANK[23:16]								00h
67H	OTP_PROG_BANK[31:24]								00h

Description

OTP_PROG_START[7:0]：OTP Bank Programming Start
- This command is used to set OTP bank programming start.
- When OTP bank programming is done, register value will be set to EDh.

‘AAh’ = Start OTP bank programming.
‘Others’ = Not programming.

OTP_PROG_UNLOCK[7:0]：OTP Programming Function Unlock
- This command is used to set OTP programming function unlock.

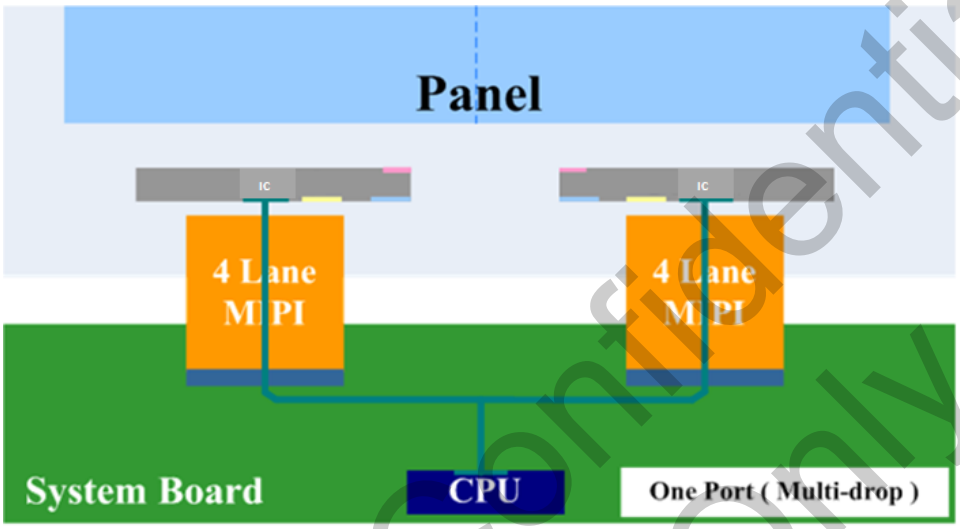
‘96h’ = Unlock OTP programming function.
‘Others’ = Lock OTP programming function.

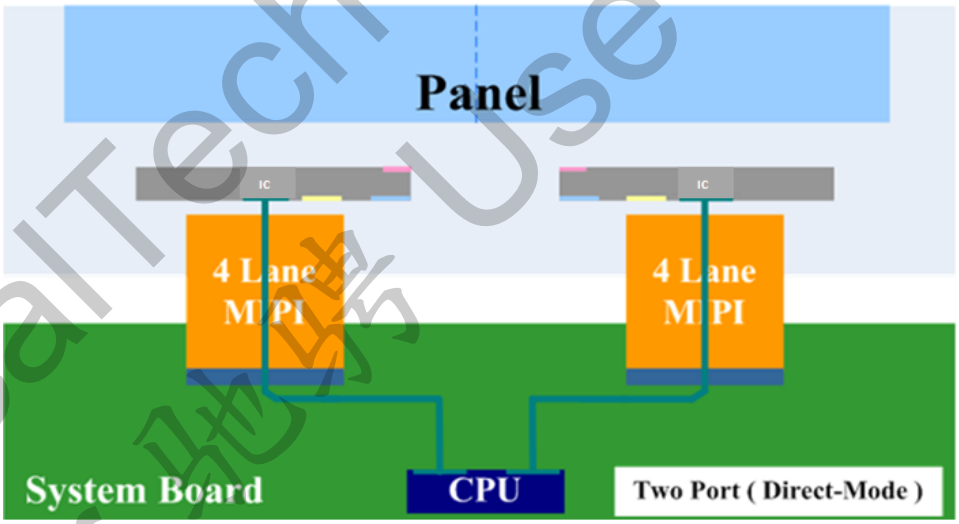
_PROG_BANK[31:0]：OTP Programming Bank Set
- This command is used to set OTP programming bank from Register/SRAM into OTP.

6. FUNCTIONS

6.1. Interface Architecture

FT7150 can support both multi-drop and direct mode architecture for MIPI interface for 2-chip configuration.





6.2. Interface Type Selection

FT7150 support D-PHY MIPI 2/3/4-Lane and lvds interface, depend on IM pad setting.

IM	Interface Selection
0	DPHY MIPI-4Lane
1	LVDS 4 lane

LANSEL[1:0]	Interface Selection
00	Reserved
01	MIPI-2Lane
10	MIPI-3Lane
11	MIPI-4Lane

	PNSWAP	DSWAP[1:0]	DSI-D2+	DSI-D2-	DSI-D1+	DSI-D1-	DSI-CLK+	DSI-CLK-	DSI-D0+	DSI-D0-	DSI-D3+	DSI-D3-
DPHY	0	00	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+
		01	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+
		10	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+
		11	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-	D0+	D3-	D3+
	1	00	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-
		01	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-
		10	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-
		11	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-

LVDS swap table:

LVDS Lanes SWAP table												
SOFT controller	IIW controller		PAD Name									
register setting (reg_lvds_dswap_M/S[2])	PSWAP	DSWAP[1:0]	DATA2P	DATA2N	DATA1P	DATA1N	CLKP	CLKN	DATA0P	DATA0N	DATA3P	DATA3N
0	0	00	D3N	D3P	D2N	D2P	CLKN	CLKP	D1N	D1P	D0N	D0P
		01	D3N	D3P	D0N	D0P	CLKN	CLKP	D1N	D1P	D2N	D2P
		10	D0N	D0P	D1N	D1P	CLKN	CLKP	D2N	D2P	D3N	D3P
		11	D2N	D2P	D1N	D1P	CLKN	CLKP	D0N	D0P	D3N	D3P
	1	00	D3P	D3N	D2P	D2N	CLKP	CLKN	D1P	D1N	D0P	D0N
		01	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
		10	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
		11	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
1	0	00	D0N	D0P	D2N	D2P	D1N	D1P	D3N	D3P	CLKN	CLKP
		01	D2N	D2P	D0N	D0P	D1N	D1P	CLKN	CLKP	D3N	D3P
		10	D1N	D1P	D2N	D2P	CLKN	CLKP	D3N	D3P	D0N	D0P
		11	D2N	D2P	D1N	D1P	CLKN	CLKP	D0N	D0P	D3N	D3P
	1	00	D0P	D0N	D2P	D2N	D1P	D1N	D3P	D3N	CLKP	CLKN
		01	D2P	D2N	D0P	D0N	D1P	D1N	CLKP	CLKN	D3P	D3N
		10	D1P	D1N	D2P	D2N	CLKP	CLKN	D3P	D3N	D0P	D0N
		11	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N

6.3. MIPI-DSI Interface (D-option)

6.3.1. General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication
- Packet level : High level communication

6.3.2. Interface level communication

6.3.2.1 General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode. Data lane1 can be driven High Speed mode only.

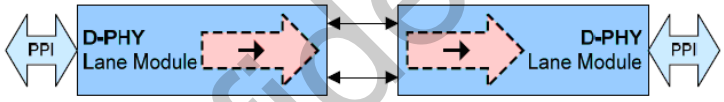
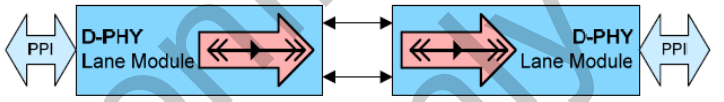
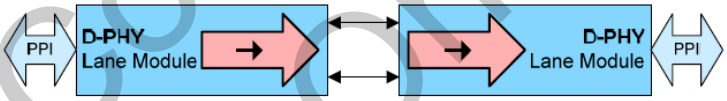
-	Lane support mode	MPU(Host) FT7150(Slave)
Clock Lane	Unidirectional lane • High-Speed Clock only • Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane • Forward high-speed only • Bi-directional Escape Mode • Bi-direction LPDT	
Data Lane1	Unidirectional lane • Forward high-speed only • Simplified Escape Mode (ULPS Only)	

Table: Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

6.3.2.2 DSI-CLK lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

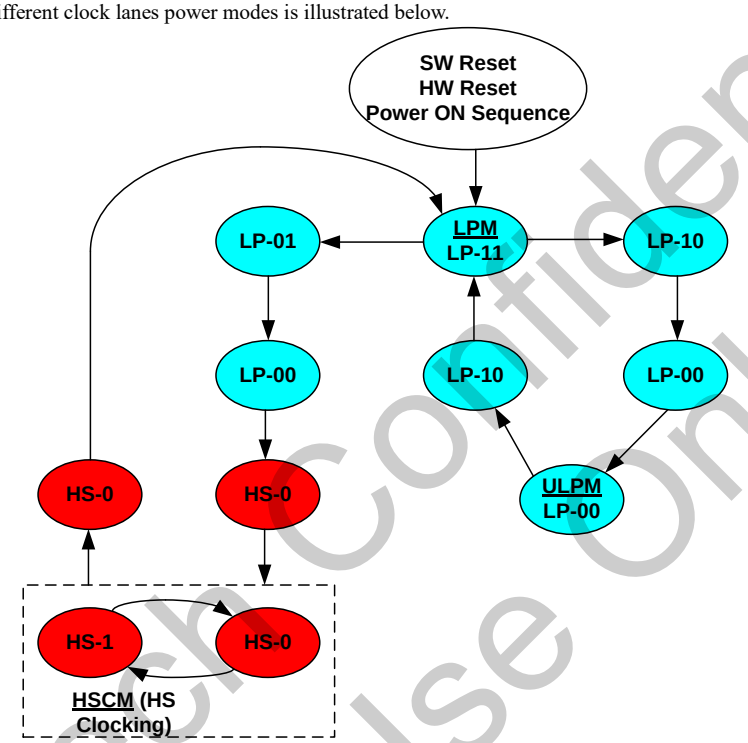


Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

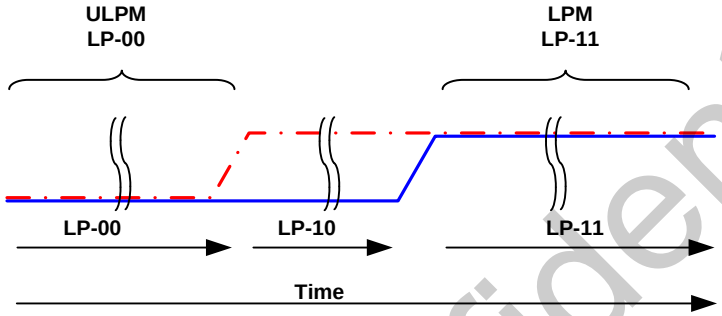


Figure: From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

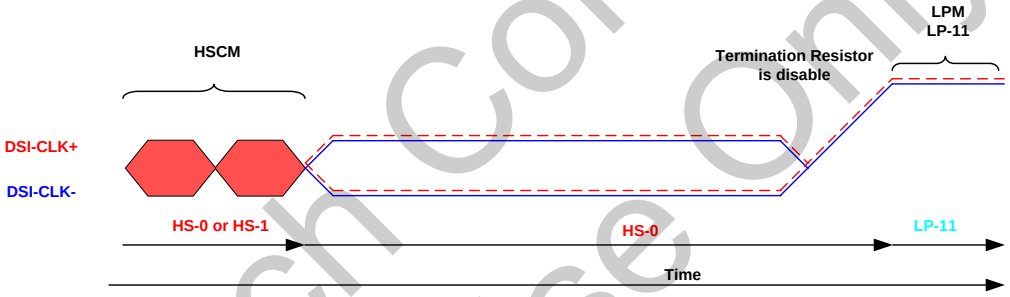


Figure: From HSCM to LPM

All three mode changes are illustrated a flow chart below.

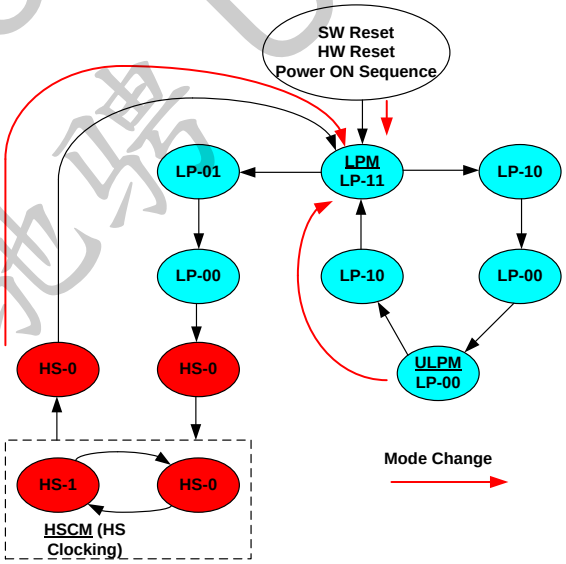


Figure: All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

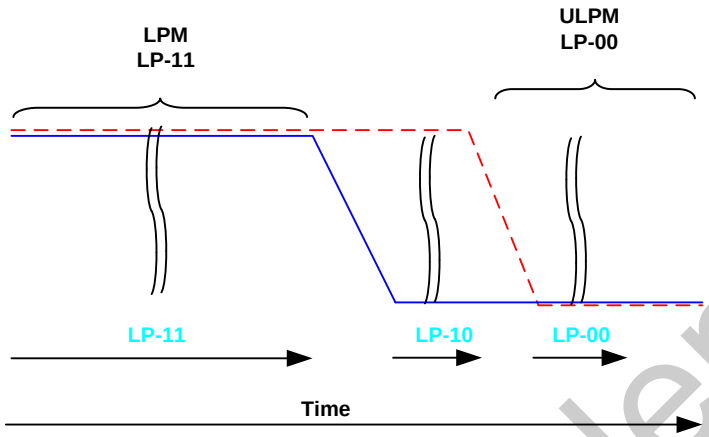


Figure: From LPM to UPLM

The mode change is also illustrated below:

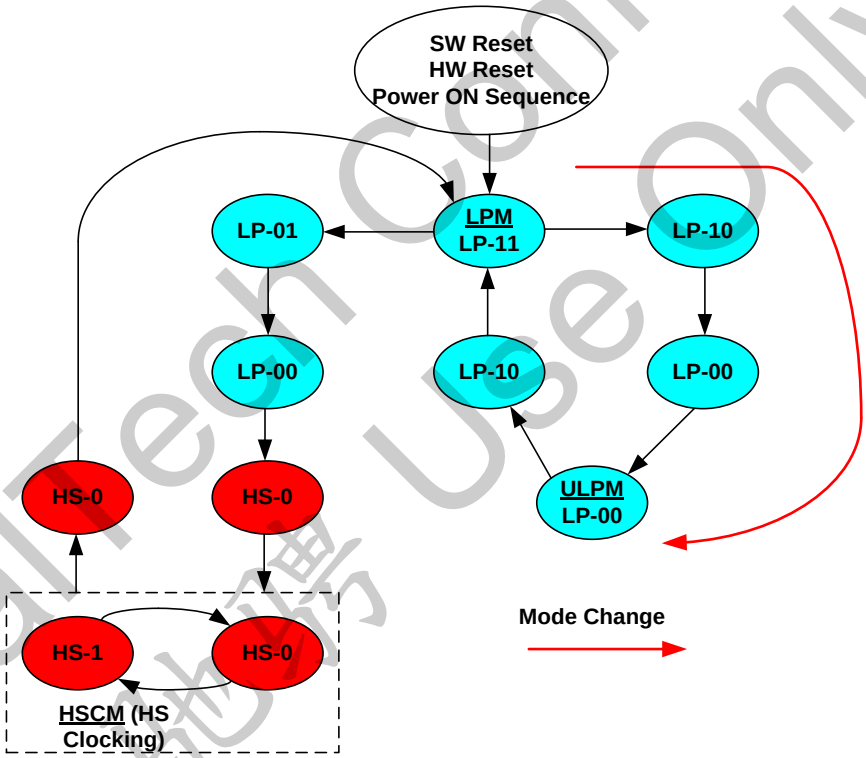


Figure: The mode change from LPM to UPLM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

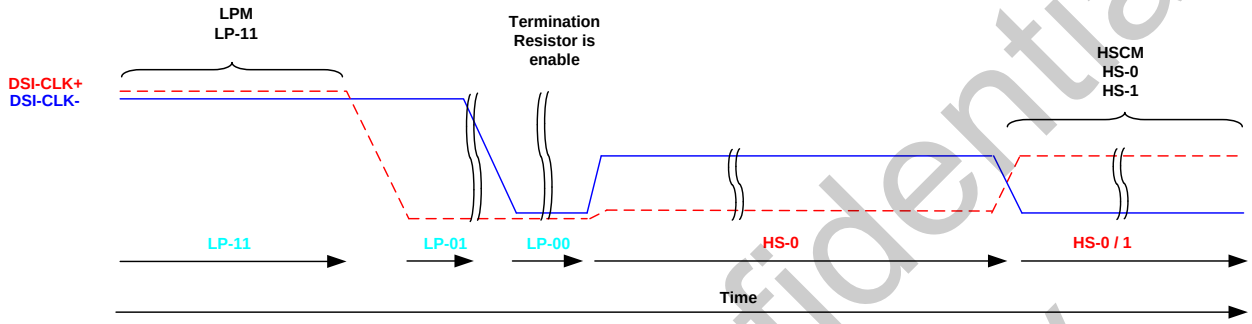


Figure: From LPM to HSCM

The mode change is also illustrated below:

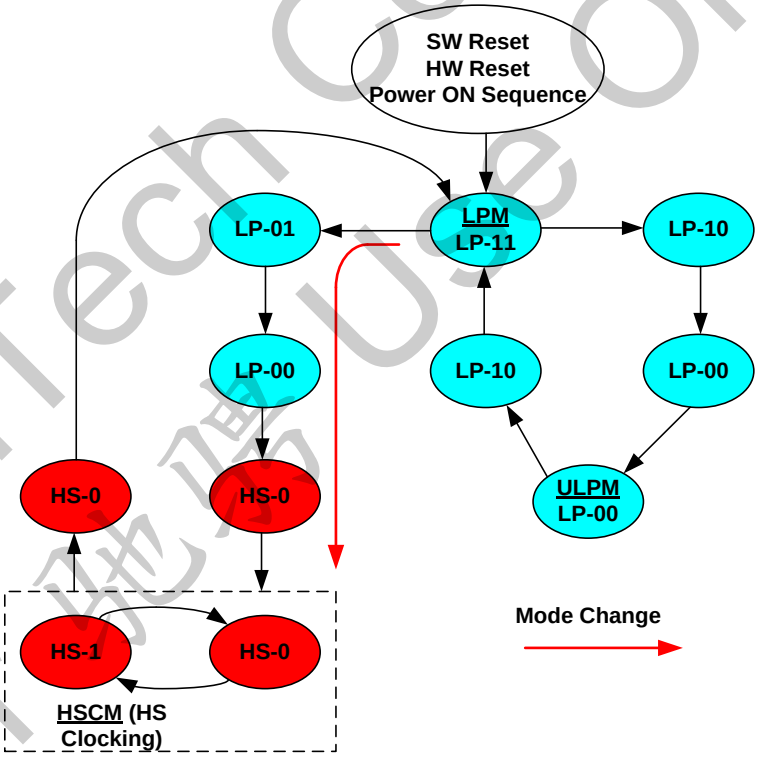


Figure: Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

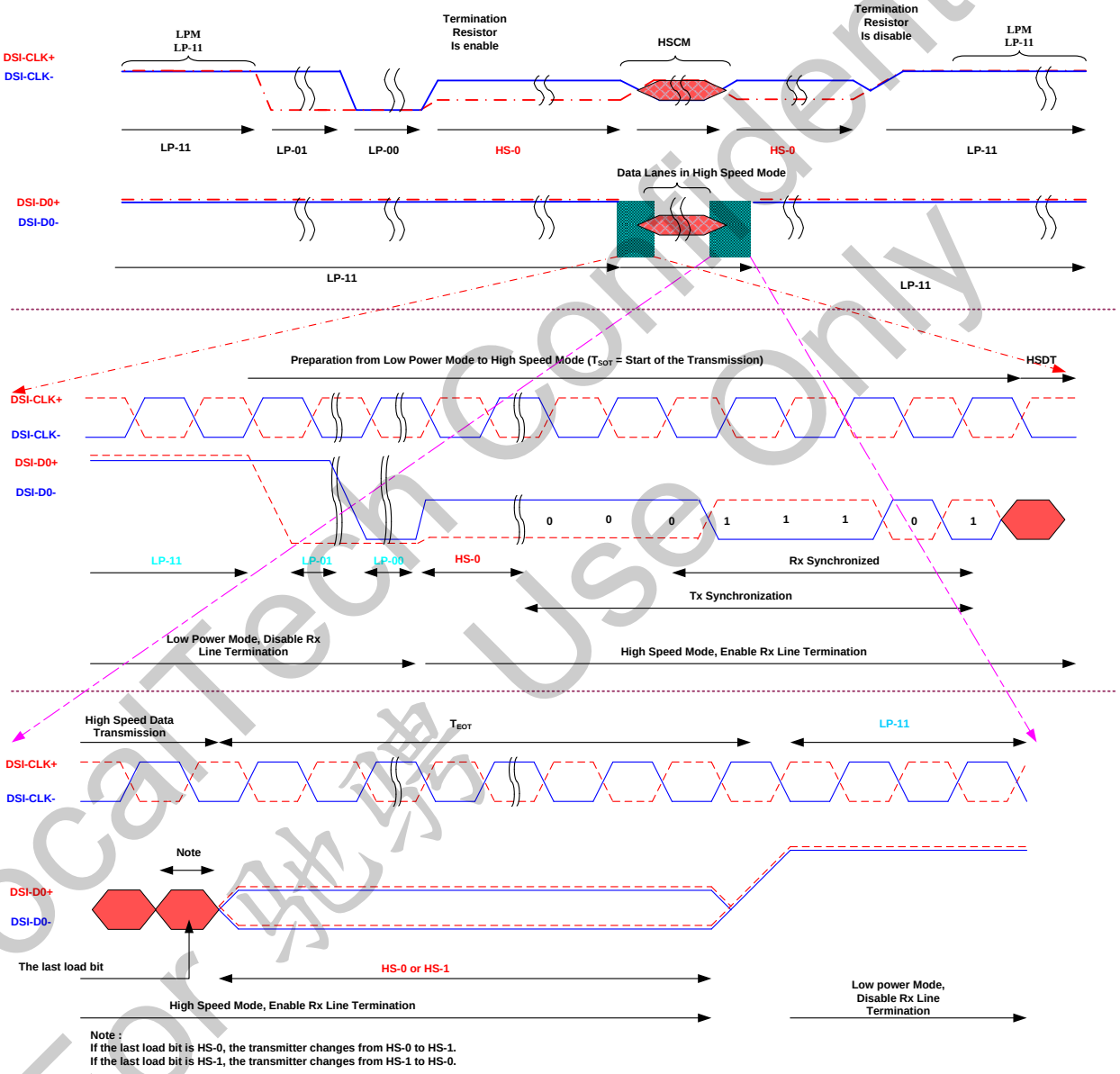


Figure: High speed clock burst

6.3.3. DSI data lanes

6.3.3.1. General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI_D0 data lane pair)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

6.3.3.2. Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command, which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.
- A payload stream if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action.

All currently available Escape mode commands and actions are list below.

- Send or receive “Low-Power Data Transmission” (LPDT)
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function)
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

For Data Lane1 and 2, only support ULPS Escape mode commands.

- Drive data lanes to "Ultra-Low Power State" (ULPS)

The basic construction is illustrated below:

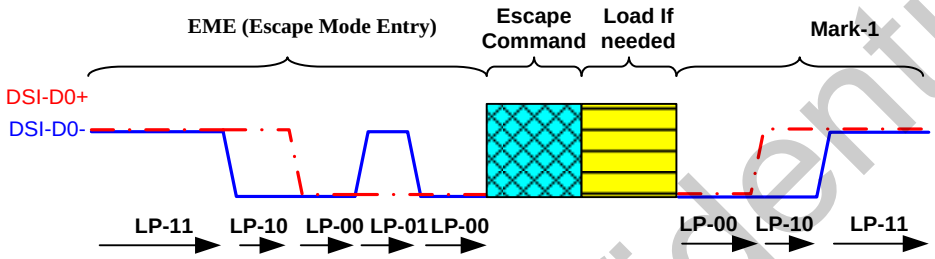


Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided 2 different groups: Mode or Trigger. Escape command groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode.

The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

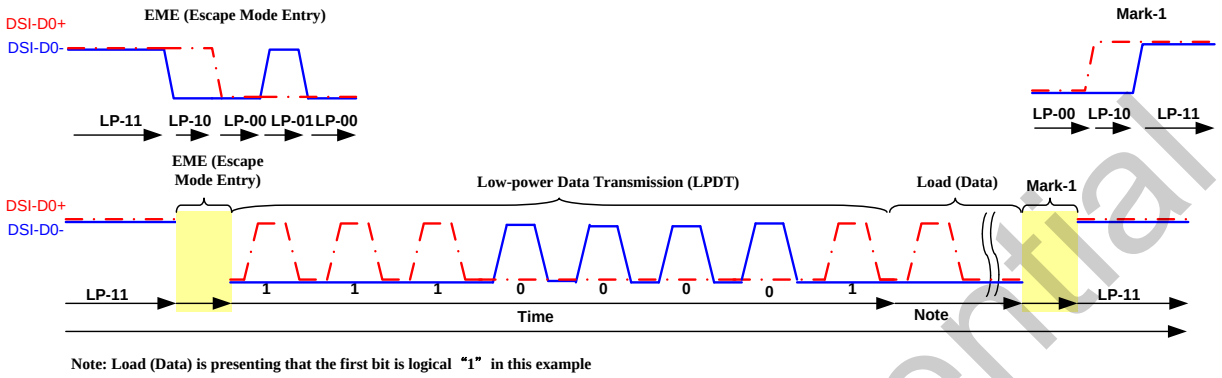
Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Payload (Data):
  - One or more bytes
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load (Data) is presenting that the first bit is logical "1" in this example

Figure: Low-power data transmission

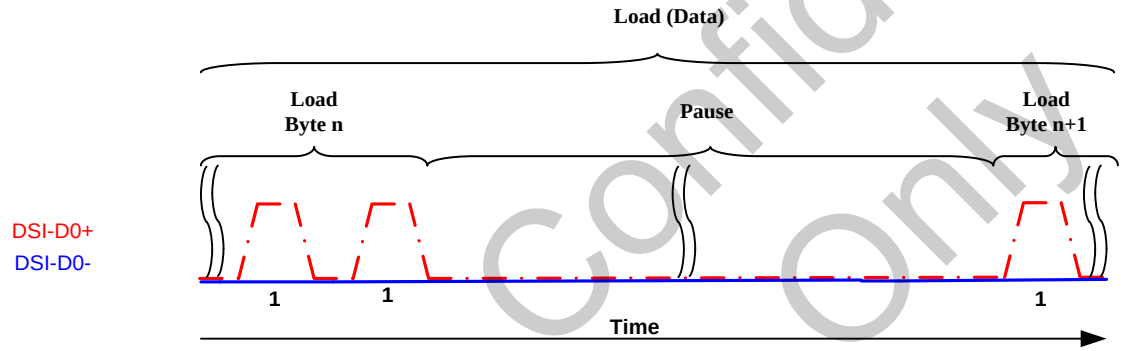


Figure: Pause (example)

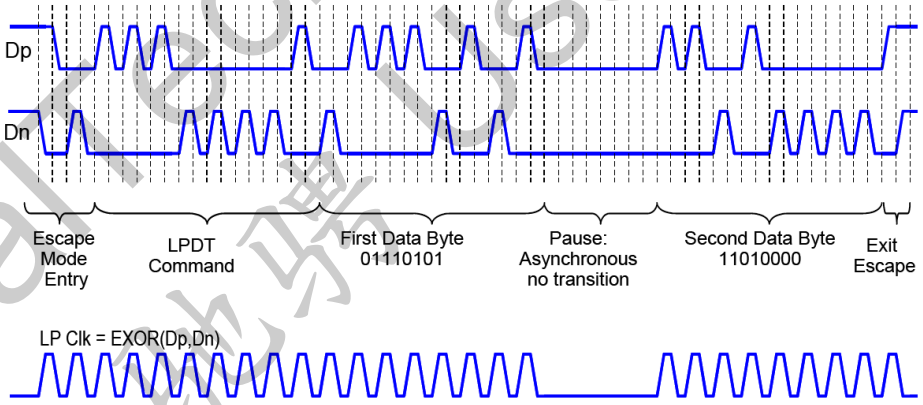


Figure: Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

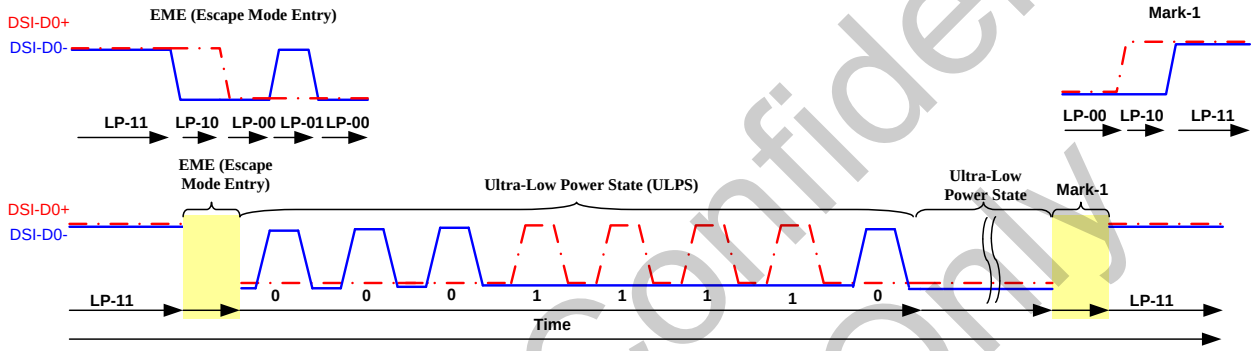


Figure: Ultra-low power state (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

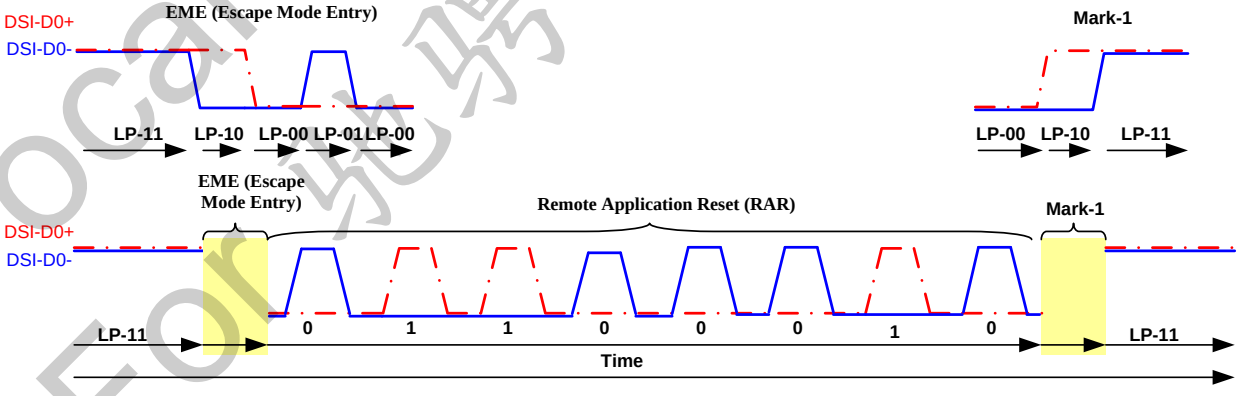


Figure: Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

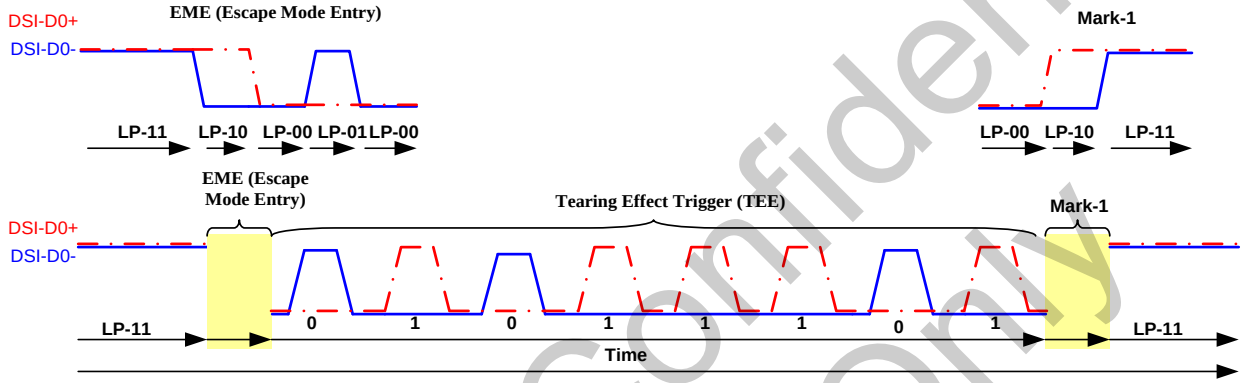


Figure: Tearing effect (TEE)

Acknowledgement (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

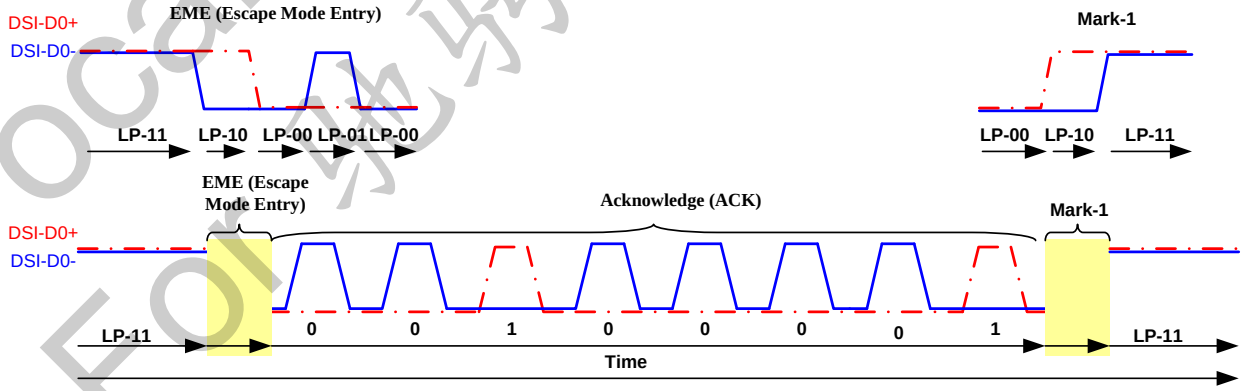


Figure: Acknowledgement (ACK)

6.3.3.3. High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T_{sot} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission(HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

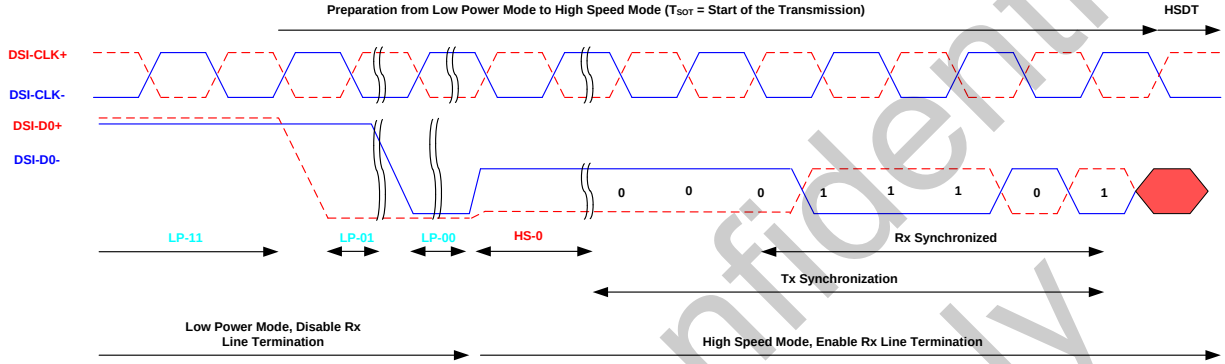


Figure: Tsot of HSDT

Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI- CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes

DSI-D0+/- are in LP-11 mode. See more information on chapter "7.2.2 High-Speed Clock Mode (HSCM)".

Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

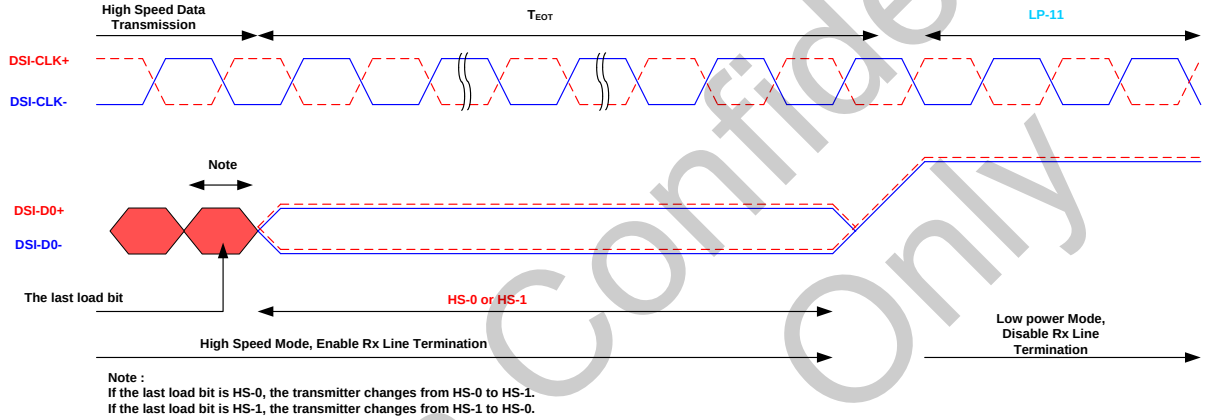


Figure: TEOT of HSDT

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (Lpa) or Short (Spa) packets. These packets are defined on chapter "Short Packet (Spa) and Long Packet (Lpa) Structures".

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

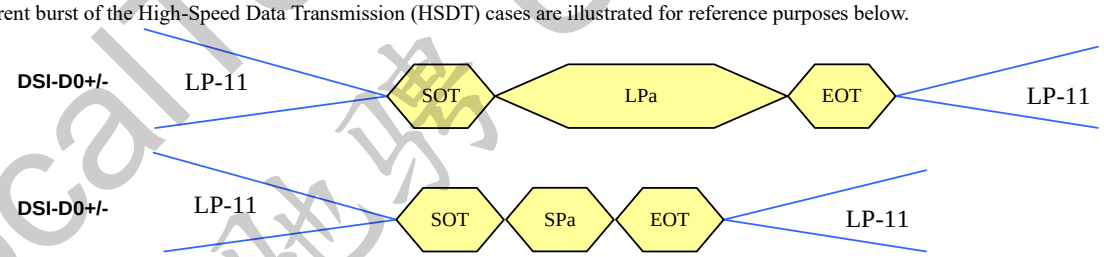


Figure: Single packet in HSDT

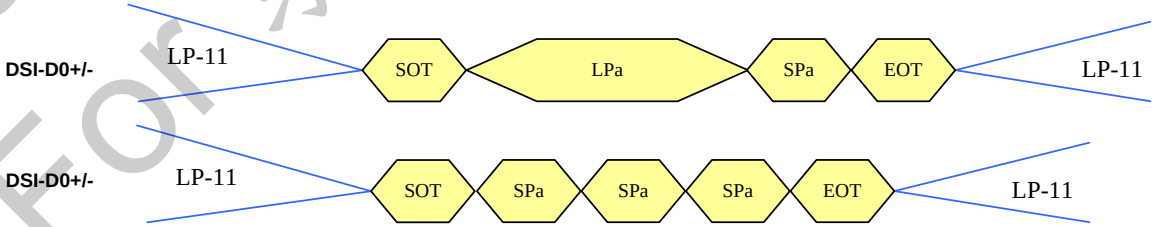


Figure: Multiple packets in HSDT

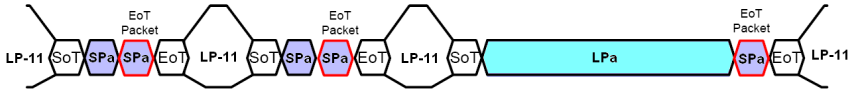


Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are ‘1’s (Stop Mode)
SOT	Start of the Transmission
Lpa	Long Packet
Spa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

6.3.3.4. Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used.

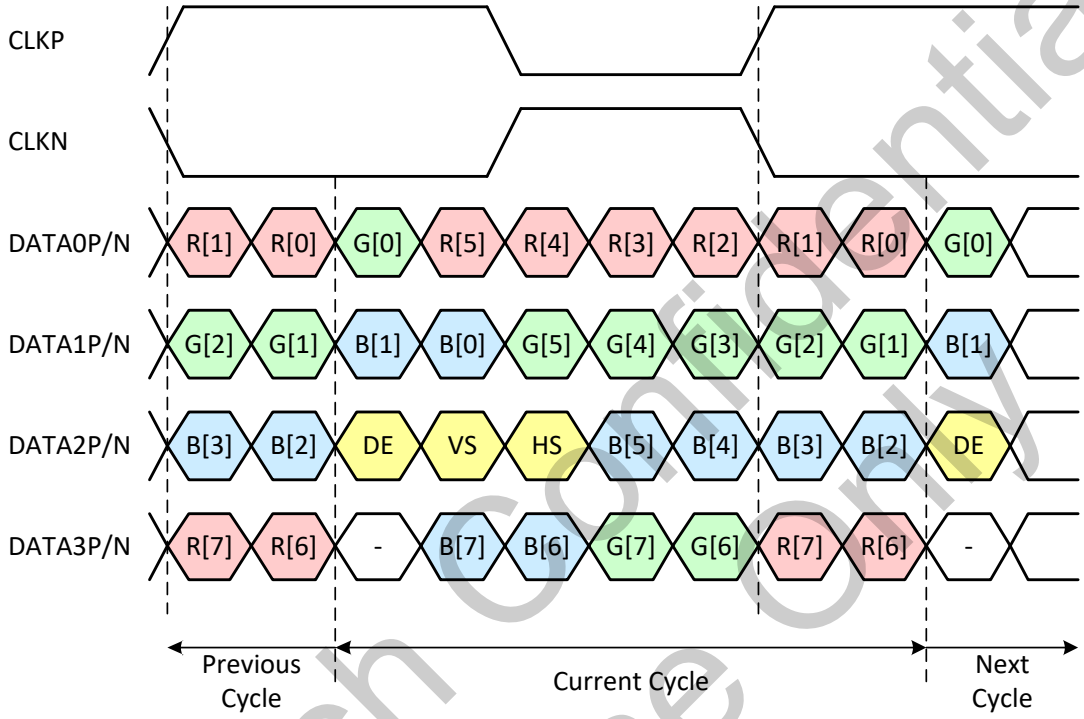
This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00
- The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

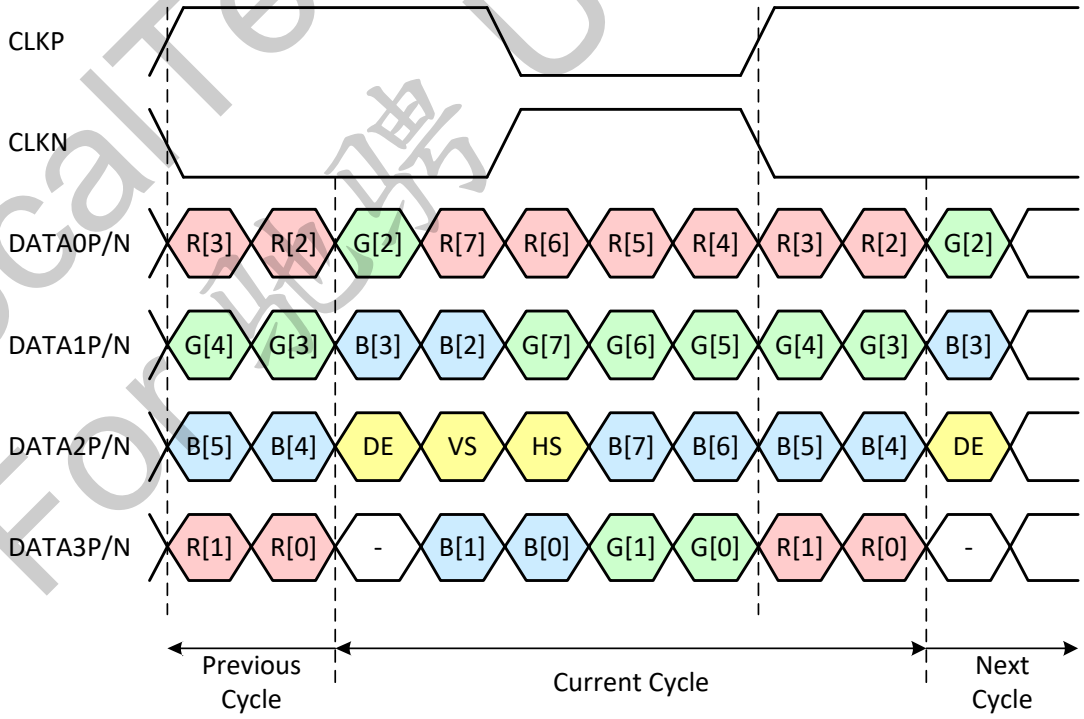
6.4.LVDS Interface

It supports different display resolutions with single port LVDS interface.

6.4.1. 1-port LVDS signals, VESA format (8-bit)

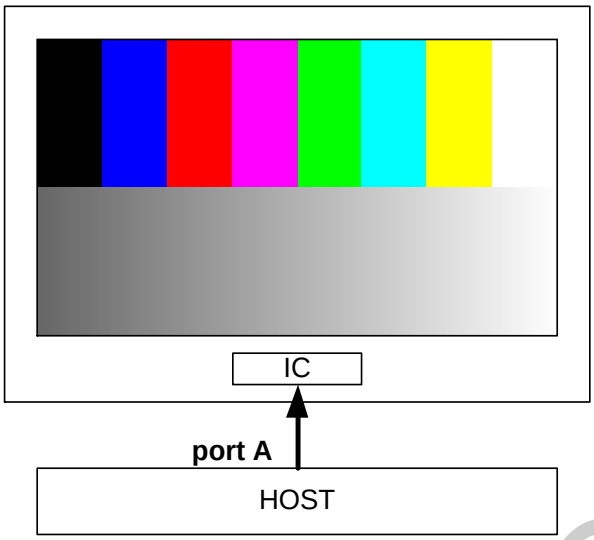


6.4.2. 1-port LVDS signals, JEIDA format (8-bit)



6.4.3. LVDS architecture

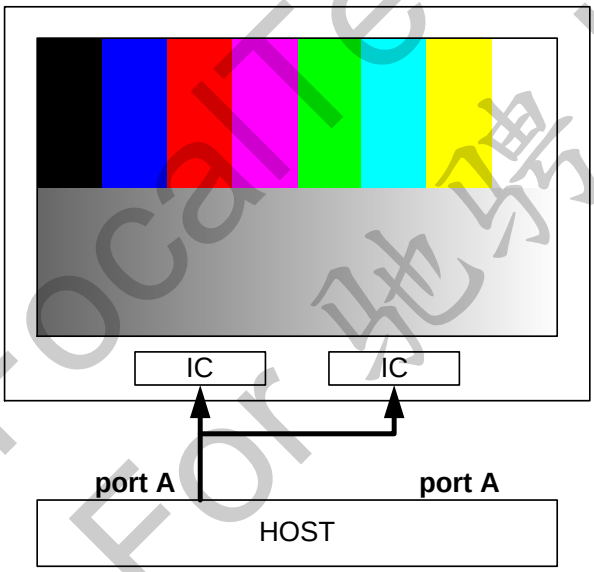
Cascade 1 IC
Single Port LVDS



CLK rate = 110 MHz

Option: Need 5 Resistors (100 ohm/Resistor)

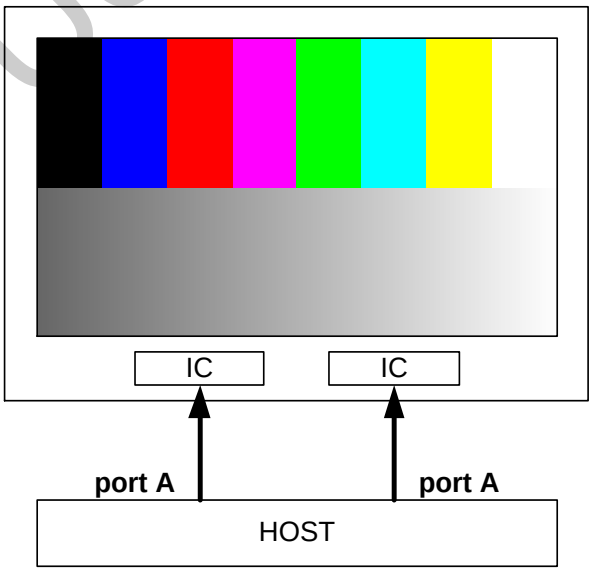
Cascade 2 ICs
Single port LVDS by multi-drop architecture



CLK rate = 110 MHz

Option :Need 5 Resistors (100 ohm/Resistor)

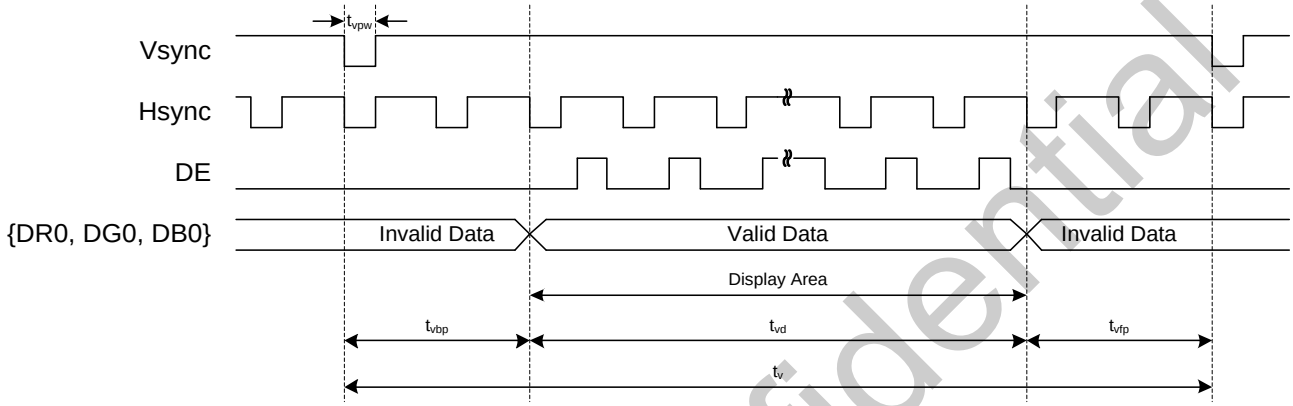
Cascade 2 ICs
Single port LVDS by point to point architecture



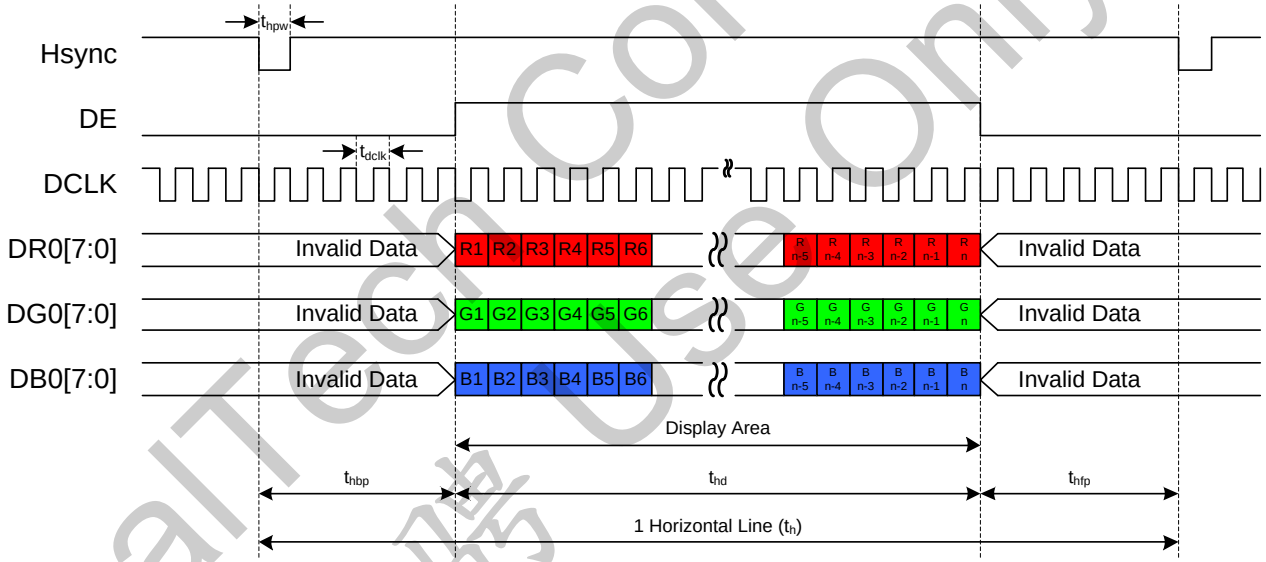
CLK rate = 55 MHz
Host IC need to split the whole image as 2 blocks
Option: Need 10 Resistors (100 ohm/Resistor)

6.4.4. LVDS Video Input Timing

Vertical timing after LVDS 1-port client decode (internal signal) is:



Horizontal timing after LVDS 1-port client decode (internal signal) is:

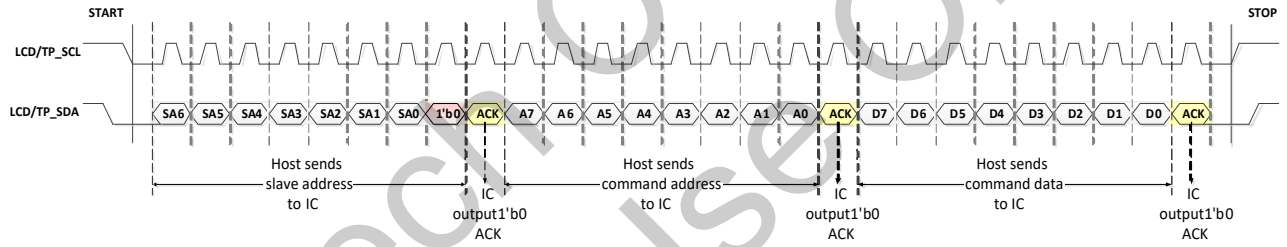


6.5.2-wire Serial Interface (I2C) to set LCD initial code

The I2C interface is used to communication between the micro controller and the LCD driver chip. To use I2C interface to write/read register to/from FT7150, when using LCD I2C to set LCD initial code please set LCD_GPIO[2] pin to 1'b1, else for using TP I2C please set LCD_GPIO[2] pin to 1'b0. The I2C interface contains LCD/TP_SCL (serial clock), LCD/TP_SDA (serial data input/output). Serial clock (LCD/TP_SCL) is used for interface with host only, so it can be stopped when no communication is necessary. The host is required to keep LCD/TP_SDA high-impedance when FT7150 output ACK=0 or the time read data is output from FT7150.

6.5.1. I2C Write Sequence

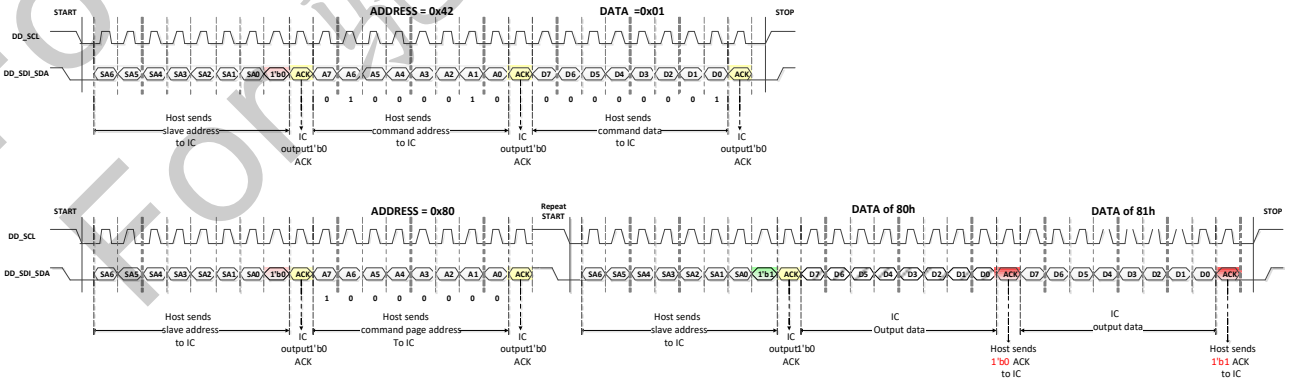
A simple I2C write sequence is shown as below. The valid sequence is start by a START condition waveform and end by a STOP condition waveform. The first 7-bit is I2C SLAVE address, FT7150 I2C SLAVE address is defined to 7'h52 when one chip is used. The 8th input bit is WRITE(1'b0)/READ(1'b1) bit. At the 9th LCD/TP_SCL cycle, FT7150 will output 1'b0 as ACK. The continuous 8-bit is defined as command (or page). The 18th LCD/TP_SCL cycle, FT7150 will output 1'b0 as ACK. The continuous 8-bit is defined as data. At the last LCD/TP_SCL cycle, FT7150 will output 1'b0 as ACK.



6.5.2. I2C read CMD

The read sequence is shown as below. When read sequence is finished, please send the last ACK=1'b1 and then send a STOP condition waveform.

Example: Read bank 01h, 80~81h data



6.5.3. I2C Write/Read Specific Chip

When cascaded more than one chip, host can write/read specific chip register value. I2C write/read specific chip function is controlled

by I2C_SLAVE address, please refer to the following truth table for write case and read case.

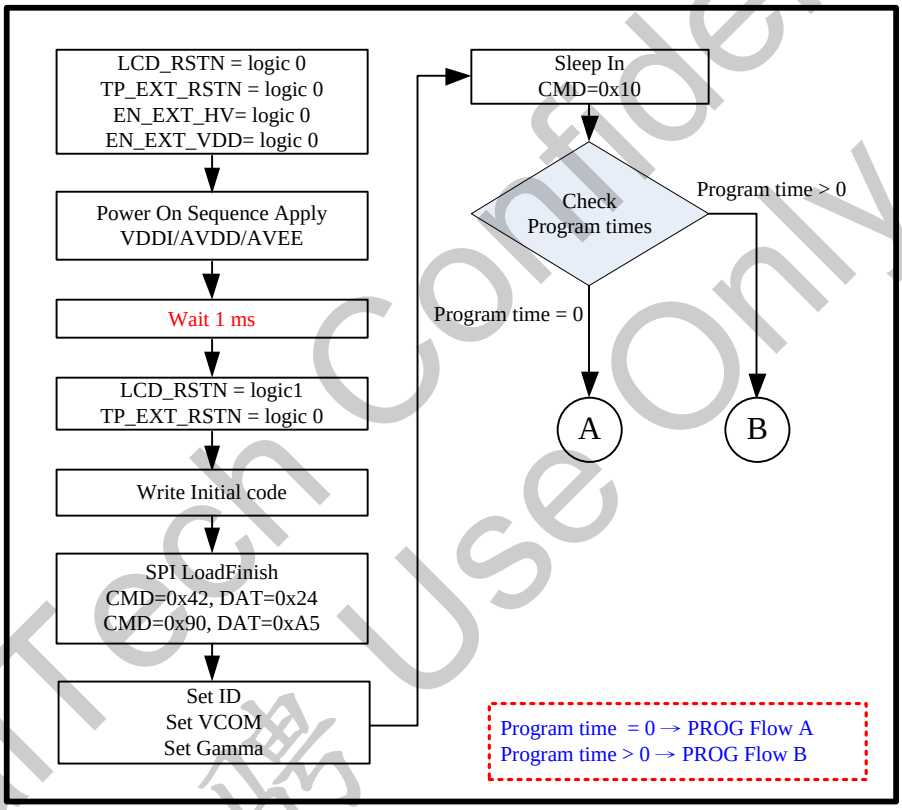
I2C_SLAVE address	Description
7'h50	Read/Write master (TP_MS = 1'b1) enable Read/Write slave (TP_MS = 1'b0) enable
7'h52	Read/Write master (TP_MS = 1'b1) enable
7'h54	Read/Write slave (TP_MS = 1'b0) enable

6.6.NVM Programming Procedure

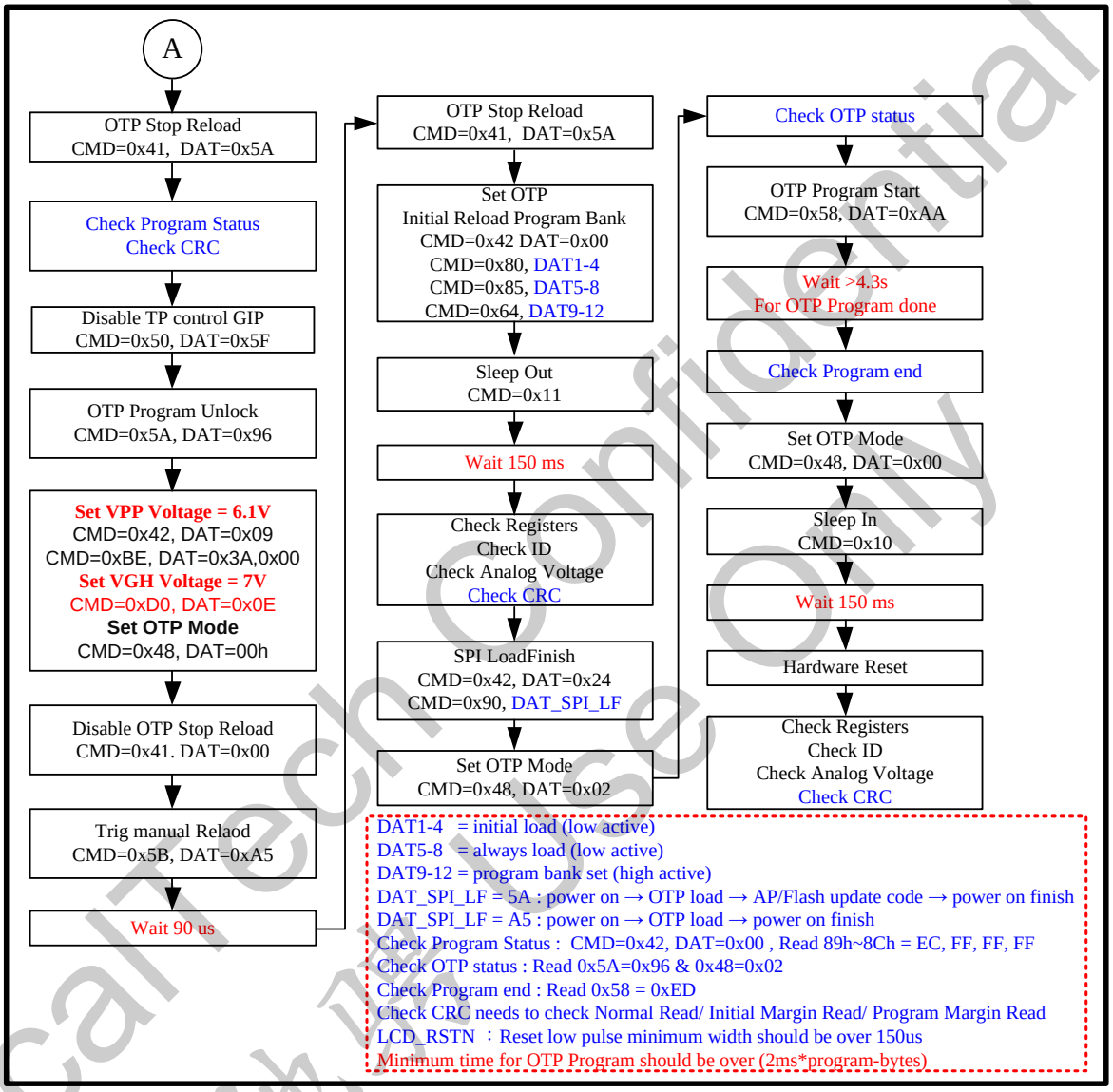
6.6.1. NVM program flow chart with internal power

1. TCON registers must include correct panel timing configurations to program NVM on panel.
2. TP_EXT_RSTN has to keep low during NVM program flow.
3. Bank8 ~ Bank31 are suggested to set "**Initial load**" for the 1st time OTP download at power on, but not to set "**always load**" for OTP-auto-reload periodically. It allows HOST/FW to update settings within Bank8 ~ Bank31 and would not be overwritten by OTP-auto-reload.

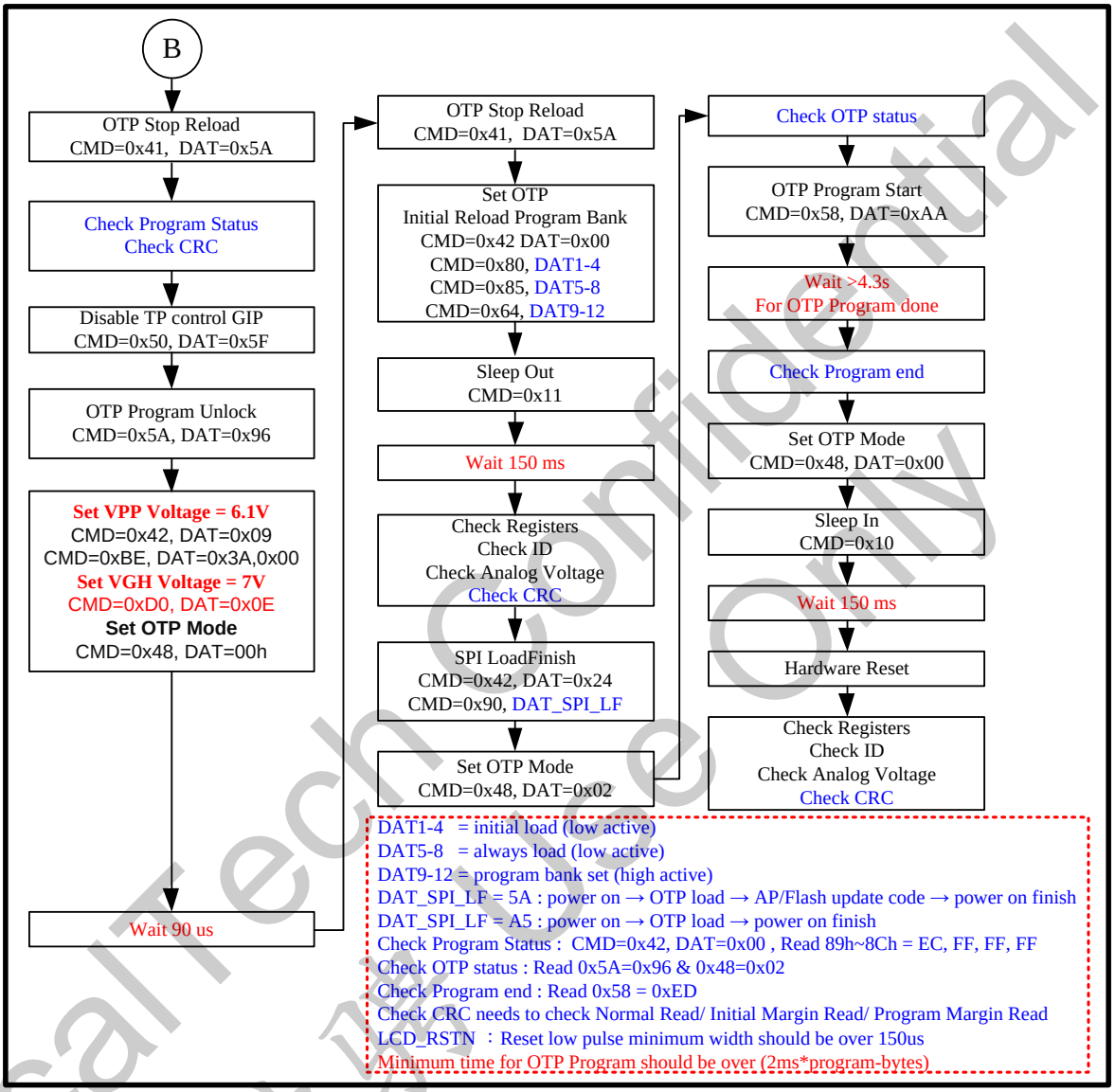
OTP program flow with internal power (part1)



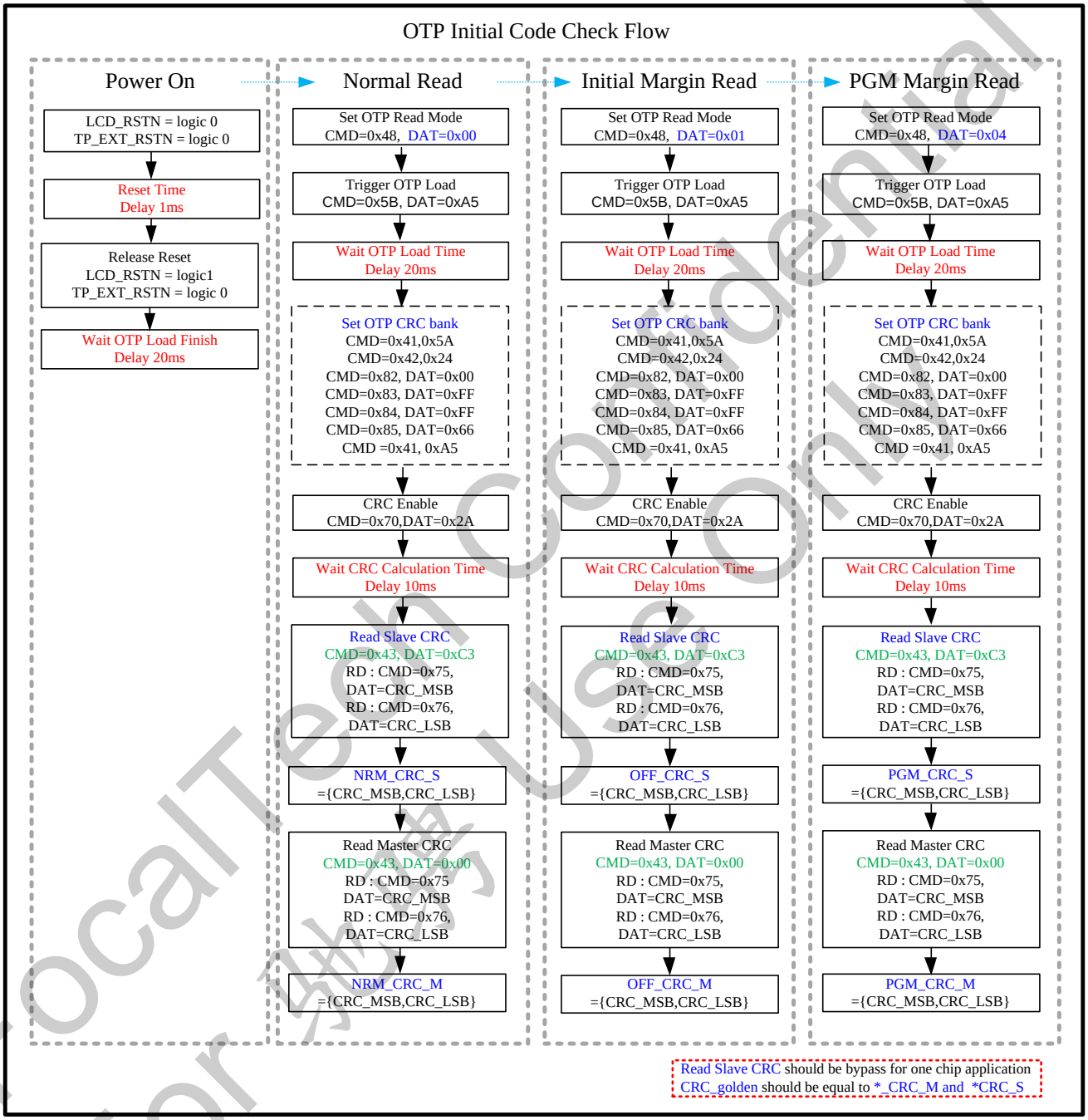
OTP program flow with internal power (part2)



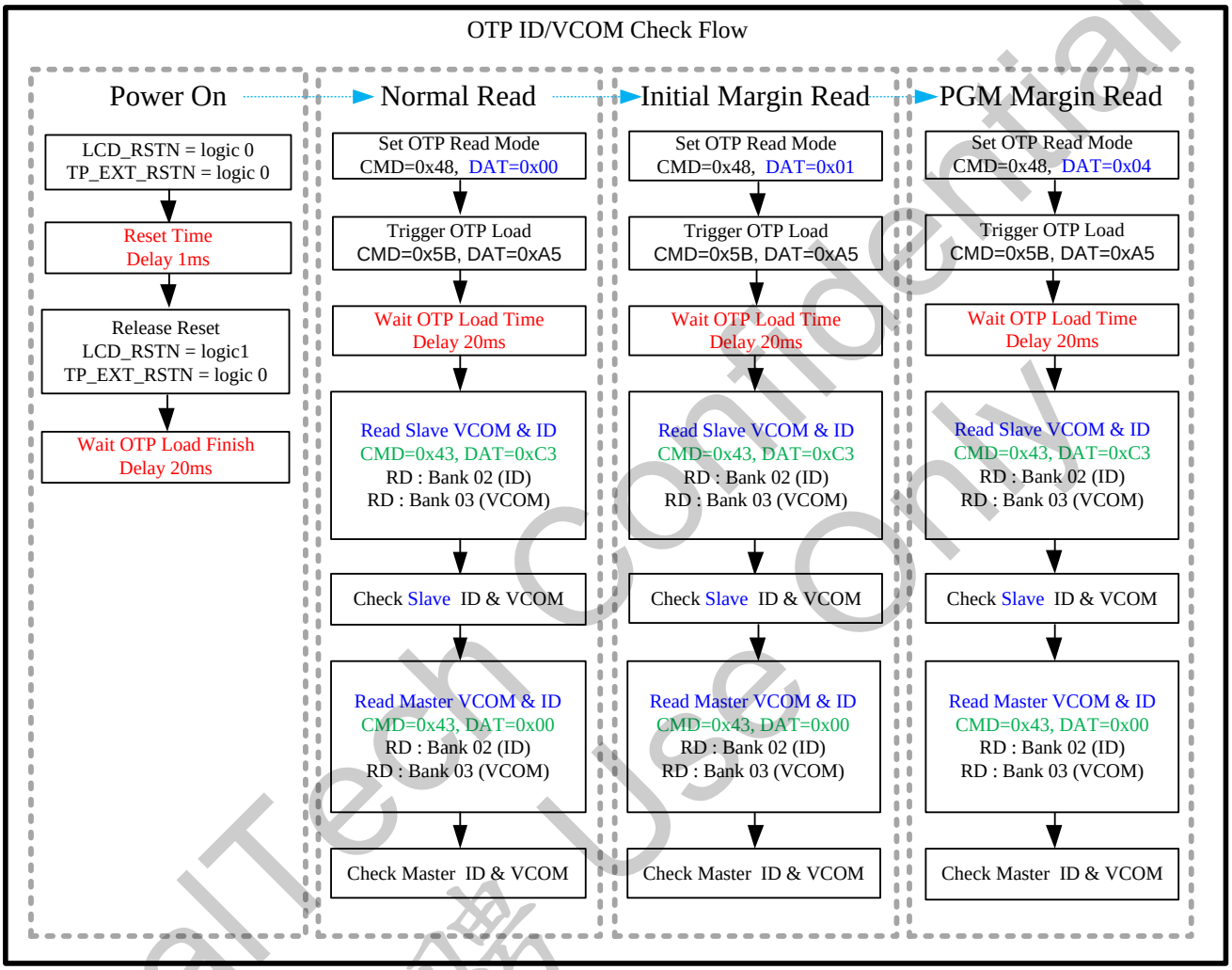
OTP program flow with internal power (part3)



OTP CRC Flow (all bank)



OTP ID and VCOM Check Flow



7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

(AVDD = 4.5V ~ 6.5V, AVEE = -4.5V ~ -6.5V, VDDI = 1.65V ~ 1.95V(MIPI) or 2.7V~3.6V(LVDS), Ta = -30^{O}C ~ 85^{O}C)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	VDDI-VSS	-0.3 ~ +1.95	V	MIPI application
Power Supply Voltage 1	VDDI-VSS	-0.3 ~ +3.6	V	LVDS application
Power Supply Voltage 2	VDD-VSS	-0.3 ~ +1.35	V	
Power Supply Voltage 3	AVDD-VSS	-0.3 ~ +6.5	V	
Power Supply Voltage 4	VSS-AVEE	-0.3 ~ +6.5	V	
Power Supply Voltage 5	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ VDDI+0.3	V	
Operating Temperature	Topr	-30 ~ +85	^{O}C	
Storage Temperature	Tstg	-55 ~ +110	^{O}C	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

7.2 DC Characteristics

7.2.1 Basic DC characteristic

(AVDD = 4.5V~6.5V,AVEE = -4.5V~-6.5V,VDDI = 1.65V~1.95V(MIPI) or 2.7V~3.6V(LVDS),VDD_EXT=1.2V~1.35V, Ta = -30ºC ~ 85º C)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	AVDD	Operating Voltage	4.5	5.5	6.5	V	
Analog Operating voltage	AVEE	Operating Voltage	-6.5	-5.5	-4.5	V	
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	1.95	V	MIPI
Logic Operating voltage	VDDI	I/O supply voltage	2.7	3.3	3.6	V	LVDSRX
Digital Operating voltage (4 power mode)	VDD_EXT	External Digital voltage	-	1.3	1.35	V	
Input / Output							
Logic High level input voltage	VIH	-	0.7VDDI	-	VDDI	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDI	V	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2VDDI	V	
Logic High level input current	IIH	Vin = VDDI	-	-	1	uA	
Logic Low level input current	IIL	Vin = VDDI	-1	-	-	uA	
VCOM Operation							
VCOMDC output voltage	VCOM	AVDD=AVEE=+/-5V	-3.85	-	0.3	V	
Source Driver							
Gamma positive reference voltage	VGMP	VGMP<AVDD-0.2V	3.75	-	6.3	V	
Gamma negative reference voltage	VGMN	VGMN>AVEE-0.2V	-6.3	-	-3.75	V	
Source output voltage	VSD	-	VGMN	-	VGMP	-	
Output deviation voltage (Source positive output channel)	V,dev	Sout >=+4.2V, Sout<=+0.8V	-	-	20	mV	
		+4.2V>Sout>+0.8V	-	-	10	mV	
Output deviation voltage (Source negative output channel)	V,dev	Sout <=-4.2V, Sout>=-0.8V	-	-	20	mV	
		-4.2V<Sout<-0.8V	-	-	10	mV	
Output offset voltage	V_{OFSET}	-	-	-	100	mv	
Reference Voltage							
Internal reference voltage	VREF_TP	-	3	3.5	4.4	V	
Booster operation							
Pump output voltage	VGH	Range=(AVDD-AVEE) ~(2AVDD-2AVEE)	6.0	-	22.2	V	
Pump output voltage	VGL	Range=(AVEE-AVDD) ~(2AVEE-AVDD)	-18.0	-	-5.3	V	
Regulator output voltage	VCL	-	-5	-4.5	-3.5	V	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

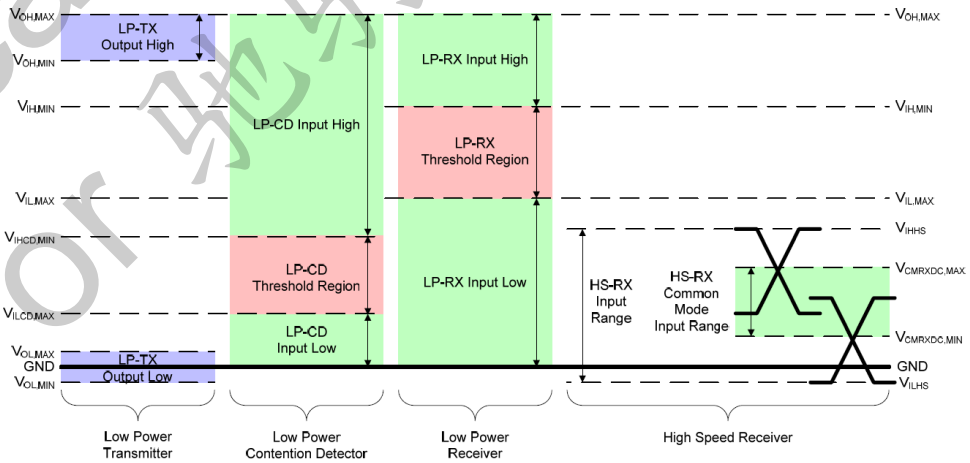
7.2.2 MIPI D-PHY DC character

D-PHY DC characteristics for MIPI-DSI

(Ta = -30ºC ~ 85ºC)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	LVDSVDD	-	1.15	1.2	1.25	V
LPDT Input Characteristics						
Pad signal voltage range	V_I	-	-50	-	1350	mV
Ground Shift	V_{GNDSH}	-	-50	-	50	mV
Logic 0 input threshold	V_{IL}	-	-	-	550	mV
Logic 1 input threshold	V_{IH}	-	880	-		mV
Input hysteresis	V_{HYST}	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	V_{OL}	-	-50	-	50	mV
Output high level	V_{OH}	Note 1	1.15	1.2	1.25	V
Logic 0 contention threshold	V_{ILCD}	-	-	-	200	mV
Logic 1 contention threshold	V_{IHCD}	-	450	-	-	mV
Output impedance of LPDT	Z_{OLP}	-	110	-	-	Ω
Hi-speed Input Characteristics						
Single-end input low voltage	V_{ILHS}	-	-40	-	-	mV
Single-end input high voltage	V_{IHHS}	-	-	-	460	mV
Single-end threshold for HS termination enable	$V_{TERM-EN}$	-	-	-	450	mV
Differential input low threshold	V_{IDTL}	-	-70	-	-	mV
Differential input high threshold	V_{IDTH}	-	-	-	70	mV
Common mode voltage	V_{CMRXDC}	-	70	-	330	mV
Differential input impedance	Z_{ID}	-	80	100	125	Ω

Note1: Output high level follow Power supply voltage for MIPI



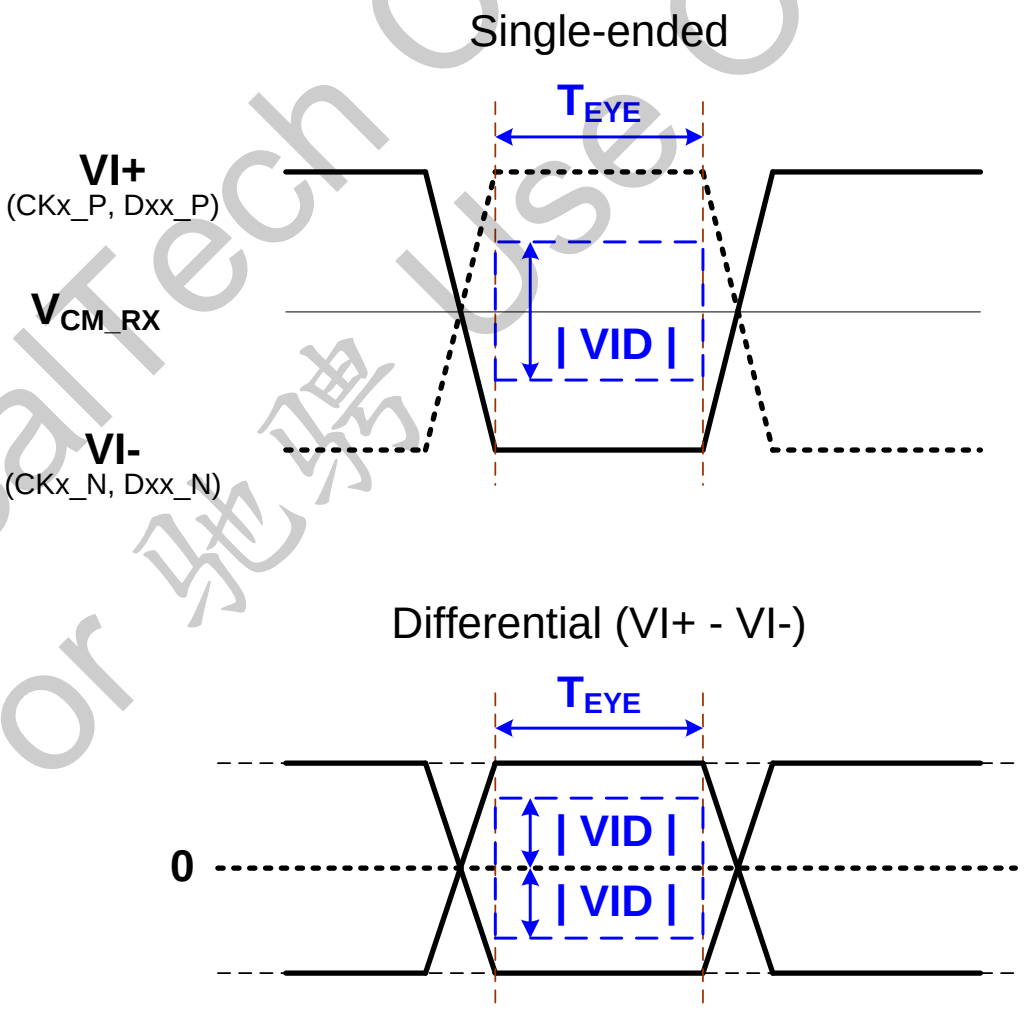
7.2.3 LVDS DC characteristic

Table: DC characteristics for LVDS

(VDDI = 2.7~3.6V, AVDD=4.5~6.5V, AVEE=-4.5~-6.5V, VSS = AVSS = 0V, T_{OP} = 25℃)

Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
For The Digital Circuit: LVDS Mode						
Operating frequency LVDS mode (including SSC operation)	FLVDS	By resolution	15		110	MHz
Differential input common mode voltage	VCM_RX		0.6		1.5	V
Differential input voltage (NOTE 1)	|VID|		90	350	600	mV
Differential input data eye width	T_{EYE}		0.6	-	-	UI
Differential input leakage current	RXI_Ikg		-10	-	+10	μA

NOTE1：Input Differential Voltage VID = VI+ - VI-



7.2.4 SPI DC characteristics

DC characteristics for SPI

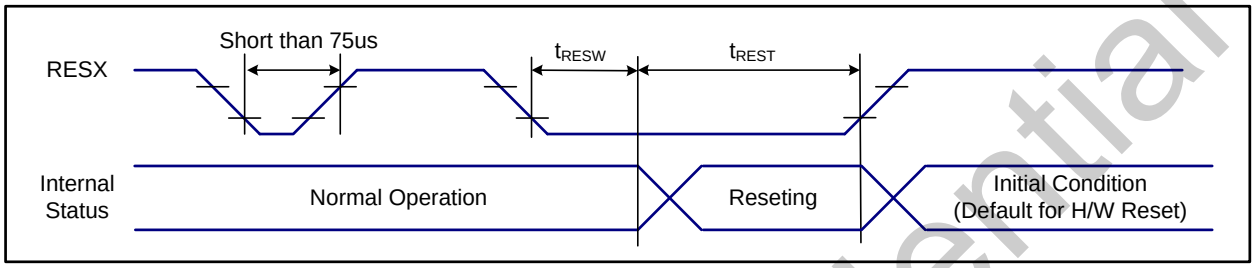
Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Input terminal : CS, SCL, MOSI						
Input High Voltage	VIH	-	0.9*VDDI	-	-	V
Input Low Voltage	VIL	-	-	-	0.1*VDDI	V
Input Capacitance	Cin	-	-	10	-	pF
Output terminal : MISO						
Output High Voltage	VOH		-	0.9*VDDI*	-	V
Output Low Voltage	VOL		-	0.1*VDDI*	-	V

*VDDI=1.8V(MIPI) or 2.7~3.6V(LVDS)

7.3 AC Characteristics

7.3.1 Reset timing characteristics

t_{RESW} shorter than 75us, Reset will be rejected.



VSS=0V, VDDI = 1.65V ~ 1.95V(MIPI) or 2.7~3.6(LVDS), Ta = -30ºC to 85ºC

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse minimum width	150	-	-	Reset signal recognized	us
t_{REST}	*2) Reset complete time	5	-	120	Reset action complete	ms

Table: Reset input timing

Note 1. RESX low pulse that is too short does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 75us	Reset Rejected
Longer than 150us	Reset Recognized
Between 75us and 150us	Reset sequence starts (It depends on voltage and temperature condition.)

Note 2. Once Reset low pulse is recognized, system requires RESX remaining low for another 5ms to complete H/W reset.

Note 3. During H/W Reset flow, ID0 ~ ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when H/W reset is complete ; The H/W reset sequence is complete when RESX is remaining low longer than tRESW + tREST.

Note 4. It is necessary to wait 15msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

7.3.2 I²C interface characteristics

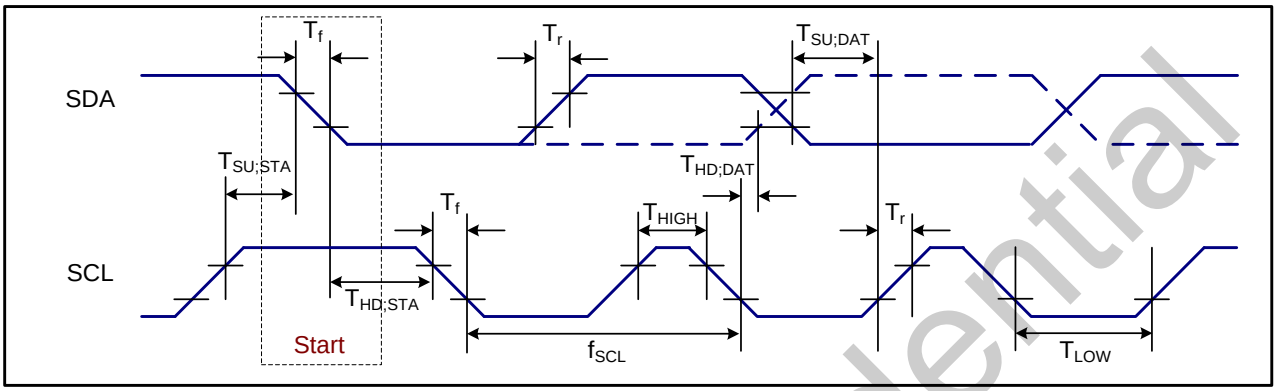


Table: I2C Interface Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCLK}	SCL clock frequency	-	10	-	400	kHz
T_{LOW}	SCL clock LOW period	-	1.2	-	-	us
T_{HIGH}	SCL clock HIGH period	-	0.6	-	-	us
$T_{SU;DATA}$	data set-up time	-	250	-	-	ns
$T_{HD;DATA}$	data hold time	-	0	-	0.9	us
T_r	SCL and SDA rise time	Note 2	$20+0.1C_b$	-	300	ns
T_f	SCL and SDA fall time	Note 2	$20+0.1C_b$	-	300	ns
T_f	SDA fall time for read out	-	$20+0.1C_b$	-	1000	ns
C_b	Capacitive load represented by each bus line	-	-	-	400	pF
$T_{SU;STA}$	Setup time for a repeated START condition	-	0.6	-	-	us
$T_{HD;STA}$	START condition hold time	-	0.6	-	-	us
$T_{SU;STO}$	Setup time for STOP condition	-	0.6	-	-	us
T_{SW}	Tolerable spike width on bus	Note 1	-	-	50	ns
T_{BUF}	BUS free time between a STOP and START condition	-	4.7	-	-	us

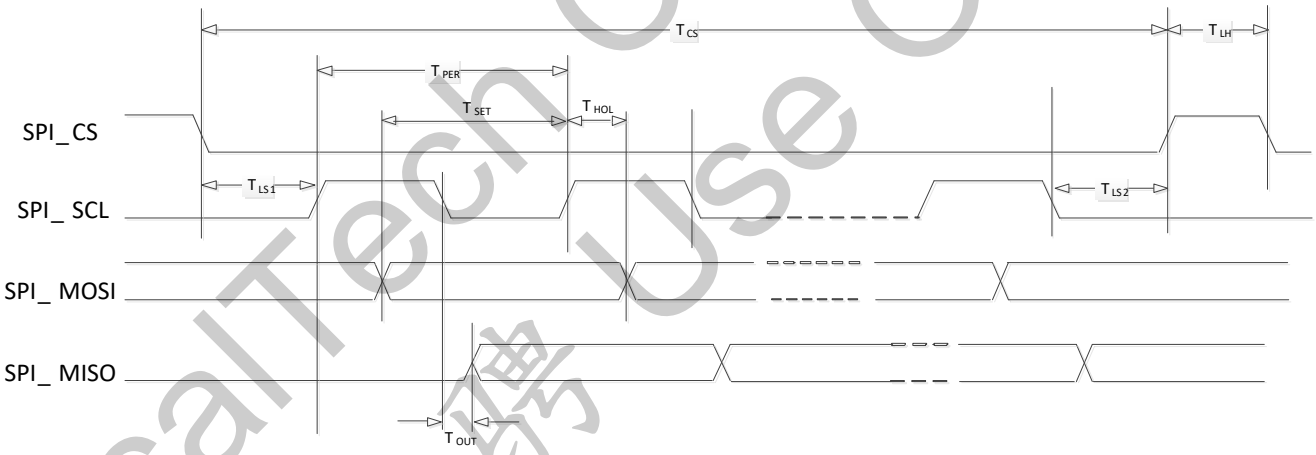
Note1: The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $<t_{SW(max)}$.

Note2: The rise and fall times specified here refer to the driver device and are part of the general fast I²C-bus specification. C_b = capacitive load per bus line.

Note3: All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing of VSS to VDDI

7.3.3 SPI characteristics

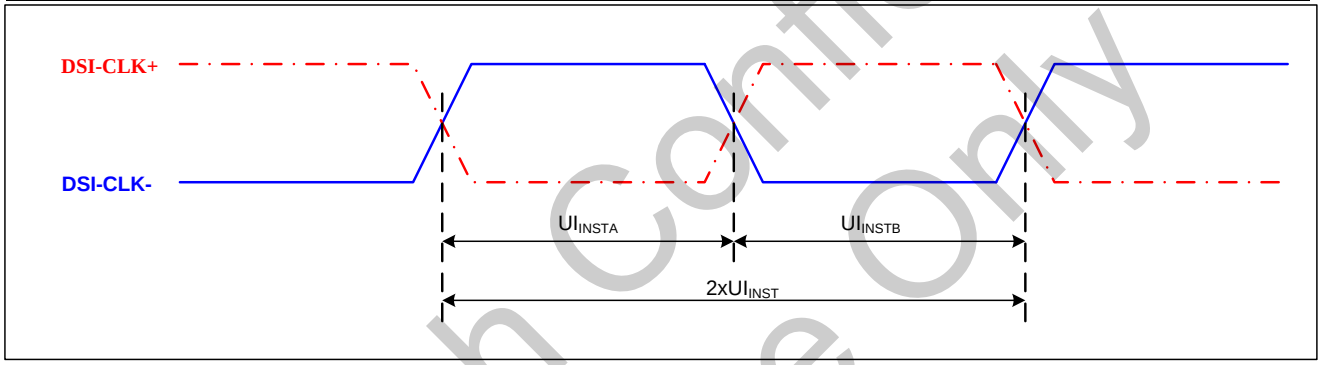
Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Terminal : SCL and CS						
Time from CS(10%) to SCL(90%)	TLS1	-	150	-	-	ns
Time from SCL(10%) to CS(90%)	TLS2	-	150	-	-	ns
Terminal : SCL and MOSI						
Data Setup Time : Time from changing MOSI(10%, 90%) to SCL(90%)	TSET	-	10	-	-	ns
Data Hold Time : Time from changing SCL(90%) to MOSI(10%, 90%)	THOL	-	5	-	-	ns
Terminal : SCL and MISO						
Time from SCL(10%) to stable MISO(10%, 90%)	TOUT	100pF,6Ω	-	-	30	ns
Terminal : CS						
Time between SPI cycles, CS at high level (90%)	TLH	-	150	-	-	us
SPI SCL Freq	-	-	-	-	14	MHz

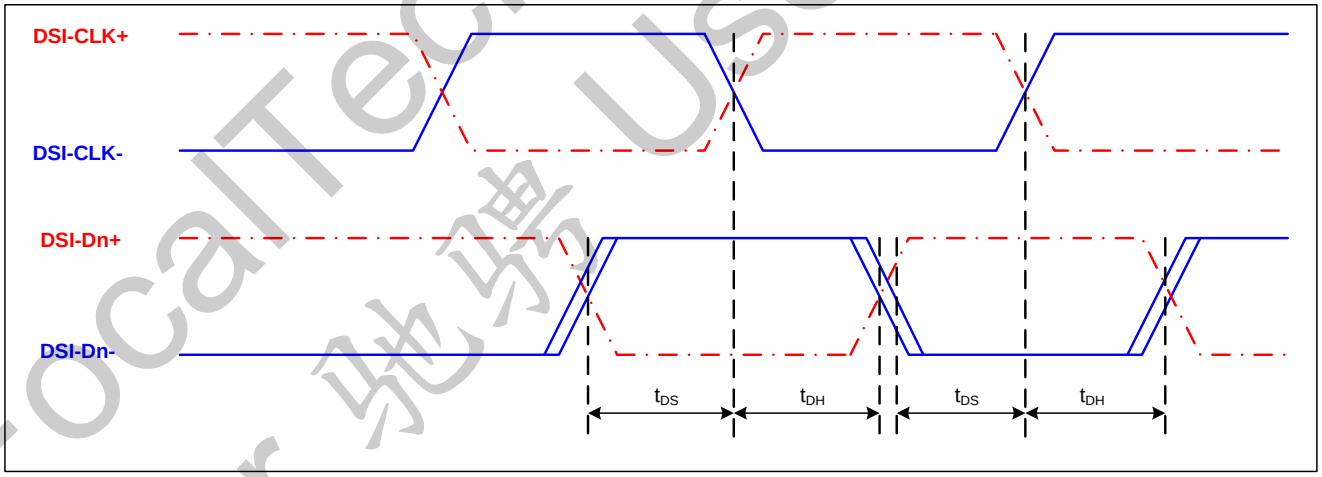


7.3.4 MIPI D-PHY AC characteristics

7.3.4.1 High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	1.82	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	0.91	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps





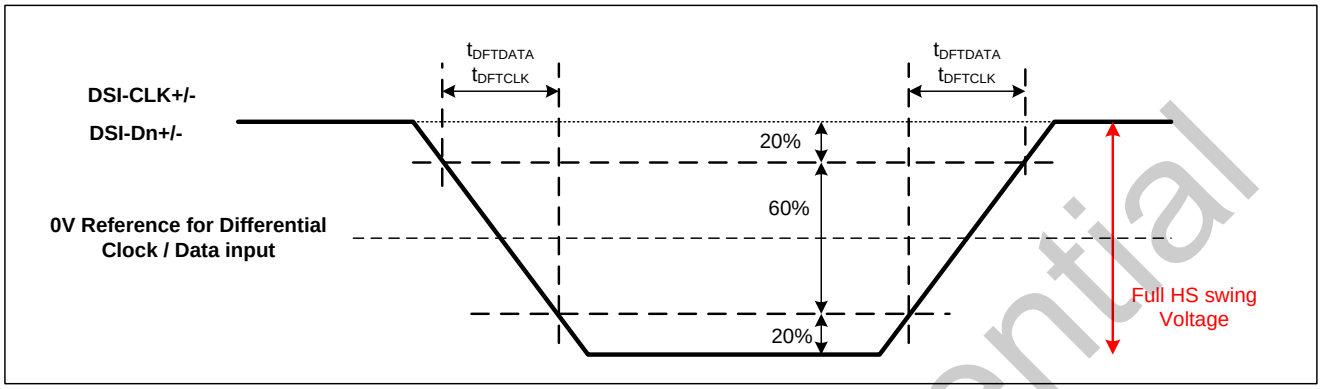


Figure: AC characteristics for MIPI-DSI High speed mode

7.3.4.2 Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPX-M}	Transmitted length of any Low-Power state period (MCU)	50	-	-	ns
DSI-D0+/-	$T_{TA-SURE-M}$	The display module waits after the LP-10 before transmitting the LP-00 (MCU)	T_{LPX-M}	-	$2XT_{LPX-M}$	ns
DSI-D0+/-	$T_{TA-GET-M}$	The display module drives the LP-00 before releasing MCU control	$5XT_{LPX-M}$	-	-	ns
DSI-D0+/-	$T_{TA-GO-M}$	The display drives the LP-00 after accepting control	$4XT_{LPX-M}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of (TLPX-M/TLPX-D) for driving overlap	2/3	-	3/2	-
DSI-D0+/-	T_{LPX-D}	Transmitted length of any Low-Power state period (Display)	50	58	-	ns
DSI-D0+/-	$T_{TA-SURE-D}$	The MCU waits after the LP-10 before transmitting the LP-00 (Display)	T_{LPX-D}	-	$2XT_{LPX-D}$	ns
DSI-D0+/-	$T_{TA-GET-D}$	The MCU drives the LP-00 before releasing Display control	$5XT_{LPX-D}$	-	-	ns
DSI-D0+/-	$T_{TA-GO-D}$	The MCU drives the LP-00 after accepting control	$4XT_{LPX-D}$	-	-	ns

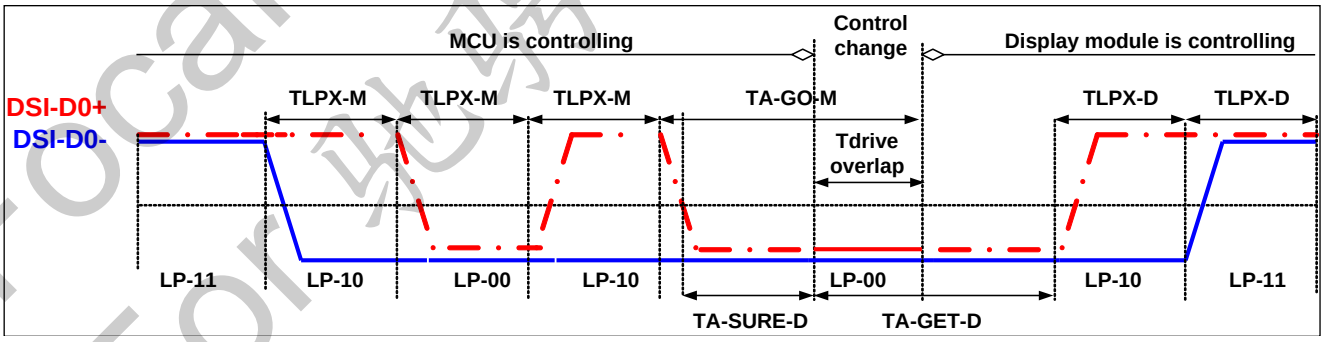


Figure: BTA from the MCU to the Display Module

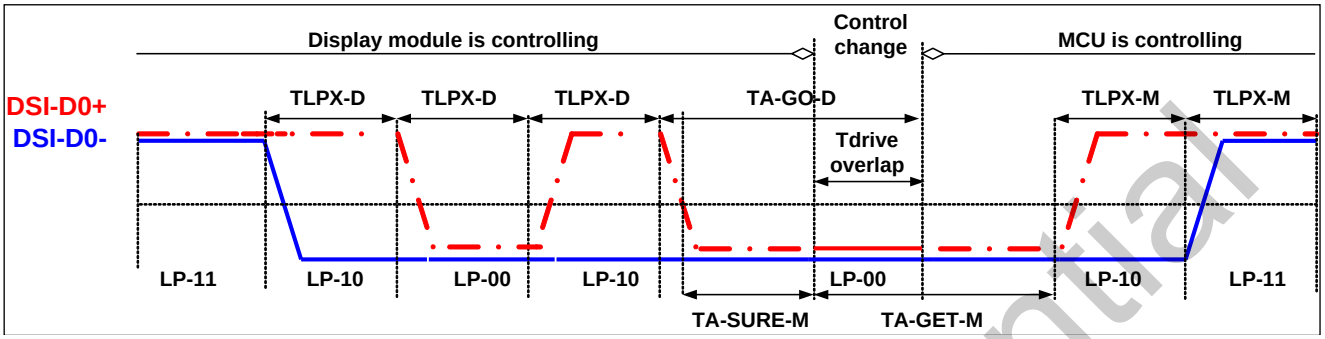


Figure: BTA from the Display Module to the MCU

7.3.4.3 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

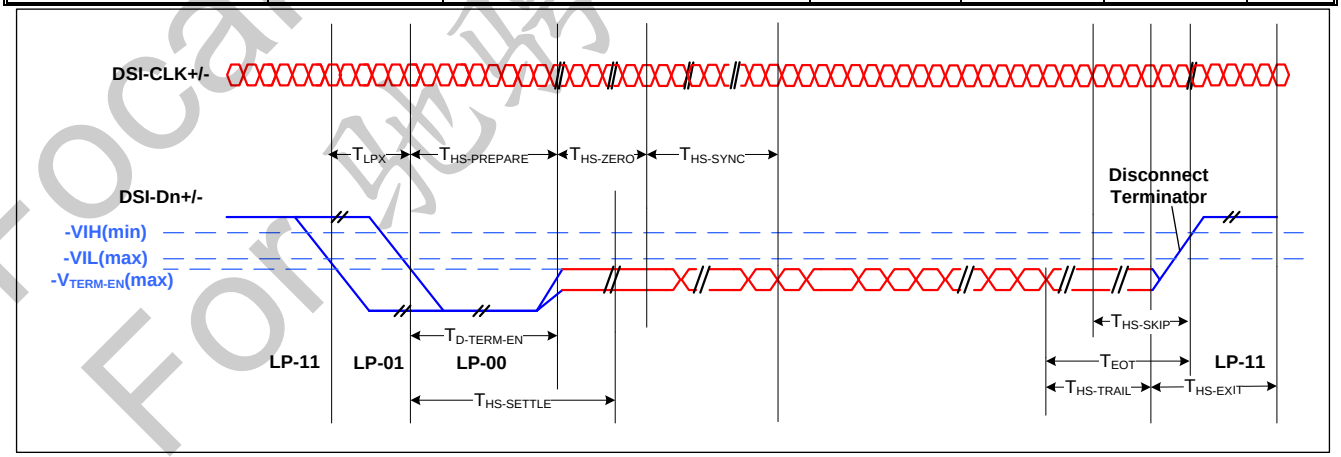


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

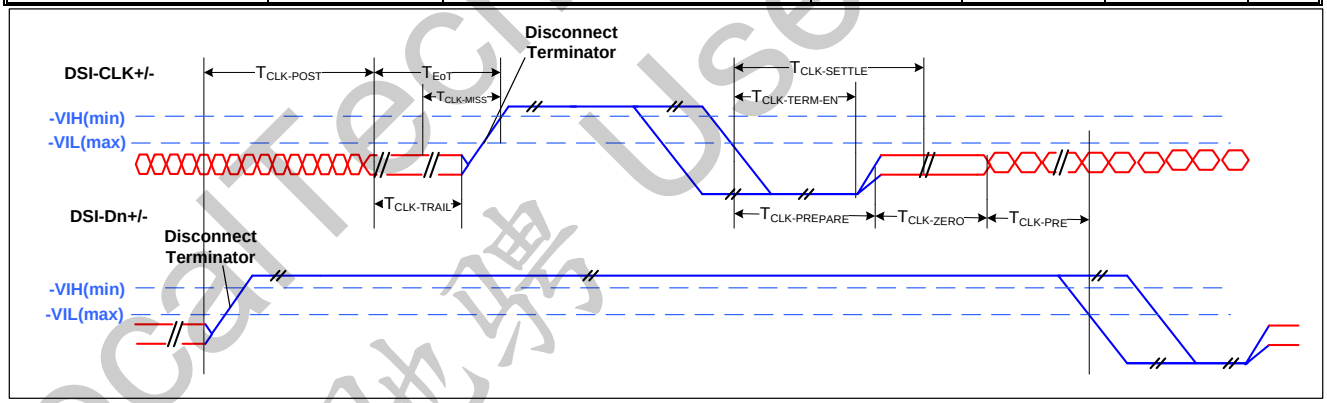


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

7.3.4.4 LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

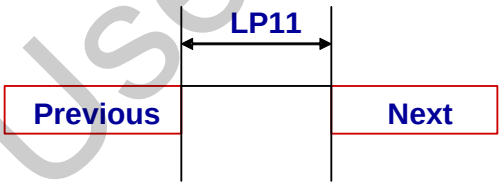
1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	100 ns	-	100 ns	-
HSDT	60ns + 52UI	-	60ns + 52UI	-	60ns + 52UI	-
BTA	100 ns	-	100 ns	-	100 ns	-



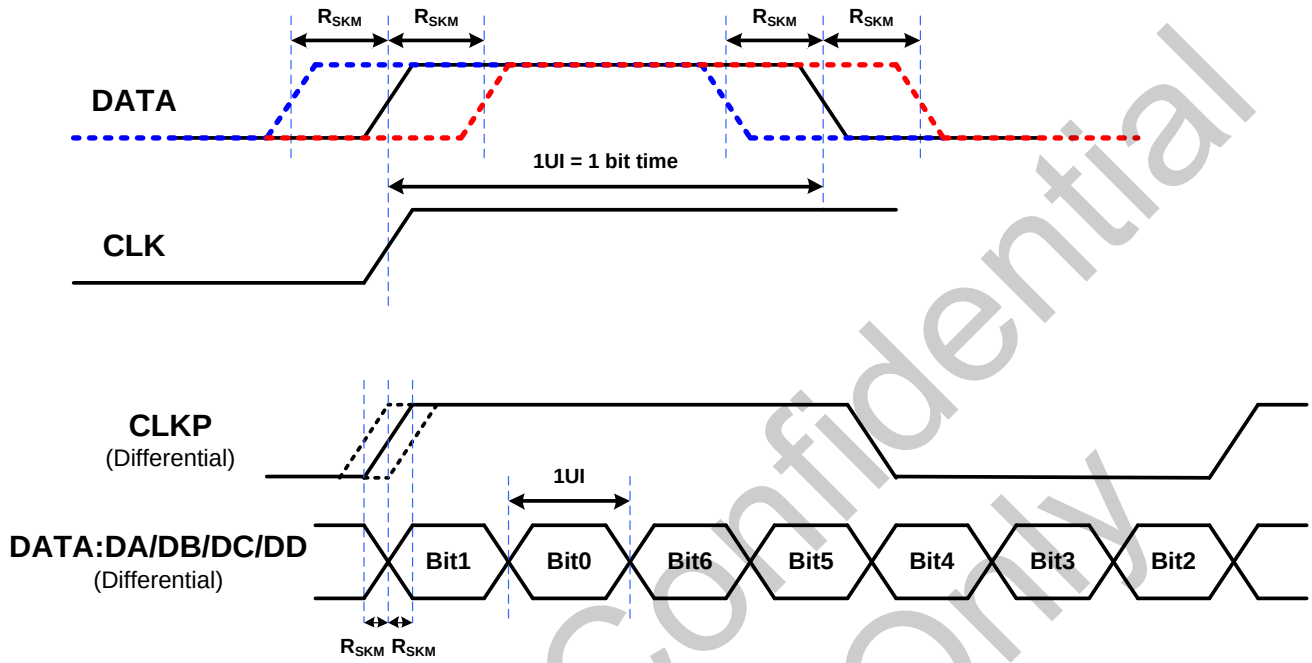
7.3.5 LVDS AC timing characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min	Typ	Max	
Input data skew margin	RSKM (1)	FLVDS = 110MHz |VID| = 200mV VCM_RX = 1.2v	-	-	0.2	UI
Clock high time	TLVCH (2)	-	-	4/(7*FLVDS)	-	nS
Clock low time	TLVCL (2)	-	-	3/(7*FLVDS)	-	nS
PLL wake-up time	TPLLwkup (3)	-	-	-	150	µS
Sync skew margin between point to point	$T_{SYNCSKEW}$ (4)	-	-	-	7	UI
Modulation Frequency	SSCMF (5)	FLVDS = 110 MHz	20	-	200	KHz
Modulation Rate	SSCMR (5)	FLVDS = 110 MHz	-5	-	+5	%

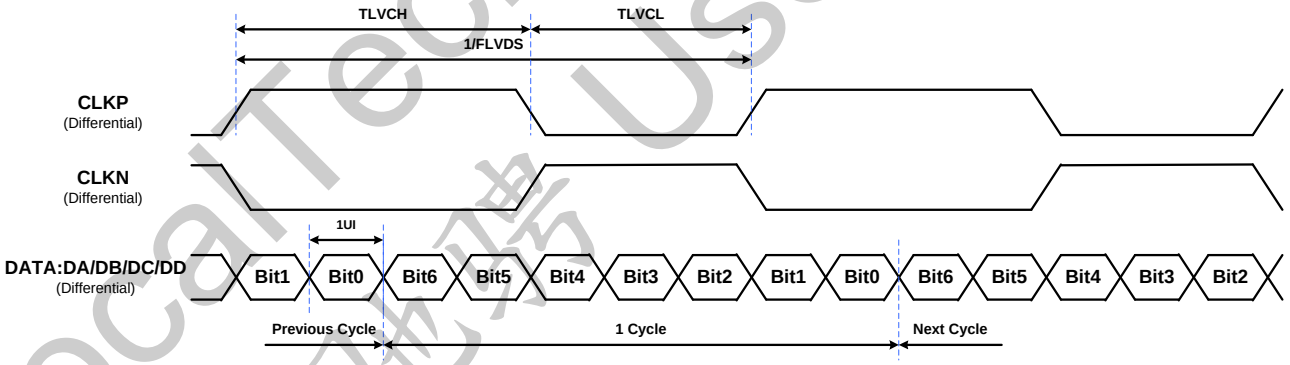
NOTE1： FLVDS = 15 MHz ~ 110 MHz (including SSC operation)

NOTE2： Support DE mode H-blanking maximum +/- 16 clks jitter range

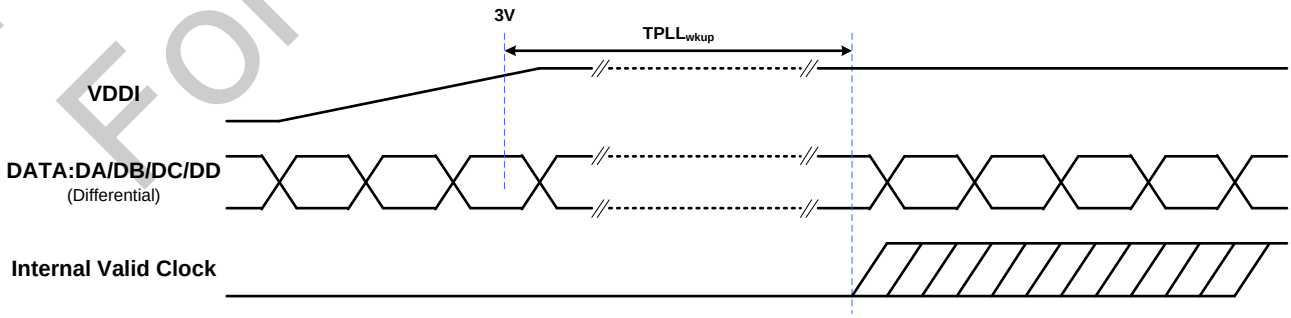
(1)



(2)

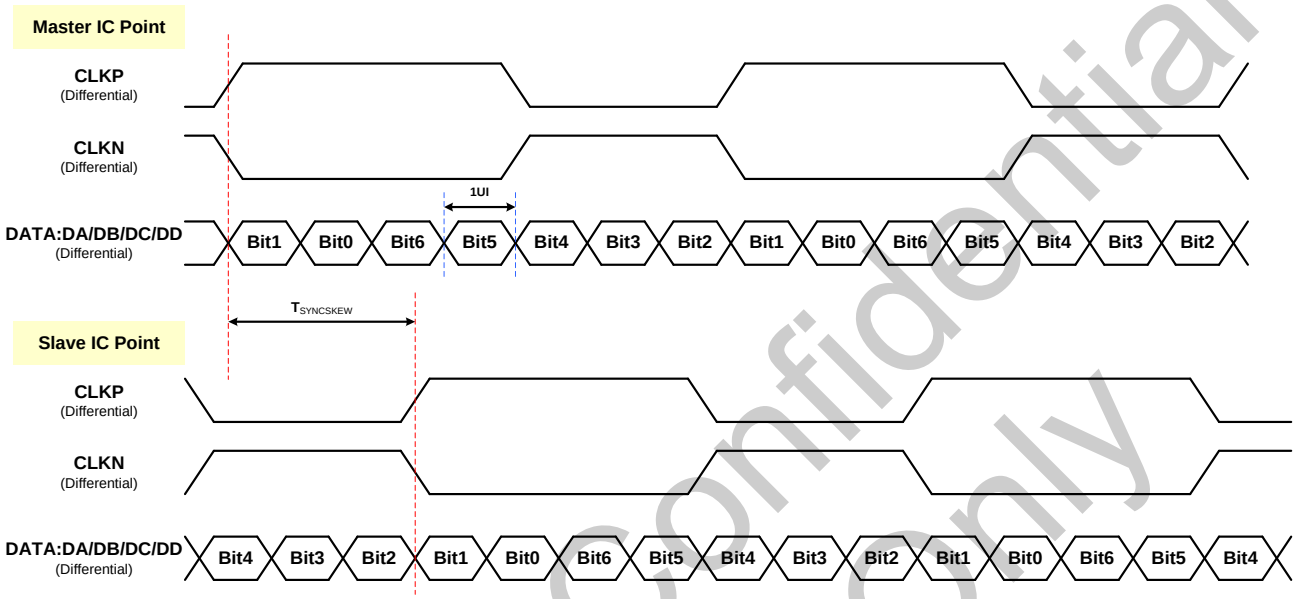


(3)

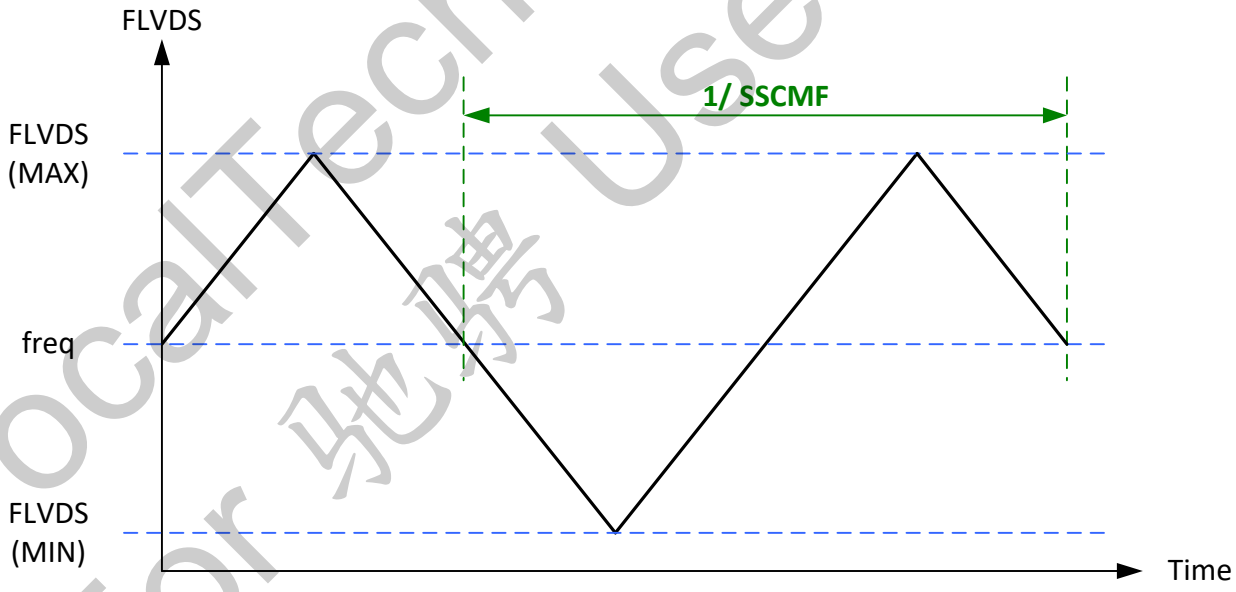


(4) LVDS point to point architecture

$T_{SYNCSKEW}$ must smaller than 7 UIs (1 CLKP/N) between ICs.



(5)



※1：FLVDS = freq * (1 + SSCMR)

※2：FLVDS (MAX) ≦110MHz

7.3.6 Power On/Off Sequence

During power on, if LCD is in Sleep Out mode, VDDI must be powered down minimum 120 ms after RESX has been released.

During power off, if LCD is in Sleep In mode, VDDI can be powered down minimum 0 ms after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has higher priority than CSX.

Notes:

1). There will be no damage to the display module if the power sequences are not met.

2). There will be no abnormal visible effects on the display panel during the Power On/Off sequences.

3). There will be no abnormal visible effects on the display between end of Power On sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off sequence.

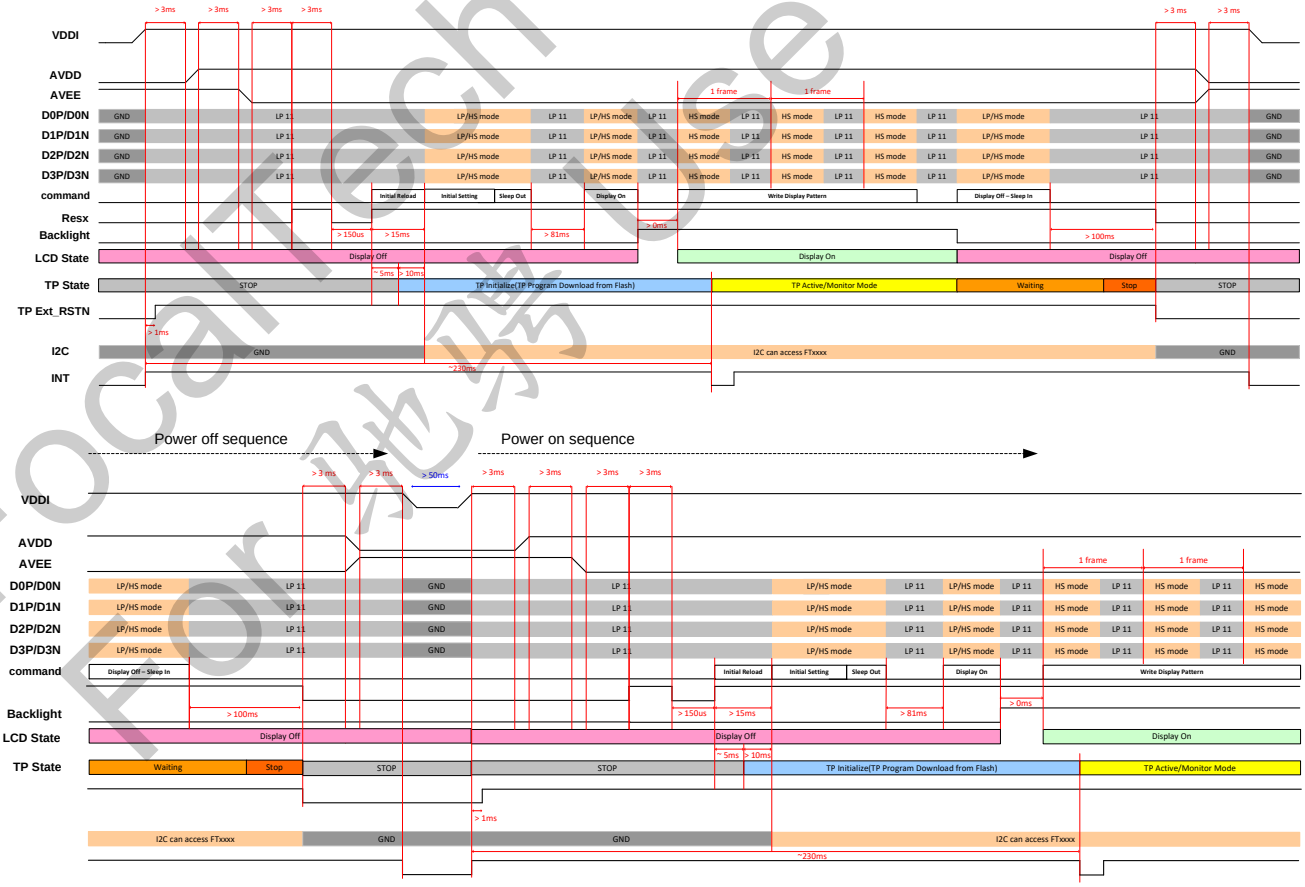
4). If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a hardware reset (RESX) after host Power On sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

5). There is not a limit for Rise/Fall time on VDDI

6). The display module can also initialize and calibrate DSI-CLK +/- and DSI-D0 +/- lanes within 5ms after LP-11 (Clock and Data Channels), VDDI are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).

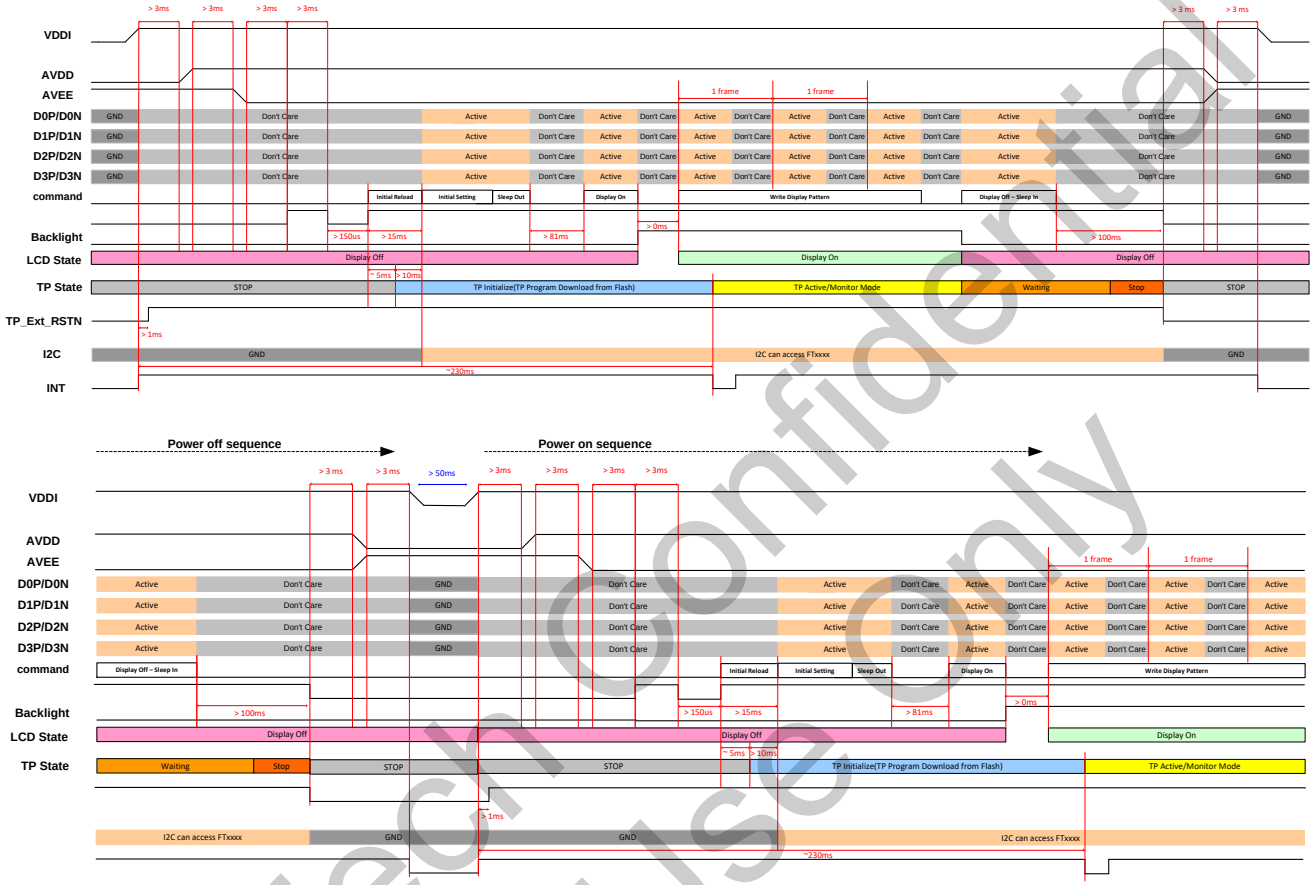
w/i Flash (3 Power mode) (MIPI)

3 Power mode Power on/off sequence

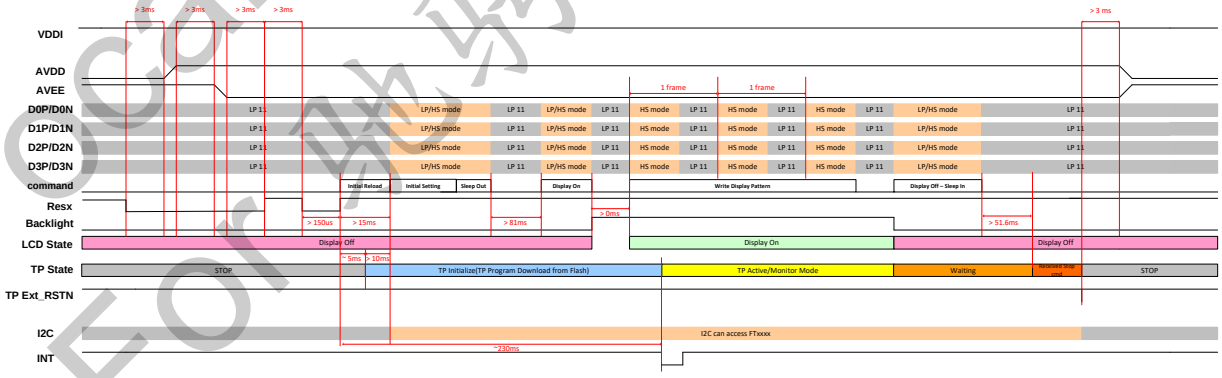


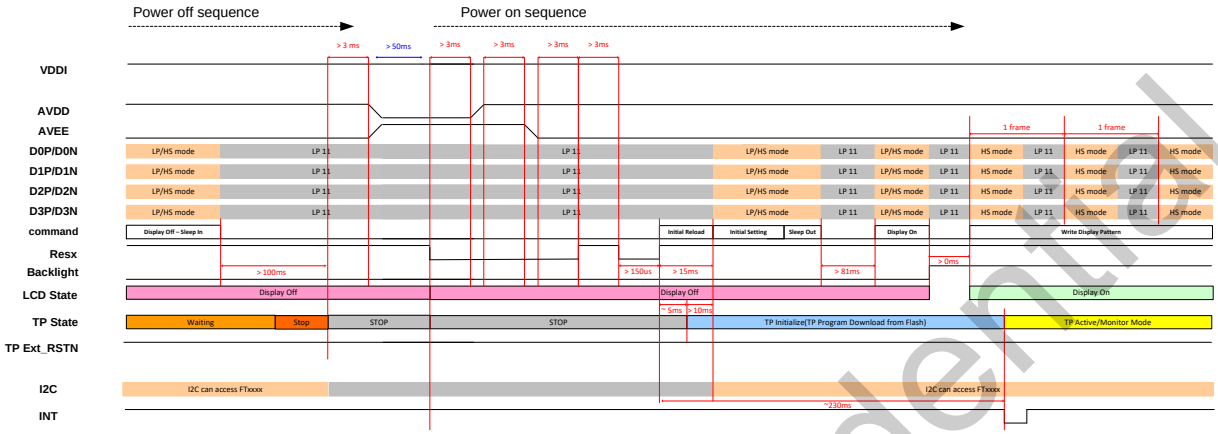
w/i Flash (3 Power mode) (LVDS)

3 Power mode Power on/off sequence

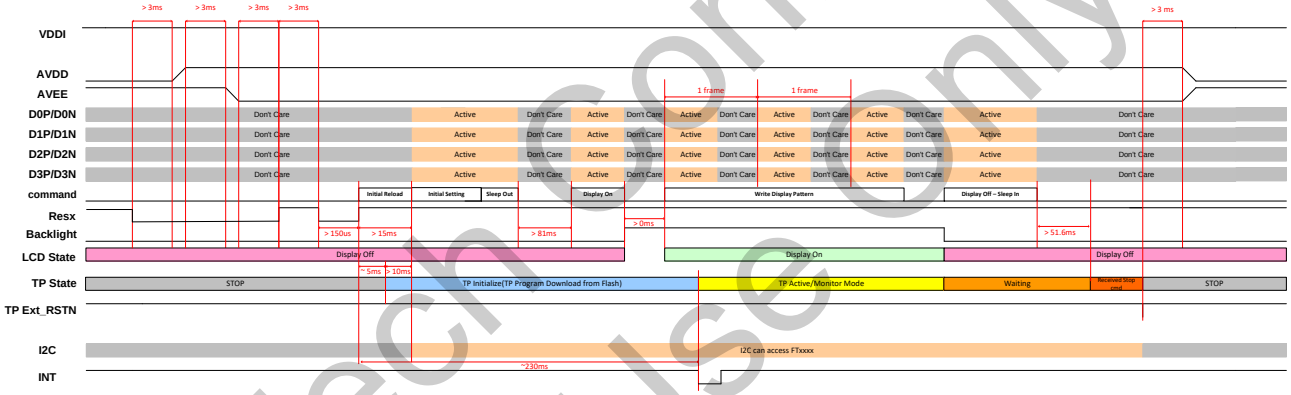


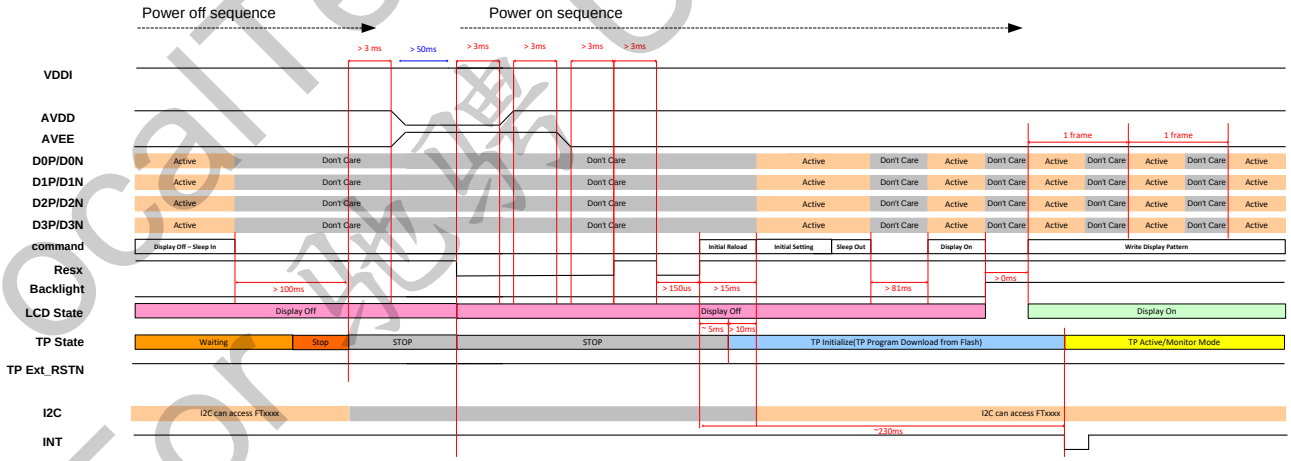
3 Power mode Power on/off sequence(VDDI keep) (MIPI)





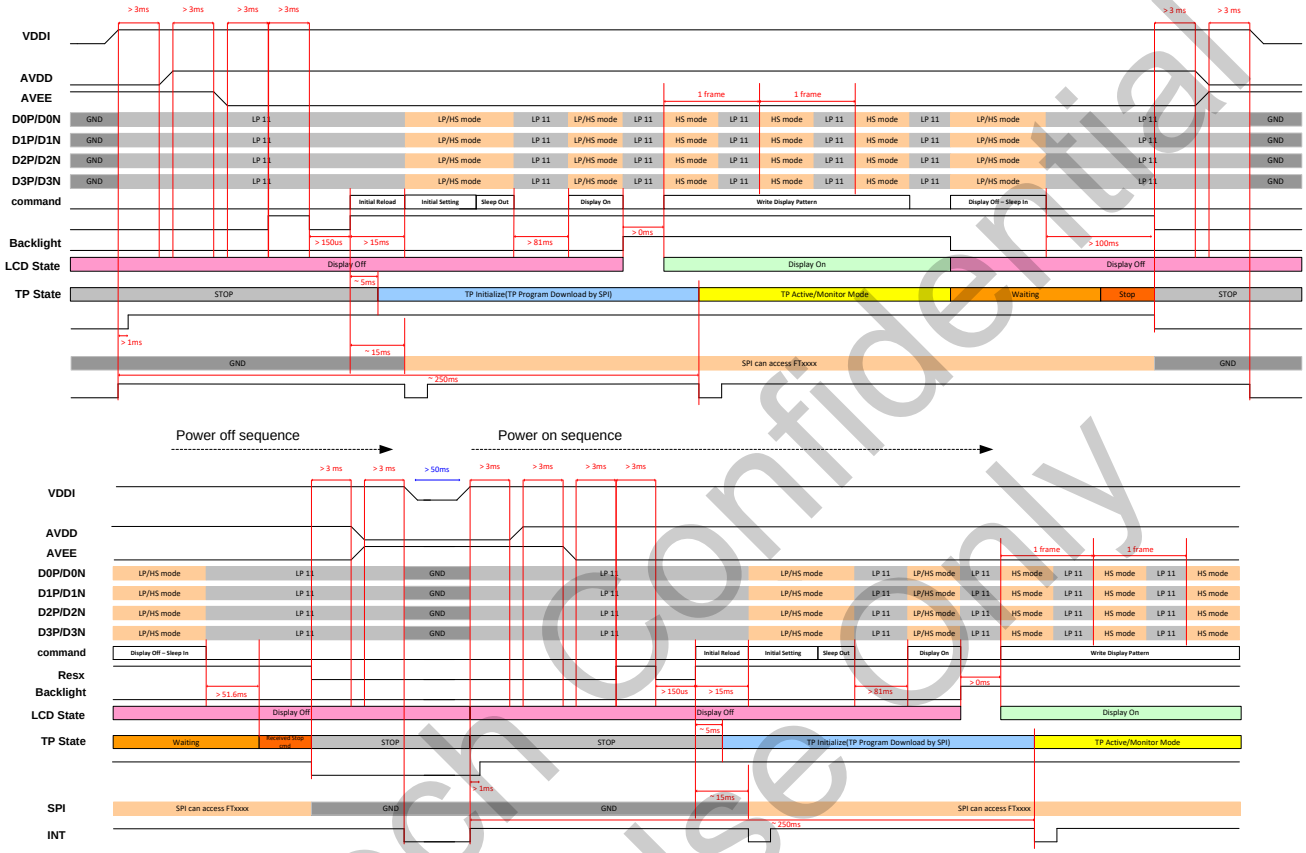
3 Power mode Power on/off sequence(VDDI keep)(LVDS)





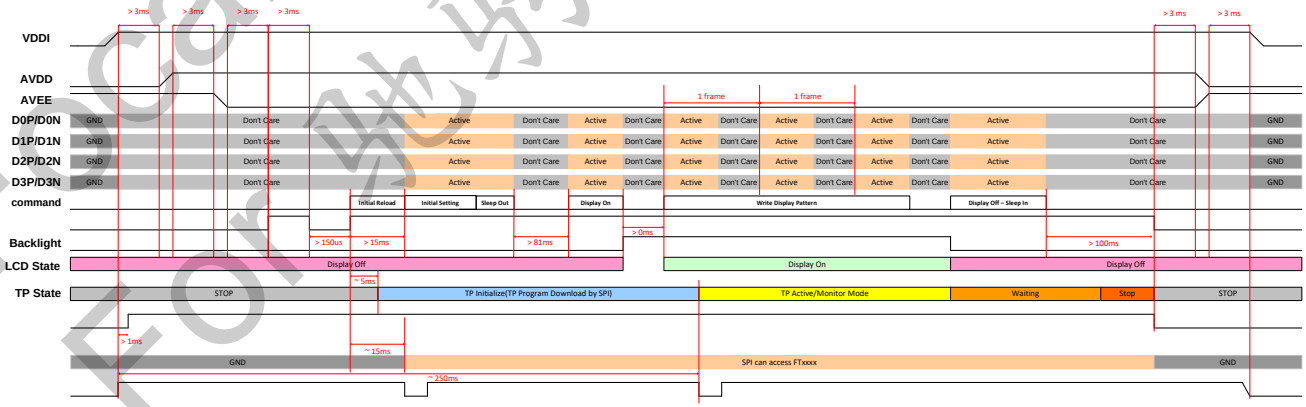
w/o Flash (3 Power mode) (MIPI)

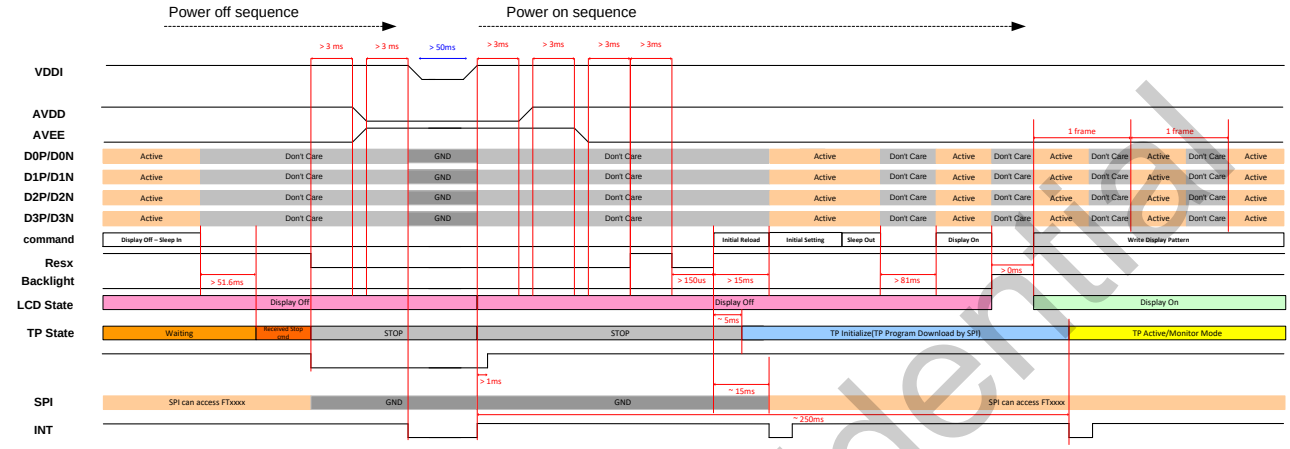
3 Power mode Power on/off sequence



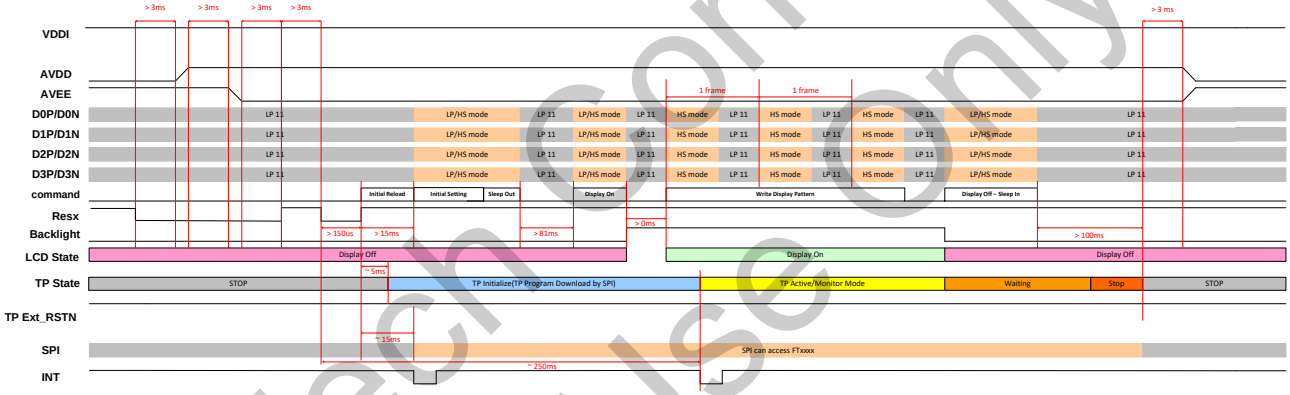
w/o Flash (3 Power mode) (LVDS)

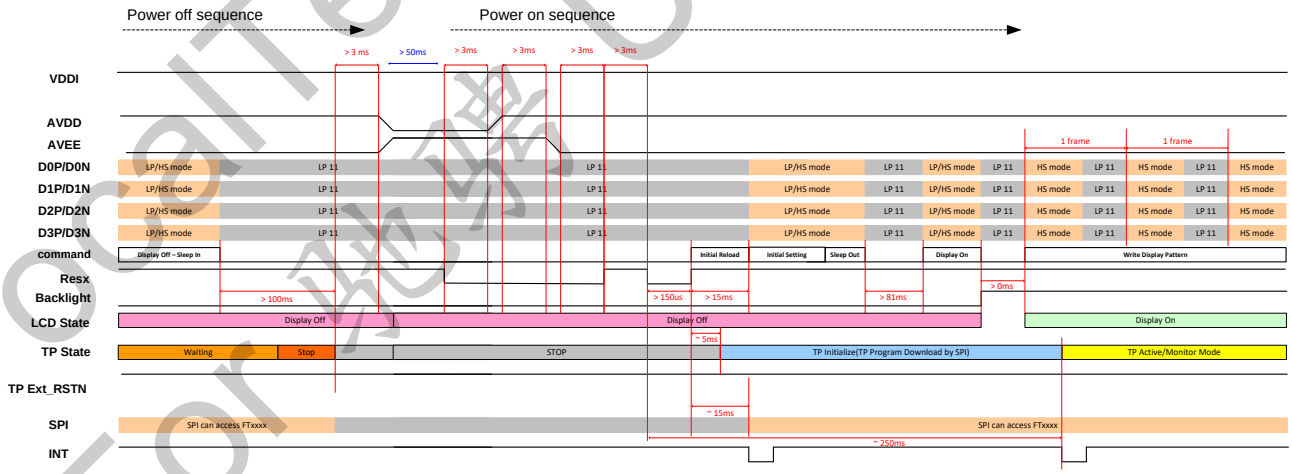
3 Power mode Power on/off sequence



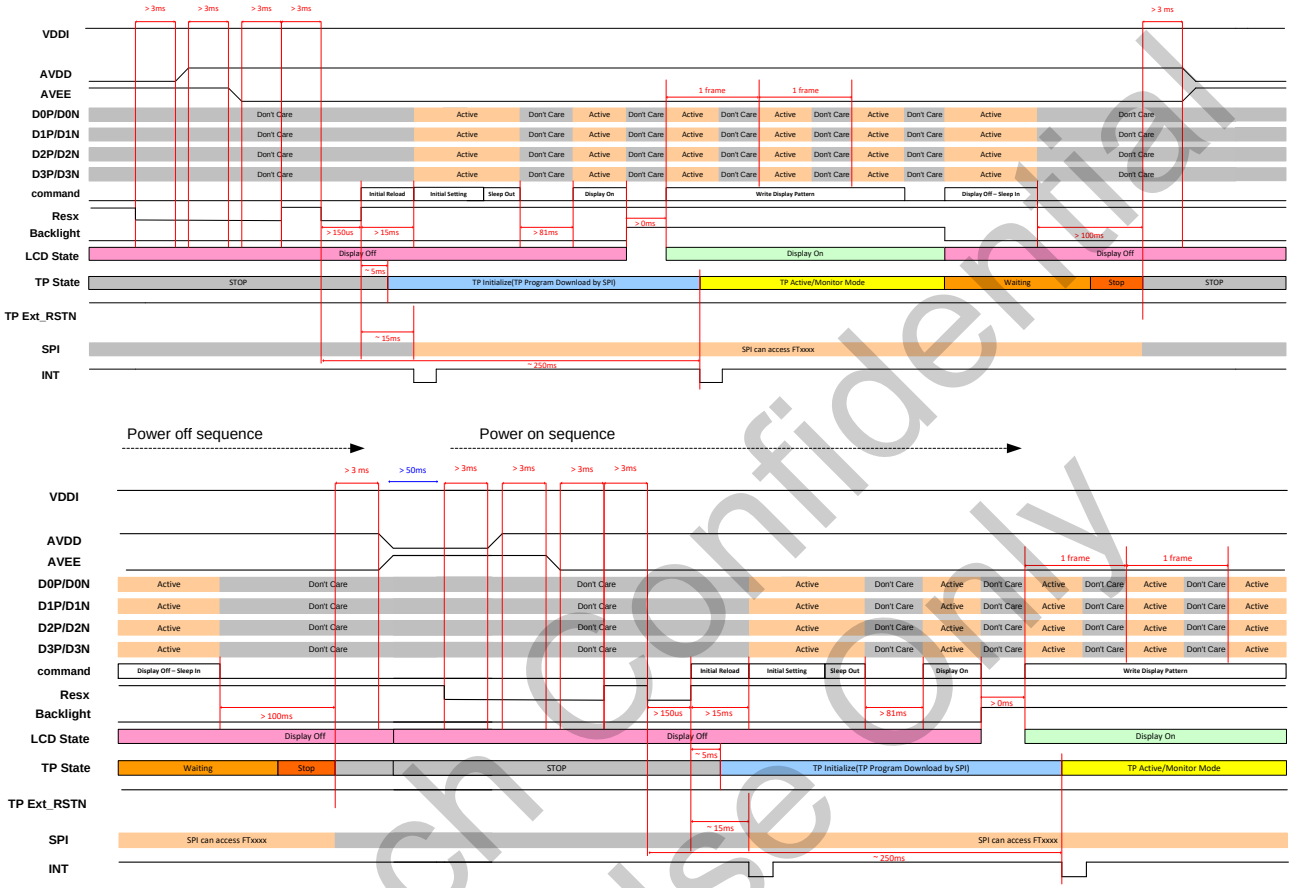


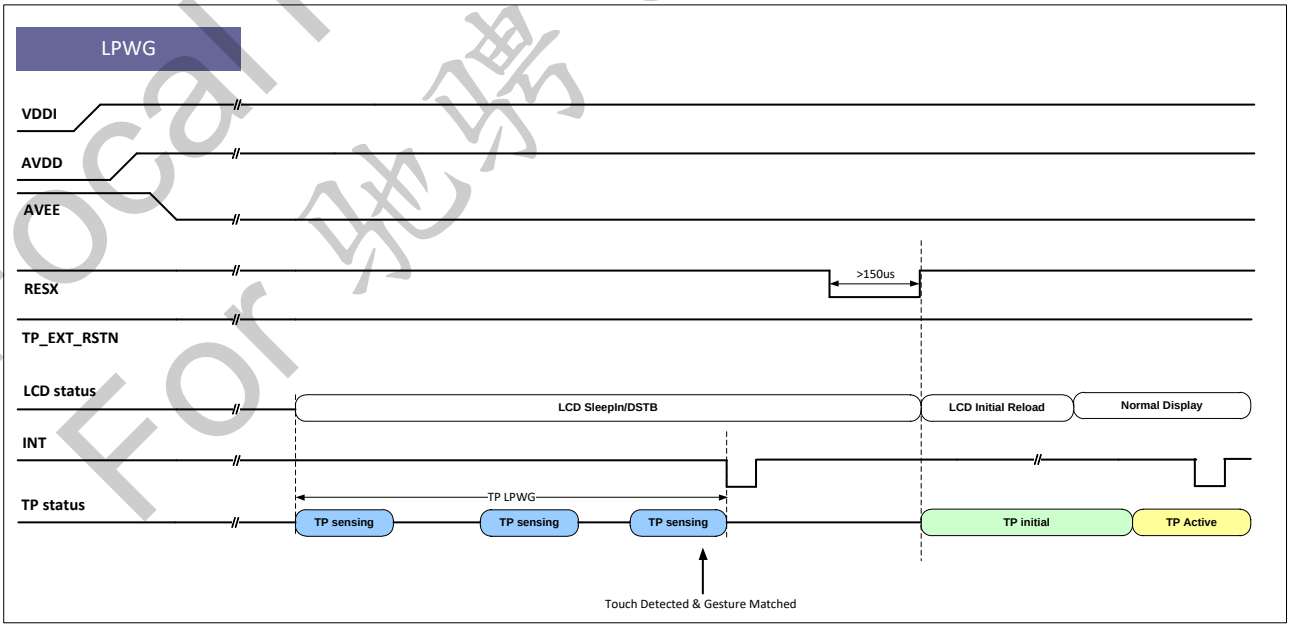
3 Power mode Power on/off sequence(VDDI keep) (MIPI)



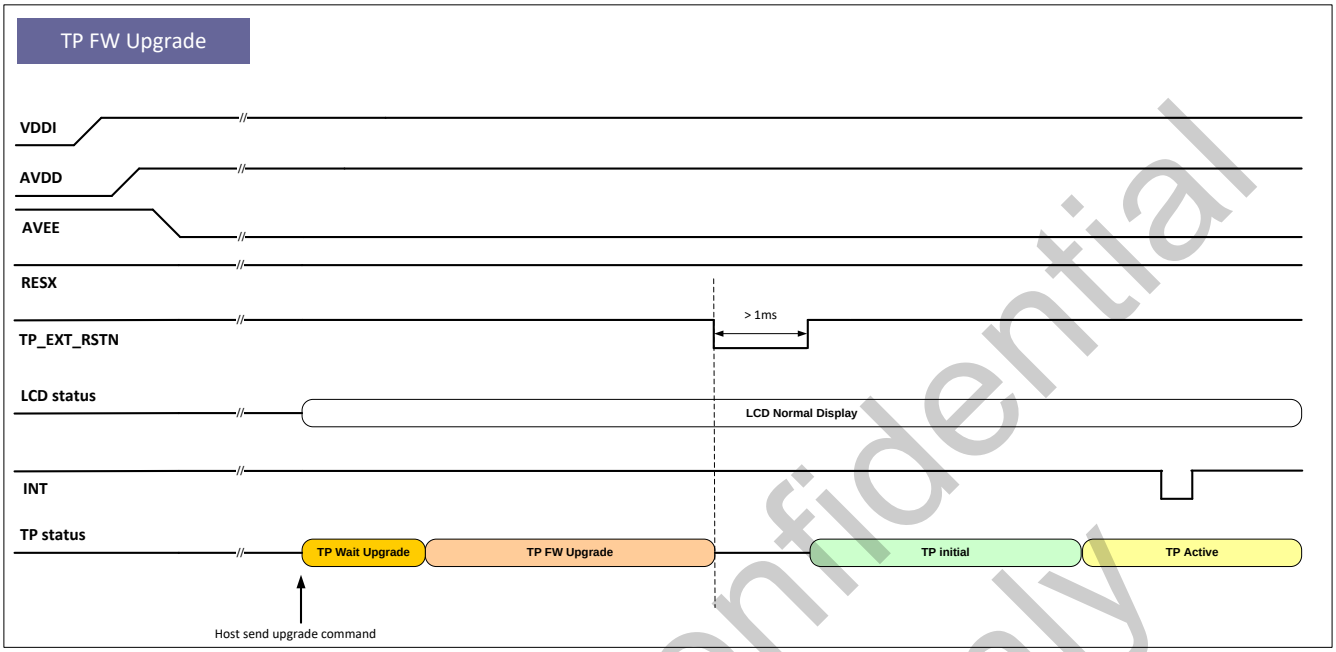


3 Power mode Power on/off sequence(VDDI keep) (LVDS)





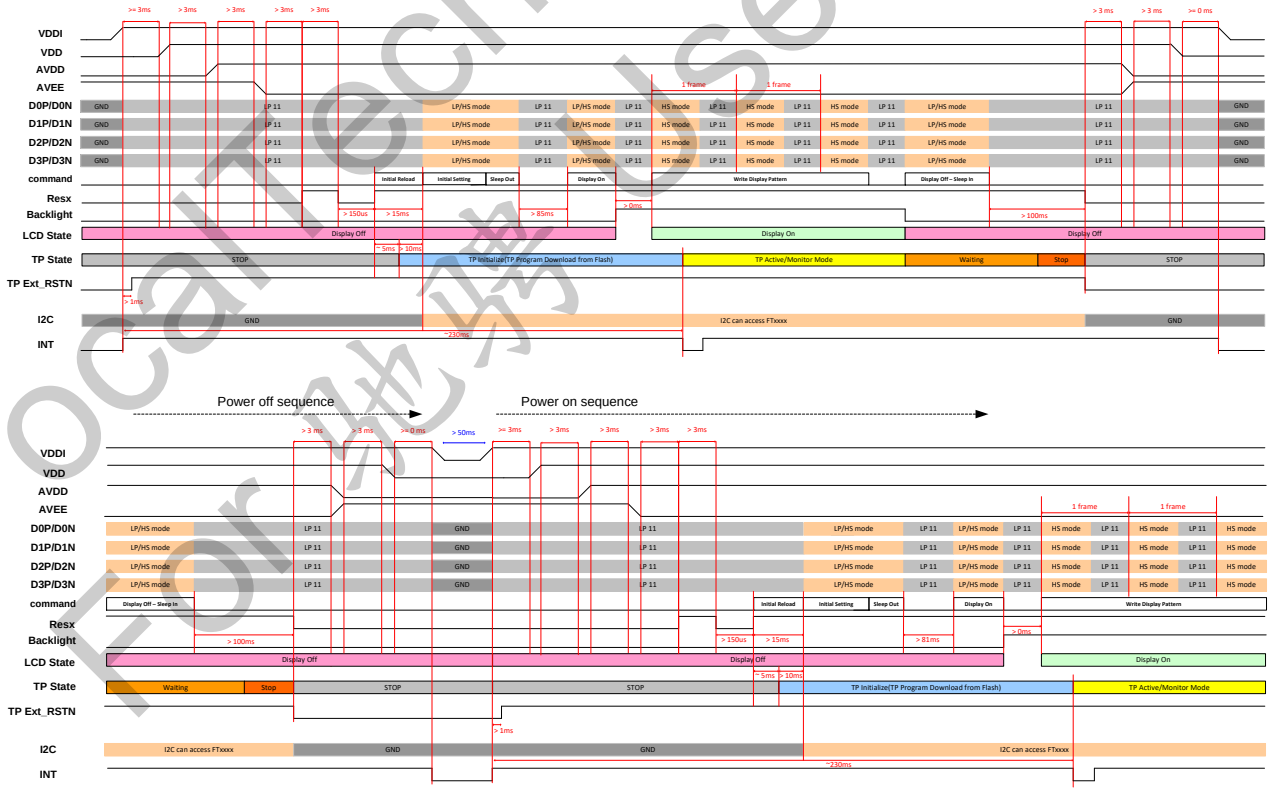
3 Power mode LPWG sequence



3 Power mode TP FW Upgrade

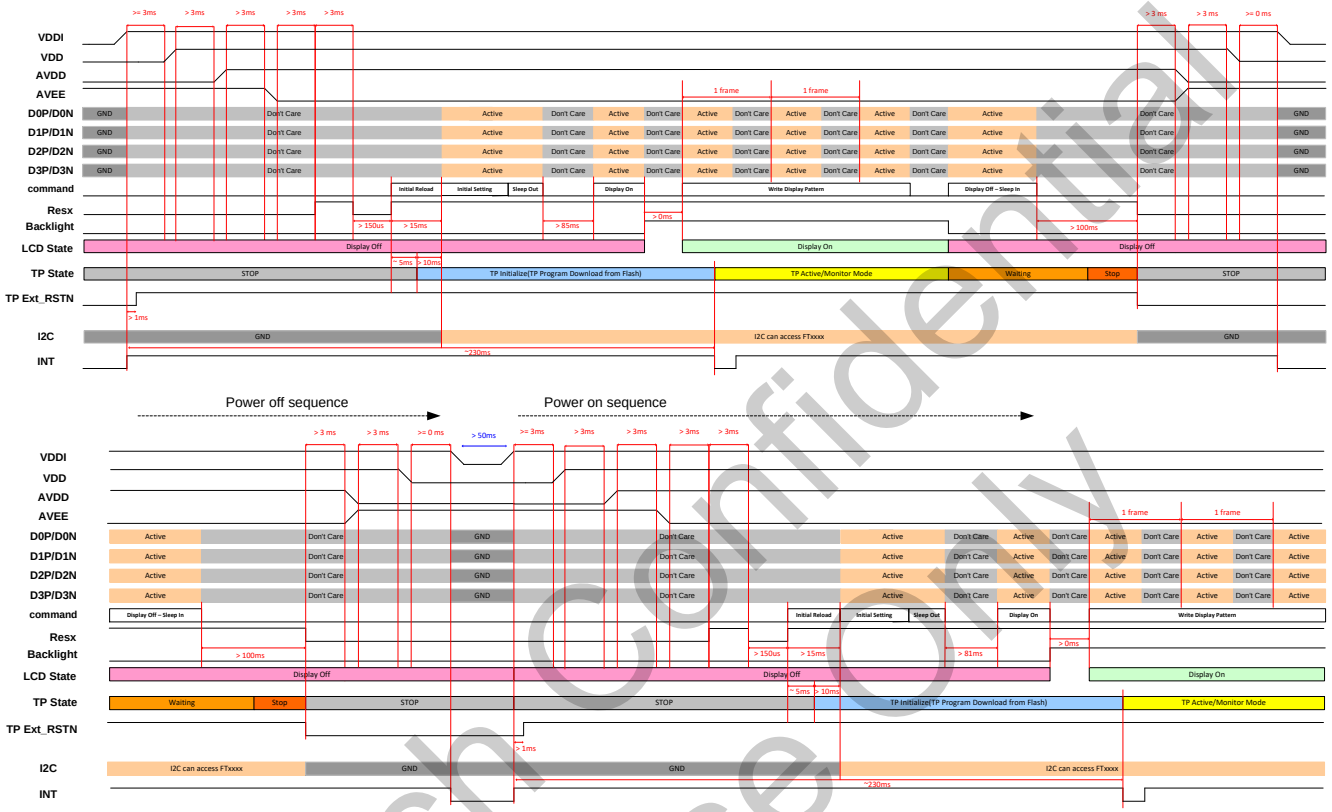
w/i Flash (4 Power mode) (MIPI)

4 Power mode Power on/off sequence

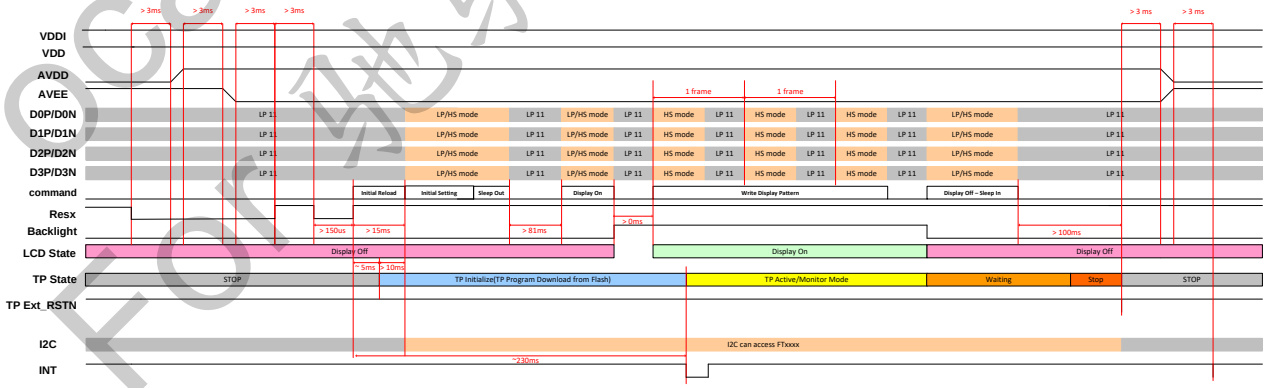


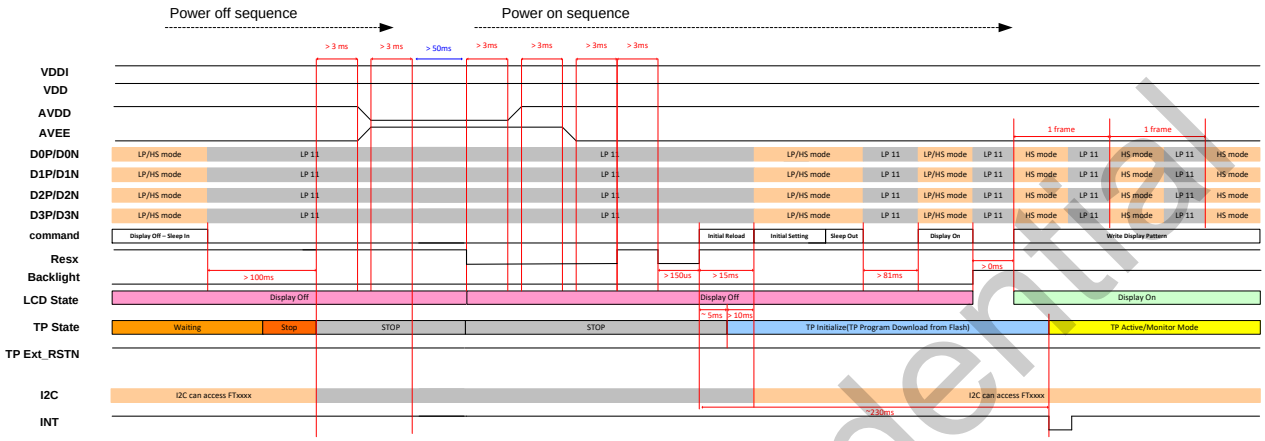
w/i Flash (4 Power mode) (LVDS)

4 Power mode Power on/off sequence

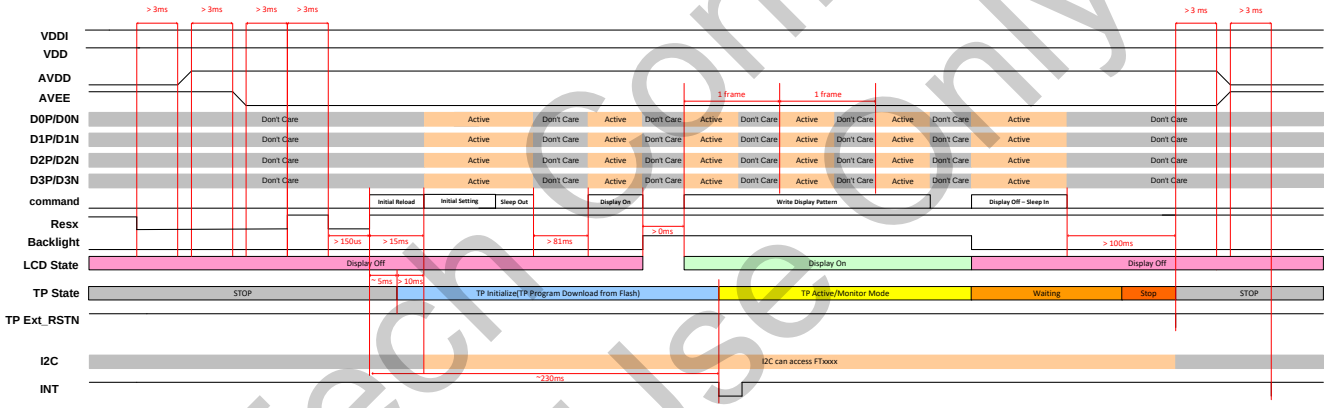


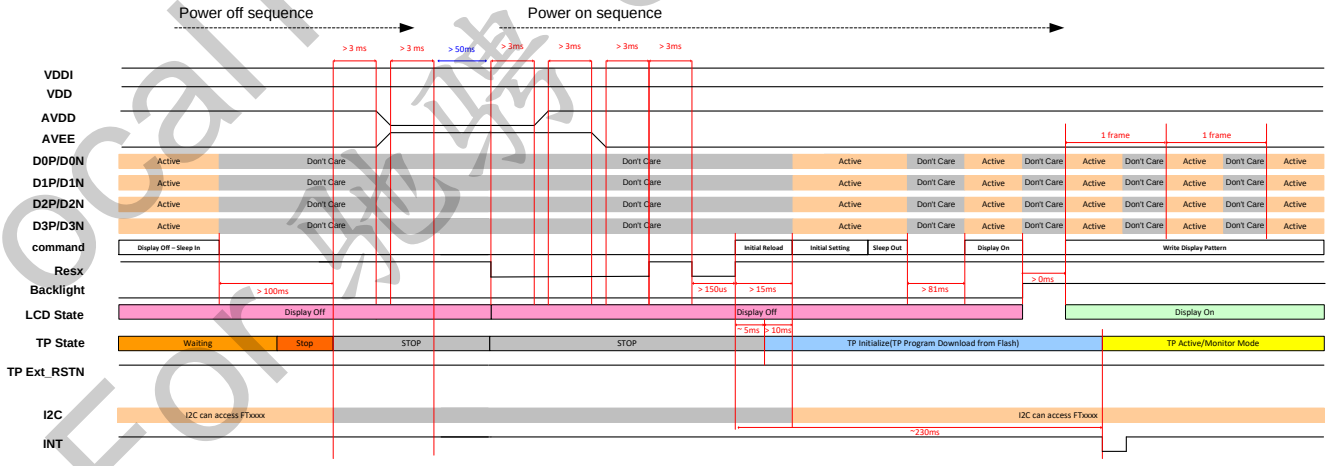
4 Power mode Power on/off sequence(VDDI/VDD keep) (MIPI)





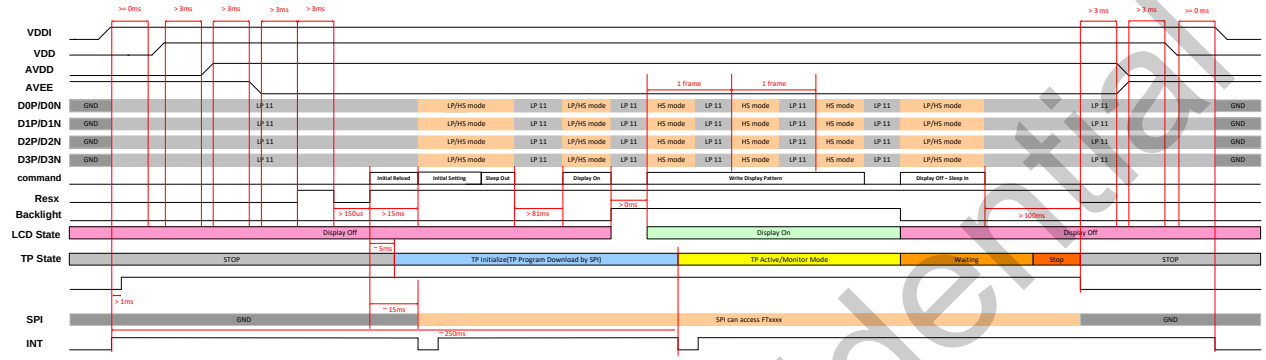
4 Power mode Power on/off sequence(VDDI/VDD keep) (LVDS)

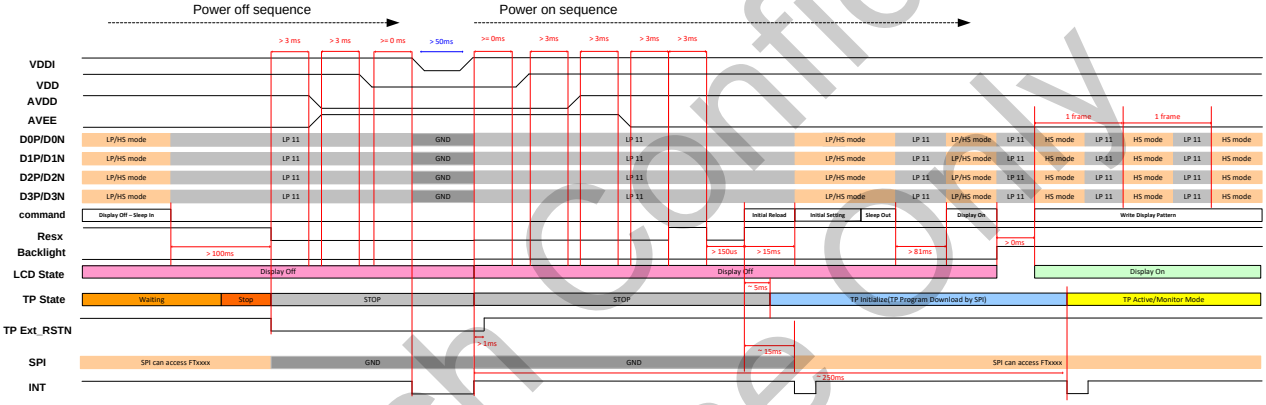




w/o Flash (4 Power mode) (MIPI)

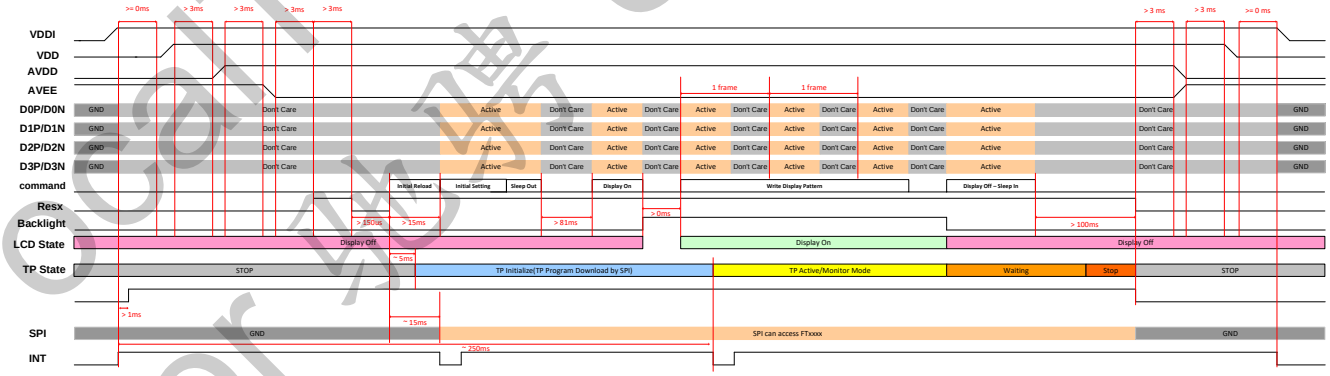
4 Power mode Power on/off sequence

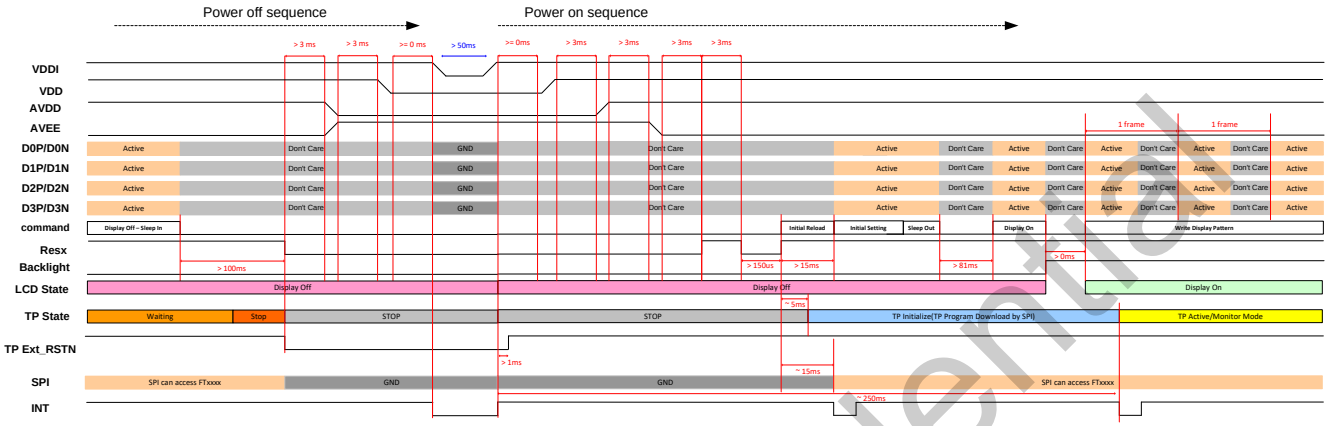




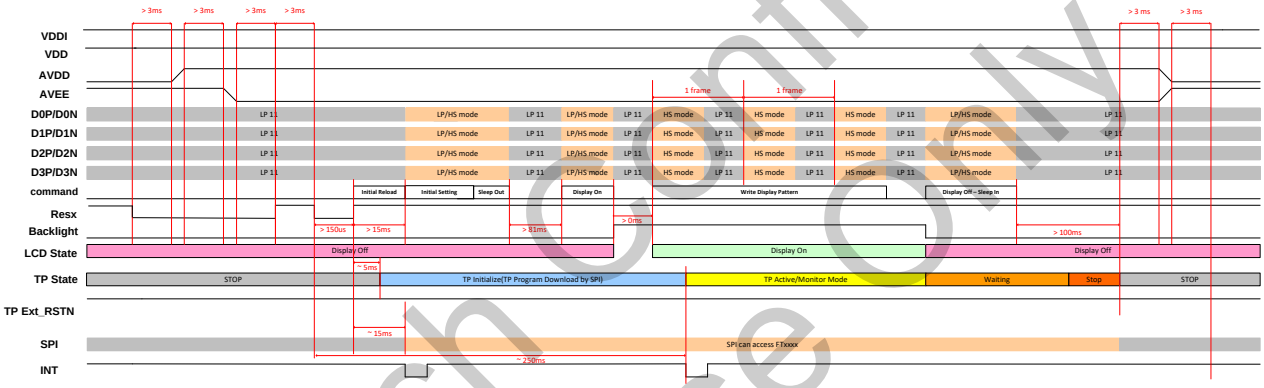
w/o Flash (4 Power mode) (LVDS)

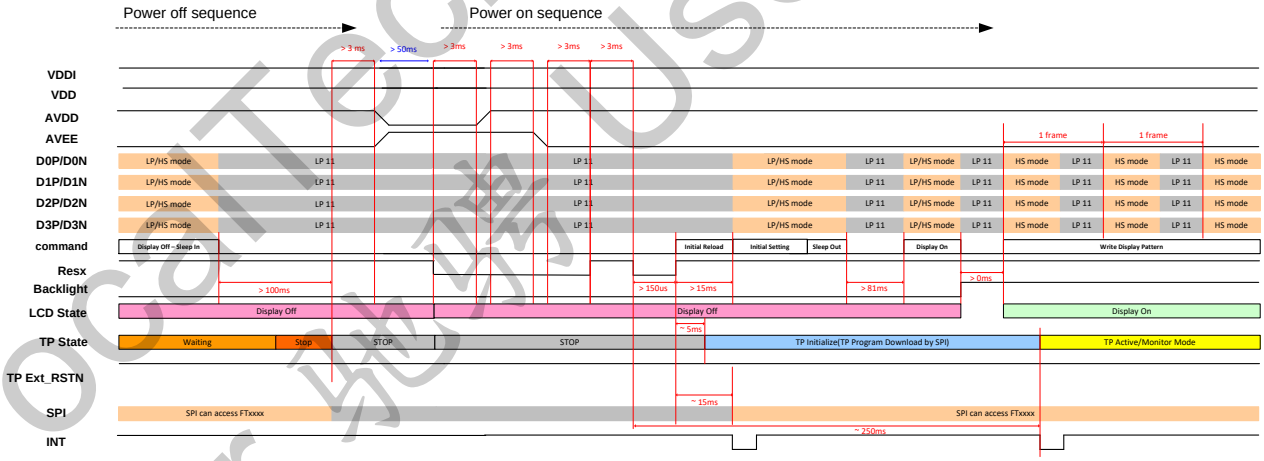
4 Power mode Power on/off sequence



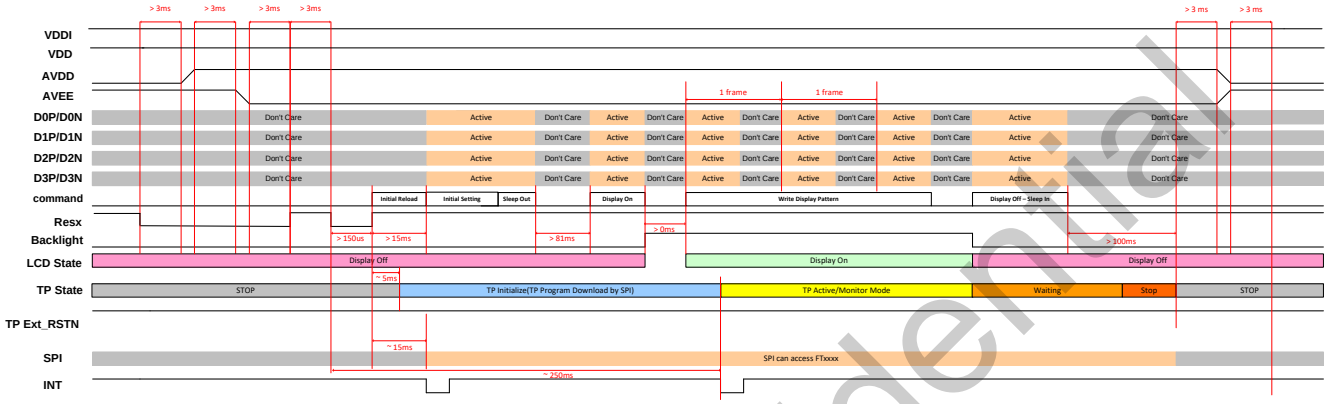


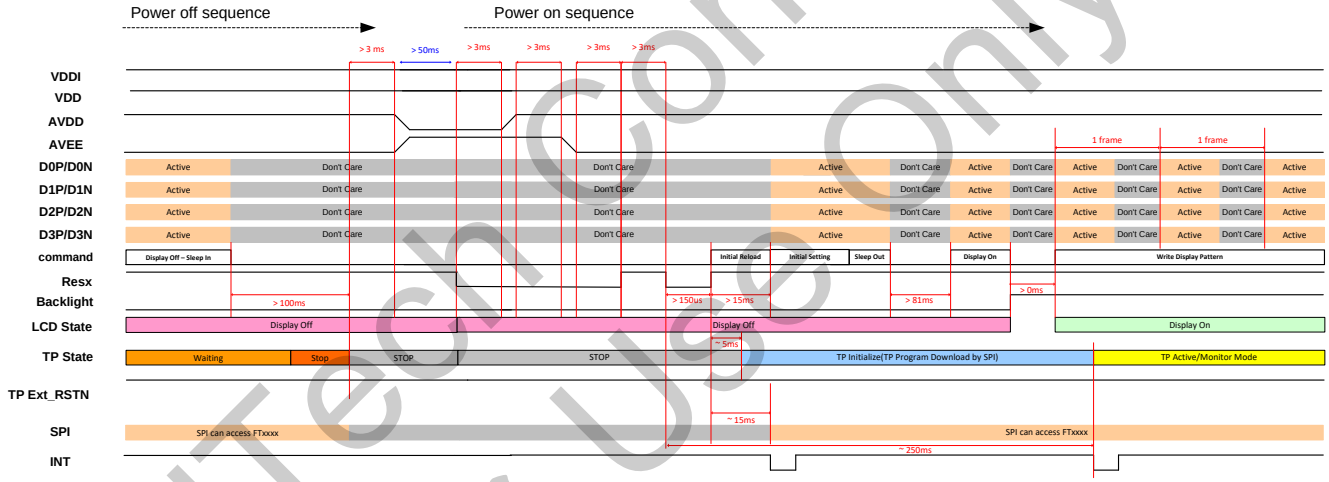
4 Power mode Power on/off sequence(VDDI/VDD keep) (MIPI)

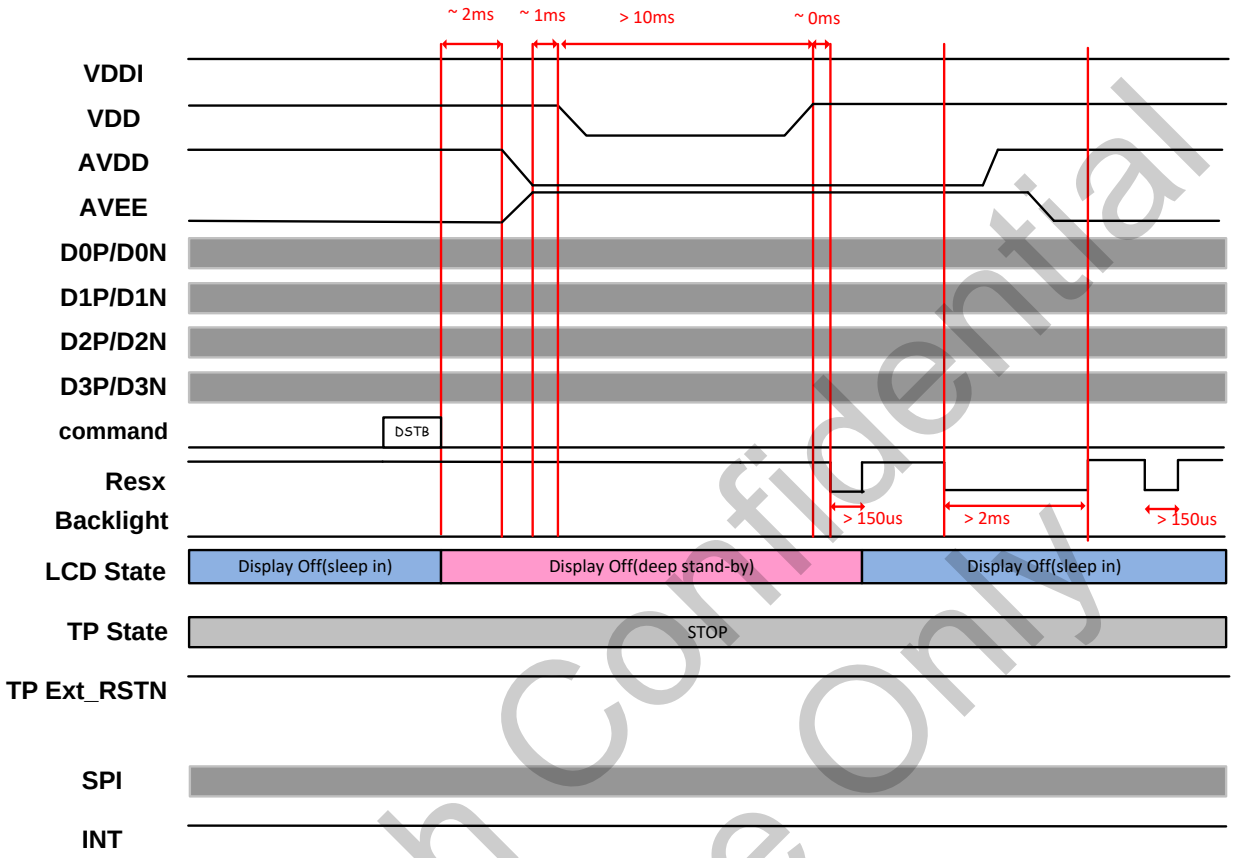




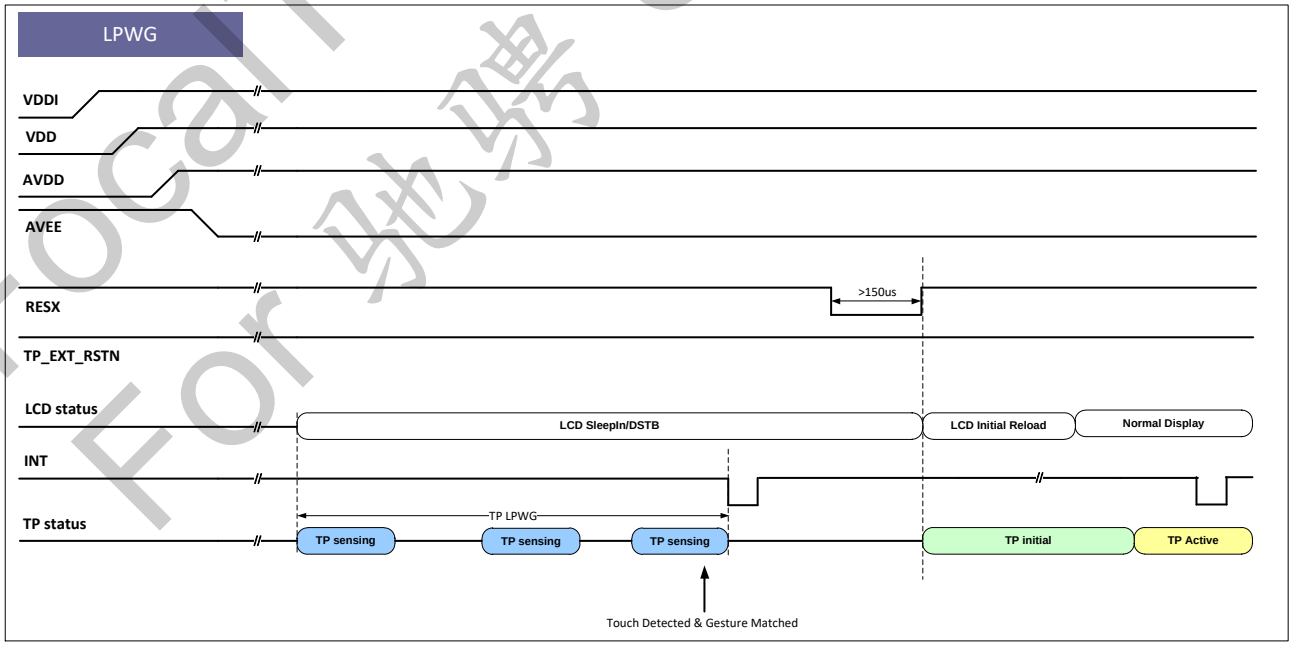
4 Power mode Power on/off sequence(VDDI/VDD keep) (LVDS)



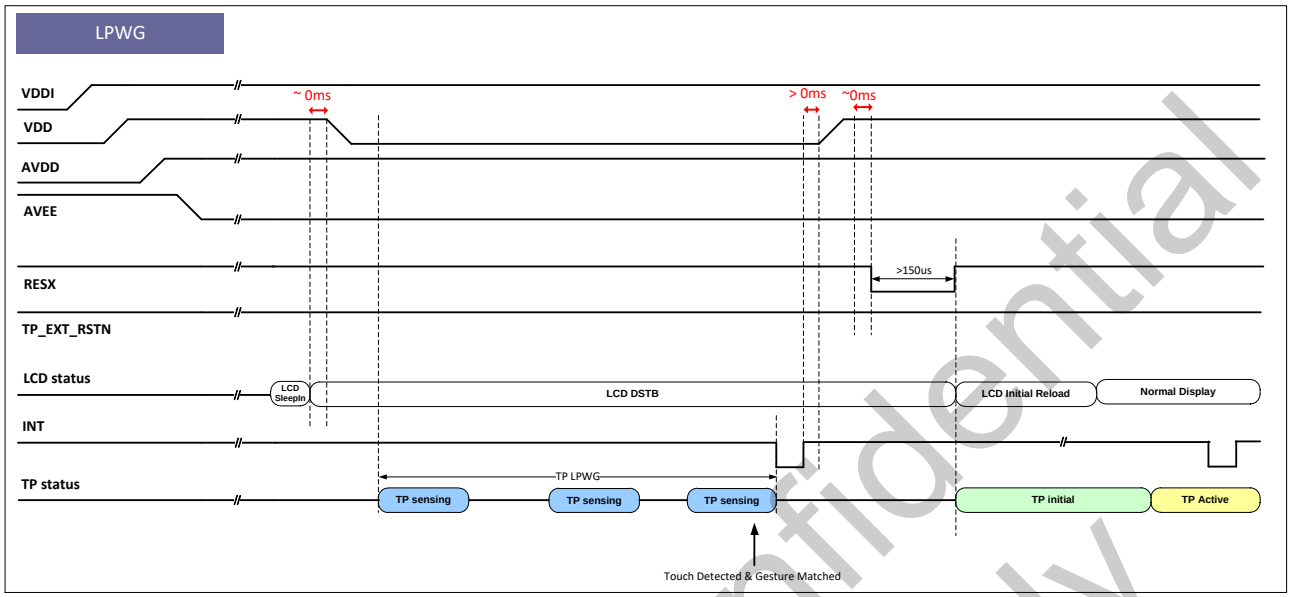




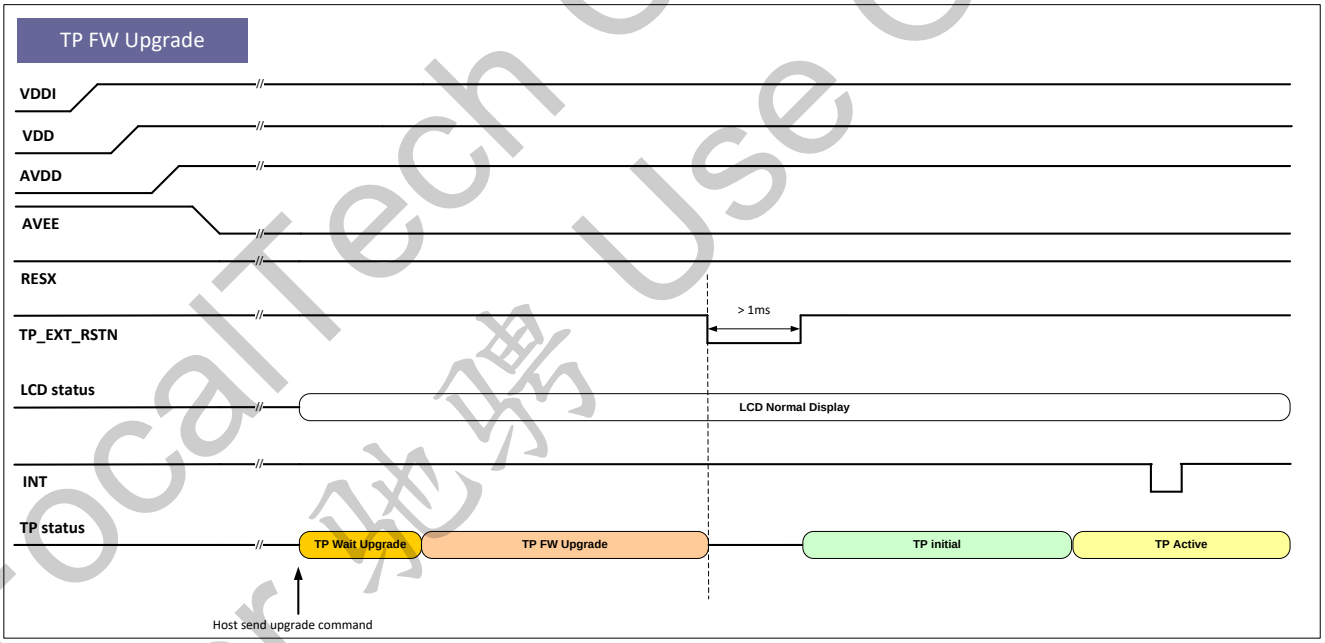
4 Power mode Power on/off sequence(Only VDDI keep)



4 Power mode LPWG sequence(VDD is exist)



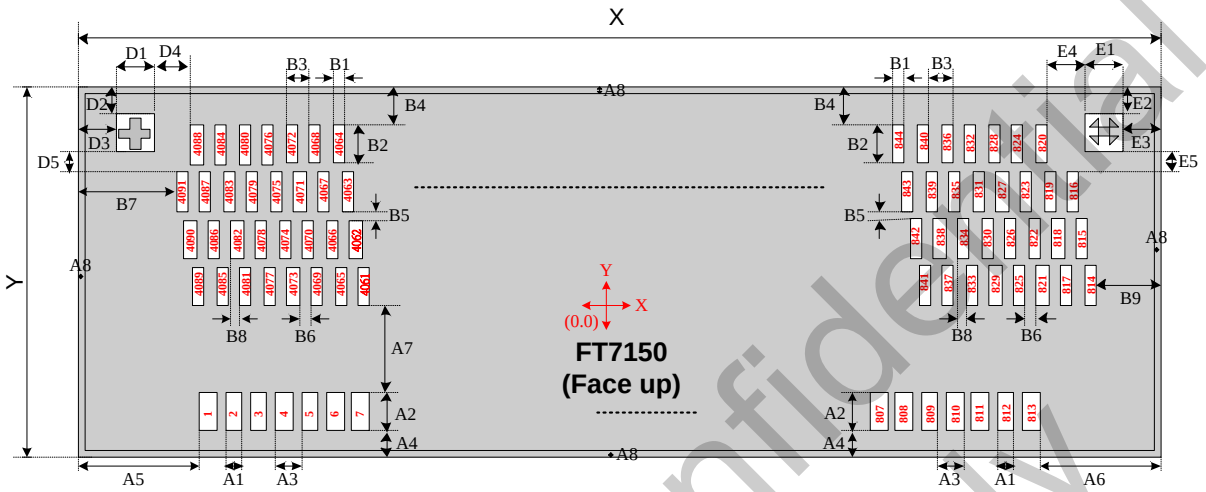
4 Power mode LPWG sequence(VDD is not exist)



4 Power mode TP FW Upgrade

8 CHIP INFORMATION

8.1 PAD Assignment



Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size
A1	24	B1	15	D1	115	E1	115
A2	100	B2	100	D2	48.2	E2	48.2
A3	39	B3	38.8	D3	113.1	E3	113.1
A4	75	B4	83.2	D4	30.35	E4	78.85
A5	288.5	B5	20	D5	40	E5	40
A6	299.5	B6	23.8				
A7	402	B7	229.35			X	32280
A8	30	B8	9.7			Y	1120.2
		B9	239.05			Unit: um	

Note : Chip Size and Bump space including scribe line

8.2 PAD Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	--	32280	1120.2	um
Chip Thickness	--	TBD.		
Pad Pitch	1~813	39	--	
	814~4091	38.8	--	
Pad Size	1~813	24	100	
	814~4091	15	100	

Note1: Chip size included scribe line

8.3 PAD Locations

No.	PAD Name	X	Y
1	GOUT_L[1]	-15839.5	-435.1
2	GOUT_L[2]	-15800.5	-435.1
3	GOUT_L[3]	-15761.5	-435.1
4	GOUT_L[4]	-15722.5	-435.1
5	GOUT_L[5]	-15683.5	-435.1
6	GOUT_L[6]	-15644.5	-435.1
7	GOUT_L[7]	-15605.5	-435.1
8	GOUT_L[8]	-15566.5	-435.1
9	GOUT_L[9]	-15527.5	-435.1
10	GOUT_L[10]	-15488.5	-435.1
11	GOUT_L[11]	-15449.5	-435.1
12	GOUT_L[12]	-15410.5	-435.1
13	GOUT_L[13]	-15371.5	-435.1
14	GOUT_L[14]	-15332.5	-435.1
15	GOUT_L[15]	-15293.5	-435.1
16	GOUT_L[16]	-15254.5	-435.1
17	GOUT_L[17]	-15215.5	-435.1
18	GOUT_L[18]	-15176.5	-435.1
19	GOUT_L[19]	-15137.5	-435.1
20	GOUT_L[20]	-15098.5	-435.1
21	GOUT_L[21]	-15059.5	-435.1
22	GOUT_L[22]	-15020.5	-435.1
23	SYNC_CTRL_L[0]	-14981.5	-435.1
24	SYNC_CTRL_L[1]	-14942.5	-435.1
25	SYNC_CTRL_L[2]	-14903.5	-435.1
26	SYNC_CTRL_L[3]	-14864.5	-435.1
27	SYNC_CTRL_L[4]	-14825.5	-435.1
28	SYNC_CTRL_L[5]	-14786.5	-435.1
29	SYNC_CTRL_L[6]	-14747.5	-435.1
30	SYNC_CTRL_L[7]	-14708.5	-435.1
31	SYNC_DAT_L[0]	-14669.5	-435.1
32	SYNC_DAT_L[1]	-14630.5	-435.1
33	SYNC_DAT_L[2]	-14591.5	-435.1
34	SYNC_DAT_L[3]	-14552.5	-435.1
35	SYNC_DAT_L[4]	-14513.5	-435.1
36	SYNC_DAT_L[5]	-14474.5	-435.1
37	SYNC_DAT_L[6]	-14435.5	-435.1
38	SYNC_DAT_L[7]	-14396.5	-435.1
39	VSS	-14357.5	-435.1
40	VSS	-14318.5	-435.1
41	VDDI	-14279.5	-435.1
42	VDDI	-14240.5	-435.1
43	TP_CASCADE_L[0]	-14201.5	-435.1
44	TP_CASCADE_L[0]	-14162.5	-435.1
45	TP_CASCADE_L[1]	-14123.5	-435.1
46	TP_CASCADE_L[2]	-14084.5	-435.1
47	TP_CASCADE_L[3]	-14045.5	-435.1
48	TP_CASCADE_L[4]	-14006.5	-435.1
49	TP_CASCADE_L[5]	-13967.5	-435.1
50	TP_CASCADE_L[6]	-13928.5	-435.1
51	TP_CASCADE_L[7]	-13889.5	-435.1
52	TP_CASCADE_L[7]	-13850.5	-435.1
53	TP_CASCADE_L[8]	-13811.5	-435.1
54	TP_CASCADE_L[8]	-13772.5	-435.1
55	TP_CASCADE_L[9]	-13733.5	-435.1
56	TP_CASCADE_L[9]	-13694.5	-435.1
57	TP_CASCADE_L[10]	-13655.5	-435.1
58	TP_CASCADE_L[10]	-13616.5	-435.1
59	TP_CASCADE_L[11]	-13577.5	-435.1
60	TP_CASCADE_L[11]	-13538.5	-435.1
61	TP_CASCADE_L[12]	-13499.5	-435.1
62	TP_CASCADE_L[12]	-13460.5	-435.1
63	TP_CASCADE_L[13]	-13421.5	-435.1
64	TP_CASCADE_L[13]	-13382.5	-435.1
65	TP_CASCADE_L[14]	-13343.5	-435.1
66	TP_CASCADE_L[14]	-13304.5	-435.1
67	DCHG2	-13265.5	-435.1
68	DCHG1	-13226.5	-435.1
69	VGLO_L	-13187.5	-435.1
70	VGLO_L	-13148.5	-435.1
71	VGLO_L	-13109.5	-435.1
72	VGH2_L	-13070.5	-435.1
73	VGH1_L	-13031.5	-435.1
74	VGH1_L	-12992.5	-435.1
75	VGH1_L	-12953.5	-435.1
76	AFE_TEST_L[0]	-12914.5	-435.1
77	AFE_TEST_L[1]	-12875.5	-435.1
78	AVSS	-12836.5	-435.1
79	AVSS	-12797.5	-435.1
80	AVSS	-12758.5	-435.1
81	AVSS	-12719.5	-435.1
82	AVSS	-12680.5	-435.1
83	AVSS	-12641.5	-435.1
84	AVSS	-12602.5	-435.1
85	AVSS	-12563.5	-435.1
86	AVSS	-12524.5	-435.1
87	AVSS	-12485.5	-435.1
88	AVSS	-12446.5	-435.1
89	AVSS	-12407.5	-435.1
90	AVSS	-12368.5	-435.1
91	AVDD	-12329.5	-435.1
92	AVDD	-12290.5	-435.1
93	AVDD	-12251.5	-435.1
94	AVDD	-12212.5	-435.1
95	AVDD	-12173.5	-435.1
96	AVDD	-12134.5	-435.1
97	AVDD	-12095.5	-435.1
98	VDD5_L	-12056.5	-435.1
99	VDD5_L	-12017.5	-435.1
100	VDD5_L	-11978.5	-435.1
101	VREF_TP_L	-11939.5	-435.1
102	VREF_TP_L	-11900.5	-435.1
103	VREF_TP_L	-11861.5	-435.1
104	VREF_TP_L	-11822.5	-435.1
105	VREF_TP_L	-11783.5	-435.1
106	AVEE	-11744.5	-435.1
107	AVEE	-11705.5	-435.1
108	AVEE	-11666.5	-435.1
109	AVEE	-11627.5	-435.1
110	AVEE	-11588.5	-435.1
111	AVEE	-11549.5	-435.1
112	VCOM_PASS_L	-11510.5	-435.1
113	VCOM_PASS_L	-11471.5	-435.1
114	VCOM_PASS_L	-11432.5	-435.1
115	VCOM_PASS_L	-11393.5	-435.1
116	VGHO_L	-11354.5	-435.1
117	VGHO_L	-11315.5	-435.1
118	VGHO_L	-11276.5	-435.1
119	VGHO_L	-11237.5	-435.1
120	VGHO_L	-11198.5	-435.1
121	VGHO_L	-11159.5	-435.1
122	VCOM_OPT0	-11120.5	-435.1
123	VCOM_OPT0	-11081.5	-435.1
124	VCOM_OPT0	-11042.5	-435.1
125	VCOM_OPT0	-11003.5	-435.1
126	VCOM_OPT0	-10964.5	-435.1
127	VCOM_OPT0	-10925.5	-435.1
128	VCOM_OPT0	-10886.5	-435.1
129	VCOM_OPT0	-10847.5	-435.1
130	VGHO_L	-10808.5	-435.1
131	VGHO_L	-10769.5	-435.1
132	VGHO_L	-10730.5	-435.1
133	VGHO_L	-10691.5	-435.1
134	VGHO_L	-10652.5	-435.1
135	VGHO_L	-10613.5	-435.1
136	VGHO1B	-10574.5	-435.1
137	VGHO1B	-10535.5	-435.1
138	VGHO1B	-10496.5	-435.1
139	VGHO1B	-10457.5	-435.1
140	VGHO1B	-10418.5	-435.1
141	VGHO1B	-10379.5	-435.1
142	VDDI	-10340.5	-435.1
143	VDDI	-10301.5	-435.1
144	VDD_TP	-10262.5	-435.1
145	VDD_TP	-10223.5	-435.1
146	VDD_TP	-10184.5	-435.1
147	VDD_TP	-10145.5	-435.1
148	VDD_TP	-10106.5	-435.1
149	VDD_TP	-10067.5	-435.1
150	VCOM	-10028.5	-435.1
151	VCOM	-9989.5	-435.1
152	VCOM	-9950.5	-435.1
153	VCOM	-9911.5	-435.1
154	VCOM	-9872.5	-435.1
155	VCOM	-9833.5	-435.1
156	VSS	-9794.5	-435.1
157	VSS	-9755.5	-435.1
158	VSS	-9716.5	-435.1
159	VSS	-9677.5	-435.1
160	VSS	-9638.5	-435.1
161	VSS	-9599.5	-435.1
162	VGL	-9560.5	-435.1
163	VGL	-9521.5	-435.1
164	VGL	-9482.5	-435.1
165	VGL	-9443.5	-435.1
166	VGL	-9404.5	-435.1
167	VGL	-9365.5	-435.1
168	VGH_L	-9326.5	-435.1
169	VGH_L	-9287.5	-435.1
170	VGH_L	-9248.5	-435.1
171	VGH_L	-9209.5	-435.1
172	VGH_L	-9170.5	-435.1
173	VGH_L	-9131.5	-435.1
174	C21P	-9092.5	-435.1
175	C21P	-9053.5	-435.1
176	C21P	-9014.5	-435.1
177	C21P	-8975.5	-435.1
178	C21P	-8936.5	-435.1
179	C21P	-8897.5	-435.1
180	C21N	-8858.5	-435.1
181	C21N	-8819.5	-435.1
182	C21N	-8780.5	-435.1
183	C21N	-8741.5	-435.1
184	C21N	-8702.5	-435.1
185	C21N	-8663.5	-435.1
186	AVDD	-8624.5	-435.1
187	AVDD	-8585.5	-435.1
188	AVDD	-8546.5	-435.1
189	AVDD	-8507.5	-435.1
190	AVDD	-8468.5	-435.1
191	AVDD	-8429.5	-435.1
192	AVEE	-8390.5	-435.1
193	AVEE	-8351.5	-435.1
194	AVEE	-8312.5	-435.1
195	AVEE	-8273.5	-435.1
196	AVEE	-8234.5	-435.1
197	AVEE	-8195.5	-435.1
198	AVSS	-8156.5	-435.1
199	AVSS	-8117.5	-435.1
200	AVSS	-8078.5	-435.1
201	AVSS	-8039.5	-435.1
202	AVSS	-8000.5	-435.1
203	AVSS	-7961.5	-435.1
204	C22P	-7922.5	-435.1
205	C22P	-7883.5	-435.1
206	C22P	-7844.5	-435.1
207	C22P	-7805.5	-435.1
208	C22P	-7766.5	-435.1
209	C22P	-7727.5	-435.1
210	C22N	-7688.5	-435.1
211	C22N	-7649.5	-435.1
212	C22N	-7610.5	-435.1
213	C22N	-7571.5	-435.1
214	C22N	-7532.5	-435.1
215	AVDD	-7493.5	-435.1
216	AVDD	-7454.5	-435.1
217	AVDD	-7415.5	-435.1
218	AVDD	-7376.5	-435.1
219	AVDD	-7337.5	-435.1
220	AVDD	-7298.5	-435.1
221	AVEE	-7259.5	-435.1
222	AVEE	-7220.5	-435.1
223	AVEE	-7181.5	-435.1
224	AVEE	-7142.5	-435.1
225	AVEE	-7103.5	-435.1
226	AVEE	-7064.5	-435.1
227	AVSS	-7025.5	-435.1
228	AVSS	-6986.5	-435.1
229	AVSS	-6947.5	-435.1
230	AVSS	-6908.5	-435.1
231	AVSS	-6869.5	-435.1
232	AVSS	-6830.5	-435.1
233	VGHB	-6791.5	-435.1
234	VGHB	-6752.5	-435.1
235	VGHB	-6713.5	-435.1
236	VGHB	-6674.5	-435.1
237	VGHB	-6635.5	-435.1
238	VSS	-6596.5	-435.1
239	VSS	-6557.5	-435.1
240	VSS	-6518.5	-435.1
241	VSS	-6479.5	-435.1
242	VSS	-6440.5	-435.1
243	VSS	-6401.5	-435.1
244	VDD_TP	-6362.5	-435.1
245	VDD_TP	-6323.5	-435.1
246	VDD_TP	-6284.5	-435.1

No.	PAD Name	X	Y
247	VDD_TP	-6245.5	-435.1
248	VDD_TP	-6206.5	-435.1
249	VDD_TP	-6167.5	-435.1
250	VDDI	-6128.5	-435.1
251	VDDI	-6089.5	-435.1
252	VDDI	-6050.5	-435.1
253	VDDI	-6011.5	-435.1
254	VDDI	-5972.5	-435.1
255	VDDI	-5933.5	-435.1
256	VDDI	-5894.5	-435.1
257	VDDI	-5855.5	-435.1
258	VDDI	-5816.5	-435.1
259	VDDI	-5777.5	-435.1
260	VDD	-5738.5	-435.1
261	VDD	-5699.5	-435.1
262	VDD	-5660.5	-435.1
263	VDD	-5621.5	-435.1
264	VDD	-5582.5	-435.1
265	VDD	-5543.5	-435.1
266	VSS	-5504.5	-435.1
267	VSS	-5465.5	-435.1
268	VSS	-5426.5	-435.1
269	VSS	-5387.5	-435.1
270	VSS	-5348.5	-435.1
271	VSS	-5309.5	-435.1
272	LVDSVDD	-5270.5	-435.1
273	LVDSVDD	-5231.5	-435.1
274	LVDSVDD	-5192.5	-435.1
275	VDDAM	-5153.5	-435.1
276	VDDAM	-5114.5	-435.1
277	VDDAM	-5075.5	-435.1
278	VDDAM	-5036.5	-435.1
279	LVDSVDD	-4997.5	-435.1
280	LVDSVDD	-4958.5	-435.1
281	LVDSVDD	-4919.5	-435.1
282	LVDSVSS	-4880.5	-435.1
283	LVDSVSS	-4841.5	-435.1
284	LVDSVSS	-4802.5	-435.1
285	DATA2P	-4763.5	-435.1
286	DATA2P	-4724.5	-435.1
287	DATA2P	-4685.5	-435.1
288	DATA2P	-4646.5	-435.1
289	DATA2P	-4607.5	-435.1
290	DUMMYPHY2	-4568.5	-435.1
291	DUMMYPHY2	-4529.5	-435.1
292	DATA2N	-4490.5	-435.1
293	DATA2N	-4451.5	-435.1
294	DATA2N	-4412.5	-435.1
295	DATA2N	-4373.5	-435.1
296	DATA2N	-4334.5	-435.1
297	LVDSVSS	-4295.5	-435.1
298	LVDSVSS	-4256.5	-435.1
299	DATA1P	-4217.5	-435.1
300	DATA1P	-4178.5	-435.1
301	DATA1P	-4139.5	-435.1
302	DATA1P	-4100.5	-435.1
303	DATA1P	-4061.5	-435.1
304	DUMMYPHY1	-4022.5	-435.1
305	DUMMYPHY1	-3983.5	-435.1
306	DATA1N	-3944.5	-435.1
307	DATA1N	-3905.5	-435.1
308	DATA1N	-3866.5	-435.1
309	DATA1N	-3827.5	-435.1
310	DATA1N	-3788.5	-435.1
311	LVDSVSS	-3749.5	-435.1
312	LVDSVSS	-3710.5	-435.1
313	CLKP	-3671.5	-435.1
314	CLKP	-3632.5	-435.1
315	CLKP	-3593.5	-435.1
316	CLKP	-3554.5	-435.1
317	CLKP	-3515.5	-435.1
318	DUMMYPHYCK	-3476.5	-435.1
319	DUMMYPHYCK	-3437.5	-435.1
320	CLKN	-3398.5	-435.1
321	CLKN	-3359.5	-435.1
322	CLKN	-3320.5	-435.1
323	CLKN	-3281.5	-435.1
324	CLKN	-3242.5	-435.1
325	LVDSVSS	-3203.5	-435.1
326	LVDSVSS	-3164.5	-435.1
327	DATA0P	-3125.5	-435.1
328	DATA0P	-3086.5	-435.1
329	DATA0P	-3047.5	-435.1
330	DATA0P	-3008.5	-435.1
331	DATA0P	-2969.5	-435.1
332	DUMMYPHY0	-2930.5	-435.1
333	DUMMYPHY0	-2891.5	-435.1
334	DATA0N	-2852.5	-435.1
335	DATA0N	-2813.5	-435.1
336	DATA0N	-2774.5	-435.1
337	DATA0N	-2735.5	-435.1
338	DATA0N	-2696.5	-435.1
339	LVDSVSS	-2657.5	-435.1
340	LVDSVSS	-2618.5	-435.1
341	DATA3P	-2579.5	-435.1
342	DATA3P	-2540.5	-435.1
343	DATA3P	-2501.5	-435.1
344	DATA3P	-2462.5	-435.1
345	DATA3P	-2423.5	-435.1
346	DUMMYPHY3	-2384.5	-435.1
347	DUMMYPHY3	-2345.5	-435.1
348	DATA3N	-2306.5	-435.1
349	DATA3N	-2267.5	-435.1
350	DATA3N	-2228.5	-435.1
351	DATA3N	-2189.5	-435.1
352	DATA3N	-2150.5	-435.1
353	LVDSVSS	-2111.5	-435.1
354	LVDSVSS	-2072.5	-435.1
355	LVDSVSS	-2033.5	-435.1
356	LVDSVDD	-1994.5	-435.1
357	LVDSVDD	-1955.5	-435.1
358	LVDSVDD	-1916.5	-435.1
359	VSS	-1877.5	-435.1
360	VSS	-1838.5	-435.1
361	VSS	-1799.5	-435.1
362	VSS	-1760.5	-435.1
363	VDD	-1721.5	-435.1
364	VDD	-1682.5	-435.1
365	VDD	-1643.5	-435.1
366	VDD	-1604.5	-435.1
367	VDD	-1565.5	-435.1
368	VDD	-1526.5	-435.1
369	VDDI	-1487.5	-435.1
370	VDDI	-1448.5	-435.1
371	VDDI	-1409.5	-435.1
372	VDDI	-1370.5	-435.1
373	VDDI	-1331.5	-435.1
374	VDDI	-1292.5	-435.1
375	VDD_TP	-1253.5	-435.1
376	VDD_TP	-1214.5	-435.1
377	VDD_TP	-1175.5	-435.1
378	VDD_TP	-1136.5	-435.1
379	VDD_TP	-1097.5	-435.1
380	VDD_TP	-1058.5	-435.1
381	AVSS	-1019.5	-435.1
382	AVSS	-980.5	-435.1
383	AVSS	-941.5	-435.1
384	AVSS	-902.5	-435.1
385	AVSS	-863.5	-435.1
386	AVSS	-824.5	-435.1
387	AVDD	-785.5	-435.1
388	AVDD	-746.5	-435.1
389	AVDD	-707.5	-435.1
390	AVDD	-668.5	-435.1
391	AVDD	-629.5	-435.1
392	AVDD	-590.5	-435.1
393	AVEE	-551.5	-435.1
394	AVEE	-512.5	-435.1
395	AVEE	-473.5	-435.1
396	AVEE	-434.5	-435.1
397	AVEE	-395.5	-435.1
398	AVEE	-356.5	-435.1
399	DUMMYB[1]	-317.5	-435.1
400	VDD	-278.5	-435.1
401	VDD	-239.5	-435.1
402	VDD	-200.5	-435.1
403	VDD	-161.5	-435.1
404	VDD	-122.5	-435.1
405	VDD	-83.5	-435.1
406	VDD	-44.5	-435.1
407	DUMMYB[2]	-5.5	-435.1
408	DUMMYB[3]	33.5	-435.1
409	DUMMYB[4]	72.5	-435.1
410	DUMMYB[5]	111.5	-435.1
411	DUMMYB[6]	150.5	-435.1
412	DUMMYB[7]	189.5	-435.1
413	DUMMYB[8]	228.5	-435.1
414	DUMMYB[9]	267.5	-435.1
415	DUMMYB[10]	306.5	-435.1
416	DUMMYB[11]	345.5	-435.1
417	DUMMYB[12]	384.5	-435.1
418	DUMMYB[13]	423.5	-435.1
419	EMR_GPIO[0]	462.5	-435.1
420	EMR_GPIO[1]	501.5	-435.1
421	EMR_GPIO[2]	540.5	-435.1
422	LCD_GPIO[2]	579.5	-435.1
423	EXT_LV	618.5	-435.1
424	EXT_LV	657.5	-435.1
425	IM	696.5	-435.1
426	TEST[0]	735.5	-435.1
427	TEST[1]	774.5	-435.1
428	TEST[2]	813.5	-435.1
429	TEST[3]	852.5	-435.1
430	TEST[4]	891.5	-435.1
431	TEST[5]	930.5	-435.1
432	TEST[6]	969.5	-435.1
433	TEST[7]	1008.5	-435.1
434	TEST[8]	1047.5	-435.1
435	VSS	1086.5	-435.1
436	VSS	1125.5	-435.1
437	VDDI	1164.5	-435.1
438	VDDI	1203.5	-435.1
439	TEST[9]	1242.5	-435.1
440	TEST[10]	1281.5	-435.1
441	TEST[11]	1320.5	-435.1
442	TEST[12]	1359.5	-435.1
443	TEST[13]	1398.5	-435.1
444	TEST[14]	1437.5	-435.1
445	TEST[15]	1476.5	-435.1
446	TEST[16]	1515.5	-435.1
447	LCD_EXT_OSC	1554.5	-435.1
448	LCD_EXT_OSC	1593.5	-435.1
449	LCD_EXT_OSC	1632.5	-435.1
450	LCD_SCL	1671.5	-435.1
451	LCD_SCL	1710.5	-435.1
452	LCD_SDA	1749.5	-435.1
453	LCD_SDA	1788.5	-435.1
454	LCD_GPIO[0]	1827.5	-435.1
455	LCD_GPIO[0]	1866.5	-435.1
456	LCD_GPIO[1]	1905.5	-435.1
457	LCD_GPIO[1]	1944.5	-435.1
458	FCS	1983.5	-435.1
459	FCS	2022.5	-435.1
460	PON	2061.5	-435.1
461	PON	2100.5	-435.1
462	TP_GPIO[0]	2139.5	-435.1
463	TP_GPIO[0]	2178.5	-435.1
464	TP_GPIO[1]	2217.5	-435.1
465	TP_GPIO[1]	2256.5	-435.1
466	BIST_EN	2295.5	-435.1
467	DSWAP[0]	2334.5	-435.1
468	DSWAP[1]	2373.5	-435.1
469	PNSWAP	2412.5	-435.1
470	LANSEL[0]	2451.5	-435.1
471	LANSEL[1]	2490.5	-435.1
472	TP_MS	2529.5	-435.1
473	EN_EXT_VCOM	2568.5	-435.1
474	RESX	2607.5	-435.1
475	ENB_CASCADE	2646.5	-435.1
476	VDDI	2685.5	-435.1
477	VDDI	2724.5	-435.1
478	VSS	2763.5	-435.1
479	VSS	2802.5	-435.1
480	VDDI	2841.5	-435.1
481	VDDI	2880.5	-435.1
482	TP_AFE_SCAN_MODE	2919.5	-435.1
483	POR12_T	2958.5	-435.1
484	POR18_T	2997.5	-435.1
485	TP_BOOTDEVICE	3036.5	-435.1
486	TP_WAKE	3075.5	-435.1
487	TP_EXT_RSTN	3114.5	-435.1
488	TP_SCL	3153.5	-435.1
489	TP_SDA	3192.5	-435.1
490	TP_INT	3231.5	-435.1
491	TP_HOLD	3270.5	-435.1
492	TP_WP	3309.5	-435.1
493	TP_CS	3348.5	-435.1
494	TP_SCLK	3387.5	-435.1

No.	PAD Name	X	Y
495	TP_SCLK	3426.5	-435.1
496	TP_MOSI	3465.5	-435.1
497	TP_MOSI	3504.5	-435.1
498	TP_MISO	3543.5	-435.1
499	TP_MISO	3582.5	-435.1
500	DISP	3621.5	-435.1
501	DISP	3660.5	-435.1
502	RL	3699.5	-435.1
503	RL	3738.5	-435.1
504	VSS	3777.5	-435.1
505	VSS	3816.5	-435.1
506	VSS	3855.5	-435.1
507	VSS	3894.5	-435.1
508	VSS	3933.5	-435.1
509	VSS	3972.5	-435.1
510	VDD	4011.5	-435.1
511	VDD	4050.5	-435.1
512	VDD	4089.5	-435.1
513	VDD	4128.5	-435.1
514	VDD	4167.5	-435.1
515	VDD	4206.5	-435.1
516	VDDI	4245.5	-435.1
517	VDDI	4284.5	-435.1
518	VDDI	4323.5	-435.1
519	VDDI	4362.5	-435.1
520	VDDI	4401.5	-435.1
521	VDDI	4440.5	-435.1
522	VDD_TP	4479.5	-435.1
523	VDD_TP	4518.5	-435.1
524	VDD_TP	4557.5	-435.1
525	VDD_TP	4596.5	-435.1
526	VDD_TP	4635.5	-435.1
527	VDD_TP	4674.5	-435.1
528	VDD_TP	4713.5	-435.1
529	VCOM	4752.5	-435.1
530	VCOM	4791.5	-435.1
531	VCOM	4830.5	-435.1
532	VCOM	4869.5	-435.1
533	VCOM	4908.5	-435.1
534	VCOM	4947.5	-435.1
535	VCOM	4986.5	-435.1
536	VCOM	5025.5	-435.1
537	VCOM	5064.5	-435.1
538	VCOM	5103.5	-435.1
539	VCOM	5142.5	-435.1
540	VCOM	5181.5	-435.1
541	VCOM	5220.5	-435.1
542	VCL	5259.5	-435.1
543	VCL	5298.5	-435.1
544	VCL	5337.5	-435.1
545	VCL	5376.5	-435.1
546	VCL	5415.5	-435.1
547	VCL	5454.5	-435.1
548	VCL	5493.5	-435.1
549	AVSSR	5532.5	-435.1
550	AVSSR	5571.5	-435.1
551	AVSSR	5610.5	-435.1
552	AVSSR	5649.5	-435.1
553	AVSSR	5688.5	-435.1
554	AVSSR	5727.5	-435.1
555	AVSSR	5766.5	-435.1
556	AVSSR	5805.5	-435.1
557	AVSSR	5844.5	-435.1
558	AVSSR	5883.5	-435.1
559	AVEER	5922.5	-435.1
560	AVEER	5961.5	-435.1
561	AVEER	6000.5	-435.1
562	AVEER	6039.5	-435.1
563	AVEER	6078.5	-435.1
564	VREF_PAD	6117.5	-435.1
565	VREF_PAD	6156.5	-435.1
566	VREF_PAD	6195.5	-435.1
567	GVDD_PAD	6234.5	-435.1
568	GVDD_PAD	6273.5	-435.1
569	GVDD_PAD	6312.5	-435.1
570	NGVDD_PAD	6351.5	-435.1
571	NGVDD_PAD	6390.5	-435.1
572	NGVDD_PAD	6429.5	-435.1
573	AVDDR	6468.5	-435.1
574	AVDDR	6507.5	-435.1
575	AVDDR	6546.5	-435.1
576	AVDDR	6585.5	-435.1
577	AVDDR	6624.5	-435.1
578	AVDDR	6663.5	-435.1
579	VDDI	6702.5	-435.1
580	VDDI	6741.5	-435.1
581	VDDI	6780.5	-435.1
582	VDDI	6819.5	-435.1
583	VDDI	6858.5	-435.1
584	VDDI	6897.5	-435.1
585	VDDI	6936.5	-435.1
586	VDDI	6975.5	-435.1
587	VDDI	7014.5	-435.1
588	VDDI	7053.5	-435.1
589	VDDI	7092.5	-435.1
590	VDDI	7131.5	-435.1
591	VDD_TP	7170.5	-435.1
592	VDD_TP	7209.5	-435.1
593	VDD_TP	7248.5	-435.1
594	VDD_TP	7287.5	-435.1
595	VDD_TP	7326.5	-435.1
596	VDD_TP	7365.5	-435.1
597	VSS	7404.5	-435.1
598	VSS	7443.5	-435.1
599	VSS	7482.5	-435.1
600	VSS	7521.5	-435.1
601	VSS	7560.5	-435.1
602	VSS	7599.5	-435.1
603	VREF_TP	7638.5	-435.1
604	VREF_TP	7677.5	-435.1
605	VREF_TP	7716.5	-435.1
606	VREF_TP	7755.5	-435.1
607	VREF_TP	7794.5	-435.1
608	VREF_TP	7833.5	-435.1
609	AVDD	7872.5	-435.1
610	AVDD	7911.5	-435.1
611	AVDD	7950.5	-435.1
612	AVDD	7989.5	-435.1
613	AVDD	8028.5	-435.1
614	AVDD	8067.5	-435.1
615	AVSS	8106.5	-435.1
616	AVSS	8145.5	-435.1
617	AVSS	8184.5	-435.1
618	AVSS	8223.5	-435.1
619	AVSS	8262.5	-435.1
620	AVSS	8301.5	-435.1
621	AVSS	8340.5	-435.1
622	AVSS	8379.5	-435.1
623	AVEE	8418.5	-435.1
624	AVEE	8457.5	-435.1
625	AVEE	8496.5	-435.1
626	AVEE	8535.5	-435.1
627	AVEE	8574.5	-435.1
628	AVEE	8613.5	-435.1
629	C31P	8652.5	-435.1
630	C31P	8691.5	-435.1
631	C31P	8730.5	-435.1
632	C31P	8769.5	-435.1
633	C31P	8808.5	-435.1
634	C31P	8847.5	-435.1
635	C31N	8886.5	-435.1
636	C31N	8925.5	-435.1
637	C31N	8964.5	-435.1
638	C31N	9003.5	-435.1
639	C31N	9042.5	-435.1
640	C31N	9081.5	-435.1
641	VGL	9120.5	-435.1
642	VGL	9159.5	-435.1
643	VGL	9198.5	-435.1
644	VGL	9237.5	-435.1
645	VGL	9276.5	-435.1
646	VGL	9315.5	-435.1
647	VGH_R	9354.5	-435.1
648	VGH_R	9393.5	-435.1
649	VGH_R	9432.5	-435.1
650	VGH_R	9471.5	-435.1
651	VGH_R	9510.5	-435.1
652	VGH_R	9549.5	-435.1
653	AVSS	9588.5	-435.1
654	AVSS	9627.5	-435.1
655	AVSS	9666.5	-435.1
656	AVSS	9705.5	-435.1
657	AVSS	9744.5	-435.1
658	AVSS	9783.5	-435.1
659	VCOM	9822.5	-435.1
660	VCOM	9861.5	-435.1
661	VCOM	9900.5	-435.1
662	VCOM	9939.5	-435.1
663	VCOM	9978.5	-435.1
664	VCOM	10017.5	-435.1
665	AVSS	10056.5	-435.1
666	AVSS	10095.5	-435.1
667	AVSS	10134.5	-435.1
668	AVSS	10173.5	-435.1
669	AVSS	10212.5	-435.1
670	VGLO1B	10251.5	-435.1
671	VGLO1B	10290.5	-435.1
672	VGLO1B	10329.5	-435.1
673	VGLO1B	10368.5	-435.1
674	VGLO1B	10407.5	-435.1
675	VGLO1B	10446.5	-435.1
676	VGLO_R	10485.5	-435.1
677	VGLO_R	10524.5	-435.1
678	VGLO_R	10563.5	-435.1
679	VGLO_R	10602.5	-435.1
680	VGLO_R	10641.5	-435.1
681	VGLO_R	10680.5	-435.1
682	VCOM_OPT1	10719.5	-435.1
683	VCOM_OPT1	10758.5	-435.1
684	VCOM_OPT1	10797.5	-435.1
685	VCOM_OPT1	10836.5	-435.1
686	VCOM_OPT1	10875.5	-435.1
687	VCOM_OPT1	10914.5	-435.1
688	VCOM_OPT1	10953.5	-435.1
689	VCOM_OPT1	10992.5	-435.1
690	VGLO	11031.5	-435.1
691	VGLO	11070.5	-435.1
692	VGLO	11109.5	-435.1
693	VGLO	11148.5	-435.1
694	VGLO	11187.5	-435.1
695	VGLO	11226.5	-435.1
696	VCOM_FB	11265.5	-435.1
697	VCOM_FB	11304.5	-435.1
698	VCOM_FB	11343.5	-435.1
699	VCOM_PASS_R	11382.5	-435.1
700	VCOM_PASS_R	11421.5	-435.1
701	VCOM_PASS_R	11460.5	-435.1
702	VCOM_PASS_R	11499.5	-435.1
703	AVEE	11538.5	-435.1
704	AVEE	11577.5	-435.1
705	AVEE	11616.5	-435.1
706	AVEE	11655.5	-435.1
707	AVEE	11694.5	-435.1
708	AVEE	11733.5	-435.1
709	VREF_TP_R	11772.5	-435.1
710	VREF_TP_R	11811.5	-435.1
711	VREF_TP_R	11850.5	-435.1
712	VREF_TP_R	11889.5	-435.1
713	VREF_TP_R	11928.5	-435.1
714	VDD5_R	11967.5	-435.1
715	VDD5_R	12006.5	-435.1
716	VDD5_R	12045.5	-435.1
717	AVDD	12084.5	-435.1
718	AVDD	12123.5	-435.1
719	AVDD	12162.5	-435.1
720	AVDD	12201.5	-435.1
721	AVDD	12240.5	-435.1
722	AVDD	12279.5	-435.1
723	AVDD	12318.5	-435.1
724	AVSS	12357.5	-435.1
725	AVSS	12396.5	-435.1
726	AVSS	12435.5	-435.1
727	AVSS	12474.5	-435.1
728	AVSS	12513.5	-435.1
729	AVSS	12552.5	-435.1
730	AVSS	12591.5	-435.1
731	AVSS	12630.5	-435.1
732	AVSS	12669.5	-435.1
733	AVSS	12708.5	-435.1
734	AVSS	12747.5	-435.1

No.	PAD Name	X	Y
735	AVSS	12786.5	-435.1
736	AVSS	12825.5	-435.1
737	AFE_TEST_R[1]	12864.5	-435.1
738	AFE_TEST_R[0]	12903.5	-435.1
739	VGH1_R	12942.5	-435.1
740	VGH1_R	12981.5	-435.1
741	VGH1_R	13020.5	-435.1
742	VGH2_R	13059.5	-435.1
743	VGHO_R	13098.5	-435.1
744	VGHO_R	13137.5	-435.1
745	VGHO_R	13176.5	-435.1
746	AVSS	13215.5	-435.1
747	AVSS	13254.5	-435.1
748	TP_CASCADE_R[14]	13293.5	-435.1
749	TP_CASCADE_R[14]	13332.5	-435.1
750	TP_CASCADE_R[13]	13371.5	-435.1
751	TP_CASCADE_R[13]	13410.5	-435.1
752	TP_CASCADE_R[12]	13449.5	-435.1
753	TP_CASCADE_R[12]	13488.5	-435.1
754	TP_CASCADE_R[11]	13527.5	-435.1
755	TP_CASCADE_R[11]	13566.5	-435.1
756	TP_CASCADE_R[10]	13605.5	-435.1
757	TP_CASCADE_R[10]	13644.5	-435.1
758	TP_CASCADE_R[9]	13683.5	-435.1
759	TP_CASCADE_R[9]	13722.5	-435.1
760	TP_CASCADE_R[8]	13761.5	-435.1
761	TP_CASCADE_R[8]	13800.5	-435.1
762	TP_CASCADE_R[7]	13839.5	-435.1
763	TP_CASCADE_R[7]	13878.5	-435.1
764	TP_CASCADE_R[6]	13917.5	-435.1
765	TP_CASCADE_R[5]	13956.5	-435.1
766	TP_CASCADE_R[4]	13995.5	-435.1
767	TP_CASCADE_R[3]	14034.5	-435.1
768	TP_CASCADE_R[2]	14073.5	-435.1
769	TP_CASCADE_R[1]	14112.5	-435.1
770	TP_CASCADE_R[0]	14151.5	-435.1
771	TP_CASCADE_R[0]	14190.5	-435.1
772	VDDI	14229.5	-435.1
773	VDDI	14268.5	-435.1
774	VSS	14307.5	-435.1
775	VSS	14346.5	-435.1
776	SYNC_DAT_R[7]	14385.5	-435.1
777	SYNC_DAT_R[6]	14424.5	-435.1
778	SYNC_DAT_R[5]	14463.5	-435.1
779	SYNC_DAT_R[4]	14502.5	-435.1
780	SYNC_DAT_R[3]	14541.5	-435.1
781	SYNC_DAT_R[2]	14580.5	-435.1
782	SYNC_DAT_R[1]	14619.5	-435.1
783	SYNC_DAT_R[0]	14658.5	-435.1
784	SYNC_CTRL_R[7]	14697.5	-435.1
785	SYNC_CTRL_R[6]	14736.5	-435.1
786	SYNC_CTRL_R[5]	14775.5	-435.1
787	SYNC_CTRL_R[4]	14814.5	-435.1
788	SYNC_CTRL_R[3]	14853.5	-435.1
789	SYNC_CTRL_R[2]	14892.5	-435.1
790	SYNC_CTRL_R[1]	14931.5	-435.1
791	SYNC_CTRL_R[0]	14970.5	-435.1
792	GOUT_R[22]	15009.5	-435.1
793	GOUT_R[21]	15048.5	-435.1
794	GOUT_R[20]	15087.5	-435.1
795	GOUT_R[19]	15126.5	-435.1
796	GOUT_R[18]	15165.5	-435.1
797	GOUT_R[17]	15204.5	-435.1
798	GOUT_R[16]	15243.5	-435.1
799	GOUT_R[15]	15282.5	-435.1
800	GOUT_R[14]	15321.5	-435.1
801	GOUT_R[13]	15360.5	-435.1
802	GOUT_R[12]	15399.5	-435.1
803	GOUT_R[11]	15438.5	-435.1
804	GOUT_R[10]	15477.5	-435.1
805	GOUT_R[9]	15516.5	-435.1
806	GOUT_R[8]	15555.5	-435.1
807	GOUT_R[7]	15594.5	-435.1
808	GOUT_R[6]	15633.5	-435.1
809	GOUT_R[5]	15672.5	-435.1
810	GOUT_R[4]	15711.5	-435.1
811	GOUT_R[3]	15750.5	-435.1
812	GOUT_R[2]	15789.5	-435.1
813	GOUT_R[1]	15828.5	-435.1
814	DUMMY_OR[1]	15893.45	66.9
815	DUMMY_OR[2]	15883.75	186.9
816	DUMMY_OR[3]	15874.05	306.9
817	SYNC_GAM_R[0]	15854.65	66.9
818	SYNC_GAM_R[1]	15844.95	186.9
819	SYNC_GAM_R[2]	15835.25	306.9
820	DUMMY_OR[4]	15825.55	426.9
821	SYNC_GAM_R[3]	15815.85	66.9
822	SYNC_GAM_R[4]	15806.15	186.9
823	SYNC_GAM_R[5]	15796.45	306.9
824	DUMMY_OR[5]	15786.75	426.9
825	VCOM_PASS_R	15777.05	66.9
826	VCOM_PASS_R	15767.35	186.9
827	VCOM_PASS_R	15757.65	306.9
828	DUMMY_OR[6]	15747.95	426.9
829	VCOM_PASS_R	15738.25	66.9
830	VCOM_PASS_R	15728.55	186.9
831	VCOM_PASS_R	15718.85	306.9
832	DUMMY_OR[7]	15709.15	426.9
833	DUMMY_OR[8]	15699.45	66.9
834	DUMMY_OR[9]	15689.75	186.9
835	DUMMY_OR[10]	15680.05	306.9
836	DUMMY_OR[11]	15670.35	426.9
837	DUMMY_OR[12]	15660.65	66.9
838	SDUM[0]	15650.95	186.9
839	SDUM[1]	15641.25	306.9
840	SXDUM1	15631.55	426.9
841	S[1]	15621.85	66.9
842	S[2]	15612.15	186.9
843	S[3]	15602.45	306.9
844	RX[800]	15592.75	426.9
845	S[4]	15583.05	66.9
846	S[5]	15573.35	186.9
847	S[6]	15563.65	306.9
848	RX[799]	15553.95	426.9
849	S[7]	15544.25	66.9
850	S[8]	15534.55	186.9
851	S[9]	15524.85	306.9
852	RX[798]	15515.15	426.9
853	S[10]	15505.45	66.9
854	S[11]	15495.75	186.9
855	S[12]	15486.05	306.9
856	RX[797]	15476.35	426.9
857	S[13]	15466.65	66.9
858	S[14]	15456.95	186.9
859	S[15]	15447.25	306.9
860	RX[796]	15437.55	426.9
861	S[16]	15427.85	66.9
862	S[17]	15418.15	186.9
863	S[18]	15408.45	306.9
864	RX[795]	15398.75	426.9
865	S[19]	15389.05	66.9
866	S[20]	15379.35	186.9
867	S[21]	15369.65	306.9
868	RX[794]	15359.95	426.9
869	S[22]	15350.25	66.9
870	S[23]	15340.55	186.9
871	S[24]	15330.85	306.9
872	RX[793]	15321.15	426.9
873	S[25]	15311.45	66.9
874	S[26]	15301.75	186.9
875	S[27]	15292.05	306.9
876	RX[792]	15282.35	426.9
877	S[28]	15272.65	66.9
878	S[29]	15262.95	186.9
879	S[30]	15253.25	306.9
880	RX[791]	15243.55	426.9
881	S[31]	15233.85	66.9
882	S[32]	15224.15	186.9
883	S[33]	15214.45	306.9
884	RX[790]	15204.75	426.9
885	S[34]	15195.05	66.9
886	S[35]	15185.35	186.9
887	S[36]	15175.65	306.9
888	RX[789]	15165.95	426.9
889	S[37]	15156.25	66.9
890	S[38]	15146.55	186.9
891	S[39]	15136.85	306.9
892	RX[788]	15127.15	426.9
893	S[40]	15117.45	66.9
894	S[41]	15107.75	186.9
895	S[42]	15098.05	306.9
896	RX[787]	15088.35	426.9
897	S[43]	15078.65	66.9
898	S[44]	15068.95	186.9
899	S[45]	15059.25	306.9
900	RX[786]	15049.55	426.9
901	S[46]	15039.85	66.9
902	S[47]	15030.15	186.9
903	S[48]	15020.45	306.9
904	RX[785]	15010.75	426.9
905	S[49]	15001.05	66.9
906	S[50]	14991.35	186.9
907	S[51]	14981.65	306.9
908	RX[784]	14971.95	426.9
909	S[52]	14962.25	66.9
910	S[53]	14952.55	186.9
911	S[54]	14942.85	306.9
912	RX[783]	14933.15	426.9
913	S[55]	14923.45	66.9
914	S[56]	14913.75	186.9
915	S[57]	14904.05	306.9
916	RX[782]	14894.35	426.9
917	S[58]	14884.65	66.9
918	S[59]	14874.95	186.9
919	S[60]	14865.25	306.9
920	RX[781]	14855.55	426.9
921	S[61]	14845.85	66.9
922	S[62]	14836.15	186.9
923	S[63]	14826.45	306.9
924	RX[780]	14816.75	426.9
925	S[64]	14807.05	66.9
926	S[65]	14797.35	186.9
927	S[66]	14787.65	306.9
928	RX[779]	14777.95	426.9
929	S[67]	14768.25	66.9
930	S[68]	14758.55	186.9
931	S[69]	14748.85	306.9
932	RX[778]	14739.15	426.9
933	S[70]	14729.45	66.9
934	S[71]	14719.75	186.9
935	S[72]	14710.05	306.9
936	RX[777]	14700.35	426.9
937	S[73]	14690.65	66.9
938	S[74]	14680.95	186.9
939	S[75]	14671.25	306.9
940	RX[776]	14661.55	426.9
941	S[76]	14651.85	66.9
942	S[77]	14642.15	186.9
943	S[78]	14632.45	306.9
944	RX[775]	14622.75	426.9
945	S[79]	14613.05	66.9
946	S[80]	14603.35	186.9
947	S[81]	14593.65	306.9
948	RX[774]	14583.95	426.9
949	S[82]	14574.25	66.9
950	S[83]	14564.55	186.9
951	S[84]	14554.85	306.9
952	RX[773]	14545.15	426.9
953	S[85]	14535.45	66.9
954	S[86]	14525.75	186.9
955	S[87]	14516.05	306.9
956	RX[772]	14506.35	426.9
957	S[88]	14496.65	66.9
958	S[89]	14486.95	186.9
959	S[90]	14477.25	306.9
960	RX[771]	14467.55	426.9
961	S[91]	14457.85	66.9
962	S[92]	14448.15	186.9
963	S[93]	14438.45	306.9
964	RX[770]	14428.75	426.9
965	S[94]	14419.05	66.9
966	S[95]	14409.35	186.9
967	S[96]	14399.65	306.9
968	RX[769]	14389.95	426.9
969	S[97]	14380.25	66.9
970	S[98]	14370.55	186.9
971	S[99]	14360.85	306.9
972	RX[768]	14351.15	426.9
973	S[100]	14341.45	66.9
974	S[101]	14331.75	186.9
975	S[102]	14322.05	306.9
976	RX[767]	14312.35	426.9
977	S[103]	14302.65	66.9
978	S[104]	14292.95	186.9
979	S[105]	14283.25	306.9
980	RX[766]	14273.55	426.9
981	S[106]	14263.85	66.9
982	S[107]	14254.15	186.9

No.	PAD Name	X	Y
983	S[108]	14244.45	306.9
984	RX[765]	14234.75	426.9
985	S[109]	14225.05	66.9
986	S[110]	14215.35	186.9
987	S[111]	14205.65	306.9
988	RX[764]	14195.95	426.9
989	S[112]	14186.25	66.9
990	S[113]	14176.55	186.9
991	S[114]	14166.85	306.9
992	RX[763]	14157.15	426.9
993	S[115]	14147.45	66.9
994	S[116]	14137.75	186.9
995	S[117]	14128.05	306.9
996	RX[762]	14118.35	426.9
997	S[118]	14108.65	66.9
998	S[119]	14098.95	186.9
999	S[120]	14089.25	306.9
1000	RX[761]	14079.55	426.9
1001	S[121]	14069.85	66.9
1002	S[122]	14060.15	186.9
1003	S[123]	14050.45	306.9
1004	RX[760]	14040.75	426.9
1005	S[124]	14031.05	66.9
1006	S[125]	14021.35	186.9
1007	S[126]	14011.65	306.9
1008	RX[759]	14001.95	426.9
1009	S[127]	13992.25	66.9
1010	S[128]	13982.55	186.9
1011	S[129]	13972.85	306.9
1012	RX[758]	13963.15	426.9
1013	S[130]	13953.45	66.9
1014	S[131]	13943.75	186.9
1015	S[132]	13934.05	306.9
1016	RX[757]	13924.35	426.9
1017	S[133]	13914.65	66.9
1018	S[134]	13904.95	186.9
1019	S[135]	13895.25	306.9
1020	RX[756]	13885.55	426.9
1021	S[136]	13875.85	66.9
1022	S[137]	13866.15	186.9
1023	S[138]	13856.45	306.9
1024	RX[755]	13846.75	426.9
1025	S[139]	13837.05	66.9
1026	S[140]	13827.35	186.9
1027	S[141]	13817.65	306.9
1028	RX[754]	13807.95	426.9
1029	S[142]	13798.25	66.9
1030	S[143]	13788.55	186.9
1031	S[144]	13778.85	306.9
1032	RX[753]	13769.15	426.9
1033	S[145]	13759.45	66.9
1034	S[146]	13749.75	186.9
1035	S[147]	13740.05	306.9
1036	RX[752]	13730.35	426.9
1037	S[148]	13720.65	66.9
1038	S[149]	13710.95	186.9
1039	S[150]	13701.25	306.9
1040	RX[751]	13691.55	426.9
1041	S[151]	13681.85	66.9
1042	S[152]	13672.15	186.9
1043	S[153]	13662.45	306.9
1044	RX[750]	13652.75	426.9
1045	S[154]	13643.05	66.9
1046	S[155]	13633.35	186.9
1047	S[156]	13623.65	306.9
1048	RX[749]	13613.95	426.9
1049	S[157]	13604.25	66.9
1050	S[158]	13594.55	186.9
1051	S[159]	13584.85	306.9
1052	RX[748]	13575.15	426.9
1053	S[160]	13565.45	66.9
1054	S[161]	13555.75	186.9
1055	S[162]	13546.05	306.9
1056	RX[747]	13536.35	426.9
1057	S[163]	13526.65	66.9
1058	S[164]	13516.95	186.9
1059	S[165]	13507.25	306.9
1060	RX[746]	13497.55	426.9
1061	S[166]	13487.85	66.9
1062	S[167]	13478.15	186.9
1063	S[168]	13468.45	306.9
1064	RX[745]	13458.75	426.9
1065	S[169]	13449.05	66.9
1066	S[170]	13439.35	186.9
1067	S[171]	13429.65	306.9
1068	RX[744]	13419.95	426.9
1069	S[172]	13410.25	66.9
1070	S[173]	13400.55	186.9
1071	S[174]	13390.85	306.9
1072	RX[743]	13381.15	426.9
1073	S[175]	13371.45	66.9
1074	S[176]	13361.75	186.9
1075	S[177]	13352.05	306.9
1076	RX[742]	13342.35	426.9
1077	S[178]	13332.65	66.9
1078	S[179]	13322.95	186.9
1079	S[180]	13313.25	306.9
1080	RX[741]	13303.55	426.9
1081	S[181]	13293.85	66.9
1082	S[182]	13284.15	186.9
1083	S[183]	13274.45	306.9
1084	RX[740]	13264.75	426.9
1085	S[184]	13255.05	66.9
1086	S[185]	13245.35	186.9
1087	S[186]	13235.65	306.9
1088	RX[739]	13225.95	426.9
1089	S[187]	13216.25	66.9
1090	S[188]	13206.55	186.9
1091	S[189]	13196.85	306.9
1092	RX[738]	13187.15	426.9
1093	S[190]	13177.45	66.9
1094	S[191]	13167.75	186.9
1095	S[192]	13158.05	306.9
1096	RX[737]	13148.35	426.9
1097	S[193]	13138.65	66.9
1098	S[194]	13128.95	186.9
1099	S[195]	13119.25	306.9
1100	RX[736]	13109.55	426.9
1101	S[196]	13099.85	66.9
1102	S[197]	13090.15	186.9
1103	S[198]	13080.45	306.9
1104	RX[735]	13070.75	426.9
1105	S[199]	13061.05	66.9
1106	S[200]	13051.35	186.9
1107	S[201]	13041.65	306.9
1108	RX[734]	13031.95	426.9
1109	S[202]	13022.25	66.9
1110	S[203]	13012.55	186.9
1111	S[204]	13002.85	306.9
1112	RX[733]	12993.15	426.9
1113	S[205]	12983.45	66.9
1114	S[206]	12973.75	186.9
1115	S[207]	12964.05	306.9
1116	RX[732]	12954.35	426.9
1117	S[208]	12944.65	66.9
1118	S[209]	12934.95	186.9
1119	S[210]	12925.25	306.9
1120	RX[731]	12915.55	426.9
1121	S[211]	12905.85	66.9
1122	S[212]	12896.15	186.9
1123	S[213]	12886.45	306.9
1124	RX[730]	12876.75	426.9
1125	S[214]	12867.05	66.9
1126	S[215]	12857.35	186.9
1127	S[216]	12847.65	306.9
1128	RX[729]	12837.95	426.9
1129	S[217]	12828.25	66.9
1130	S[218]	12818.55	186.9
1131	S[219]	12808.85	306.9
1132	RX[728]	12799.15	426.9
1133	S[220]	12789.45	66.9
1134	S[221]	12779.75	186.9
1135	S[222]	12770.05	306.9
1136	RX[727]	12760.35	426.9
1137	S[223]	12750.65	66.9
1138	S[224]	12740.95	186.9
1139	S[225]	12731.25	306.9
1140	RX[726]	12721.55	426.9
1141	S[226]	12711.85	66.9
1142	S[227]	12702.15	186.9
1143	S[228]	12692.45	306.9
1144	RX[725]	12682.75	426.9
1145	S[229]	12673.05	66.9
1146	S[230]	12663.35	186.9
1147	S[231]	12653.65	306.9
1148	RX[724]	12643.95	426.9
1149	S[232]	12634.25	66.9
1150	S[233]	12624.55	186.9
1151	S[234]	12614.85	306.9
1152	RX[723]	12605.15	426.9
1153	S[235]	12595.45	66.9
1154	S[236]	12585.75	186.9
1155	S[237]	12576.05	306.9
1156	RX[722]	12566.35	426.9
1157	S[238]	12556.65	66.9
1158	S[239]	12546.95	186.9
1159	S[240]	12537.25	306.9
1160	RX[721]	12527.55	426.9
1161	S[241]	12517.85	66.9
1162	S[242]	12508.15	186.9
1163	S[243]	12498.45	306.9
1164	RX[720]	12488.75	426.9
1165	S[244]	12479.05	66.9
1166	S[245]	12469.35	186.9
1167	S[246]	12459.65	306.9
1168	RX[719]	12449.95	426.9
1169	S[247]	12440.25	66.9
1170	S[248]	12430.55	186.9
1171	S[249]	12420.85	306.9
1172	RX[718]	12411.15	426.9
1173	S[250]	12401.45	66.9
1174	S[251]	12391.75	186.9
1175	S[252]	12382.05	306.9
1176	RX[717]	12372.35	426.9
1177	S[253]	12362.65	66.9
1178	S[254]	12352.95	186.9
1179	S[255]	12343.25	306.9
1180	RX[716]	12333.55	426.9
1181	S[256]	12323.85	66.9
1182	S[257]	12314.15	186.9
1183	S[258]	12304.45	306.9
1184	RX[715]	12294.75	426.9
1185	S[259]	12285.05	66.9
1186	S[260]	12275.35	186.9
1187	S[261]	12265.65	306.9
1188	RX[714]	12255.95	426.9
1189	S[262]	12246.25	66.9
1190	S[263]	12236.55	186.9
1191	S[264]	12226.85	306.9
1192	RX[713]	12217.15	426.9
1193	S[265]	12207.45	66.9
1194	S[266]	12197.75	186.9
1195	S[267]	12188.05	306.9
1196	RX[712]	12178.35	426.9
1197	S[268]	12168.65	66.9
1198	S[269]	12158.95	186.9
1199	S[270]	12149.25	306.9
1200	RX[711]	12139.55	426.9
1201	S[271]	12129.85	66.9
1202	S[272]	12120.15	186.9
1203	S[273]	12110.45	306.9
1204	RX[710]	12100.75	426.9
1205	S[274]	12091.05	66.9
1206	S[275]	12081.35	186.9
1207	S[276]	12071.65	306.9
1208	RX[709]	12061.95	426.9
1209	S[277]	12052.25	66.9
1210	S[278]	12042.55	186.9
1211	S[279]	12032.85	306.9
1212	RX[708]	12023.15	426.9
1213	S[280]	12013.45	66.9
1214	S[281]	12003.75	186.9
1215	S[282]	11994.05	306.9
1216	RX[707]	11984.35	426.9
1217	S[283]	11974.65	66.9
1218	S[284]	11964.95	186.9
1219	S[285]	11955.25	306.9
1220	RX[706]	11945.55	426.9
1221	S[286]	11935.85	66.9
1222	S[287]	11926.15	186.9
1223	S[288]	11916.45	306.9
1224	RX[705]	11906.75	426.9
1225	S[289]	11897.05	66.9
1226	S[290]	11887.35	186.9
1227	S[291]	11877.65	306.9
1228	RX[704]	11867.95	426.9
1229	S[292]	11858.25	66.9
1230	S[293]	11848.55	186.9
1231	S[294]	11838.85	306.9
1232	RX[703]	11829.15	426.9
1233	S[295]	11819.45	66.9
1234	S[296]	11809.75	186.9

No.	PAD Name	X	Y
1235	S[297]	11800.05	306.9
1236	RX[702]	11790.35	426.9
1237	S[298]	11780.65	66.9
1238	S[299]	11770.95	186.9
1239	S[300]	11761.25	306.9
1240	RX[701]	11751.55	426.9
1241	S[301]	11741.85	66.9
1242	S[302]	11732.15	186.9
1243	S[303]	11722.45	306.9
1244	RX[700]	11712.75	426.9
1245	S[304]	11703.05	66.9
1246	S[305]	11693.35	186.9
1247	S[306]	11683.65	306.9
1248	RX[699]	11673.95	426.9
1249	S[307]	11664.25	66.9
1250	S[308]	11654.55	186.9
1251	S[309]	11644.85	306.9
1252	RX[698]	11635.15	426.9
1253	S[310]	11625.45	66.9
1254	S[311]	11615.75	186.9
1255	S[312]	11606.05	306.9
1256	RX[697]	11596.35	426.9
1257	S[313]	11586.65	66.9
1258	S[314]	11576.95	186.9
1259	S[315]	11567.25	306.9
1260	RX[696]	11557.55	426.9
1261	S[316]	11547.85	66.9
1262	S[317]	11538.15	186.9
1263	S[318]	11528.45	306.9
1264	RX[695]	11518.75	426.9
1265	S[319]	11509.05	66.9
1266	S[320]	11499.35	186.9
1267	S[321]	11489.65	306.9
1268	RX[694]	11479.95	426.9
1269	S[322]	11470.25	66.9
1270	S[323]	11460.55	186.9
1271	S[324]	11450.85	306.9
1272	RX[693]	11441.15	426.9
1273	S[325]	11431.45	66.9
1274	S[326]	11421.75	186.9
1275	S[327]	11412.05	306.9
1276	RX[692]	11402.35	426.9
1277	S[328]	11392.65	66.9
1278	S[329]	11382.95	186.9
1279	S[330]	11373.25	306.9
1280	RX[691]	11363.55	426.9
1281	S[331]	11353.85	66.9
1282	S[332]	11344.15	186.9
1283	S[333]	11334.45	306.9
1284	RX[690]	11324.75	426.9
1285	S[334]	11315.05	66.9
1286	S[335]	11305.35	186.9
1287	S[336]	11295.65	306.9
1288	RX[689]	11285.95	426.9
1289	S[337]	11276.25	66.9
1290	S[338]	11266.55	186.9
1291	S[339]	11256.85	306.9
1292	RX[688]	11247.15	426.9
1293	S[340]	11237.45	66.9
1294	S[341]	11227.75	186.9
1295	S[342]	11218.05	306.9
1296	RX[687]	11208.35	426.9
1297	S[343]	11198.65	66.9
1298	S[344]	11188.95	186.9
1299	S[345]	11179.25	306.9
1300	RX[686]	11169.55	426.9
1301	S[346]	11159.85	66.9
1302	S[347]	11150.15	186.9
1303	S[348]	11140.45	306.9
1304	RX[685]	11130.75	426.9
1305	S[349]	11121.05	66.9
1306	S[350]	11111.35	186.9
1307	S[351]	11101.65	306.9
1308	RX[684]	11091.95	426.9
1309	S[352]	11082.25	66.9
1310	S[353]	11072.55	186.9
1311	S[354]	11062.85	306.9
1312	RX[683]	11053.15	426.9
1313	S[355]	11043.45	66.9
1314	S[356]	11033.75	186.9
1315	S[357]	11024.05	306.9
1316	RX[682]	11014.35	426.9
1317	S[358]	11004.65	66.9
1318	S[359]	10994.95	186.9
1319	S[360]	10985.25	306.9
1320	RX[681]	10975.55	426.9
1321	S[361]	10965.85	66.9
1322	S[362]	10956.15	186.9
1323	S[363]	10946.45	306.9
1324	RX[680]	10936.75	426.9
1325	S[364]	10927.05	66.9
1326	S[365]	10917.35	186.9
1327	S[366]	10907.65	306.9
1328	RX[679]	10897.95	426.9
1329	S[367]	10888.25	66.9
1330	S[368]	10878.55	186.9
1331	S[369]	10868.85	306.9
1332	RX[678]	10859.15	426.9
1333	S[370]	10849.45	66.9
1334	S[371]	10839.75	186.9
1335	S[372]	10830.05	306.9
1336	RX[677]	10820.35	426.9
1337	S[373]	10810.65	66.9
1338	S[374]	10800.95	186.9
1339	S[375]	10791.25	306.9
1340	RX[676]	10781.55	426.9
1341	S[376]	10771.85	66.9
1342	S[377]	10762.15	186.9
1343	S[378]	10752.45	306.9
1344	RX[675]	10742.75	426.9
1345	S[379]	10733.05	66.9
1346	S[380]	10723.35	186.9
1347	S[381]	10713.65	306.9
1348	RX[674]	10703.95	426.9
1349	S[382]	10694.25	66.9
1350	S[383]	10684.55	186.9
1351	S[384]	10674.85	306.9
1352	RX[673]	10665.15	426.9
1353	S[385]	10655.45	66.9
1354	S[386]	10645.75	186.9
1355	S[387]	10636.05	306.9
1356	RX[672]	10626.35	426.9
1357	S[388]	10616.65	66.9
1358	S[389]	10606.95	186.9
1359	S[390]	10597.25	306.9
1360	RX[671]	10587.55	426.9
1361	S[391]	10577.85	66.9
1362	S[392]	10568.15	186.9
1363	S[393]	10558.45	306.9
1364	RX[670]	10548.75	426.9
1365	S[394]	10539.05	66.9
1366	S[395]	10529.35	186.9
1367	S[396]	10519.65	306.9
1368	RX[669]	10509.95	426.9
1369	S[397]	10500.25	66.9
1370	S[398]	10490.55	186.9
1371	S[399]	10480.85	306.9
1372	RX[668]	10471.15	426.9
1373	S[400]	10461.45	66.9
1374	S[401]	10451.75	186.9
1375	S[402]	10442.05	306.9
1376	RX[667]	10432.35	426.9
1377	S[403]	10422.65	66.9
1378	S[404]	10412.95	186.9
1379	S[405]	10403.25	306.9
1380	RX[666]	10393.55	426.9
1381	S[406]	10383.85	66.9
1382	S[407]	10374.15	186.9
1383	S[408]	10364.45	306.9
1384	RX[665]	10354.75	426.9
1385	S[409]	10345.05	66.9
1386	S[410]	10335.35	186.9
1387	S[411]	10325.65	306.9
1388	RX[664]	10315.95	426.9
1389	S[412]	10306.25	66.9
1390	S[413]	10296.55	186.9
1391	S[414]	10286.85	306.9
1392	RX[663]	10277.15	426.9
1393	S[415]	10267.45	66.9
1394	S[416]	10257.75	186.9
1395	S[417]	10248.05	306.9
1396	RX[662]	10238.35	426.9
1397	S[418]	10228.65	66.9
1398	S[419]	10218.95	186.9
1399	S[420]	10209.25	306.9
1400	RX[661]	10199.55	426.9
1401	S[421]	10189.85	66.9
1402	S[422]	10180.15	186.9
1403	S[423]	10170.45	306.9
1404	RX[660]	10160.75	426.9
1405	S[424]	10151.05	66.9
1406	S[425]	10141.35	186.9
1407	S[426]	10131.65	306.9
1408	RX[659]	10121.95	426.9
1409	S[427]	10112.25	66.9
1410	S[428]	10102.55	186.9
1411	S[429]	10092.85	306.9
1412	RX[658]	10083.15	426.9
1413	S[430]	10073.45	66.9
1414	S[431]	10063.75	186.9
1415	S[432]	10054.05	306.9
1416	RX[657]	10044.35	426.9
1417	S[433]	10034.65	66.9
1418	S[434]	10024.95	186.9
1419	S[435]	10015.25	306.9
1420	RX[656]	10005.55	426.9
1421	S[436]	9995.85	66.9
1422	S[437]	9986.15	186.9
1423	S[438]	9976.45	306.9
1424	RX[655]	9966.75	426.9
1425	S[439]	9957.05	66.9
1426	S[440]	9947.35	186.9
1427	S[441]	9937.65	306.9
1428	RX[654]	9927.95	426.9
1429	S[442]	9918.25	66.9
1430	S[443]	9908.55	186.9
1431	S[444]	9898.85	306.9
1432	RX[653]	9889.15	426.9
1433	S[445]	9879.45	66.9
1434	S[446]	9869.75	186.9
1435	S[447]	9860.05	306.9
1436	RX[652]	9850.35	426.9
1437	S[448]	9840.65	66.9
1438	S[449]	9830.95	186.9
1439	S[450]	9821.25	306.9
1440	RX[651]	9811.55	426.9
1441	S[451]	9801.85	66.9
1442	S[452]	9792.15	186.9
1443	S[453]	9782.45	306.9
1444	RX[650]	9772.75	426.9
1445	S[454]	9763.05	66.9
1446	S[455]	9753.35	186.9
1447	S[456]	9743.65	306.9
1448	RX[649]	9733.95	426.9
1449	S[457]	9724.25	66.9
1450	S[458]	9714.55	186.9
1451	S[459]	9704.85	306.9
1452	RX[648]	9695.15	426.9
1453	S[460]	9685.45	66.9
1454	S[461]	9675.75	186.9
1455	S[462]	9666.05	306.9
1456	RX[647]	9656.35	426.9
1457	S[463]	9646.65	66.9
1458	S[464]	9636.95	186.9
1459	S[465]	9627.25	306.9
1460	RX[646]	9617.55	426.9
1461	S[466]	9607.85	66.9
1462	S[467]	9598.15	186.9
1463	S[468]	9588.45	306.9
1464	RX[645]	9578.75	426.9
1465	S[469]	9569.05	66.9
1466	S[470]	9559.35	186.9
1467	S[471]	9549.65	306.9
1468	RX[644]	9539.95	426.9
1469	S[472]	9530.25	66.9
1470	S[473]	9520.55	186.9
1471	S[474]	9510.85	306.9
1472	RX[643]	9501.15	426.9
1473	S[475]	9491.45	66.9
1474	S[476]	9481.75	186.9
1475	S[477]	9472.05	306.9
1476	RX[642]	9462.35	426.9
1477	S[478]	9452.65	66.9
1478	S[479]	9442.95	186.9
1479	S[480]	9433.25	306.9
1480	RX[641]	9423.55	426.9
1481	S[481]	9413.85	66.9
1482	S[482]	9404.15	186.9
1483	S[483]	9394.45	306.9
1484	RX[640]	9384.75	426.9
1485	S[484]	9375.05	66.9
1486	S[485]	9365.35	186.9

No.	PAD Name	X	Y
1487	S[486]	9355.65	306.9
1488	RX[639]	9345.95	426.9
1489	S[487]	9336.25	66.9
1490	S[488]	9326.55	186.9
1491	S[489]	9316.85	306.9
1492	RX[638]	9307.15	426.9
1493	S[490]	9297.45	66.9
1494	S[491]	9287.75	186.9
1495	S[492]	9278.05	306.9
1496	RX[637]	9268.35	426.9
1497	S[493]	9258.65	66.9
1498	S[494]	9248.95	186.9
1499	S[495]	9239.25	306.9
1500	RX[636]	9229.55	426.9
1501	S[496]	9219.85	66.9
1502	S[497]	9210.15	186.9
1503	S[498]	9200.45	306.9
1504	RX[635]	9190.75	426.9
1505	S[499]	9181.05	66.9
1506	S[500]	9171.35	186.9
1507	S[501]	9161.65	306.9
1508	RX[634]	9151.95	426.9
1509	S[502]	9142.25	66.9
1510	S[503]	9132.55	186.9
1511	S[504]	9122.85	306.9
1512	RX[633]	9113.15	426.9
1513	S[505]	9103.45	66.9
1514	S[506]	9093.75	186.9
1515	S[507]	9084.05	306.9
1516	RX[632]	9074.35	426.9
1517	S[508]	9064.65	66.9
1518	S[509]	9054.95	186.9
1519	S[510]	9045.25	306.9
1520	RX[631]	9035.55	426.9
1521	S[511]	9025.85	66.9
1522	S[512]	9016.15	186.9
1523	S[513]	9006.45	306.9
1524	RX[630]	8996.75	426.9
1525	S[514]	8987.05	66.9
1526	S[515]	8977.35	186.9
1527	S[516]	8967.65	306.9
1528	RX[629]	8957.95	426.9
1529	S[517]	8948.25	66.9
1530	S[518]	8938.55	186.9
1531	S[519]	8928.85	306.9
1532	RX[628]	8919.15	426.9
1533	S[520]	8909.45	66.9
1534	S[521]	8899.75	186.9
1535	S[522]	8890.05	306.9
1536	RX[627]	8880.35	426.9
1537	S[523]	8870.65	66.9
1538	S[524]	8860.95	186.9
1539	S[525]	8851.25	306.9
1540	RX[626]	8841.55	426.9
1541	S[526]	8831.85	66.9
1542	S[527]	8822.15	186.9
1543	S[528]	8812.45	306.9
1544	RX[625]	8802.75	426.9
1545	S[529]	8793.05	66.9
1546	S[530]	8783.35	186.9
1547	S[531]	8773.65	306.9
1548	RX[624]	8763.95	426.9
1549	S[532]	8754.25	66.9
1550	S[533]	8744.55	186.9
1551	S[534]	8734.85	306.9
1552	RX[623]	8725.15	426.9
1553	S[535]	8715.45	66.9
1554	S[536]	8705.75	186.9
1555	S[537]	8696.05	306.9
1556	RX[622]	8686.35	426.9
1557	S[538]	8676.65	66.9
1558	S[539]	8666.95	186.9
1559	S[540]	8657.25	306.9
1560	RX[621]	8647.55	426.9
1561	S[541]	8637.85	66.9
1562	S[542]	8628.15	186.9
1563	S[543]	8618.45	306.9
1564	RX[620]	8608.75	426.9
1565	S[544]	8599.05	66.9
1566	S[545]	8589.35	186.9
1567	S[546]	8579.65	306.9
1568	RX[619]	8569.95	426.9
1569	S[547]	8560.25	66.9
1570	S[548]	8550.55	186.9

No.	PAD Name	X	Y
1571	S[549]	8540.85	306.9
1572	RX[618]	8531.15	426.9
1573	S[550]	8521.45	66.9
1574	S[551]	8511.75	186.9
1575	S[552]	8502.05	306.9
1576	RX[617]	8492.35	426.9
1577	S[553]	8482.65	66.9
1578	S[554]	8472.95	186.9
1579	S[555]	8463.25	306.9
1580	RX[616]	8453.55	426.9
1581	S[556]	8443.85	66.9
1582	S[557]	8434.15	186.9
1583	S[558]	8424.45	306.9
1584	RX[615]	8414.75	426.9
1585	S[559]	8405.05	66.9
1586	S[560]	8395.35	186.9
1587	S[561]	8385.65	306.9
1588	RX[614]	8375.95	426.9
1589	S[562]	8366.25	66.9
1590	S[563]	8356.55	186.9
1591	S[564]	8346.85	306.9
1592	RX[613]	8337.15	426.9
1593	S[565]	8327.45	66.9
1594	S[566]	8317.75	186.9
1595	S[567]	8308.05	306.9
1596	RX[612]	8298.35	426.9
1597	S[568]	8288.65	66.9
1598	S[569]	8278.95	186.9
1599	S[570]	8269.25	306.9
1600	RX[611]	8259.55	426.9
1601	S[571]	8249.85	66.9
1602	S[572]	8240.15	186.9
1603	S[573]	8230.45	306.9
1604	RX[610]	8220.75	426.9
1605	S[574]	8211.05	66.9
1606	S[575]	8201.35	186.9
1607	S[576]	8191.65	306.9
1608	RX[609]	8181.95	426.9
1609	S[577]	8172.25	66.9
1610	S[578]	8162.55	186.9
1611	S[579]	8152.85	306.9
1612	RX[608]	8143.15	426.9
1613	S[580]	8133.45	66.9
1614	S[581]	8123.75	186.9
1615	S[582]	8114.05	306.9
1616	RX[607]	8104.35	426.9
1617	S[583]	8094.65	66.9
1618	S[584]	8084.95	186.9
1619	S[585]	8075.25	306.9
1620	RX[606]	8065.55	426.9
1621	S[586]	8055.85	66.9
1622	S[587]	8046.15	186.9
1623	S[588]	8036.45	306.9
1624	RX[605]	8026.75	426.9
1625	S[589]	8017.05	66.9
1626	S[590]	8007.35	186.9
1627	S[591]	7997.65	306.9
1628	RX[604]	7987.95	426.9
1629	S[592]	7978.25	66.9
1630	S[593]	7968.55	186.9
1631	S[594]	7958.85	306.9
1632	RX[603]	7949.15	426.9
1633	S[595]	7939.45	66.9
1634	S[596]	7929.75	186.9
1635	S[597]	7920.05	306.9
1636	RX[602]	7910.35	426.9
1637	S[598]	7900.65	66.9
1638	S[599]	7890.95	186.9
1639	S[600]	7881.25	306.9
1640	RX[601]	7871.55	426.9
1641	S[601]	7861.85	66.9
1642	S[602]	7852.15	186.9
1643	S[603]	7842.45	306.9
1644	RX[600]	7832.75	426.9
1645	S[604]	7823.05	66.9
1646	S[605]	7813.35	186.9
1647	S[606]	7803.65	306.9
1648	RX[599]	7793.95	426.9
1649	S[607]	7784.25	66.9
1650	S[608]	7774.55	186.9
1651	S[609]	7764.85	306.9
1652	RX[598]	7755.15	426.9
1653	S[610]	7745.45	66.9
1654	S[611]	7735.75	186.9

No.	PAD Name	X	Y
1655	S[612]	7726.05	306.9
1656	RX[597]	7716.35	426.9
1657	S[613]	7706.65	66.9
1658	S[614]	7696.95	186.9
1659	S[615]	7687.25	306.9
1660	RX[596]	7677.55	426.9
1661	S[616]	7667.85	66.9
1662	S[617]	7658.15	186.9
1663	S[618]	7648.45	306.9
1664	RX[595]	7638.75	426.9
1665	S[619]	7629.05	66.9
1666	S[620]	7619.35	186.9
1667	S[621]	7609.65	306.9
1668	RX[594]	7599.95	426.9
1669	S[622]	7590.25	66.9
1670	S[623]	7580.55	186.9
1671	S[624]	7570.85	306.9
1672	RX[593]	7561.15	426.9
1673	S[625]	7551.45	66.9
1674	S[626]	7541.75	186.9
1675	S[627]	7532.05	306.9
1676	RX[592]	7522.35	426.9
1677	S[628]	7512.65	66.9
1678	S[629]	7502.95	186.9
1679	S[630]	7493.25	306.9
1680	RX[591]	7483.55	426.9
1681	S[631]	7473.85	66.9
1682	S[632]	7464.15	186.9
1683	S[633]	7454.45	306.9
1684	RX[590]	7444.75	426.9
1685	S[634]	7435.05	66.9
1686	S[635]	7425.35	186.9
1687	S[636]	7415.65	306.9
1688	RX[589]	7405.95	426.9
1689	S[637]	7396.25	66.9
1690	S[638]	7386.55	186.9
1691	S[639]	7376.85	306.9
1692	RX[588]	7367.15	426.9
1693	S[640]	7357.45	66.9
1694	S[641]	7347.75	186.9
1695	S[642]	7338.05	306.9
1696	RX[587]	7328.35	426.9
1697	S[643]	7318.65	66.9
1698	S[644]	7308.95	186.9
1699	S[645]	7299.25	306.9
1700	RX[586]	7289.55	426.9
1701	S[646]	7279.85	66.9
1702	S[647]	7270.15	186.9
1703	S[648]	7260.45	306.9
1704	RX[585]	7250.75	426.9
1705	S[649]	7241.05	66.9
1706	S[650]	7231.35	186.9
1707	S[651]	7221.65	306.9
1708	RX[584]	7211.95	426.9
1709	S[652]	7202.25	66.9
1710	S[653]	7192.55	186.9
1711	S[654]	7182.85	306.9
1712	RX[583]	7173.15	426.9
1713	S[655]	7163.45	66.9
1714	S[656]	7153.75	186.9
1715	S[657]	7144.05	306.9
1716	RX[582]	7134.35	426.9
1717	S[658]	7124.65	66.9
1718	S[659]	7114.95	186.9
1719	S[660]	7105.25	306.9
1720	RX[581]	7095.55	426.9
1721	S[661]	7085.85	66.9
1722	S[662]	7076.15	186.9
1723	S[663]	7066.45	306.9
1724	RX[580]	7056.75	426.9
1725	S[664]	7047.05	66.9
1726	S[665]	7037.35	186.9
1727	S[666]	7027.65	306.9
1728	RX[579]	7017.95	426.9
1729	S[667]	7008.25	66.9
1730	S[668]	6998.55	186.9
1731	S[669]	6988.85	306.9
1732	RX[578]	6979.15	426.9
1733	S[670]	6969.45	66.9
1734	S[671]	6959.75	186.9
1735	S[672]	6950.05	306.9
1736	RX[577]	6940.35	426.9
1737	S[673]	6930.65	66.9
1738	S[674]	6920.95	186.9

No.	PAD Name	X	Y
1739	S[675]	6911.25	306.9
1740	RX[576]	6901.55	426.9
1741	S[676]	6891.85	66.9
1742	S[677]	6882.15	186.9
1743	S[678]	6872.45	306.9
1744	RX[575]	6862.75	426.9
1745	S[679]	6853.05	66.9
1746	S[680]	6843.35	186.9
1747	S[681]	6833.65	306.9
1748	RX[574]	6823.95	426.9
1749	S[682]	6814.25	66.9
1750	S[683]	6804.55	186.9
1751	S[684]	6794.85	306.9
1752	RX[573]	6785.15	426.9
1753	S[685]	6775.45	66.9
1754	S[686]	6765.75	186.9
1755	S[687]	6756.05	306.9
1756	RX[572]	6746.35	426.9
1757	S[688]	6736.65	66.9
1758	S[689]	6726.95	186.9
1759	S[690]	6717.25	306.9
1760	RX[571]	6707.55	426.9
1761	S[691]	6697.85	66.9
1762	S[692]	6688.15	186.9
1763	S[693]	6678.45	306.9
1764	RX[570]	6668.75	426.9
1765	S[694]	6659.05	66.9
1766	S[695]	6649.35	186.9
1767	S[696]	6639.65	306.9
1768	RX[569]	6629.95	426.9
1769	S[697]	6620.25	66.9
1770	S[698]	6610.55	186.9
1771	S[699]	6600.85	306.9
1772	RX[568]	6591.15	426.9
1773	S[700]	6581.45	66.9
1774	S[701]	6571.75	186.9
1775	S[702]	6562.05	306.9
1776	RX[567]	6552.35	426.9
1777	S[703]	6542.65	66.9
1778	S[704]	6532.95	186.9
1779	S[705]	6523.25	306.9
1780	RX[566]	6513.55	426.9
1781	S[706]	6503.85	66.9
1782	S[707]	6494.15	186.9
1783	S[708]	6484.45	306.9
1784	RX[565]	6474.75	426.9
1785	S[709]	6465.05	66.9
1786	S[710]	6455.35	186.9
1787	S[711]	6445.65	306.9
1788	RX[564]	6435.95	426.9
1789	S[712]	6426.25	66.9
1790	S[713]	6416.55	186.9
1791	S[714]	6406.85	306.9
1792	RX[563]	6397.15	426.9
1793	S[715]	6387.45	66.9
1794	S[716]	6377.75	186.9
1795	S[717]	6368.05	306.9
1796	RX[562]	6358.35	426.9
1797	S[718]	6348.65	66.9
1798	S[719]	6338.95	186.9
1799	S[720]	6329.25	306.9
1800	RX[561]	6319.55	426.9
1801	S[721]	6309.85	66.9
1802	S[722]	6300.15	186.9
1803	S[723]	6290.45	306.9
1804	RX[560]	6280.75	426.9
1805	S[724]	6271.05	66.9
1806	S[725]	6261.35	186.9
1807	S[726]	6251.65	306.9
1808	RX[559]	6241.95	426.9
1809	S[727]	6232.25	66.9
1810	S[728]	6222.55	186.9
1811	S[729]	6212.85	306.9
1812	RX[558]	6203.15	426.9
1813	S[730]	6193.45	66.9
1814	S[731]	6183.75	186.9
1815	S[732]	6174.05	306.9
1816	RX[557]	6164.35	426.9
1817	S[733]	6154.65	66.9
1818	S[734]	6144.95	186.9
1819	S[735]	6135.25	306.9
1820	RX[556]	6125.55	426.9
1821	S[736]	6115.85	66.9
1822	S[737]	6106.15	186.9

No.	PAD Name	X	Y
1823	S[738]	6096.45	306.9
1824	RX[555]	6086.75	426.9
1825	S[739]	6077.05	66.9
1826	S[740]	6067.35	186.9
1827	S[741]	6057.65	306.9
1828	RX[554]	6047.95	426.9
1829	S[742]	6038.25	66.9
1830	S[743]	6028.55	186.9
1831	S[744]	6018.85	306.9
1832	RX[553]	6009.15	426.9
1833	S[745]	5999.45	66.9
1834	S[746]	5989.75	186.9
1835	S[747]	5980.05	306.9
1836	RX[552]	5970.35	426.9
1837	S[748]	5960.65	66.9
1838	S[749]	5950.95	186.9
1839	S[750]	5941.25	306.9
1840	RX[551]	5931.55	426.9
1841	S[751]	5921.85	66.9
1842	S[752]	5912.15	186.9
1843	S[753]	5902.45	306.9
1844	RX[550]	5892.75	426.9
1845	S[754]	5883.05	66.9
1846	S[755]	5873.35	186.9
1847	S[756]	5863.65	306.9
1848	RX[549]	5853.95	426.9
1849	S[757]	5844.25	66.9
1850	S[758]	5834.55	186.9
1851	S[759]	5824.85	306.9
1852	RX[548]	5815.15	426.9
1853	S[760]	5805.45	66.9
1854	S[761]	5795.75	186.9
1855	S[762]	5786.05	306.9
1856	RX[547]	5776.35	426.9
1857	S[763]	5766.65	66.9
1858	S[764]	5756.95	186.9
1859	S[765]	5747.25	306.9
1860	RX[546]	5737.55	426.9
1861	S[766]	5727.85	66.9
1862	S[767]	5718.15	186.9
1863	S[768]	5708.45	306.9
1864	RX[545]	5698.75	426.9
1865	S[769]	5689.05	66.9
1866	S[770]	5679.35	186.9
1867	S[771]	5669.65	306.9
1868	RX[544]	5659.95	426.9
1869	S[772]	5650.25	66.9
1870	S[773]	5640.55	186.9
1871	S[774]	5630.85	306.9
1872	RX[543]	5621.15	426.9
1873	S[775]	5611.45	66.9
1874	S[776]	5601.75	186.9
1875	S[777]	5592.05	306.9
1876	RX[542]	5582.35	426.9
1877	S[778]	5572.65	66.9
1878	S[779]	5562.95	186.9
1879	S[780]	5553.25	306.9
1880	RX[541]	5543.55	426.9
1881	S[781]	5533.85	66.9
1882	S[782]	5524.15	186.9
1883	S[783]	5514.45	306.9
1884	RX[540]	5504.75	426.9
1885	S[784]	5495.05	66.9
1886	S[785]	5485.35	186.9
1887	S[786]	5475.65	306.9
1888	RX[539]	5465.95	426.9
1889	S[787]	5456.25	66.9
1890	S[788]	5446.55	186.9
1891	S[789]	5436.85	306.9
1892	RX[538]	5427.15	426.9
1893	S[790]	5417.45	66.9
1894	S[791]	5407.75	186.9
1895	S[792]	5398.05	306.9
1896	RX[537]	5388.35	426.9
1897	S[793]	5378.65	66.9
1898	S[794]	5368.95	186.9
1899	S[795]	5359.25	306.9
1900	RX[536]	5349.55	426.9
1901	S[796]	5339.85	66.9
1902	S[797]	5330.15	186.9
1903	S[798]	5320.45	306.9
1904	RX[535]	5310.75	426.9
1905	S[799]	5301.05	66.9
1906	S[800]	5291.35	186.9

No.	PAD Name	X	Y
1907	S[801]	5281.65	306.9
1908	RX[534]	5271.95	426.9
1909	S[802]	5262.25	66.9
1910	S[803]	5252.55	186.9
1911	S[804]	5242.85	306.9
1912	RX[533]	5233.15	426.9
1913	S[805]	5223.45	66.9
1914	S[806]	5213.75	186.9
1915	S[807]	5204.05	306.9
1916	RX[532]	5194.35	426.9
1917	S[808]	5184.65	66.9
1918	S[809]	5174.95	186.9
1919	S[810]	5165.25	306.9
1920	RX[531]	5155.55	426.9
1921	S[811]	5145.85	66.9
1922	S[812]	5136.15	186.9
1923	S[813]	5126.45	306.9
1924	RX[530]	5116.75	426.9
1925	S[814]	5107.05	66.9
1926	S[815]	5097.35	186.9
1927	S[816]	5087.65	306.9
1928	RX[529]	5077.95	426.9
1929	S[817]	5068.25	66.9
1930	S[818]	5058.55	186.9
1931	S[819]	5048.85	306.9
1932	RX[528]	5039.15	426.9
1933	S[820]	5029.45	66.9
1934	S[821]	5019.75	186.9
1935	S[822]	5010.05	306.9
1936	RX[527]	5000.35	426.9
1937	S[823]	4990.65	66.9
1938	S[824]	4980.95	186.9
1939	S[825]	4971.25	306.9
1940	RX[526]	4961.55	426.9
1941	S[826]	4951.85	66.9
1942	S[827]	4942.15	186.9
1943	S[828]	4932.45	306.9
1944	RX[525]	4922.75	426.9
1945	S[829]	4913.05	66.9
1946	S[830]	4903.35	186.9
1947	S[831]	4893.65	306.9
1948	RX[524]	4883.95	426.9
1949	S[832]	4874.25	66.9
1950	S[833]	4864.55	186.9
1951	S[834]	4854.85	306.9
1952	RX[523]	4845.15	426.9
1953	S[835]	4835.45	66.9
1954	S[836]	4825.75	186.9
1955	S[837]	4816.05	306.9
1956	RX[522]	4806.35	426.9
1957	S[838]	4796.65	66.9
1958	S[839]	4786.95	186.9
1959	S[840]	4777.25	306.9
1960	RX[521]	4767.55	426.9
1961	S[841]	4757.85	66.9
1962	S[842]	4748.15	186.9
1963	S[843]	4738.45	306.9
1964	RX[520]	4728.75	426.9
1965	S[844]	4719.05	66.9
1966	S[845]	4709.35	186.9
1967	S[846]	4699.65	306.9
1968	RX[519]	4689.95	426.9
1969	S[847]	4680.25	66.9
1970	S[848]	4670.55	186.9
1971	S[849]	4660.85	306.9
1972	RX[518]	4651.15	426.9
1973	S[850]	4641.45	66.9
1974	S[851]	4631.75	186.9
1975	S[852]	4622.05	306.9
1976	RX[517]	4612.35	426.9
1977	S[853]	4602.65	66.9
1978	S[854]	4592.95	186.9
1979	S[855]	4583.25	306.9
1980	RX[516]	4573.55	426.9
1981	S[856]	4563.85	66.9
1982	S[857]	4554.15	186.9
1983	S[858]	4544.45	306.9
1984	RX[515]	4534.75	426.9
1985	S[859]	4525.05	66.9
1986	S[860]	4515.35	186.9
1987	S[861]	4505.65	306.9
1988	RX[514]	4495.95	426.9
1989	S[862]	4486.25	66.9
1990	S[863]	4476.55	186.9

No.	PAD Name	X	Y
1991	S[864]	4466.85	306.9
1992	RX[513]	4457.15	426.9
1993	S[865]	4447.45	66.9
1994	S[866]	4437.75	186.9
1995	S[867]	4428.05	306.9
1996	RX[512]	4418.35	426.9
1997	S[868]	4408.65	66.9
1998	S[869]	4398.95	186.9
1999	S[870]	4389.25	306.9
2000	RX[511]	4379.55	426.9
2001	S[871]	4369.85	66.9
2002	S[872]	4360.15	186.9
2003	S[873]	4350.45	306.9
2004	RX[510]	4340.75	426.9
2005	S[874]	4331.05	66.9
2006	S[875]	4321.35	186.9
2007	S[876]	4311.65	306.9
2008	RX[509]	4301.95	426.9
2009	S[877]	4292.25	66.9
2010	S[878]	4282.55	186.9
2011	S[879]	4272.85	306.9
2012	RX[508]	4263.15	426.9
2013	S[880]	4253.45	66.9
2014	S[881]	4243.75	186.9
2015	S[882]	4234.05	306.9
2016	RX[507]	4224.35	426.9
2017	S[883]	4214.65	66.9
2018	S[884]	4204.95	186.9
2019	S[885]	4195.25	306.9
2020	RX[506]	4185.55	426.9
2021	S[886]	4175.85	66.9
2022	S[887]	4166.15	186.9
2023	S[888]	4156.45	306.9
2024	RX[505]	4146.75	426.9
2025	S[889]	4137.05	66.9
2026	S[890]	4127.35	186.9
2027	S[891]	4117.65	306.9
2028	RX[504]	4107.95	426.9
2029	S[892]	4098.25	66.9
2030	S[893]	4088.55	186.9
2031	S[894]	4078.85	306.9
2032	RX[503]	4069.15	426.9
2033	S[895]	4059.45	66.9
2034	S[896]	4049.75	186.9
2035	S[897]	4040.05	306.9
2036	RX[502]	4030.35	426.9
2037	S[898]	4020.65	66.9
2038	S[899]	4010.95	186.9
2039	S[900]	4001.25	306.9
2040	RX[501]	3991.55	426.9
2041	S[901]	3981.85	66.9
2042	S[902]	3972.15	186.9
2043	S[903]	3962.45	306.9
2044	RX[500]	3952.75	426.9
2045	S[904]	3943.05	66.9
2046	S[905]	3933.35	186.9
2047	S[906]	3923.65	306.9
2048	RX[499]	3913.95	426.9
2049	S[907]	3904.25	66.9
2050	S[908]	3894.55	186.9
2051	S[909]	3884.85	306.9
2052	RX[498]	3875.15	426.9
2053	S[910]	3865.45	66.9
2054	S[911]	3855.75	186.9
2055	S[912]	3846.05	306.9
2056	RX[497]	3836.35	426.9
2057	S[913]	3826.65	66.9
2058	S[914]	3816.95	186.9
2059	S[915]	3807.25	306.9
2060	RX[496]	3797.55	426.9
2061	S[916]	3787.85	66.9
2062	S[917]	3778.15	186.9
2063	S[918]	3768.45	306.9
2064	RX[495]	3758.75	426.9
2065	S[919]	3749.05	66.9
2066	S[920]	3739.35	186.9
2067	S[921]	3729.65	306.9
2068	RX[494]	3719.95	426.9
2069	S[922]	3710.25	66.9
2070	S[923]	3700.55	186.9
2071	S[924]	3690.85	306.9
2072	RX[493]	3681.15	426.9
2073	S[925]	3671.45	66.9
2074	S[926]	3661.75	186.9

No.	PAD Name	X	Y
2075	S[927]	3652.05	306.9
2076	RX[492]	3642.35	426.9
2077	S[928]	3632.65	66.9
2078	S[929]	3622.95	186.9
2079	S[930]	3613.25	306.9
2080	RX[491]	3603.55	426.9
2081	S[931]	3593.85	66.9
2082	S[932]	3584.15	186.9
2083	S[933]	3574.45	306.9
2084	RX[490]	3564.75	426.9
2085	S[934]	3555.05	66.9
2086	S[935]	3545.35	186.9
2087	S[936]	3535.65	306.9
2088	RX[489]	3525.95	426.9
2089	S[937]	3516.25	66.9
2090	S[938]	3506.55	186.9
2091	S[939]	3496.85	306.9
2092	RX[488]	3487.15	426.9
2093	S[940]	3477.45	66.9
2094	S[941]	3467.75	186.9
2095	S[942]	3458.05	306.9
2096	RX[487]	3448.35	426.9
2097	S[943]	3438.65	66.9
2098	S[944]	3428.95	186.9
2099	S[945]	3419.25	306.9
2100	RX[486]	3409.55	426.9
2101	S[946]	3399.85	66.9
2102	S[947]	3390.15	186.9
2103	S[948]	3380.45	306.9
2104	RX[485]	3370.75	426.9
2105	S[949]	3361.05	66.9
2106	S[950]	3351.35	186.9
2107	S[951]	3341.65	306.9
2108	RX[484]	3331.95	426.9
2109	S[952]	3322.25	66.9
2110	S[953]	3312.55	186.9
2111	S[954]	3302.85	306.9
2112	RX[483]	3293.15	426.9
2113	S[955]	3283.45	66.9
2114	S[956]	3273.75	186.9
2115	S[957]	3264.05	306.9
2116	RX[482]	3254.35	426.9
2117	S[958]	3244.65	66.9
2118	S[959]	3234.95	186.9
2119	S[960]	3225.25	306.9
2120	RX[481]	3215.55	426.9
2121	S[961]	3205.85	66.9
2122	S[962]	3196.15	186.9
2123	S[963]	3186.45	306.9
2124	RX[480]	3176.75	426.9
2125	S[964]	3167.05	66.9
2126	S[965]	3157.35	186.9
2127	S[966]	3147.65	306.9
2128	RX[479]	3137.95	426.9
2129	S[967]	3128.25	66.9
2130	S[968]	3118.55	186.9
2131	S[969]	3108.85	306.9
2132	RX[478]	3099.15	426.9
2133	S[970]	3089.45	66.9
2134	S[971]	3079.75	186.9
2135	S[972]	3070.05	306.9
2136	RX[477]	3060.35	426.9
2137	S[973]	3050.65	66.9
2138	S[974]	3040.95	186.9
2139	S[975]	3031.25	306.9
2140	RX[476]	3021.55	426.9
2141	S[976]	3011.85	66.9
2142	S[977]	3002.15	186.9
2143	S[978]	2992.45	306.9
2144	RX[475]	2982.75	426.9
2145	S[979]	2973.05	66.9
2146	S[980]	2963.35	186.9
2147	S[981]	2953.65	306.9
2148	RX[474]	2943.95	426.9
2149	S[982]	2934.25	66.9
2150	S[983]	2924.55	186.9
2151	S[984]	2914.85	306.9
2152	RX[473]	2905.15	426.9
2153	S[985]	2895.45	66.9
2154	S[986]	2885.75	186.9
2155	S[987]	2876.05	306.9
2156	RX[472]	2866.35	426.9
2157	S[988]	2856.65	66.9
2158	S[989]	2846.95	186.9

No.	PAD Name	X	Y
2159	S[990]	2837.25	306.9
2160	RX[471]	2827.55	426.9
2161	S[991]	2817.85	66.9
2162	S[992]	2808.15	186.9
2163	S[993]	2798.45	306.9
2164	RX[470]	2788.75	426.9
2165	S[994]	2779.05	66.9
2166	S[995]	2769.35	186.9
2167	S[996]	2759.65	306.9
2168	RX[469]	2749.95	426.9
2169	S[997]	2740.25	66.9
2170	S[998]	2730.55	186.9
2171	S[999]	2720.85	306.9
2172	RX[468]	2711.15	426.9
2173	S[1000]	2701.45	66.9
2174	S[1001]	2691.75	186.9
2175	S[1002]	2682.05	306.9
2176	RX[467]	2672.35	426.9
2177	S[1003]	2662.65	66.9
2178	S[1004]	2652.95	186.9
2179	S[1005]	2643.25	306.9
2180	RX[466]	2633.55	426.9
2181	S[1006]	2623.85	66.9
2182	S[1007]	2614.15	186.9
2183	S[1008]	2604.45	306.9
2184	RX[465]	2594.75	426.9
2185	S[1009]	2585.05	66.9
2186	S[1010]	2575.35	186.9
2187	S[1011]	2565.65	306.9
2188	RX[464]	2555.95	426.9
2189	S[1012]	2546.25	66.9
2190	S[1013]	2536.55	186.9
2191	S[1014]	2526.85	306.9
2192	RX[463]	2517.15	426.9
2193	S[1015]	2507.45	66.9
2194	S[1016]	2497.75	186.9
2195	S[1017]	2488.05	306.9
2196	RX[462]	2478.35	426.9
2197	S[1018]	2468.65	66.9
2198	S[1019]	2458.95	186.9
2199	S[1020]	2449.25	306.9
2200	RX[461]	2439.55	426.9
2201	S[1021]	2429.85	66.9
2202	S[1022]	2420.15	186.9
2203	S[1023]	2410.45	306.9
2204	RX[460]	2400.75	426.9
2205	S[1024]	2391.05	66.9
2206	S[1025]	2381.35	186.9
2207	S[1026]	2371.65	306.9
2208	RX[459]	2361.95	426.9
2209	S[1027]	2352.25	66.9
2210	S[1028]	2342.55	186.9
2211	S[1029]	2332.85	306.9
2212	RX[458]	2323.15	426.9
2213	S[1030]	2313.45	66.9
2214	S[1031]	2303.75	186.9
2215	S[1032]	2294.05	306.9
2216	RX[457]	2284.35	426.9
2217	S[1033]	2274.65	66.9
2218	S[1034]	2264.95	186.9
2219	S[1035]	2255.25	306.9
2220	RX[456]	2245.55	426.9
2221	S[1036]	2235.85	66.9
2222	S[1037]	2226.15	186.9
2223	S[1038]	2216.45	306.9
2224	RX[455]	2206.75	426.9
2225	S[1039]	2197.05	66.9
2226	S[1040]	2187.35	186.9
2227	S[1041]	2177.65	306.9
2228	RX[454]	2167.95	426.9
2229	S[1042]	2158.25	66.9
2230	S[1043]	2148.55	186.9
2231	S[1044]	2138.85	306.9
2232	RX[453]	2129.15	426.9
2233	S[1045]	2119.45	66.9
2234	S[1046]	2109.75	186.9
2235	S[1047]	2100.05	306.9
2236	RX[452]	2090.35	426.9
2237	S[1048]	2080.65	66.9
2238	S[1049]	2070.95	186.9
2239	S[1050]	2061.25	306.9
2240	RX[451]	2051.55	426.9
2241	S[1051]	2041.85	66.9
2242	S[1052]	2032.15	186.9

No.	PAD Name	X	Y
2243	S[1053]	2022.45	306.9
2244	RX[450]	2012.75	426.9
2245	S[1054]	2003.05	66.9
2246	S[1055]	1993.35	186.9
2247	S[1056]	1983.65	306.9
2248	RX[449]	1973.95	426.9
2249	S[1057]	1964.25	66.9
2250	S[1058]	1954.55	186.9
2251	S[1059]	1944.85	306.9
2252	RX[448]	1935.15	426.9
2253	S[1060]	1925.45	66.9
2254	S[1061]	1915.75	186.9
2255	S[1062]	1906.05	306.9
2256	RX[447]	1896.35	426.9
2257	S[1063]	1886.65	66.9
2258	S[1064]	1876.95	186.9
2259	S[1065]	1867.25	306.9
2260	RX[446]	1857.55	426.9
2261	S[1066]	1847.85	66.9
2262	S[1067]	1838.15	186.9
2263	S[1068]	1828.45	306.9
2264	RX[445]	1818.75	426.9
2265	S[1069]	1809.05	66.9
2266	S[1070]	1799.35	186.9
2267	S[1071]	1789.65	306.9
2268	RX[444]	1779.95	426.9
2269	S[1072]	1770.25	66.9
2270	S[1073]	1760.55	186.9
2271	S[1074]	1750.85	306.9
2272	RX[443]	1741.15	426.9
2273	S[1075]	1731.45	66.9
2274	S[1076]	1721.75	186.9
2275	S[1077]	1712.05	306.9
2276	RX[442]	1702.35	426.9
2277	S[1078]	1692.65	66.9
2278	S[1079]	1682.95	186.9
2279	S[1080]	1673.25	306.9
2280	RX[441]	1663.55	426.9
2281	S[1081]	1653.85	66.9
2282	S[1082]	1644.15	186.9
2283	S[1083]	1634.45	306.9
2284	RX[440]	1624.75	426.9
2285	S[1084]	1615.05	66.9
2286	S[1085]	1605.35	186.9
2287	S[1086]	1595.65	306.9
2288	RX[439]	1585.95	426.9
2289	S[1087]	1576.25	66.9
2290	S[1088]	1566.55	186.9
2291	S[1089]	1556.85	306.9
2292	RX[438]	1547.15	426.9
2293	S[1090]	1537.45	66.9
2294	S[1091]	1527.75	186.9
2295	S[1092]	1518.05	306.9
2296	RX[437]	1508.35	426.9
2297	S[1093]	1498.65	66.9
2298	S[1094]	1488.95	186.9
2299	S[1095]	1479.25	306.9
2300	RX[436]	1469.55	426.9
2301	S[1096]	1459.85	66.9
2302	S[1097]	1450.15	186.9
2303	S[1098]	1440.45	306.9
2304	RX[435]	1430.75	426.9
2305	S[1099]	1421.05	66.9
2306	S[1100]	1411.35	186.9
2307	S[1101]	1401.65	306.9
2308	RX[434]	1391.95	426.9
2309	S[1102]	1382.25	66.9
2310	S[1103]	1372.55	186.9
2311	S[1104]	1362.85	306.9
2312	RX[433]	1353.15	426.9
2313	S[1105]	1343.45	66.9
2314	S[1106]	1333.75	186.9
2315	S[1107]	1324.05	306.9
2316	RX[432]	1314.35	426.9
2317	S[1108]	1304.65	66.9
2318	S[1109]	1294.95	186.9
2319	S[1110]	1285.25	306.9
2320	RX[431]	1275.55	426.9
2321	S[1111]	1265.85	66.9
2322	S[1112]	1256.15	186.9
2323	S[1113]	1246.45	306.9
2324	RX[430]	1236.75	426.9
2325	S[1114]	1227.05	66.9
2326	S[1115]	1217.35	186.9

No.	PAD Name	X	Y
2327	S[1116]	1207.65	306.9
2328	RX[429]	1197.95	426.9
2329	S[1117]	1188.25	66.9
2330	S[1118]	1178.55	186.9
2331	S[1119]	1168.85	306.9
2332	RX[428]	1159.15	426.9
2333	S[1120]	1149.45	66.9
2334	S[1121]	1139.75	186.9
2335	S[1122]	1130.05	306.9
2336	RX[427]	1120.35	426.9
2337	S[1123]	1110.65	66.9
2338	S[1124]	1100.95	186.9
2339	S[1125]	1091.25	306.9
2340	RX[426]	1081.55	426.9
2341	S[1126]	1071.85	66.9
2342	S[1127]	1062.15	186.9
2343	S[1128]	1052.45	306.9
2344	RX[425]	1042.75	426.9
2345	S[1129]	1033.05	66.9
2346	S[1130]	1023.35	186.9
2347	S[1131]	1013.65	306.9
2348	RX[424]	1003.95	426.9
2349	S[1132]	994.25	66.9
2350	S[1133]	984.55	186.9
2351	S[1134]	974.85	306.9
2352	RX[423]	965.15	426.9
2353	S[1135]	955.45	66.9
2354	S[1136]	945.75	186.9
2355	S[1137]	936.05	306.9
2356	RX[422]	926.35	426.9
2357	S[1138]	916.65	66.9
2358	S[1139]	906.95	186.9
2359	S[1140]	897.25	306.9
2360	RX[421]	887.55	426.9
2361	S[1141]	877.85	66.9
2362	S[1142]	868.15	186.9
2363	S[1143]	858.45	306.9
2364	RX[420]	848.75	426.9
2365	S[1144]	839.05	66.9
2366	S[1145]	829.35	186.9
2367	S[1146]	819.65	306.9
2368	RX[419]	809.95	426.9
2369	S[1147]	800.25	66.9
2370	S[1148]	790.55	186.9
2371	S[1149]	780.85	306.9
2372	RX[418]	771.15	426.9
2373	S[1150]	761.45	66.9
2374	S[1151]	751.75	186.9
2375	S[1152]	742.05	306.9
2376	RX[417]	732.35	426.9
2377	S[1153]	722.65	66.9
2378	S[1154]	712.95	186.9
2379	S[1155]	703.25	306.9
2380	RX[416]	693.55	426.9
2381	S[1156]	683.85	66.9
2382	S[1157]	674.15	186.9
2383	S[1158]	664.45	306.9
2384	RX[415]	654.75	426.9
2385	S[1159]	645.05	66.9
2386	S[1160]	635.35	186.9
2387	S[1161]	625.65	306.9
2388	RX[414]	615.95	426.9
2389	S[1162]	606.25	66.9
2390	S[1163]	596.55	186.9
2391	S[1164]	586.85	306.9
2392	RX[413]	577.15	426.9
2393	S[1165]	567.45	66.9
2394	S[1166]	557.75	186.9
2395	S[1167]	548.05	306.9
2396	RX[412]	538.35	426.9
2397	S[1168]	528.65	66.9
2398	S[1169]	518.95	186.9
2399	S[1170]	509.25	306.9
2400	RX[411]	499.55	426.9
2401	S[1171]	489.85	66.9
2402	S[1172]	480.15	186.9
2403	S[1173]	470.45	306.9
2404	RX[410]	460.75	426.9
2405	S[1174]	451.05	66.9
2406	S[1175]	441.35	186.9
2407	S[1176]	431.65	306.9
2408	RX[409]	421.95	426.9
2409	S[1177]	412.25	66.9
2410	S[1178]	402.55	186.9

No.	PAD Name	X	Y
2411	S[1179]	392.85	306.9
2412	RX[408]	383.15	426.9
2413	S[1180]	373.45	66.9
2414	S[1181]	363.75	186.9
2415	S[1182]	354.05	306.9
2416	RX[407]	344.35	426.9
2417	S[1183]	334.65	66.9
2418	S[1184]	324.95	186.9
2419	S[1185]	315.25	306.9
2420	RX[406]	305.55	426.9
2421	S[1186]	295.85	66.9
2422	S[1187]	286.15	186.9
2423	S[1188]	276.45	306.9
2424	RX[405]	266.75	426.9
2425	S[1189]	257.05	66.9
2426	S[1190]	247.35	186.9
2427	S[1191]	237.65	306.9
2428	RX[404]	227.95	426.9
2429	S[1192]	218.25	66.9
2430	S[1193]	208.55	186.9
2431	S[1194]	198.85	306.9
2432	RX[403]	189.15	426.9
2433	S[1195]	179.45	66.9
2434	S[1196]	169.75	186.9
2435	S[1197]	160.05	306.9
2436	RX[402]	150.35	426.9
2437	S[1198]	140.65	66.9
2438	S[1199]	130.95	186.9
2439	S[1200]	121.25	306.9
2440	RX[401]	111.55	426.9
2441	AVSS	101.85	66.9
2442	AVSS	92.15	186.9
2443	AVSS	82.45	306.9
2444	AVSS	72.75	426.9
2445	AVSS	63.05	66.9
2446	AVSS	53.35	186.9
2447	AVSS	43.65	306.9
2448	AVSS	33.95	426.9
2449	AVSS	24.25	66.9
2450	AVSS	14.55	186.9
2451	AVSS	4.85	306.9
2452	AVSS	-4.85	426.9
2453	AVSS	-14.55	66.9
2454	AVSS	-24.25	186.9
2455	AVSS	-33.95	306.9
2456	AVSS	-43.65	426.9
2457	AVSS	-53.35	66.9
2458	AVSS	-63.05	186.9
2459	AVSS	-72.75	306.9
2460	AVSS	-82.45	426.9
2461	AVSS	-92.15	66.9
2462	AVSS	-101.85	186.9
2463	AVSS	-111.55	306.9
2464	AVSS	-121.25	426.9
2465	S[1201]	-130.95	66.9
2466	S[1202]	-140.65	186.9
2467	S[1203]	-150.35	306.9
2468	RX[400]	-160.05	426.9
2469	S[1204]	-169.75	66.9
2470	S[1205]	-179.45	186.9
2471	S[1206]	-189.15	306.9
2472	RX[399]	-198.85	426.9
2473	S[1207]	-208.55	66.9
2474	S[1208]	-218.25	186.9
2475	S[1209]	-227.95	306.9
2476	RX[398]	-237.65	426.9
2477	S[1210]	-247.35	66.9
2478	S[1211]	-257.05	186.9
2479	S[1212]	-266.75	306.9
2480	RX[397]	-276.45	426.9
2481	S[1213]	-286.15	66.9
2482	S[1214]	-295.85	186.9
2483	S[1215]	-305.55	306.9
2484	RX[396]	-315.25	426.9
2485	S[1216]	-324.95	66.9
2486	S[1217]	-334.65	186.9
2487	S[1218]	-344.35	306.9
2488	RX[395]	-354.05	426.9
2489	S[1219]	-363.75	66.9
2490	S[1220]	-373.45	186.9
2491	S[1221]	-383.15	306.9
2492	RX[394]	-392.85	426.9
2493	S[1222]	-402.55	66.9
2494	S[1223]	-412.25	186.9

No.	PAD Name	X	Y
2495	S[1224]	-421.95	306.9
2496	RX[393]	-431.65	426.9
2497	S[1225]	-441.35	66.9
2498	S[1226]	-451.05	186.9
2499	S[1227]	-460.75	306.9
2500	RX[392]	-470.45	426.9
2501	S[1228]	-480.15	66.9
2502	S[1229]	-489.85	186.9
2503	S[1230]	-499.55	306.9
2504	RX[391]	-509.25	426.9
2505	S[1231]	-518.95	66.9
2506	S[1232]	-528.65	186.9
2507	S[1233]	-538.35	306.9
2508	RX[390]	-548.05	426.9
2509	S[1234]	-557.75	66.9
2510	S[1235]	-567.45	186.9
2511	S[1236]	-577.15	306.9
2512	RX[389]	-586.85	426.9
2513	S[1237]	-596.55	66.9
2514	S[1238]	-606.25	186.9
2515	S[1239]	-615.95	306.9
2516	RX[388]	-625.65	426.9
2517	S[1240]	-635.35	66.9
2518	S[1241]	-645.05	186.9
2519	S[1242]	-654.75	306.9
2520	RX[387]	-664.45	426.9
2521	S[1243]	-674.15	66.9
2522	S[1244]	-683.85	186.9
2523	S[1245]	-693.55	306.9
2524	RX[386]	-703.25	426.9
2525	S[1246]	-712.95	66.9
2526	S[1247]	-722.65	186.9
2527	S[1248]	-732.35	306.9
2528	RX[385]	-742.05	426.9
2529	S[1249]	-751.75	66.9
2530	S[1250]	-761.45	186.9
2531	S[1251]	-771.15	306.9
2532	RX[384]	-780.85	426.9
2533	S[1252]	-790.55	66.9
2534	S[1253]	-800.25	186.9
2535	S[1254]	-809.95	306.9
2536	RX[383]	-819.65	426.9
2537	S[1255]	-829.35	66.9
2538	S[1256]	-839.05	186.9
2539	S[1257]	-848.75	306.9
2540	RX[382]	-858.45	426.9
2541	S[1258]	-868.15	66.9
2542	S[1259]	-877.85	186.9
2543	S[1260]	-887.55	306.9
2544	RX[381]	-897.25	426.9
2545	S[1261]	-906.95	66.9
2546	S[1262]	-916.65	186.9
2547	S[1263]	-926.35	306.9
2548	RX[380]	-936.05	426.9
2549	S[1264]	-945.75	66.9
2550	S[1265]	-955.45	186.9
2551	S[1266]	-965.15	306.9
2552	RX[379]	-974.85	426.9
2553	S[1267]	-984.55	66.9
2554	S[1268]	-994.25	186.9
2555	S[1269]	-1003.95	306.9
2556	RX[378]	-1013.65	426.9
2557	S[1270]	-1023.35	66.9
2558	S[1271]	-1033.05	186.9
2559	S[1272]	-1042.75	306.9
2560	RX[377]	-1052.45	426.9
2561	S[1273]	-1062.15	66.9
2562	S[1274]	-1071.85	186.9
2563	S[1275]	-1081.55	306.9
2564	RX[376]	-1091.25	426.9
2565	S[1276]	-1100.95	66.9
2566	S[1277]	-1110.65	186.9
2567	S[1278]	-1120.35	306.9
2568	RX[375]	-1130.05	426.9
2569	S[1279]	-1139.75	66.9
2570	S[1280]	-1149.45	186.9
2571	S[1281]	-1159.15	306.9
2572	RX[374]	-1168.85	426.9
2573	S[1282]	-1178.55	66.9
2574	S[1283]	-1188.25	186.9
2575	S[1284]	-1197.95	306.9
2576	RX[373]	-1207.65	426.9
2577	S[1285]	-1217.35	66.9
2578	S[1286]	-1227.05	186.9

No.	PAD Name	X	Y
2579	S[1287]	-1236.75	306.9
2580	RX[372]	-1246.45	426.9
2581	S[1288]	-1256.15	66.9
2582	S[1289]	-1265.85	186.9
2583	S[1290]	-1275.55	306.9
2584	RX[371]	-1285.25	426.9
2585	S[1291]	-1294.95	66.9
2586	S[1292]	-1304.65	186.9
2587	S[1293]	-1314.35	306.9
2588	RX[370]	-1324.05	426.9
2589	S[1294]	-1333.75	66.9
2590	S[1295]	-1343.45	186.9
2591	S[1296]	-1353.15	306.9
2592	RX[369]	-1362.85	426.9
2593	S[1297]	-1372.55	66.9
2594	S[1298]	-1382.25	186.9
2595	S[1299]	-1391.95	306.9
2596	RX[368]	-1401.65	426.9
2597	S[1300]	-1411.35	66.9
2598	S[1301]	-1421.05	186.9
2599	S[1302]	-1430.75	306.9
2600	RX[367]	-1440.45	426.9
2601	S[1303]	-1450.15	66.9
2602	S[1304]	-1459.85	186.9
2603	S[1305]	-1469.55	306.9
2604	RX[366]	-1479.25	426.9
2605	S[1306]	-1488.95	66.9
2606	S[1307]	-1498.65	186.9
2607	S[1308]	-1508.35	306.9
2608	RX[365]	-1518.05	426.9
2609	S[1309]	-1527.75	66.9
2610	S[1310]	-1537.45	186.9
2611	S[1311]	-1547.15	306.9
2612	RX[364]	-1556.85	426.9
2613	S[1312]	-1566.55	66.9
2614	S[1313]	-1576.25	186.9
2615	S[1314]	-1585.95	306.9
2616	RX[363]	-1595.65	426.9
2617	S[1315]	-1605.35	66.9
2618	S[1316]	-1615.05	186.9
2619	S[1317]	-1624.75	306.9
2620	RX[362]	-1634.45	426.9
2621	S[1318]	-1644.15	66.9
2622	S[1319]	-1653.85	186.9
2623	S[1320]	-1663.55	306.9
2624	RX[361]	-1673.25	426.9
2625	S[1321]	-1682.95	66.9
2626	S[1322]	-1692.65	186.9
2627	S[1323]	-1702.35	306.9
2628	RX[360]	-1712.05	426.9
2629	S[1324]	-1721.75	66.9
2630	S[1325]	-1731.45	186.9
2631	S[1326]	-1741.15	306.9
2632	RX[359]	-1750.85	426.9
2633	S[1327]	-1760.55	66.9
2634	S[1328]	-1770.25	186.9
2635	S[1329]	-1779.95	306.9
2636	RX[358]	-1789.65	426.9
2637	S[1330]	-1799.35	66.9
2638	S[1331]	-1809.05	186.9
2639	S[1332]	-1818.75	306.9
2640	RX[357]	-1828.45	426.9
2641	S[1333]	-1838.15	66.9
2642	S[1334]	-1847.85	186.9
2643	S[1335]	-1857.55	306.9
2644	RX[356]	-1867.25	426.9
2645	S[1336]	-1876.95	66.9
2646	S[1337]	-1886.65	186.9
2647	S[1338]	-1896.35	306.9
2648	RX[355]	-1906.05	426.9
2649	S[1339]	-1915.75	66.9
2650	S[1340]	-1925.45	186.9
2651	S[1341]	-1935.15	306.9
2652	RX[354]	-1944.85	426.9
2653	S[1342]	-1954.55	66.9
2654	S[1343]	-1964.25	186.9
2655	S[1344]	-1973.95	306.9
2656	RX[353]	-1983.65	426.9
2657	S[1345]	-1993.35	66.9
2658	S[1346]	-2003.05	186.9
2659	S[1347]	-2012.75	306.9
2660	RX[352]	-2022.45	426.9
2661	S[1348]	-2032.15	66.9
2662	S[1349]	-2041.85	186.9

No.	PAD Name	X	Y
2663	S[1350]	-2051.55	306.9
2664	RX[351]	-2061.25	426.9
2665	S[1351]	-2070.95	66.9
2666	S[1352]	-2080.65	186.9
2667	S[1353]	-2090.35	306.9
2668	RX[350]	-2100.05	426.9
2669	S[1354]	-2109.75	66.9
2670	S[1355]	-2119.45	186.9
2671	S[1356]	-2129.15	306.9
2672	RX[349]	-2138.85	426.9
2673	S[1357]	-2148.55	66.9
2674	S[1358]	-2158.25	186.9
2675	S[1359]	-2167.95	306.9
2676	RX[348]	-2177.65	426.9
2677	S[1360]	-2187.35	66.9
2678	S[1361]	-2197.05	186.9
2679	S[1362]	-2206.75	306.9
2680	RX[347]	-2216.45	426.9
2681	S[1363]	-2226.15	66.9
2682	S[1364]	-2235.85	186.9
2683	S[1365]	-2245.55	306.9
2684	RX[346]	-2255.25	426.9
2685	S[1366]	-2264.95	66.9
2686	S[1367]	-2274.65	186.9
2687	S[1368]	-2284.35	306.9
2688	RX[345]	-2294.05	426.9
2689	S[1369]	-2303.75	66.9
2690	S[1370]	-2313.45	186.9
2691	S[1371]	-2323.15	306.9
2692	RX[344]	-2332.85	426.9
2693	S[1372]	-2342.55	66.9
2694	S[1373]	-2352.25	186.9
2695	S[1374]	-2361.95	306.9
2696	RX[343]	-2371.65	426.9
2697	S[1375]	-2381.35	66.9
2698	S[1376]	-2391.05	186.9
2699	S[1377]	-2400.75	306.9
2700	RX[342]	-2410.45	426.9
2701	S[1378]	-2420.15	66.9
2702	S[1379]	-2429.85	186.9
2703	S[1380]	-2439.55	306.9
2704	RX[341]	-2449.25	426.9
2705	S[1381]	-2458.95	66.9
2706	S[1382]	-2468.65	186.9
2707	S[1383]	-2478.35	306.9
2708	RX[340]	-2488.05	426.9
2709	S[1384]	-2497.75	66.9
2710	S[1385]	-2507.45	186.9
2711	S[1386]	-2517.15	306.9
2712	RX[339]	-2526.85	426.9
2713	S[1387]	-2536.55	66.9
2714	S[1388]	-2546.25	186.9
2715	S[1389]	-2555.95	306.9
2716	RX[338]	-2565.65	426.9
2717	S[1390]	-2575.35	66.9
2718	S[1391]	-2585.05	186.9
2719	S[1392]	-2594.75	306.9
2720	RX[337]	-2604.45	426.9
2721	S[1393]	-2614.15	66.9
2722	S[1394]	-2623.85	186.9
2723	S[1395]	-2633.55	306.9
2724	RX[336]	-2643.25	426.9
2725	S[1396]	-2652.95	66.9
2726	S[1397]	-2662.65	186.9
2727	S[1398]	-2672.35	306.9
2728	RX[335]	-2682.05	426.9
2729	S[1399]	-2691.75	66.9
2730	S[1400]	-2701.45	186.9
2731	S[1401]	-2711.15	306.9
2732	RX[334]	-2720.85	426.9
2733	S[1402]	-2730.55	66.9
2734	S[1403]	-2740.25	186.9
2735	S[1404]	-2749.95	306.9
2736	RX[333]	-2759.65	426.9
2737	S[1405]	-2769.35	66.9
2738	S[1406]	-2779.05	186.9
2739	S[1407]	-2788.75	306.9
2740	RX[332]	-2798.45	426.9
2741	S[1408]	-2808.15	66.9
2742	S[1409]	-2817.85	186.9
2743	S[1410]	-2827.55	306.9
2744	RX[331]	-2837.25	426.9
2745	S[1411]	-2846.95	66.9
2746	S[1412]	-2856.65	186.9

No.	PAD Name	X	Y
2747	S[1413]	-2866.35	306.9
2748	RX[330]	-2876.05	426.9
2749	S[1414]	-2885.75	66.9
2750	S[1415]	-2895.45	186.9
2751	S[1416]	-2905.15	306.9
2752	RX[329]	-2914.85	426.9
2753	S[1417]	-2924.55	66.9
2754	S[1418]	-2934.25	186.9
2755	S[1419]	-2943.95	306.9
2756	RX[328]	-2953.65	426.9
2757	S[1420]	-2963.35	66.9
2758	S[1421]	-2973.05	186.9
2759	S[1422]	-2982.75	306.9
2760	RX[327]	-2992.45	426.9
2761	S[1423]	-3002.15	66.9
2762	S[1424]	-3011.85	186.9
2763	S[1425]	-3021.55	306.9
2764	RX[326]	-3031.25	426.9
2765	S[1426]	-3040.95	66.9
2766	S[1427]	-3050.65	186.9
2767	S[1428]	-3060.35	306.9
2768	RX[325]	-3070.05	426.9
2769	S[1429]	-3079.75	66.9
2770	S[1430]	-3089.45	186.9
2771	S[1431]	-3099.15	306.9
2772	RX[324]	-3108.85	426.9
2773	S[1432]	-3118.55	66.9
2774	S[1433]	-3128.25	186.9
2775	S[1434]	-3137.95	306.9
2776	RX[323]	-3147.65	426.9
2777	S[1435]	-3157.35	66.9
2778	S[1436]	-3167.05	186.9
2779	S[1437]	-3176.75	306.9
2780	RX[322]	-3186.45	426.9
2781	S[1438]	-3196.15	66.9
2782	S[1439]	-3205.85	186.9
2783	S[1440]	-3215.55	306.9
2784	RX[321]	-3225.25	426.9
2785	S[1441]	-3234.95	66.9
2786	S[1442]	-3244.65	186.9
2787	S[1443]	-3254.35	306.9
2788	RX[320]	-3264.05	426.9
2789	S[1444]	-3273.75	66.9
2790	S[1445]	-3283.45	186.9
2791	S[1446]	-3293.15	306.9
2792	RX[319]	-3302.85	426.9
2793	S[1447]	-3312.55	66.9
2794	S[1448]	-3322.25	186.9
2795	S[1449]	-3331.95	306.9
2796	RX[318]	-3341.65	426.9
2797	S[1450]	-3351.35	66.9
2798	S[1451]	-3361.05	186.9
2799	S[1452]	-3370.75	306.9
2800	RX[317]	-3380.45	426.9
2801	S[1453]	-3390.15	66.9
2802	S[1454]	-3399.85	186.9
2803	S[1455]	-3409.55	306.9
2804	RX[316]	-3419.25	426.9
2805	S[1456]	-3428.95	66.9
2806	S[1457]	-3438.65	186.9
2807	S[1458]	-3448.35	306.9
2808	RX[315]	-3458.05	426.9
2809	S[1459]	-3467.75	66.9
2810	S[1460]	-3477.45	186.9
2811	S[1461]	-3487.15	306.9
2812	RX[314]	-3496.85	426.9
2813	S[1462]	-3506.55	66.9
2814	S[1463]	-3516.25	186.9
2815	S[1464]	-3525.95	306.9
2816	RX[313]	-3535.65	426.9
2817	S[1465]	-3545.35	66.9
2818	S[1466]	-3555.05	186.9
2819	S[1467]	-3564.75	306.9
2820	RX[312]	-3574.45	426.9
2821	S[1468]	-3584.15	66.9
2822	S[1469]	-3593.85	186.9
2823	S[1470]	-3603.55	306.9
2824	RX[311]	-3613.25	426.9
2825	S[1471]	-3622.95	66.9
2826	S[1472]	-3632.65	186.9
2827	S[1473]	-3642.35	306.9
2828	RX[310]	-3652.05	426.9
2829	S[1474]	-3661.75	66.9
2830	S[1475]	-3671.45	186.9
2831	S[1476]	-3681.15	306.9
2832	RX[309]	-3690.85	426.9
2833	S[1477]	-3700.55	66.9
2834	S[1478]	-3710.25	186.9
2835	S[1479]	-3719.95	306.9
2836	RX[308]	-3729.65	426.9
2837	S[1480]	-3739.35	66.9
2838	S[1481]	-3749.05	186.9
2839	S[1482]	-3758.75	306.9
2840	RX[307]	-3768.45	426.9
2841	S[1483]	-3778.15	66.9
2842	S[1484]	-3787.85	186.9
2843	S[1485]	-3797.55	306.9
2844	RX[306]	-3807.25	426.9
2845	S[1486]	-3816.95	66.9
2846	S[1487]	-3826.65	186.9
2847	S[1488]	-3836.35	306.9
2848	RX[305]	-3846.05	426.9
2849	S[1489]	-3855.75	66.9
2850	S[1490]	-3865.45	186.9
2851	S[1491]	-3875.15	306.9
2852	RX[304]	-3884.85	426.9
2853	S[1492]	-3894.55	66.9
2854	S[1493]	-3904.25	186.9
2855	S[1494]	-3913.95	306.9
2856	RX[303]	-3923.65	426.9
2857	S[1495]	-3933.35	66.9
2858	S[1496]	-3943.05	186.9
2859	S[1497]	-3952.75	306.9
2860	RX[302]	-3962.45	426.9
2861	S[1498]	-3972.15	66.9
2862	S[1499]	-3981.85	186.9
2863	S[1500]	-3991.55	306.9
2864	RX[301]	-4001.25	426.9
2865	S[1501]	-4010.95	66.9
2866	S[1502]	-4020.65	186.9
2867	S[1503]	-4030.35	306.9
2868	RX[300]	-4040.05	426.9
2869	S[1504]	-4049.75	66.9
2870	S[1505]	-4059.45	186.9
2871	S[1506]	-4069.15	306.9
2872	RX[299]	-4078.85	426.9
2873	S[1507]	-4088.55	66.9
2874	S[1508]	-4098.25	186.9
2875	S[1509]	-4107.95	306.9
2876	RX[298]	-4117.65	426.9
2877	S[1510]	-4127.35	66.9
2878	S[1511]	-4137.05	186.9
2879	S[1512]	-4146.75	306.9
2880	RX[297]	-4156.45	426.9
2881	S[1513]	-4166.15	66.9
2882	S[1514]	-4175.85	186.9
2883	S[1515]	-4185.55	306.9
2884	RX[296]	-4195.25	426.9
2885	S[1516]	-4204.95	66.9
2886	S[1517]	-4214.65	186.9
2887	S[1518]	-4224.35	306.9
2888	RX[295]	-4234.05	426.9
2889	S[1519]	-4243.75	66.9
2890	S[1520]	-4253.45	186.9
2891	S[1521]	-4263.15	306.9
2892	RX[294]	-4272.85	426.9
2893	S[1522]	-4282.55	66.9
2894	S[1523]	-4292.25	186.9
2895	S[1524]	-4301.95	306.9
2896	RX[293]	-4311.65	426.9
2897	S[1525]	-4321.35	66.9
2898	S[1526]	-4331.05	186.9
2899	S[1527]	-4340.75	306.9
2900	RX[292]	-4350.45	426.9
2901	S[1528]	-4360.15	66.9
2902	S[1529]	-4369.85	186.9
2903	S[1530]	-4379.55	306.9
2904	RX[291]	-4389.25	426.9
2905	S[1531]	-4398.95	66.9
2906	S[1532]	-4408.65	186.9
2907	S[1533]	-4418.35	306.9
2908	RX[290]	-4428.05	426.9
2909	S[1534]	-4437.75	66.9
2910	S[1535]	-4447.45	186.9
2911	S[1536]	-4457.15	306.9
2912	RX[289]	-4466.85	426.9
2913	S[1537]	-4476.55	66.9
2914	S[1538]	-4486.25	186.9
2915	S[1539]	-4495.95	306.9
2916	RX[288]	-4505.65	426.9
2917	S[1540]	-4515.35	66.9
2918	S[1541]	-4525.05	186.9
2919	S[1542]	-4534.75	306.9
2920	RX[287]	-4544.45	426.9
2921	S[1543]	-4554.15	66.9
2922	S[1544]	-4563.85	186.9
2923	S[1545]	-4573.55	306.9
2924	RX[286]	-4583.25	426.9
2925	S[1546]	-4592.95	66.9
2926	S[1547]	-4602.65	186.9
2927	S[1548]	-4612.35	306.9
2928	RX[285]	-4622.05	426.9
2929	S[1549]	-4631.75	66.9
2930	S[1550]	-4641.45	186.9
2931	S[1551]	-4651.15	306.9
2932	RX[284]	-4660.85	426.9
2933	S[1552]	-4670.55	66.9
2934	S[1553]	-4680.25	186.9
2935	S[1554]	-4689.95	306.9
2936	RX[283]	-4699.65	426.9
2937	S[1555]	-4709.35	66.9
2938	S[1556]	-4719.05	186.9
2939	S[1557]	-4728.75	306.9
2940	RX[282]	-4738.45	426.9
2941	S[1558]	-4748.15	66.9
2942	S[1559]	-4757.85	186.9
2943	S[1560]	-4767.55	306.9
2944	RX[281]	-4777.25	426.9
2945	S[1561]	-4786.95	66.9
2946	S[1562]	-4796.65	186.9
2947	S[1563]	-4806.35	306.9
2948	RX[280]	-4816.05	426.9
2949	S[1564]	-4825.75	66.9
2950	S[1565]	-4835.45	186.9
2951	S[1566]	-4845.15	306.9
2952	RX[279]	-4854.85	426.9
2953	S[1567]	-4864.55	66.9
2954	S[1568]	-4874.25	186.9
2955	S[1569]	-4883.95	306.9
2956	RX[278]	-4893.65	426.9
2957	S[1570]	-4903.35	66.9
2958	S[1571]	-4913.05	186.9
2959	S[1572]	-4922.75	306.9
2960	RX[277]	-4932.45	426.9
2961	S[1573]	-4942.15	66.9
2962	S[1574]	-4951.85	186.9
2963	S[1575]	-4961.55	306.9
2964	RX[276]	-4971.25	426.9
2965	S[1576]	-4980.95	66.9
2966	S[1577]	-4990.65	186.9
2967	S[1578]	-5000.35	306.9
2968	RX[275]	-5010.05	426.9
2969	S[1579]	-5019.75	66.9
2970	S[1580]	-5029.45	186.9
2971	S[1581]	-5039.15	306.9
2972	RX[274]	-5048.85	426.9
2973	S[1582]	-5058.55	66.9
2974	S[1583]	-5068.25	186.9
2975	S[1584]	-5077.95	306.9
2976	RX[273]	-5087.65	426.9
2977	S[1585]	-5097.35	66.9
2978	S[1586]	-5107.05	186.9
2979	S[1587]	-5116.75	306.9
2980	RX[272]	-5126.45	426.9
2981	S[1588]	-5136.15	66.9
2982	S[1589]	-5145.85	186.9
2983	S[1590]	-5155.55	306.9
2984	RX[271]	-5165.25	426.9
2985	S[1591]	-5174.95	66.9
2986	S[1592]	-5184.65	186.9
2987	S[1593]	-5194.35	306.9
2988	RX[270]	-5204.05	426.9
2989	S[1594]	-5213.75	66.9
2990	S[1595]	-5223.45	186.9
2991	S[1596]	-5233.15	306.9
2992	RX[269]	-5242.85	426.9
2993	S[1597]	-5252.55	66.9
2994	S[1598]	-5262.25	186.9
2995	S[1599]	-5271.95	306.9
2996	RX[268]	-5281.65	426.9
2997	S[1600]	-5291.35	66.9
2998	S[1601]	-5301.05	186.9

No.	PAD Name	X	Y
2999	S[1602]	-5310.75	306.9
3000	RX[267]	-5320.45	426.9
3001	S[1603]	-5330.15	66.9
3002	S[1604]	-5339.85	186.9
3003	S[1605]	-5349.55	306.9
3004	RX[266]	-5359.25	426.9
3005	S[1606]	-5368.95	66.9
3006	S[1607]	-5378.65	186.9
3007	S[1608]	-5388.35	306.9
3008	RX[265]	-5398.05	426.9
3009	S[1609]	-5407.75	66.9
3010	S[1610]	-5417.45	186.9
3011	S[1611]	-5427.15	306.9
3012	RX[264]	-5436.85	426.9
3013	S[1612]	-5446.55	66.9
3014	S[1613]	-5456.25	186.9
3015	S[1614]	-5465.95	306.9
3016	RX[263]	-5475.65	426.9
3017	S[1615]	-5485.35	66.9
3018	S[1616]	-5495.05	186.9
3019	S[1617]	-5504.75	306.9
3020	RX[262]	-5514.45	426.9
3021	S[1618]	-5524.15	66.9
3022	S[1619]	-5533.85	186.9
3023	S[1620]	-5543.55	306.9
3024	RX[261]	-5553.25	426.9
3025	S[1621]	-5562.95	66.9
3026	S[1622]	-5572.65	186.9
3027	S[1623]	-5582.35	306.9
3028	RX[260]	-5592.05	426.9
3029	S[1624]	-5601.75	66.9
3030	S[1625]	-5611.45	186.9
3031	S[1626]	-5621.15	306.9
3032	RX[259]	-5630.85	426.9
3033	S[1627]	-5640.55	66.9
3034	S[1628]	-5650.25	186.9
3035	S[1629]	-5659.95	306.9
3036	RX[258]	-5669.65	426.9
3037	S[1630]	-5679.35	66.9
3038	S[1631]	-5689.05	186.9
3039	S[1632]	-5698.75	306.9
3040	RX[257]	-5708.45	426.9
3041	S[1633]	-5718.15	66.9
3042	S[1634]	-5727.85	186.9
3043	S[1635]	-5737.55	306.9
3044	RX[256]	-5747.25	426.9
3045	S[1636]	-5756.95	66.9
3046	S[1637]	-5766.65	186.9
3047	S[1638]	-5776.35	306.9
3048	RX[255]	-5786.05	426.9
3049	S[1639]	-5795.75	66.9
3050	S[1640]	-5805.45	186.9
3051	S[1641]	-5815.15	306.9
3052	RX[254]	-5824.85	426.9
3053	S[1642]	-5834.55	66.9
3054	S[1643]	-5844.25	186.9
3055	S[1644]	-5853.95	306.9
3056	RX[253]	-5863.65	426.9
3057	S[1645]	-5873.35	66.9
3058	S[1646]	-5883.05	186.9
3059	S[1647]	-5892.75	306.9
3060	RX[252]	-5902.45	426.9
3061	S[1648]	-5912.15	66.9
3062	S[1649]	-5921.85	186.9
3063	S[1650]	-5931.55	306.9
3064	RX[251]	-5941.25	426.9
3065	S[1651]	-5950.95	66.9
3066	S[1652]	-5960.65	186.9
3067	S[1653]	-5970.35	306.9
3068	RX[250]	-5980.05	426.9
3069	S[1654]	-5989.75	66.9
3070	S[1655]	-5999.45	186.9
3071	S[1656]	-6009.15	306.9
3072	RX[249]	-6018.85	426.9
3073	S[1657]	-6028.55	66.9
3074	S[1658]	-6038.25	186.9
3075	S[1659]	-6047.95	306.9
3076	RX[248]	-6057.65	426.9
3077	S[1660]	-6067.35	66.9
3078	S[1661]	-6077.05	186.9
3079	S[1662]	-6086.75	306.9
3080	RX[247]	-6096.45	426.9
3081	S[1663]	-6106.15	66.9
3082	S[1664]	-6115.85	186.9
3083	S[1665]	-6125.55	306.9
3084	RX[246]	-6135.25	426.9
3085	S[1666]	-6144.95	66.9
3086	S[1667]	-6154.65	186.9
3087	S[1668]	-6164.35	306.9
3088	RX[245]	-6174.05	426.9
3089	S[1669]	-6183.75	66.9
3090	S[1670]	-6193.45	186.9
3091	S[1671]	-6203.15	306.9
3092	RX[244]	-6212.85	426.9
3093	S[1672]	-6222.55	66.9
3094	S[1673]	-6232.25	186.9
3095	S[1674]	-6241.95	306.9
3096	RX[243]	-6251.65	426.9
3097	S[1675]	-6261.35	66.9
3098	S[1676]	-6271.05	186.9
3099	S[1677]	-6280.75	306.9
3100	RX[242]	-6290.45	426.9
3101	S[1678]	-6300.15	66.9
3102	S[1679]	-6309.85	186.9
3103	S[1680]	-6319.55	306.9
3104	RX[241]	-6329.25	426.9
3105	S[1681]	-6338.95	66.9
3106	S[1682]	-6348.65	186.9
3107	S[1683]	-6358.35	306.9
3108	RX[240]	-6368.05	426.9
3109	S[1684]	-6377.75	66.9
3110	S[1685]	-6387.45	186.9
3111	S[1686]	-6397.15	306.9
3112	RX[239]	-6406.85	426.9
3113	S[1687]	-6416.55	66.9
3114	S[1688]	-6426.25	186.9
3115	S[1689]	-6435.95	306.9
3116	RX[238]	-6445.65	426.9
3117	S[1690]	-6455.35	66.9
3118	S[1691]	-6465.05	186.9
3119	S[1692]	-6474.75	306.9
3120	RX[237]	-6484.45	426.9
3121	S[1693]	-6494.15	66.9
3122	S[1694]	-6503.85	186.9
3123	S[1695]	-6513.55	306.9
3124	RX[236]	-6523.25	426.9
3125	S[1696]	-6532.95	66.9
3126	S[1697]	-6542.65	186.9
3127	S[1698]	-6552.35	306.9
3128	RX[235]	-6562.05	426.9
3129	S[1699]	-6571.75	66.9
3130	S[1700]	-6581.45	186.9
3131	S[1701]	-6591.15	306.9
3132	RX[234]	-6600.85	426.9
3133	S[1702]	-6610.55	66.9
3134	S[1703]	-6620.25	186.9
3135	S[1704]	-6629.95	306.9
3136	RX[233]	-6639.65	426.9
3137	S[1705]	-6649.35	66.9
3138	S[1706]	-6659.05	186.9
3139	S[1707]	-6668.75	306.9
3140	RX[232]	-6678.45	426.9
3141	S[1708]	-6688.15	66.9
3142	S[1709]	-6697.85	186.9
3143	S[1710]	-6707.55	306.9
3144	RX[231]	-6717.25	426.9
3145	S[1711]	-6726.95	66.9
3146	S[1712]	-6736.65	186.9
3147	S[1713]	-6746.35	306.9
3148	RX[230]	-6756.05	426.9
3149	S[1714]	-6765.75	66.9
3150	S[1715]	-6775.45	186.9
3151	S[1716]	-6785.15	306.9
3152	RX[229]	-6794.85	426.9
3153	S[1717]	-6804.55	66.9
3154	S[1718]	-6814.25	186.9
3155	S[1719]	-6823.95	306.9
3156	RX[228]	-6833.65	426.9
3157	S[1720]	-6843.35	66.9
3158	S[1721]	-6853.05	186.9
3159	S[1722]	-6862.75	306.9
3160	RX[227]	-6872.45	426.9
3161	S[1723]	-6882.15	66.9
3162	S[1724]	-6891.85	186.9
3163	S[1725]	-6901.55	306.9
3164	RX[226]	-6911.25	426.9
3165	S[1726]	-6920.95	66.9
3166	S[1727]	-6930.65	186.9
3167	S[1728]	-6940.35	306.9
3168	RX[225]	-6950.05	426.9
3169	S[1729]	-6959.75	66.9
3170	S[1730]	-6969.45	186.9
3171	S[1731]	-6979.15	306.9
3172	RX[224]	-6988.85	426.9
3173	S[1732]	-6998.55	66.9
3174	S[1733]	-7008.25	186.9
3175	S[1734]	-7017.95	306.9
3176	RX[223]	-7027.65	426.9
3177	S[1735]	-7037.35	66.9
3178	S[1736]	-7047.05	186.9
3179	S[1737]	-7056.75	306.9
3180	RX[222]	-7066.45	426.9
3181	S[1738]	-7076.15	66.9
3182	S[1739]	-7085.85	186.9
3183	S[1740]	-7095.55	306.9
3184	RX[221]	-7105.25	426.9
3185	S[1741]	-7114.95	66.9
3186	S[1742]	-7124.65	186.9
3187	S[1743]	-7134.35	306.9
3188	RX[220]	-7144.05	426.9
3189	S[1744]	-7153.75	66.9
3190	S[1745]	-7163.45	186.9
3191	S[1746]	-7173.15	306.9
3192	RX[219]	-7182.85	426.9
3193	S[1747]	-7192.55	66.9
3194	S[1748]	-7202.25	186.9
3195	S[1749]	-7211.95	306.9
3196	RX[218]	-7221.65	426.9
3197	S[1750]	-7231.35	66.9
3198	S[1751]	-7241.05	186.9
3199	S[1752]	-7250.75	306.9
3200	RX[217]	-7260.45	426.9
3201	S[1753]	-7270.15	66.9
3202	S[1754]	-7279.85	186.9
3203	S[1755]	-7289.55	306.9
3204	RX[216]	-7299.25	426.9
3205	S[1756]	-7308.95	66.9
3206	S[1757]	-7318.65	186.9
3207	S[1758]	-7328.35	306.9
3208	RX[215]	-7338.05	426.9
3209	S[1759]	-7347.75	66.9
3210	S[1760]	-7357.45	186.9
3211	S[1761]	-7367.15	306.9
3212	RX[214]	-7376.85	426.9
3213	S[1762]	-7386.55	66.9
3214	S[1763]	-7396.25	186.9
3215	S[1764]	-7405.95	306.9
3216	RX[213]	-7415.65	426.9
3217	S[1765]	-7425.35	66.9
3218	S[1766]	-7435.05	186.9
3219	S[1767]	-7444.75	306.9
3220	RX[212]	-7454.45	426.9
3221	S[1768]	-7464.15	66.9
3222	S[1769]	-7473.85	186.9
3223	S[1770]	-7483.55	306.9
3224	RX[211]	-7493.25	426.9
3225	S[1771]	-7502.95	66.9
3226	S[1772]	-7512.65	186.9
3227	S[1773]	-7522.35	306.9
3228	RX[210]	-7532.05	426.9
3229	S[1774]	-7541.75	66.9
3230	S[1775]	-7551.45	186.9
3231	S[1776]	-7561.15	306.9
3232	RX[209]	-7570.85	426.9
3233	S[1777]	-7580.55	66.9
3234	S[1778]	-7590.25	186.9
3235	S[1779]	-7599.95	306.9
3236	RX[208]	-7609.65	426.9
3237	S[1780]	-7619.35	66.9
3238	S[1781]	-7629.05	186.9
3239	S[1782]	-7638.75	306.9
3240	RX[207]	-7648.45	426.9
3241	S[1783]	-7658.15	66.9
3242	S[1784]	-7667.85	186.9
3243	S[1785]	-7677.55	306.9
3244	RX[206]	-7687.25	426.9
3245	S[1786]	-7696.95	66.9
3246	S[1787]	-7706.65	186.9
3247	S[1788]	-7716.35	306.9
3248	RX[205]	-7726.05	426.9
3249	S[1789]	-7735.75	66.9
3250	S[1790]	-7745.45	186.9

No.	PAD Name	X	Y
3251	S[1791]	-7755.15	306.9
3252	RX[204]	-7764.85	426.9
3253	S[1792]	-7774.55	66.9
3254	S[1793]	-7784.25	186.9
3255	S[1794]	-7793.95	306.9
3256	RX[203]	-7803.65	426.9
3257	S[1795]	-7813.35	66.9
3258	S[1796]	-7823.05	186.9
3259	S[1797]	-7832.75	306.9
3260	RX[202]	-7842.45	426.9
3261	S[1798]	-7852.15	66.9
3262	S[1799]	-7861.85	186.9
3263	S[1800]	-7871.55	306.9
3264	RX[201]	-7881.25	426.9
3265	S[1801]	-7890.95	66.9
3266	S[1802]	-7900.65	186.9
3267	S[1803]	-7910.35	306.9
3268	RX[200]	-7920.05	426.9
3269	S[1804]	-7929.75	66.9
3270	S[1805]	-7939.45	186.9
3271	S[1806]	-7949.15	306.9
3272	RX[199]	-7958.85	426.9
3273	S[1807]	-7968.55	66.9
3274	S[1808]	-7978.25	186.9
3275	S[1809]	-7987.95	306.9
3276	RX[198]	-7997.65	426.9
3277	S[1810]	-8007.35	66.9
3278	S[1811]	-8017.05	186.9
3279	S[1812]	-8026.75	306.9
3280	RX[197]	-8036.45	426.9
3281	S[1813]	-8046.15	66.9
3282	S[1814]	-8055.85	186.9
3283	S[1815]	-8065.55	306.9
3284	RX[196]	-8075.25	426.9
3285	S[1816]	-8084.95	66.9
3286	S[1817]	-8094.65	186.9
3287	S[1818]	-8104.35	306.9
3288	RX[195]	-8114.05	426.9
3289	S[1819]	-8123.75	66.9
3290	S[1820]	-8133.45	186.9
3291	S[1821]	-8143.15	306.9
3292	RX[194]	-8152.85	426.9
3293	S[1822]	-8162.55	66.9
3294	S[1823]	-8172.25	186.9
3295	S[1824]	-8181.95	306.9
3296	RX[193]	-8191.65	426.9
3297	S[1825]	-8201.35	66.9
3298	S[1826]	-8211.05	186.9
3299	S[1827]	-8220.75	306.9
3300	RX[192]	-8230.45	426.9
3301	S[1828]	-8240.15	66.9
3302	S[1829]	-8249.85	186.9
3303	S[1830]	-8259.55	306.9
3304	RX[191]	-8269.25	426.9
3305	S[1831]	-8278.95	66.9
3306	S[1832]	-8288.65	186.9
3307	S[1833]	-8298.35	306.9
3308	RX[190]	-8308.05	426.9
3309	S[1834]	-8317.75	66.9
3310	S[1835]	-8327.45	186.9
3311	S[1836]	-8337.15	306.9
3312	RX[189]	-8346.85	426.9
3313	S[1837]	-8356.55	66.9
3314	S[1838]	-8366.25	186.9
3315	S[1839]	-8375.95	306.9
3316	RX[188]	-8385.65	426.9
3317	S[1840]	-8395.35	66.9
3318	S[1841]	-8405.05	186.9
3319	S[1842]	-8414.75	306.9
3320	RX[187]	-8424.45	426.9
3321	S[1843]	-8434.15	66.9
3322	S[1844]	-8443.85	186.9
3323	S[1845]	-8453.55	306.9
3324	RX[186]	-8463.25	426.9
3325	S[1846]	-8472.95	66.9
3326	S[1847]	-8482.65	186.9
3327	S[1848]	-8492.35	306.9
3328	RX[185]	-8502.05	426.9
3329	S[1849]	-8511.75	66.9
3330	S[1850]	-8521.45	186.9
3331	S[1851]	-8531.15	306.9
3332	RX[184]	-8540.85	426.9
3333	S[1852]	-8550.55	66.9
3334	S[1853]	-8560.25	186.9
3335	S[1854]	-8569.95	306.9
3336	RX[183]	-8579.65	426.9
3337	S[1855]	-8589.35	66.9
3338	S[1856]	-8599.05	186.9
3339	S[1857]	-8608.75	306.9
3340	RX[182]	-8618.45	426.9
3341	S[1858]	-8628.15	66.9
3342	S[1859]	-8637.85	186.9
3343	S[1860]	-8647.55	306.9
3344	RX[181]	-8657.25	426.9
3345	S[1861]	-8666.95	66.9
3346	S[1862]	-8676.65	186.9
3347	S[1863]	-8686.35	306.9
3348	RX[180]	-8696.05	426.9
3349	S[1864]	-8705.75	66.9
3350	S[1865]	-8715.45	186.9
3351	S[1866]	-8725.15	306.9
3352	RX[179]	-8734.85	426.9
3353	S[1867]	-8744.55	66.9
3354	S[1868]	-8754.25	186.9
3355	S[1869]	-8763.95	306.9
3356	RX[178]	-8773.65	426.9
3357	S[1870]	-8783.35	66.9
3358	S[1871]	-8793.05	186.9
3359	S[1872]	-8802.75	306.9
3360	RX[177]	-8812.45	426.9
3361	S[1873]	-8822.15	66.9
3362	S[1874]	-8831.85	186.9
3363	S[1875]	-8841.55	306.9
3364	RX[176]	-8851.25	426.9
3365	S[1876]	-8860.95	66.9
3366	S[1877]	-8870.65	186.9
3367	S[1878]	-8880.35	306.9
3368	RX[175]	-8890.05	426.9
3369	S[1879]	-8899.75	66.9
3370	S[1880]	-8909.45	186.9
3371	S[1881]	-8919.15	306.9
3372	RX[174]	-8928.85	426.9
3373	S[1882]	-8938.55	66.9
3374	S[1883]	-8948.25	186.9
3375	S[1884]	-8957.95	306.9
3376	RX[173]	-8967.65	426.9
3377	S[1885]	-8977.35	66.9
3378	S[1886]	-8987.05	186.9
3379	S[1887]	-8996.75	306.9
3380	RX[172]	-9006.45	426.9
3381	S[1888]	-9016.15	66.9
3382	S[1889]	-9025.85	186.9
3383	S[1890]	-9035.55	306.9
3384	RX[171]	-9045.25	426.9
3385	S[1891]	-9054.95	66.9
3386	S[1892]	-9064.65	186.9
3387	S[1893]	-9074.35	306.9
3388	RX[170]	-9084.05	426.9
3389	S[1894]	-9093.75	66.9
3390	S[1895]	-9103.45	186.9
3391	S[1896]	-9113.15	306.9
3392	RX[169]	-9122.85	426.9
3393	S[1897]	-9132.55	66.9
3394	S[1898]	-9142.25	186.9
3395	S[1899]	-9151.95	306.9
3396	RX[168]	-9161.65	426.9
3397	S[1900]	-9171.35	66.9
3398	S[1901]	-9181.05	186.9
3399	S[1902]	-9190.75	306.9
3400	RX[167]	-9200.45	426.9
3401	S[1903]	-9210.15	66.9
3402	S[1904]	-9219.85	186.9
3403	S[1905]	-9229.55	306.9
3404	RX[166]	-9239.25	426.9
3405	S[1906]	-9248.95	66.9
3406	S[1907]	-9258.65	186.9
3407	S[1908]	-9268.35	306.9
3408	RX[165]	-9278.05	426.9
3409	S[1909]	-9287.75	66.9
3410	S[1910]	-9297.45	186.9
3411	S[1911]	-9307.15	306.9
3412	RX[164]	-9316.85	426.9
3413	S[1912]	-9326.55	66.9
3414	S[1913]	-9336.25	186.9
3415	S[1914]	-9345.95	306.9
3416	RX[163]	-9355.65	426.9
3417	S[1915]	-9365.35	66.9
3418	S[1916]	-9375.05	186.9
3419	S[1917]	-9384.75	306.9
3420	RX[162]	-9394.45	426.9
3421	S[1918]	-9404.15	66.9
3422	S[1919]	-9413.85	186.9
3423	S[1920]	-9423.55	306.9
3424	RX[161]	-9433.25	426.9
3425	S[1921]	-9442.95	66.9
3426	S[1922]	-9452.65	186.9
3427	S[1923]	-9462.35	306.9
3428	RX[160]	-9472.05	426.9
3429	S[1924]	-9481.75	66.9
3430	S[1925]	-9491.45	186.9
3431	S[1926]	-9501.15	306.9
3432	RX[159]	-9510.85	426.9
3433	S[1927]	-9520.55	66.9
3434	S[1928]	-9530.25	186.9
3435	S[1929]	-9539.95	306.9
3436	RX[158]	-9549.65	426.9
3437	S[1930]	-9559.35	66.9
3438	S[1931]	-9569.05	186.9
3439	S[1932]	-9578.75	306.9
3440	RX[157]	-9588.45	426.9
3441	S[1933]	-9598.15	66.9
3442	S[1934]	-9607.85	186.9
3443	S[1935]	-9617.55	306.9
3444	RX[156]	-9627.25	426.9
3445	S[1936]	-9636.95	66.9
3446	S[1937]	-9646.65	186.9
3447	S[1938]	-9656.35	306.9
3448	RX[155]	-9666.05	426.9
3449	S[1939]	-9675.75	66.9
3450	S[1940]	-9685.45	186.9
3451	S[1941]	-9695.15	306.9
3452	RX[154]	-9704.85	426.9
3453	S[1942]	-9714.55	66.9
3454	S[1943]	-9724.25	186.9
3455	S[1944]	-9733.95	306.9
3456	RX[153]	-9743.65	426.9
3457	S[1945]	-9753.35	66.9
3458	S[1946]	-9763.05	186.9
3459	S[1947]	-9772.75	306.9
3460	RX[152]	-9782.45	426.9
3461	S[1948]	-9792.15	66.9
3462	S[1949]	-9801.85	186.9
3463	S[1950]	-9811.55	306.9
3464	RX[151]	-9821.25	426.9
3465	S[1951]	-9830.95	66.9
3466	S[1952]	-9840.65	186.9
3467	S[1953]	-9850.35	306.9
3468	RX[150]	-9860.05	426.9
3469	S[1954]	-9869.75	66.9
3470	S[1955]	-9879.45	186.9
3471	S[1956]	-9889.15	306.9
3472	RX[149]	-9898.85	426.9
3473	S[1957]	-9908.55	66.9
3474	S[1958]	-9918.25	186.9
3475	S[1959]	-9927.95	306.9
3476	RX[148]	-9937.65	426.9
3477	S[1960]	-9947.35	66.9
3478	S[1961]	-9957.05	186.9
3479	S[1962]	-9966.75	306.9
3480	RX[147]	-9976.45	426.9
3481	S[1963]	-9986.15	66.9
3482	S[1964]	-9995.85	186.9
3483	S[1965]	-10005.55	306.9
3484	RX[146]	-10015.25	426.9
3485	S[1966]	-10024.95	66.9
3486	S[1967]	-10034.65	186.9
3487	S[1968]	-10044.35	306.9
3488	RX[145]	-10054.05	426.9
3489	S[1969]	-10063.75	66.9
3490	S[1970]	-10073.45	186.9
3491	S[1971]	-10083.15	306.9
3492	RX[144]	-10092.85	426.9
3493	S[1972]	-10102.55	66.9
3494	S[1973]	-10112.25	186.9
3495	S[1974]	-10121.95	306.9
3496	RX[143]	-10131.65	426.9
3497	S[1975]	-10141.35	66.9
3498	S[1976]	-10151.05	186.9
3499	S[1977]	-10160.75	306.9
3500	RX[142]	-10170.45	426.9
3501	S[1978]	-10180.15	66.9
3502	S[1979]	-10189.85	186.9

No.	PAD Name	X	Y
3503	S[1980]	-10199.55	306.9
3504	RX[141]	-10209.25	426.9
3505	S[1981]	-10218.95	66.9
3506	S[1982]	-10228.65	186.9
3507	S[1983]	-10238.35	306.9
3508	RX[140]	-10248.05	426.9
3509	S[1984]	-10257.75	66.9
3510	S[1985]	-10267.45	186.9
3511	S[1986]	-10277.15	306.9
3512	RX[139]	-10286.85	426.9
3513	S[1987]	-10296.55	66.9
3514	S[1988]	-10306.25	186.9
3515	S[1989]	-10315.95	306.9
3516	RX[138]	-10325.65	426.9
3517	S[1990]	-10335.35	66.9
3518	S[1991]	-10345.05	186.9
3519	S[1992]	-10354.75	306.9
3520	RX[137]	-10364.45	426.9
3521	S[1993]	-10374.15	66.9
3522	S[1994]	-10383.85	186.9
3523	S[1995]	-10393.55	306.9
3524	RX[136]	-10403.25	426.9
3525	S[1996]	-10412.95	66.9
3526	S[1997]	-10422.65	186.9
3527	S[1998]	-10432.35	306.9
3528	RX[135]	-10442.05	426.9
3529	S[1999]	-10451.75	66.9
3530	S[2000]	-10461.45	186.9
3531	S[2001]	-10471.15	306.9
3532	RX[134]	-10480.85	426.9
3533	S[2002]	-10490.55	66.9
3534	S[2003]	-10500.25	186.9
3535	S[2004]	-10509.95	306.9
3536	RX[133]	-10519.65	426.9
3537	S[2005]	-10529.35	66.9
3538	S[2006]	-10539.05	186.9
3539	S[2007]	-10548.75	306.9
3540	RX[132]	-10558.45	426.9
3541	S[2008]	-10568.15	66.9
3542	S[2009]	-10577.85	186.9
3543	S[2010]	-10587.55	306.9
3544	RX[131]	-10597.25	426.9
3545	S[2011]	-10606.95	66.9
3546	S[2012]	-10616.65	186.9
3547	S[2013]	-10626.35	306.9
3548	RX[130]	-10636.05	426.9
3549	S[2014]	-10645.75	66.9
3550	S[2015]	-10655.45	186.9
3551	S[2016]	-10665.15	306.9
3552	RX[129]	-10674.85	426.9
3553	S[2017]	-10684.55	66.9
3554	S[2018]	-10694.25	186.9
3555	S[2019]	-10703.95	306.9
3556	RX[128]	-10713.65	426.9
3557	S[2020]	-10723.35	66.9
3558	S[2021]	-10733.05	186.9
3559	S[2022]	-10742.75	306.9
3560	RX[127]	-10752.45	426.9
3561	S[2023]	-10762.15	66.9
3562	S[2024]	-10771.85	186.9
3563	S[2025]	-10781.55	306.9
3564	RX[126]	-10791.25	426.9
3565	S[2026]	-10800.95	66.9
3566	S[2027]	-10810.65	186.9
3567	S[2028]	-10820.35	306.9
3568	RX[125]	-10830.05	426.9
3569	S[2029]	-10839.75	66.9
3570	S[2030]	-10849.45	186.9
3571	S[2031]	-10859.15	306.9
3572	RX[124]	-10868.85	426.9
3573	S[2032]	-10878.55	66.9
3574	S[2033]	-10888.25	186.9
3575	S[2034]	-10897.95	306.9
3576	RX[123]	-10907.65	426.9
3577	S[2035]	-10917.35	66.9
3578	S[2036]	-10927.05	186.9
3579	S[2037]	-10936.75	306.9
3580	RX[122]	-10946.45	426.9
3581	S[2038]	-10956.15	66.9
3582	S[2039]	-10965.85	186.9
3583	S[2040]	-10975.55	306.9
3584	RX[121]	-10985.25	426.9
3585	S[2041]	-10994.95	66.9
3586	S[2042]	-11004.65	186.9
3587	S[2043]	-11014.35	306.9
3588	RX[120]	-11024.05	426.9
3589	S[2044]	-11033.75	66.9
3590	S[2045]	-11043.45	186.9
3591	S[2046]	-11053.15	306.9
3592	RX[119]	-11062.85	426.9
3593	S[2047]	-11072.55	66.9
3594	S[2048]	-11082.25	186.9
3595	S[2049]	-11091.95	306.9
3596	RX[118]	-11101.65	426.9
3597	S[2050]	-11111.35	66.9
3598	S[2051]	-11121.05	186.9
3599	S[2052]	-11130.75	306.9
3600	RX[117]	-11140.45	426.9
3601	S[2053]	-11150.15	66.9
3602	S[2054]	-11159.85	186.9
3603	S[2055]	-11169.55	306.9
3604	RX[116]	-11179.25	426.9
3605	S[2056]	-11188.95	66.9
3606	S[2057]	-11198.65	186.9
3607	S[2058]	-11208.35	306.9
3608	RX[115]	-11218.05	426.9
3609	S[2059]	-11227.75	66.9
3610	S[2060]	-11237.45	186.9
3611	S[2061]	-11247.15	306.9
3612	RX[114]	-11256.85	426.9
3613	S[2062]	-11266.55	66.9
3614	S[2063]	-11276.25	186.9
3615	S[2064]	-11285.95	306.9
3616	RX[113]	-11295.65	426.9
3617	S[2065]	-11305.35	66.9
3618	S[2066]	-11315.05	186.9
3619	S[2067]	-11324.75	306.9
3620	RX[112]	-11334.45	426.9
3621	S[2068]	-11344.15	66.9
3622	S[2069]	-11353.85	186.9
3623	S[2070]	-11363.55	306.9
3624	RX[111]	-11373.25	426.9
3625	S[2071]	-11382.95	66.9
3626	S[2072]	-11392.65	186.9
3627	S[2073]	-11402.35	306.9
3628	RX[110]	-11412.05	426.9
3629	S[2074]	-11421.75	66.9
3630	S[2075]	-11431.45	186.9
3631	S[2076]	-11441.15	306.9
3632	RX[109]	-11450.85	426.9
3633	S[2077]	-11460.55	66.9
3634	S[2078]	-11470.25	186.9
3635	S[2079]	-11479.95	306.9
3636	RX[108]	-11489.65	426.9
3637	S[2080]	-11499.35	66.9
3638	S[2081]	-11509.05	186.9
3639	S[2082]	-11518.75	306.9
3640	RX[107]	-11528.45	426.9
3641	S[2083]	-11538.15	66.9
3642	S[2084]	-11547.85	186.9
3643	S[2085]	-11557.55	306.9
3644	RX[106]	-11567.25	426.9
3645	S[2086]	-11576.95	66.9
3646	S[2087]	-11586.65	186.9
3647	S[2088]	-11596.35	306.9
3648	RX[105]	-11606.05	426.9
3649	S[2089]	-11615.75	66.9
3650	S[2090]	-11625.45	186.9
3651	S[2091]	-11635.15	306.9
3652	RX[104]	-11644.85	426.9
3653	S[2092]	-11654.55	66.9
3654	S[2093]	-11664.25	186.9
3655	S[2094]	-11673.95	306.9
3656	RX[103]	-11683.65	426.9
3657	S[2095]	-11693.35	66.9
3658	S[2096]	-11703.05	186.9
3659	S[2097]	-11712.75	306.9
3660	RX[102]	-11722.45	426.9
3661	S[2098]	-11732.15	66.9
3662	S[2099]	-11741.85	186.9
3663	S[2100]	-11751.55	306.9
3664	RX[101]	-11761.25	426.9
3665	S[2101]	-11770.95	66.9
3666	S[2102]	-11780.65	186.9
3667	S[2103]	-11790.35	306.9
3668	RX[100]	-11800.05	426.9
3669	S[2104]	-11809.75	66.9
3670	S[2105]	-11819.45	186.9
3671	S[2106]	-11829.15	306.9
3672	RX[99]	-11838.85	426.9
3673	S[2107]	-11848.55	66.9
3674	S[2108]	-11858.25	186.9
3675	S[2109]	-11867.95	306.9
3676	RX[98]	-11877.65	426.9
3677	S[2110]	-11887.35	66.9
3678	S[2111]	-11897.05	186.9
3679	S[2112]	-11906.75	306.9
3680	RX[97]	-11916.45	426.9
3681	S[2113]	-11926.15	66.9
3682	S[2114]	-11935.85	186.9
3683	S[2115]	-11945.55	306.9
3684	RX[96]	-11955.25	426.9
3685	S[2116]	-11964.95	66.9
3686	S[2117]	-11974.65	186.9
3687	S[2118]	-11984.35	306.9
3688	RX[95]	-11994.05	426.9
3689	S[2119]	-12003.75	66.9
3690	S[2120]	-12013.45	186.9
3691	S[2121]	-12023.15	306.9
3692	RX[94]	-12032.85	426.9
3693	S[2122]	-12042.55	66.9
3694	S[2123]	-12052.25	186.9
3695	S[2124]	-12061.95	306.9
3696	RX[93]	-12071.65	426.9
3697	S[2125]	-12081.35	66.9
3698	S[2126]	-12091.05	186.9
3699	S[2127]	-12100.75	306.9
3700	RX[92]	-12110.45	426.9
3701	S[2128]	-12120.15	66.9
3702	S[2129]	-12129.85	186.9
3703	S[2130]	-12139.55	306.9
3704	RX[91]	-12149.25	426.9
3705	S[2131]	-12158.95	66.9
3706	S[2132]	-12168.65	186.9
3707	S[2133]	-12178.35	306.9
3708	RX[90]	-12188.05	426.9
3709	S[2134]	-12197.75	66.9
3710	S[2135]	-12207.45	186.9
3711	S[2136]	-12217.15	306.9
3712	RX[89]	-12226.85	426.9
3713	S[2137]	-12236.55	66.9
3714	S[2138]	-12246.25	186.9
3715	S[2139]	-12255.95	306.9
3716	RX[88]	-12265.65	426.9
3717	S[2140]	-12275.35	66.9
3718	S[2141]	-12285.05	186.9
3719	S[2142]	-12294.75	306.9
3720	RX[87]	-12304.45	426.9
3721	S[2143]	-12314.15	66.9
3722	S[2144]	-12323.85	186.9
3723	S[2145]	-12333.55	306.9
3724	RX[86]	-12343.25	426.9
3725	S[2146]	-12352.95	66.9
3726	S[2147]	-12362.65	186.9
3727	S[2148]	-12372.35	306.9
3728	RX[85]	-12382.05	426.9
3729	S[2149]	-12391.75	66.9
3730	S[2150]	-12401.45	186.9
3731	S[2151]	-12411.15	306.9
3732	RX[84]	-12420.85	426.9
3733	S[2152]	-12430.55	66.9
3734	S[2153]	-12440.25	186.9
3735	S[2154]	-12449.95	306.9
3736	RX[83]	-12459.65	426.9
3737	S[2155]	-12469.35	66.9
3738	S[2156]	-12479.05	186.9
3739	S[2157]	-12488.75	306.9
3740	RX[82]	-12498.45	426.9
3741	S[2158]	-12508.15	66.9
3742	S[2159]	-12517.85	186.9
3743	S[2160]	-12527.55	306.9
3744	RX[81]	-12537.25	426.9
3745	S[2161]	-12546.95	66.9
3746	S[2162]	-12556.65	186.9
3747	S[2163]	-12566.35	306.9
3748	RX[80]	-12576.05	426.9
3749	S[2164]	-12585.75	66.9
3750	S[2165]	-12595.45	186.9
3751	S[2166]	-12605.15	306.9
3752	RX[79]	-12614.85	426.9
3753	S[2167]	-12624.55	66.9
3754	S[2168]	-12634.25	186.9

No.	PAD Name	X	Y
3755	S[2169]	-12643.95	306.9
3756	RX[78]	-12653.65	426.9
3757	S[2170]	-12663.35	66.9
3758	S[2171]	-12673.05	186.9
3759	S[2172]	-12682.75	306.9
3760	RX[77]	-12692.45	426.9
3761	S[2173]	-12702.15	66.9
3762	S[2174]	-12711.85	186.9
3763	S[2175]	-12721.55	306.9
3764	RX[76]	-12731.25	426.9
3765	S[2176]	-12740.95	66.9
3766	S[2177]	-12750.65	186.9
3767	S[2178]	-12760.35	306.9
3768	RX[75]	-12770.05	426.9
3769	S[2179]	-12779.75	66.9
3770	S[2180]	-12789.45	186.9
3771	S[2181]	-12799.15	306.9
3772	RX[74]	-12808.85	426.9
3773	S[2182]	-12818.55	66.9
3774	S[2183]	-12828.25	186.9
3775	S[2184]	-12837.95	306.9
3776	RX[73]	-12847.65	426.9
3777	S[2185]	-12857.35	66.9
3778	S[2186]	-12867.05	186.9
3779	S[2187]	-12876.75	306.9
3780	RX[72]	-12886.45	426.9
3781	S[2188]	-12896.15	66.9
3782	S[2189]	-12905.85	186.9
3783	S[2190]	-12915.55	306.9
3784	RX[71]	-12925.25	426.9
3785	S[2191]	-12934.95	66.9
3786	S[2192]	-12944.65	186.9
3787	S[2193]	-12954.35	306.9
3788	RX[70]	-12964.05	426.9
3789	S[2194]	-12973.75	66.9
3790	S[2195]	-12983.45	186.9
3791	S[2196]	-12993.15	306.9
3792	RX[69]	-13002.85	426.9
3793	S[2197]	-13012.55	66.9
3794	S[2198]	-13022.25	186.9
3795	S[2199]	-13031.95	306.9
3796	RX[68]	-13041.65	426.9
3797	S[2200]	-13051.35	66.9
3798	S[2201]	-13061.05	186.9
3799	S[2202]	-13070.75	306.9
3800	RX[67]	-13080.45	426.9
3801	S[2203]	-13090.15	66.9
3802	S[2204]	-13099.85	186.9
3803	S[2205]	-13109.55	306.9
3804	RX[66]	-13119.25	426.9
3805	S[2206]	-13128.95	66.9
3806	S[2207]	-13138.65	186.9
3807	S[2208]	-13148.35	306.9
3808	RX[65]	-13158.05	426.9
3809	S[2209]	-13167.75	66.9
3810	S[2210]	-13177.45	186.9
3811	S[2211]	-13187.15	306.9
3812	RX[64]	-13196.85	426.9
3813	S[2212]	-13206.55	66.9
3814	S[2213]	-13216.25	186.9
3815	S[2214]	-13225.95	306.9
3816	RX[63]	-13235.65	426.9
3817	S[2215]	-13245.35	66.9
3818	S[2216]	-13255.05	186.9
3819	S[2217]	-13264.75	306.9
3820	RX[62]	-13274.45	426.9
3821	S[2218]	-13284.15	66.9
3822	S[2219]	-13293.85	186.9
3823	S[2220]	-13303.55	306.9
3824	RX[61]	-13313.25	426.9
3825	S[2221]	-13322.95	66.9
3826	S[2222]	-13332.65	186.9
3827	S[2223]	-13342.35	306.9
3828	RX[60]	-13352.05	426.9
3829	S[2224]	-13361.75	66.9
3830	S[2225]	-13371.45	186.9
3831	S[2226]	-13381.15	306.9
3832	RX[59]	-13390.85	426.9
3833	S[2227]	-13400.55	66.9
3834	S[2228]	-13410.25	186.9
3835	S[2229]	-13419.95	306.9
3836	RX[58]	-13429.65	426.9
3837	S[2230]	-13439.35	66.9
3838	S[2231]	-13449.05	186.9
3839	S[2232]	-13458.75	306.9
3840	RX[57]	-13468.45	426.9
3841	S[2233]	-13478.15	66.9
3842	S[2234]	-13487.85	186.9
3843	S[2235]	-13497.55	306.9
3844	RX[56]	-13507.25	426.9
3845	S[2236]	-13516.95	66.9
3846	S[2237]	-13526.65	186.9
3847	S[2238]	-13536.35	306.9
3848	RX[55]	-13546.05	426.9
3849	S[2239]	-13555.75	66.9
3850	S[2240]	-13565.45	186.9
3851	S[2241]	-13575.15	306.9
3852	RX[54]	-13584.85	426.9
3853	S[2242]	-13594.55	66.9
3854	S[2243]	-13604.25	186.9
3855	S[2244]	-13613.95	306.9
3856	RX[53]	-13623.65	426.9
3857	S[2245]	-13633.35	66.9
3858	S[2246]	-13643.05	186.9
3859	S[2247]	-13652.75	306.9
3860	RX[52]	-13662.45	426.9
3861	S[2248]	-13672.15	66.9
3862	S[2249]	-13681.85	186.9
3863	S[2250]	-13691.55	306.9
3864	RX[51]	-13701.25	426.9
3865	S[2251]	-13710.95	66.9
3866	S[2252]	-13720.65	186.9
3867	S[2253]	-13730.35	306.9
3868	RX[50]	-13740.05	426.9
3869	S[2254]	-13749.75	66.9
3870	S[2255]	-13759.45	186.9
3871	S[2256]	-13769.15	306.9
3872	RX[49]	-13778.85	426.9
3873	S[2257]	-13788.55	66.9
3874	S[2258]	-13798.25	186.9
3875	S[2259]	-13807.95	306.9
3876	RX[48]	-13817.65	426.9
3877	S[2260]	-13827.35	66.9
3878	S[2261]	-13837.05	186.9
3879	S[2262]	-13846.75	306.9
3880	RX[47]	-13856.45	426.9
3881	S[2263]	-13866.15	66.9
3882	S[2264]	-13875.85	186.9
3883	S[2265]	-13885.55	306.9
3884	RX[46]	-13895.25	426.9
3885	S[2266]	-13904.95	66.9
3886	S[2267]	-13914.65	186.9
3887	S[2268]	-13924.35	306.9
3888	RX[45]	-13934.05	426.9
3889	S[2269]	-13943.75	66.9
3890	S[2270]	-13953.45	186.9
3891	S[2271]	-13963.15	306.9
3892	RX[44]	-13972.85	426.9
3893	S[2272]	-13982.55	66.9
3894	S[2273]	-13992.25	186.9
3895	S[2274]	-14001.95	306.9
3896	RX[43]	-14011.65	426.9
3897	S[2275]	-14021.35	66.9
3898	S[2276]	-14031.05	186.9
3899	S[2277]	-14040.75	306.9
3900	RX[42]	-14050.45	426.9
3901	S[2278]	-14060.15	66.9
3902	S[2279]	-14069.85	186.9
3903	S[2280]	-14079.55	306.9
3904	RX[41]	-14089.25	426.9
3905	S[2281]	-14098.95	66.9
3906	S[2282]	-14108.65	186.9
3907	S[2283]	-14118.35	306.9
3908	RX[40]	-14128.05	426.9
3909	S[2284]	-14137.75	66.9
3910	S[2285]	-14147.45	186.9
3911	S[2286]	-14157.15	306.9
3912	RX[39]	-14166.85	426.9
3913	S[2287]	-14176.55	66.9
3914	S[2288]	-14186.25	186.9
3915	S[2289]	-14195.95	306.9
3916	RX[38]	-14205.65	426.9
3917	S[2290]	-14215.35	66.9
3918	S[2291]	-14225.05	186.9
3919	S[2292]	-14234.75	306.9
3920	RX[37]	-14244.45	426.9
3921	S[2293]	-14254.15	66.9
3922	S[2294]	-14263.85	186.9
3923	S[2295]	-14273.55	306.9
3924	RX[36]	-14283.25	426.9
3925	S[2296]	-14292.95	66.9
3926	S[2297]	-14302.65	186.9
3927	S[2298]	-14312.35	306.9
3928	RX[35]	-14322.05	426.9
3929	S[2299]	-14331.75	66.9
3930	S[2300]	-14341.45	186.9
3931	S[2301]	-14351.15	306.9
3932	RX[34]	-14360.85	426.9
3933	S[2302]	-14370.55	66.9
3934	S[2303]	-14380.25	186.9
3935	S[2304]	-14389.95	306.9
3936	RX[33]	-14399.65	426.9
3937	S[2305]	-14409.35	66.9
3938	S[2306]	-14419.05	186.9
3939	S[2307]	-14428.75	306.9
3940	RX[32]	-14438.45	426.9
3941	S[2308]	-14448.15	66.9
3942	S[2309]	-14457.85	186.9
3943	S[2310]	-14467.55	306.9
3944	RX[31]	-14477.25	426.9
3945	S[2311]	-14486.95	66.9
3946	S[2312]	-14496.65	186.9
3947	S[2313]	-14506.35	306.9
3948	RX[30]	-14516.05	426.9
3949	S[2314]	-14525.75	66.9
3950	S[2315]	-14535.45	186.9
3951	S[2316]	-14545.15	306.9
3952	RX[29]	-14554.85	426.9
3953	S[2317]	-14564.55	66.9
3954	S[2318]	-14574.25	186.9
3955	S[2319]	-14583.95	306.9
3956	RX[28]	-14593.65	426.9
3957	S[2320]	-14603.35	66.9
3958	S[2321]	-14613.05	186.9
3959	S[2322]	-14622.75	306.9
3960	RX[27]	-14632.45	426.9
3961	S[2323]	-14642.15	66.9
3962	S[2324]	-14651.85	186.9
3963	S[2325]	-14661.55	306.9
3964	RX[26]	-14671.25	426.9
3965	S[2326]	-14680.95	66.9
3966	S[2327]	-14690.65	186.9
3967	S[2328]	-14700.35	306.9
3968	RX[25]	-14710.05	426.9
3969	S[2329]	-14719.75	66.9
3970	S[2330]	-14729.45	186.9
3971	S[2331]	-14739.15	306.9
3972	RX[24]	-14748.85	426.9
3973	S[2332]	-14758.55	66.9
3974	S[2333]	-14768.25	186.9
3975	S[2334]	-14777.95	306.9
3976	RX[23]	-14787.65	426.9
3977	S[2335]	-14797.35	66.9
3978	S[2336]	-14807.05	186.9
3979	S[2337]	-14816.75	306.9
3980	RX[22]	-14826.45	426.9
3981	S[2338]	-14836.15	66.9
3982	S[2339]	-14845.85	186.9
3983	S[2340]	-14855.55	306.9
3984	RX[21]	-14865.25	426.9
3985	S[2341]	-14874.95	66.9
3986	S[2342]	-14884.65	186.9
3987	S[2343]	-14894.35	306.9
3988	RX[20]	-14904.05	426.9
3989	S[2344]	-14913.75	66.9
3990	S[2345]	-14923.45	186.9
3991	S[2346]	-14933.15	306.9
3992	RX[19]	-14942.85	426.9
3993	S[2347]	-14952.55	66.9
3994	S[2348]	-14962.25	186.9
3995	S[2349]	-14971.95	306.9
3996	RX[18]	-14981.65	426.9
3997	S[2350]	-14991.35	66.9
3998	S[2351]	-15001.05	186.9
3999	S[2352]	-15010.75	306.9
4000	RX[17]	-15020.45	426.9
4001	S[2353]	-15030.15	66.9
4002	S[2354]	-15039.85	186.9
4003	S[2355]	-15049.55	306.9
4004	RX[16]	-15059.25	426.9
4005	S[2356]	-15068.95	66.9
4006	S[2357]	-15078.65	186.9

No.	PAD Name	X	Y
4007	S[2358]	-15088.35	306.9
4008	RX[15]	-15098.05	426.9
4009	S[2359]	-15107.75	66.9
4010	S[2360]	-15117.45	186.9
4011	S[2361]	-15127.15	306.9
4012	RX[14]	-15136.85	426.9
4013	S[2362]	-15146.55	66.9
4014	S[2363]	-15156.25	186.9
4015	S[2364]	-15165.95	306.9
4016	RX[13]	-15175.65	426.9
4017	S[2365]	-15185.35	66.9
4018	S[2366]	-15195.05	186.9
4019	S[2367]	-15204.75	306.9
4020	RX[12]	-15214.45	426.9
4021	S[2368]	-15224.15	66.9
4022	S[2369]	-15233.85	186.9
4023	S[2370]	-15243.55	306.9
4024	RX[11]	-15253.25	426.9
4025	S[2371]	-15262.95	66.9
4026	S[2372]	-15272.65	186.9
4027	S[2373]	-15282.35	306.9
4028	RX[10]	-15292.05	426.9
4029	S[2374]	-15301.75	66.9
4030	S[2375]	-15311.45	186.9
4031	S[2376]	-15321.15	306.9
4032	RX[9]	-15330.85	426.9
4033	S[2377]	-15340.55	66.9
4034	S[2378]	-15350.25	186.9
4035	S[2379]	-15359.95	306.9
4036	RX[8]	-15369.65	426.9
4037	S[2380]	-15379.35	66.9
4038	S[2381]	-15389.05	186.9
4039	S[2382]	-15398.75	306.9

No.	PAD Name	X	Y
4040	RX[7]	-15408.45	426.9
4041	S[2383]	-15418.15	66.9
4042	S[2384]	-15427.85	186.9
4043	S[2385]	-15437.55	306.9
4044	RX[6]	-15447.25	426.9
4045	S[2386]	-15456.95	66.9
4046	S[2387]	-15466.65	186.9
4047	S[2388]	-15476.35	306.9
4048	RX[5]	-15486.05	426.9
4049	S[2389]	-15495.75	66.9
4050	S[2390]	-15505.45	186.9
4051	S[2391]	-15515.15	306.9
4052	RX[4]	-15524.85	426.9
4053	S[2392]	-15534.55	66.9
4054	S[2393]	-15544.25	186.9
4055	S[2394]	-15553.95	306.9
4056	RX[3]	-15563.65	426.9
4057	S[2395]	-15573.35	66.9
4058	S[2396]	-15583.05	186.9
4059	S[2397]	-15592.75	306.9
4060	RX[2]	-15602.45	426.9
4061	S[2398]	-15612.15	66.9
4062	S[2399]	-15621.85	186.9
4063	S[2400]	-15631.55	306.9
4064	RX[1]	-15641.25	426.9
4065	SDUM[2]	-15650.95	66.9
4066	SDUM[3]	-15660.65	186.9
4067	DUMMY_OL[1]	-15670.35	306.9
4068	SXDUM2	-15680.05	426.9
4069	DUMMY_OL[2]	-15689.75	66.9
4070	DUMMY_OL[3]	-15699.45	186.9
4071	DUMMY_OL[4]	-15709.15	306.9
4072	DUMMY_OL[5]	-15718.85	426.9

No.	PAD Name	X	Y
4073	VCOM_PASS_L	-15728.55	66.9
4074	VCOM_PASS_L	-15738.25	186.9
4075	VCOM_PASS_L	-15747.95	306.9
4076	DUMMY_OL[6]	-15757.65	426.9
4077	VCOM_PASS_L	-15767.35	66.9
4078	VCOM_PASS_L	-15777.05	186.9
4079	VCOM_PASS_L	-15786.75	306.9
4080	DUMMY_OL[7]	-15796.45	426.9
4081	SYNC_GAM_L[5]	-15806.15	66.9
4082	SYNC_GAM_L[4]	-15815.85	186.9
4083	SYNC_GAM_L[3]	-15825.55	306.9
4084	DUMMY_OL[8]	-15835.25	426.9
4085	SYNC_GAM_L[2]	-15844.95	66.9
4086	SYNC_GAM_L[1]	-15854.65	186.9
4087	SYNC_GAM_L[0]	-15864.35	306.9
4088	DUMMY_OL[9]	-15874.05	426.9
4089	DUMMY_OL[10]	-15883.75	66.9
4090	DUMMY_OL[11]	-15893.45	186.9
4091	DUMMY_OL[12]	-15903.15	306.9

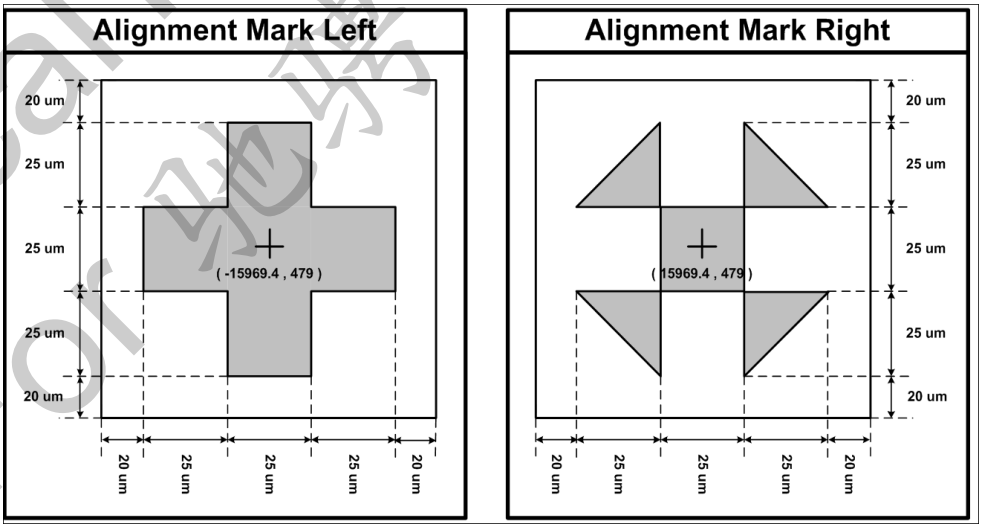
8.4 Alignment Mark

--Alignment Mark coordinate

Left (-15969.4,479)

Right (15969.4,479)

--Alignment Mark size



9 DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by FocalTech Systems are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. FocalTech Systems makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, FocalTech Systems MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. FocalTech Systems reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by FocalTech Systems for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

10 REVISION HISTORY

Date	Revision #	Description	Page	Auditor
Dec. 10, 2025	0.1	ALL	ALL	Willie Chen