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JD9366TC

Data Sheet

Single(800RGB x 1280)/ Cascade(1600x2560) dot, 16.7M color, without internal GRAM, a-Si TFT LCD Single /Cascade Driver

Version 0.03
2022/12/21

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1. Revision History

Version	Date	Description of modification
0.00	2021/03/29	New setup
0.01	2022/04/26	Update 13.Chip information in P.186~1.89
0.02	2022/11/16	1.Update maximum layout resistance table in P.20. 2.Update Power on sequence table in P.73~74. 3.Update LPWG timing chart in P.77. 4.Update HW RESET input timing in P.171
0.03	2022/12/21	1.Update Feature in P.13 2.Modify typo. of 10.3(Touch part I2C Interface) in P.85

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2. General Description

The JD9366TC is a one-chip or two-chip solution with RAM-less for a-Si TFT LCD panel. The chip is integrated “In-Cell” touch screen controller, source driver control, gate driver control and power supply circuit.

The JD9366TC can support MIPI DSI interface. It also supports 800 RGB x 1280 dots resolution in single-chip solution and 1600 RGB x 2560 dots resolution in two-chip cascade for tablet display terminals and provides the number of colors up to 16.7MHz. Moreover, the LCD driver can support gamma correction settings separately for RGB dots, 1-dot / 2-dot / column / Zigzag liquid crystal reversion mode, CABC function for the backlight control, and a deep standby mode to reduce the total power consumption of display module.

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3. Features

3.1. Display

- Single chip solution for a WXGA a-Si type LCD display
- Resolution:
  - 600~800RGB x 2560 (Max. gate line)
- Display color modes
  - Full color mode:
    - 16.7M colours (24-bit 8(R):8(G):8(B))
  - Reduce color mode:
    - 262k colours (18-bit 6(R):6(G):6(B))
    - 65k colours (16-bit 5(R):6(G):5(B))
    - 8 colors (Idle mode on): 8 colors (3-bit binary mode)

3.2. Display interface

- Display interface types supported
  - MIPI-DSI (Display Serial Interface) interface
    - Support DSI Version 1.1
    - Support D-PHY version 1.00
    - Support Muiti-drop & LR mode only for cascade application

3.3. Touch

- Programmable Scan line
- Capacitance technology adopted for multi-touch (up to 10 figures)
- Auto Noise Filter Function
- RX channel number:
  - Single chip without cascade: 800 Rx channels
  - Two chip with cascade: 1600 Rx channels
- Provides Fast Report Rate (Up to 120Hz frame rate)
  - 120Hz/60Hz report rate
- High signal-to-noise ratio (SNR) touch
- Customer Function Design (Embedded 32-bit MCU)
- Support SPI/I2C interface:
  - For I2C interface, the global address set to 0x5Ah
  - For I2C interface, the master address set to 0x68h
  - For I2C interface, the slave address set to 0x28h
- Low power wake-up gesture (LPWG)
- Independent 6-CH for Key Button function
- Support Host Processing

3.4. Input voltage ranges

- I/O and interface power supply (VDDI): 1.65V to 1.95V
- High speed interface power supply (VCCH): 1.65V to 1.95V

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- Digital power supply (VDDI_PLL): 1.65V to 1.95V
- OTP programming voltage (VPP): 8.25V ± 0.25V
- Analog volatge range for AVDD to VSSP: 4.5V ~ 6.3V
- Analog volatge range for AVEE to VSSP: -4.5V ~ -6.3V

3.5. Output voltage ranges

- On module DC/DC converter
  - AVDD= +4.5V to +6.3V
  - AVEE= -4.5V to -6.3V
  - Positive source output voltage level: VGMP= +3.0V to AVDD - 0.5V
  - Negative source output voltage level: VGMN= -3.0V to AVEE + 0.5V
  - Positive gate driver power source voltage level: VGH= 7 to 20V
  - Negative gate driver power source voltage level: VGL=-7V to -18V
  - Positive gate driver voltage level: VGHO= 7.3 to VGH - 0.5V
  - Negative gate driver voltage level: VGLO= -5.3 to VGL + 0.5V
  - VCL = -2.4V ~ -3V
  - VCOM= -3.0V to 0.08V, a step=10mv

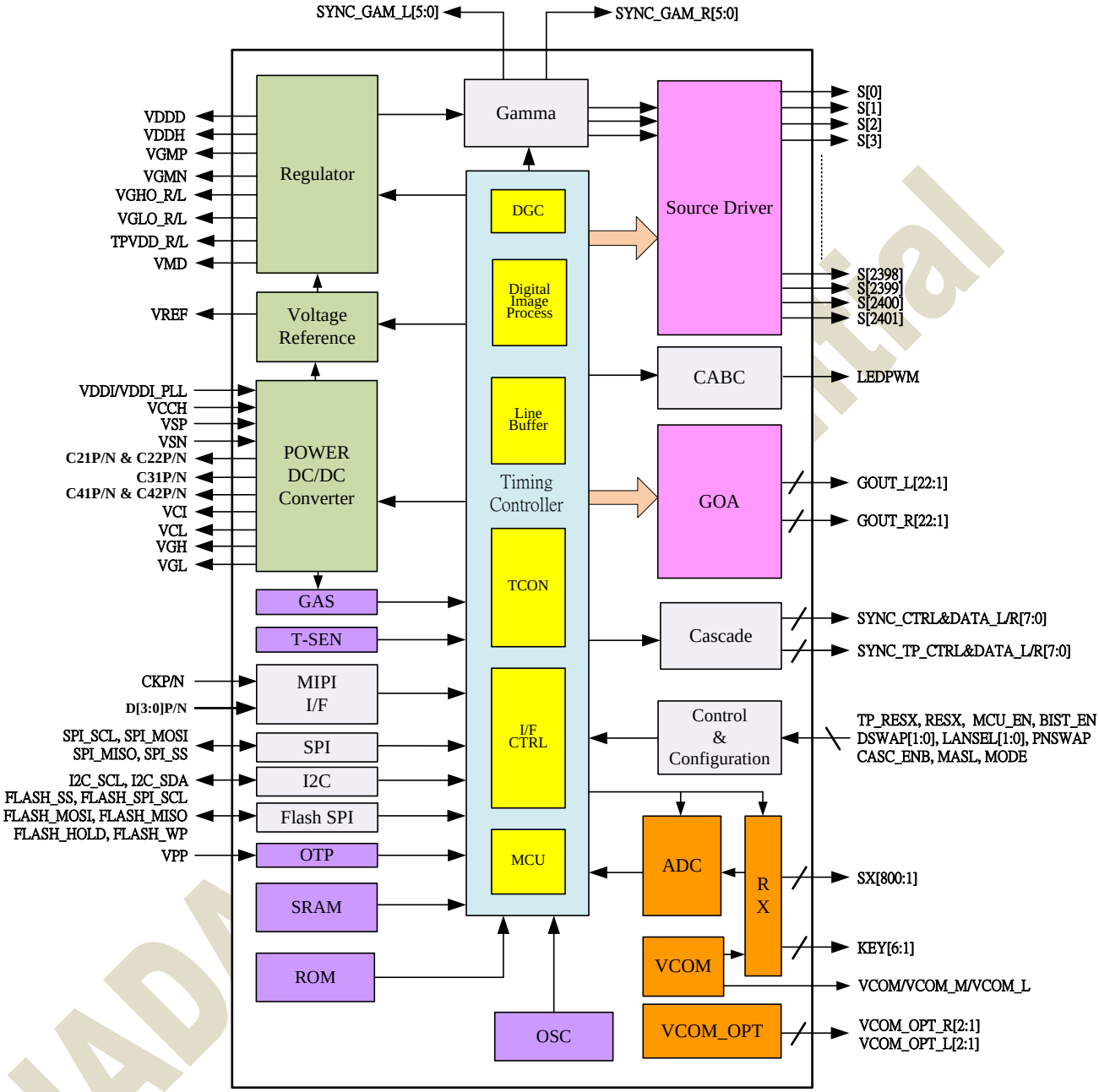
3.6. Miscellaneous of chip

- Internal level shifter for Gate Driver control
- Supports column / 1-dot / 2-dot / 4-dot / Z inversion
- Gamma correction (1 preset gamma curve)
- Internal Oscillator generation
- CMOS compatible inputs
- Proprietary multi phase driving for lower power consumption
- GAS function for preventing image sticking when abnormal power off
- Temperature range: -40 to +85 °C
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 1 times OTP for Gamma setting, 1 time OTP for DGC setting
- 5 times OTP for VCOM normal / reverse setting
- 1 times OTP for 50 bytes ID setting
- Support CABC (Content Adaptive Brightness Control) function
- Support Color enhancement
- Support Sunlight Readability Enhancement (SRE)

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4. Device Overview

4.1. Device Block Diagram



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4.2. LCD power generation scheme (DC/DC Converter)

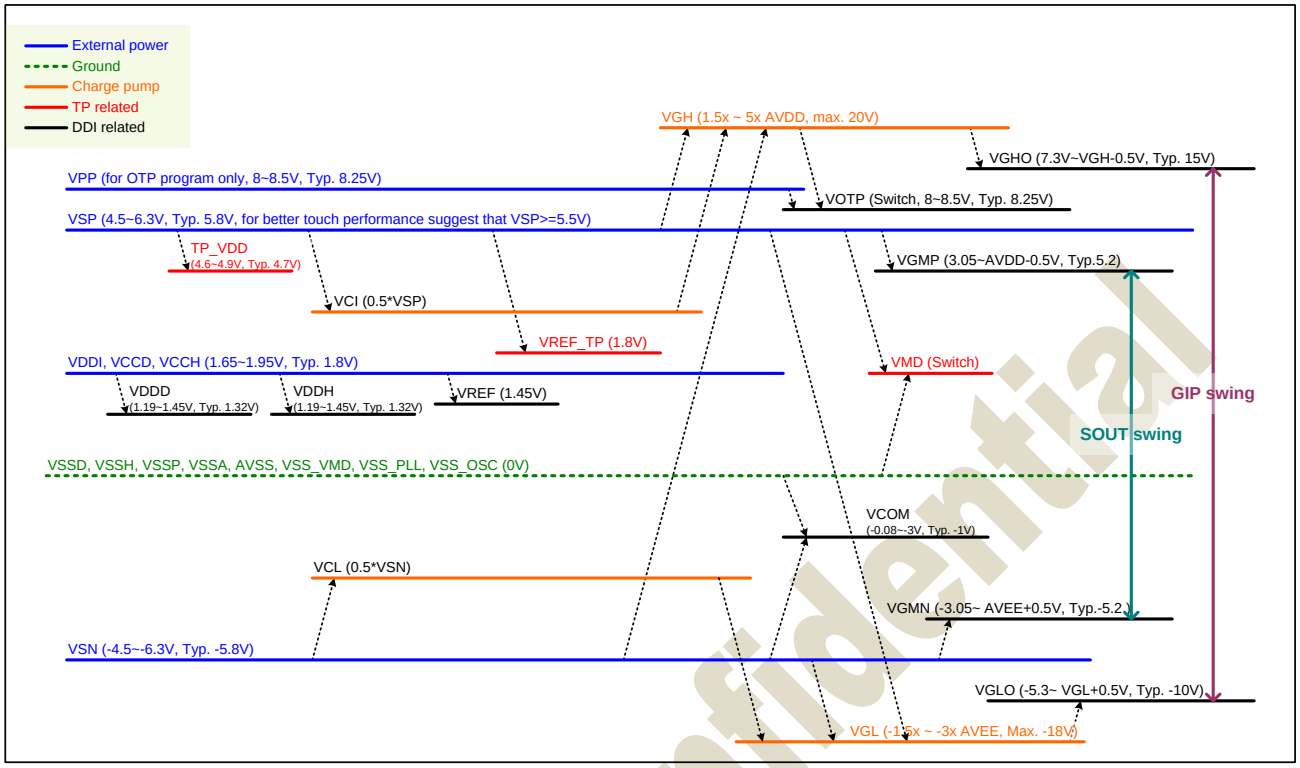


Figure 4.1: LCD power generation scheme

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4.3. Output voltage range

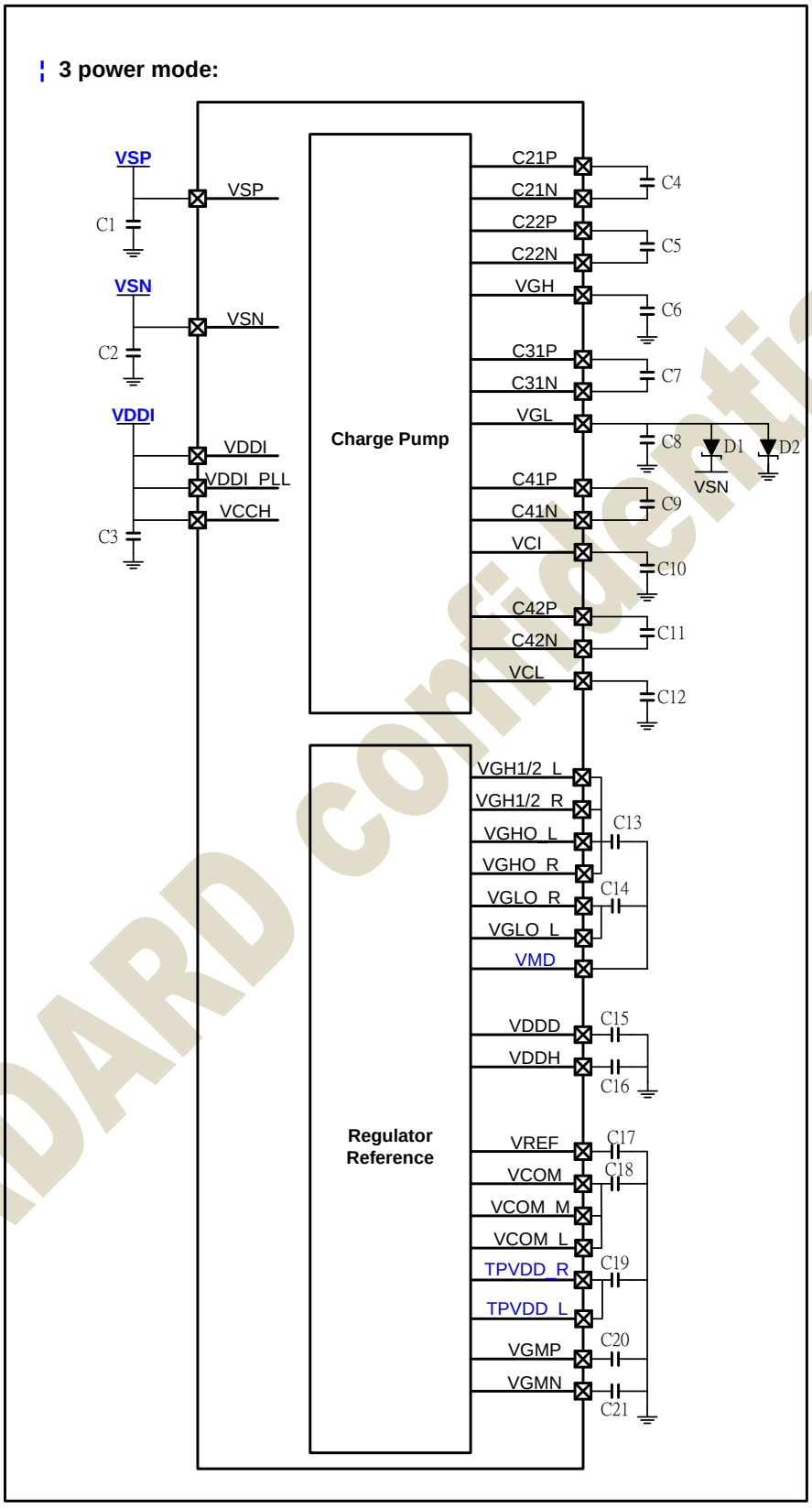
JD9366TC generates corresponding voltage with a-Si LCD panel by internal power supply circuit. Please set up each voltage output according to the LCD panel.

Name	Function	Set up value	Note
VREF	Reference voltage for regulator voltage	+1.45V	-
VREF_TP	Reference voltage for TP used	+ 1.8V	
AVDD	DC/DC converter circuit output	+4.5V ~ +6.3V	Do not exceed 6.3V
AVEE	DC/DC converter circuit output	-4.5V ~ -6.3V	Do not exceed -6.3V
VGMP	Reference voltage for gamma circuit	+3.05V ~ (AVDD – 0.5V)	Reference register
VGMN	Reference voltage for gamma circuit	-3.05V ~ (AVEE + 0.5V)	Reference register
VGH	Positive gate driver power source voltage	+7V ~ +20V	Depend on AVDD & AVEE
VGL	Negative gate driver power source voltage	-7V ~ -18V	Depend on AVDD & AVEE
VGHO	Positive gate driver output voltage level	+7.3V ~ VGH - 0.5V	
VGLO	Negative gate driver output voltage level	-5.3V ~ VGL + 0.5V	
VCL	DC/DC converter circuit output	-2.4V ~ -3V	
VCOM	VCOM DC voltage	0.08V ~ -3V	
VDDH	Analog power for High speed interface circuit	1.32V	-
VDDD	Digital power for internal digital circuit.	1.32V	-

Table 4.1: Voltage configuration

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4.4. DC/DC converter circuit



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Ref. no	Typical
C1	4.7uF/10V
C2	4.7uF/10V
C3	4.7uF/6V
C4	1uF/25V
C5	1uF/25V
C6	2.2uF/25V
C7	1uF/25V
C8	2.2uF/25V
C9	1uF/10V
C10	1uF/10V
C11	1uF/10V
C12	1uF/10V
C13	2.2uF/25V
C14	2.2uF/25V
C15	2.2uF/6V
C16	2.2uF/6V
C17	1uF/6V
C18	4.7uF/6V
C19	2.2uF/10V
C20	1uF/10V
C21	1uF/10V
D1	$V_F \leqq 0.3V$ @I_F min=10mA, VR$\geqq$30V
D2	$V_F \leqq 0.3V$ @I_F min=10mA, VR$\geqq$30V

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5. Maximum layout resistance

Name	Pin Definition	Maximum series resistance	Unit
VDDI, VCCH, VSP, VSN	Power Supply	**3**	Ω
VSSD, VSSA, VSSP, VSSH, VSS_VMD	Power Supply	**3**	Ω
AVSS, VSS_PLL, VSS_OSC	Power Supply	**5**	Ω
VCI, VDDD, VDDH, VREF, VCL	Capacitor Connection	**3**	Ω
C21P/N, C22P/N, C31P/N, C41P/N, C42P/N	Capacitor Connection	**3**	Ω
VCOM, VGH, VGL	Capacitor Connection	**3**	Ω
VGLO_L/R, VGHO_L/R,	Capacitor Connection	**5**	Ω
TPVDD, VGMP, VGMN	Capacitor Connection	**5**	Ω
VCOM_FB, VPP	Input	**10**	Ω
KEY[6:1], OSC_EXT, XCK_IN	Input	**20**	Ω
MODE, MCU_EN, BIST_EN, DSWAP[1:0], PNSWAP LANSEL[1:0], MASL, CASC_ENB, RESX, DUAL LR, BOOT_DEVICE, TP_RESX	Input	**50**	Ω
TESTI[7:0], TEST_P/N, AFE_TEST[4:0]	Input	**100**	Ω
D0P/N, D1P/N, D2P/N, D3P/N, CKP/N	MIPI pin	**5**	Ω
VCOM_PASS_L/R, VCOM_OPT_L/R[2:1], VMD	Output	**3**	Ω
VGH1_L/R, PLL_REF_CLK_OUT, XCK_OUT	Output	**10**	Ω
VGH2_L/R, GPIO[7:0], TE, TE1 LED[6:1], CABC_PWM_OUT	Output	**20**	Ω
DCHG1_L/R, DCHG2_L/R	Output	**50**	Ω
SPI_SCL, SPI_MOSI, SPI_MISO, SPI_SS, FLASH_SS, FLASH_SPI_SCL, FLASH_MOSI, FLASH_MISO, FLASH_HOLD, FLASH_WP, I2C_SCL, I2C_SDA, FLASH_SCL_IN_DUMMY, TSIX	Touch I/O	**20**	Ω
SYNC_CTRL_L/R[7:0], SYNC_DATA_L/R[7:0] SYNC_TP_CTRL_L/R[0], SYNC_TP_DATA_L/R[0]	Cascade I/O	**20**	Ω

Table 5.1: Maximum Layout Resistance

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6. Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">MIPI interface pins</td></tr>
<tr><td>D0P/D0N
D1P/D1N
D2P/D2N</td><td>In</td><td>MIPI data input pin. If not used, please float this pin.</td></tr>
<tr><td>CKP/CKN</td><td>In</td><td>MIPI clock input pin. If not used, please float this pin.</td></tr>
<tr><td colspan="3">Global pins</td></tr>
<tr><td>RESX
(VDDI)</td><td>In</td><td>Global reset pin, active low. (Default pull High)</td></tr>
<tr><td>LANSEL[1:0]
(VDDI)</td><td>In</td><td>MIPI lane number configuration.(Let it connect to VDDI or VSSD)
<table>
<tr><th>LANSEL[1:0]</th><th>MIPI lane number</th></tr>
<tr><td>00</td><td>T.B.D.</td></tr>
<tr><td>01</td><td>2 lanes</td></tr>
<tr><td>10</td><td>3 lanes</td></tr>
<tr><td>11</td><td>4 lanes</td></tr>
</table></td></tr>
<tr><td>PNSWAP,
DSWAP[1:0]
(VDDI)</td><td>In</td><td>These pins must be connected to VDDI or VSSD. PNSWAP and DSWAP1~0 are used for the combination of polarity swap and data lane swap of DSI.
(Let it connect to VDDI or VSSD)
<table>
<tr><th colspan="2">HW pin</th><th>CKP</th><th>CKN</th><th>D0P</th><th>D0N</th><th>D1P</th><th>D1N</th><th>D2P</th><th>D2N</th><th>D3P</th><th>D3N</th></tr>
<tr><td>PNSWAP</td><td>DSWAP[1:0]</td><td colspan="10">MIPI lanes mapping table</td></tr>
<tr><td>0</td><td>00</td><td>CKN</td><td>CKP</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td></tr>
<tr><td>0</td><td>01</td><td>CKN</td><td>CKP</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td></tr>
<tr><td>0</td><td>10</td><td>CKN</td><td>CKP</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>0</td><td>11</td><td>CKN</td><td>CKP</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>1</td><td>00</td><td>CKP</td><td>CKN</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>1</td><td>01</td><td>CKP</td><td>CKN</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td></tr>
<tr><td>1</td><td>10</td><td>CKP</td><td>CKN</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>1</td><td>11</td><td>CKP</td><td>CKN</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
</table></td></tr>
<tr><td>CASC_ENB
(VDDI)</td><td>In</td><td>Cascade enables. (Let it connect to VDDI or VSSD).
<table>
<tr><th>CASC_ENB</th><th>Function</th></tr>
<tr><td>1</td><td>one chip cascade application</td></tr>
<tr><td>0</td><td>two chip cascade application</td></tr>
</table></td></tr>
<tr><td>MASL
(VDDI)</td><td>In</td><td>TP Master/Slave selection. (Let it connect to VDDI or VSSD)
<table>
<tr><th>MASL</th><th>Function</th></tr>
<tr><td>1</td><td>Master IC</td></tr>
<tr><td>0</td><td>Slave IC</td></tr>
</table></td></tr>
<tr><td>MODE
(VDDI)</td><td>In</td><td>LR/Multi-drop mode selection. (Let it connect to VDDI or VSSD)
<table>
<tr><th>MODE</th><th>Function</th></tr>
<tr><td>1</td><td>LR mode</td></tr>
<tr><td>0</td><td>Multi-drop mode</td></tr>
</table></td></tr>
<tr><td>BIST_EN
(VDDI)</td><td>In</td><td>BIST mode enable, high active. (Default pull Low)</td></tr>
<tr><td>CABC_PWM
_OUT</td><td>Out</td><td>Back-light enable signal. Connect to external LED driver IC.
(If not used, let it open).</td></tr>
<tr><td>TE</td><td>Out</td><td>Serves TE (Tearing Effect) output pin.
Output signal can be selected by register setting, please refer to.
(If not used, let it open).</td></tr>
</table>

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TE1	Out	Serves TE (Tearing Effect) pin of each scan line. Output signal can be selected by register setting, please refer to. **(If not used, let it open).**
LED[4:3]	Out	2 LED respiration lighting driver.
Panel control pins		
S[2401:0]	Out	Source Driver output signals. S0 and S2401 are used for Zig-Zag inversion. **(If not used, let it open).**
SX[800:1]	Out	Touch Driver output signals. **(If not used, let it open).**
GOUT_L[22:1]	Out	GOA control signal at left side. **(If not used, let it open).**
GOUT_R[22:1]	Out	GOA control signal at right side. **(If not used, let it open).**
Power pins		
VDDI	In	Power supply for digital power and digital I/O. VDDI=1.65V to 1.95V.
VCCH	In	Power supply for MIPI RX analog power. VCCH=1.65V to 1.95V. **(Connect it to VDDI in FPC).**
VSP	In	Power supply for analog circuit. VSP=4.5V to 6V.
VSN	In	Power supply for analog circuit. VSN= -4.5V to -6V.
VPP	In	External high voltage pin used in OTP mode and operates at 8.25V. **(If not used, let it open).**
VSSH	In	GND for MIPI DSI interface. **(Connect to system GND in FPC).**
VSSA	In	Analog ground. **(Connect to system GND in FPC).**
AVSS	In	Analog ground. **(Connect to system GND in FPC).**
VSSD	In	Digital ground. **(Connect to system GND in FPC).**
VSSP	In	Power ground. **(Connect to system GND in FPC).**
VSS_VMD	In	VMD ground. **(Connect to system GND in FPC).**
VSS_OSC	In	OSC circuit ground. **(Connect to system GND in FPC).**

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VSS_PLL	In	PLL circuit ground. **(Connect to system GND in FPC).**
DC to DC Converter pins		
VGH	Out	Output voltage from the step-up circuit. **(Connect it with a stabilizing capacitor).**
VGL	Out	Output voltage from the step-up circuit. **(Connect it with a stabilizing capacitor to GND and a schottky diode to VSH).**
VCI	Out	Internal charge pump output pins. **(Connect it with a stabilizing capacitor).**
VCL	Out	Internal charge pump output pins. **(Connect it with a stabilizing capacitor).**
C21P/C21N	I/O	Connect capacitor between C21P and C21N pins. These are for VGH charge pump.
C22P/C22N	I/O	Connect capacitor between C22P and C22N pins. These are for VGH charge pump.
C31P/C31N	I/O	Connect capacitor between C31P and C31N pins. These are for VGL charge pump.
C41P/C41N	I/O	Connect capacitor between C41P and C41N pins. These are for VCI charge pump.
C42P/C42N	I/O	Connect capacitor between C42P and C42N pins. These are for VCL charge pump.
VGH1_L/R	In	Power of GOUT_L/R[16:5]. **(Connect this pin to VGHO).**
VGH2_L/R	In	Power of GOUT_L/R[22:17] and GOUT_L/R[4;1]. **(Connect this pin to VGHO).**

Regulator pins		
VDDD	Out	Internal power supply for logic circuits. **(Connect it with a stabilizing capacitor).**
VDDH	Out	Internal power supply for MIPI interface circuits. **(Connect it with a stabilizing capacitor).**
VREF	Out	Internal reference voltage. **(Connect it with a stabilizing capacitor).**
VREF_TP_L/R	Out	Internal reference voltage for TP. **(Connect it with a stabilizing capacitor).**
TPVDD_L/R	Out	Internal power supply for TP. **(Connect it with a stabilizing capacitor).**
VGMP	Out	Positive regulated voltage for GAMMA. **(Connect it with a stabilizing capacitor).**
VGMN	Out	Negative regulated voltage for GAMMA. **(Connect it with a stabilizing capacitor).**
VCOM	Out	The power supply of common voltage in DC com driving.

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VCOM_FB	Out	Feedback for VCOM circuit.
VCOM_L/M	In	The common voltage in DC com driving input.
VCOM_OPT_L [2:1]	Out	Touch screen channels(VCOM ring). **(If not used, let it open).**
VCOM_OPT_R [2:1]	Out	Touch screen channels(VCOM ring). **(If not used, let it open).**
VCOM_PASS_L	I/O	VCOM pass line from ILB to OLB.
VCOM_PASS_R	I/O	VCOM pass line from ILB to OLB.
VGHO_L/R	Out	Regulator output voltage generated from VGH.
VGLO_L/R	Out	Regulator output voltage generated from VGL.
VMD	Out	Modulated voltage pin.
Touch interface pins		
KEY[6:1]	I/O	TP sensor pins for virtual button application.
TSIX	Out	Touch screen interrupt line. Interrupt active when the line is low.
TP_RESX	In	Touch circuit reset pin, active low. **(Default pull High)**
MCU_EN	In	Test pin for internal usage. **(Default pull High)**
FLASH_SS	Out	SPI master chip select. Output for serial flash interface. **(Default pull High)**
FLASH_SPI_SCL	Out	SPI master clock output for serial flash interface.
FLASH_MOSI	I/O	SPI master data output for serial flash interface.
FLASH_MISO	In	SPI master data input for serial flash interface.
FLASH_HOLD	I/O	Flash reset pin, active low or hold signal to other Flash, active low.
FLASH_WP	I/O	Flash system clock, active low. 48MHz or write protect signal to other Flash.
Serial interface		
SPI_SS	In	Serial interface chip enable signal for SPI interface, active low. **(Default pull High)**
SPI_SCL	In	Serial interface clock input for SPI interface.
SPI_MOSI	In	Serial interface data input for SPI interface.
SPI_MOSO	Out	Serial interface data output for SPI interface.
I2C_SCL	In	Serial interface clock input for I2C interface. **(I2C interface need external pull high resistance < 2.2kohm)**
I2C_SDA	I/O	Serial interface address and data input/output for I2C interface. **(I2C interface need external pull high resistance < 2.2kohm)**
Two chips cascade synchronized signals		

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SYNC_CTRL_R[7:0]	I/O	LCD cascade signals for synchronization control.
SYNC_DATA_R[7:0]	I/O	LCD cascade signals for synchronization control.
SYNC_CTRL_L[7:0]	I/O	LCD cascade signals for synchronization control.
SYNC_DATA_L[7:0]	I/O	LCD cascade signals for synchronization control.
SYNC_GAM_R[5:0]	I/O	LCD cascade signals for synchronization control.
SYNC_GAM_L[5:0]	I/O	LCD cascade signals for synchronization control.
SYNC_TP_CTRL_R[7:0]	I/O	TP signals for synchronization control.
SYNC_TP_DATA_R[7:0]	I/O	TP signals for synchronization control.
SYNC_TP_CTRL_L[7:0]	I/O	TP signals for synchronization control.
SYNC_TP_DATA_L[7:0]	I/O	TP signals for synchronization control.
Test pins		
TEST_EN	In	Internal test pins. **(Default pull Low)**
TEST_SPI	In	Internal test pins. **(Default pull Low)**
TESTI[5:0]	In	Internal test pins. **(Default pull Low)**
TESTIO[15:0]	I/O	Internal test pins. **Please let it open.**
GPIO[7:0]	Out	General purpose IO. **(If not used, let it open).**
T_OTP_RELOAD	In	Internal test pins. **(Default pull Low)**
AFE_TEST_P1/P2	Out	AFE test output1.
AFE_TEST_N	Out	AFE test output2.
TEST_P	Out	Internal test output pins. **Please let it open.**
TEST_N	Out	Internal test output pins. **Please let it open.**
PLL_REF_CLK_OUT	Out	PLL reference output. Two chip case: **It's generated by Master chip. Please connect it to XCK_IN of Master and Slave chip.** Single chip case: **Please let it open.**
OSCD_EXT	In	Oscillator1 input for test use. **(If not used, let it open).**
OSCT_EXT	In	Oscillator2 input for test use. **(If not used, let it open).**
XCK_IN	In	Cascade clock input pin. Two chip case: **Please connect it to PLL_REF_CLK_OUT.** Single chip case: **Please let it open.**
XCK_OUT	In	Clock input for test use. **(If not used, let it open).**
DCHG1_L/R DCHG2_L/R	Out	For special use. Connect serial resistance to VSSA. **(If not used, let it open).**
Dummy pins		
VGHO1_DUMMY VGHO2_DUMMY	-	Dummy pin. Please let it floating.
VGLO1_DUMMY VGLO2_DUMMY	-	Dummy pin. Please let it floating.
DUMMY_LED[6:5]	-	Dummy pin. Please let it floating.

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DUMMY_LED[2:1]		
VREF_TP_DUMMY	-	Dummy pin. Please let it floating.
AFE_TEST_DUMMY	-	Dummy pin. Please let it floating.
SXDUM[1:0]	-	Dummy pin. Please let it floating.
SDUM[1:0]	-	Dummy pin. Please let it floating.
FLASH_SCL_IN_DUMMY	-	Dummy pin. Please let it floating.
DUAL	-	Dummy pin. Please let it floating.
LR	-	Dummy pin. Please let it floating.
BOOT_DEVICE	-	Dummy pin. Please let it floating.
DUMMY[1:21]	-	Dummy pin. Please let it floating.
VSSADUMMY0~47	-	Dummy pin. Please let it floating.

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7. Interface

7.1. DSI system interface

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards.

Figure 7.1 shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.

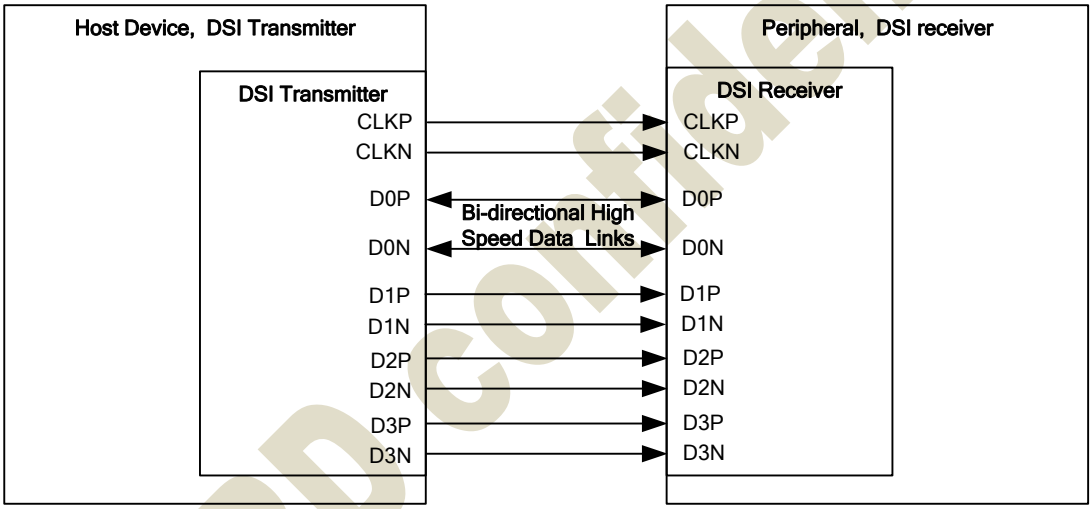


Figure 7.1: DSI transmitter and receiver interface

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A conceptual vide of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown in Figure 7.2.

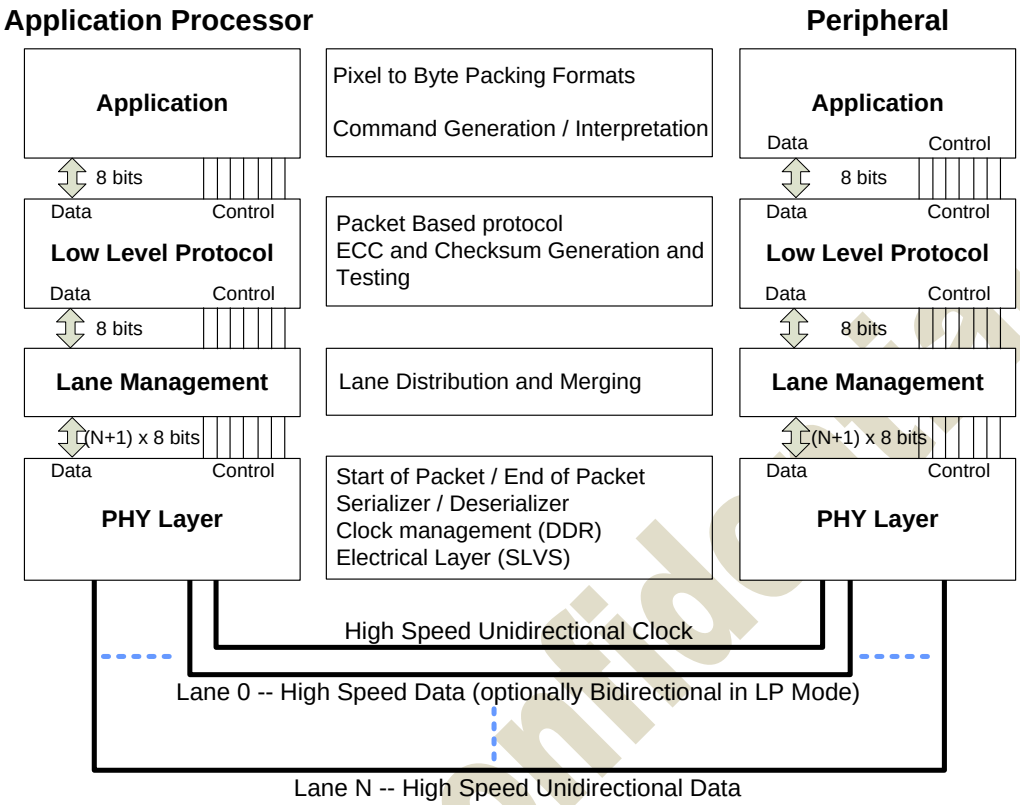


Figure 7.2: DSI Layer

PHY Layer: The PHY Layer specifies transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures “ones” and “zeroes” from the serial bit stream. Bit-level and byte-level synchronization mechanisms are included as part of the PHY.

Lane Management Layer: DSI is Lane-scalable for increased performance. The number of data signals may be 1, 2, 3, or 4 depending on the bandwidth requirements of the application. The transmitter side of the interface distributes the outgoing data stream to one or more Lanes (“distributor” function). On the receiving end, the interface collects bytes from the Lanes and merges them together into a recombined data stream that restores the original stream sequence (“merger” function).

Protocol Layer: At the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets. The protocol defines required headers for each packet, and how header information is generated and interpreted. The transmitting side of the interface appends header and error-checking information to data being transmitted. On the receiving side, the header is stripped off and interpreted by corresponding logic

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in the receiver. Error-checking information may be used to test the integrity of incoming data. DSI protocol also documents how packets may be tagged for interleaving multiple command or data streams to separate destinations using a single DSI.

Application Layer: This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module. The DSI specification describes the mapping of pixel values, commands and command parameters to bytes in the packet assembly.

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7.1.1. Command mode, Video mode and Virtual Channel

DSI-compliant peripheral support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Virtual Channel Capability

While this specification only addresses the connection of a host processor to a single peripheral, DSI incorporates a virtual channel capability for communication between a host processor and multiple, physical display modules. Since interface bandwidth is shared between peripherals, there are constraints that limit the physical extent and

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performance of multiple-peripheral systems. The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a common DSI Link. The DSI specification makes no requirements on the specific value assigned to each virtual channel used to designate interlaced fields, For clarity, the first interlaced video field may be assigned as DI[7:6] = 2'b00 and the second interlaced video field may be assigned DI[7:6] = 2'b01.

Note1: JD9365DA-H3 support both command mode and video mode.

Note2: For JD9365DA-H3, DI[7:6] for virtual channel should be set as 2’b00.

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7.1.2. Power-up Sequence Example

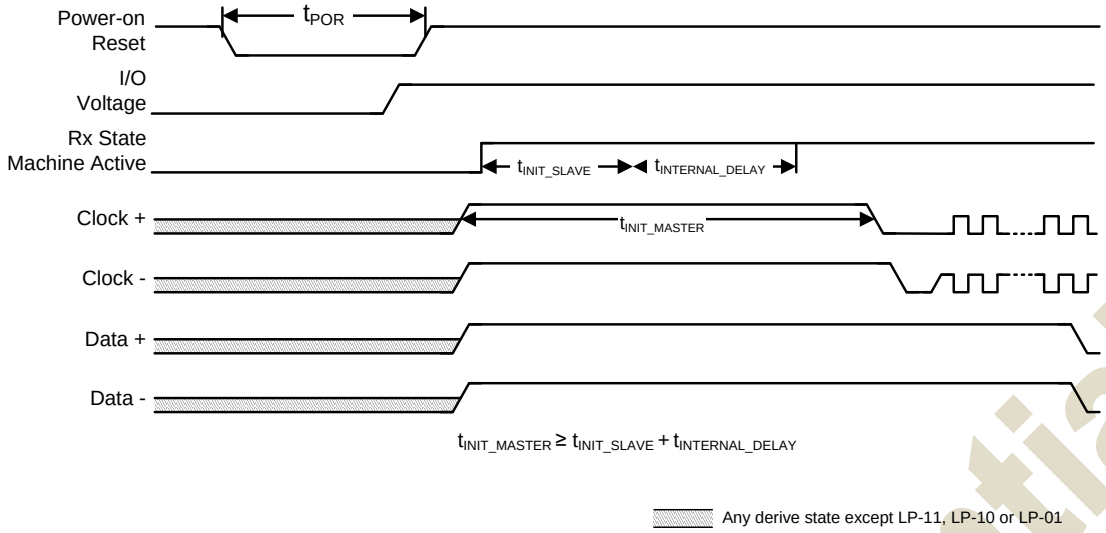


Figure 7.3: Peripheral Power-Up Sequencing Example

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7.1.3. DSI Format

Information is transferred between host processor and peripheral using one or more serial data signals and accompanying serial clock. The action of sending high-speed serial data across the bus is called a HS transmission or burst. Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 7.4 shows the basic structure of a HS transmission. N is the total number of bytes sent in the transmission

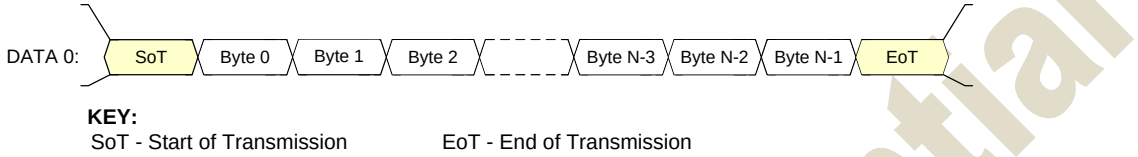


Figure 7.4: Basic HS Transmission Structure

Multi Lane Distribution and Merging

DSI is a Lane-scalable interface. Applications requiring more bandwidth than that provided by one Data Lane may expand the data path to two, three, or four Lanes wide and obtain approximately linear increases in peak bus bandwidth.

Multi-Lane implementations shall use a single common clock signal, shared by all Data Lanes. Conceptually, between the PHY and higher functional blocks is a layer that enables multi-Lane operation.

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission. Figure 7.5 & 7.6 illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

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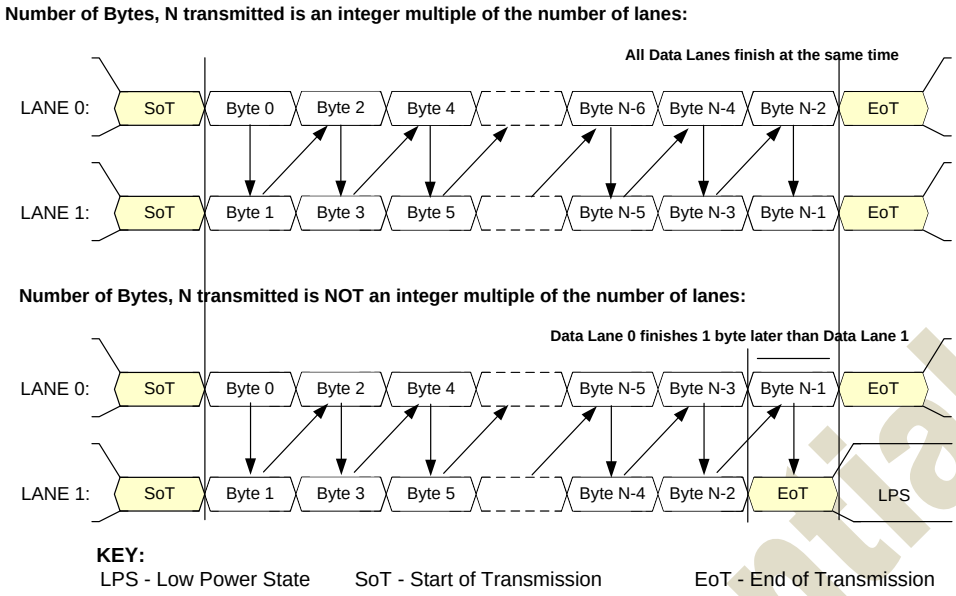


Figure 7.5: Two Lane HS Transmission Example

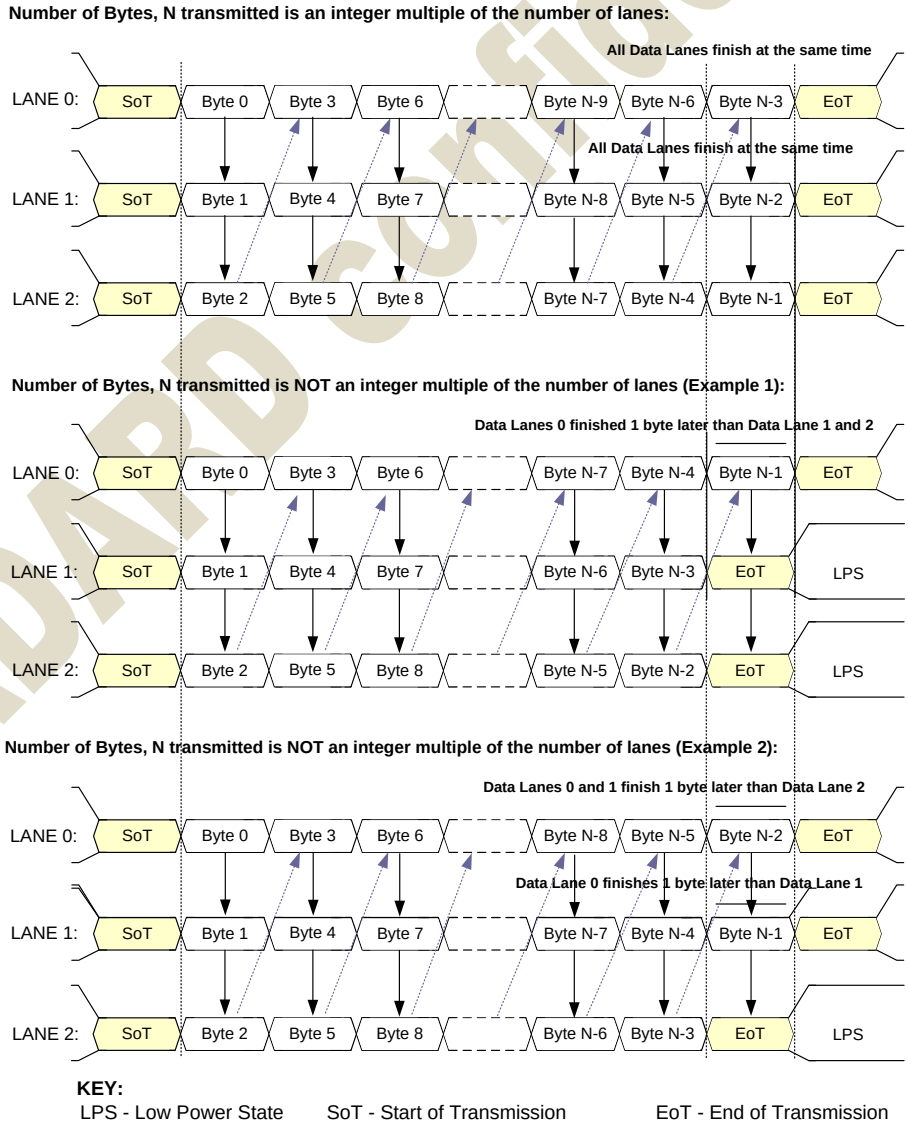


Figure 7.6: Three Lane HS Transmission Example

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7.1.4. DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets, following the packet organization documented in this section. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY.

7.1.5. Multiple Packets per Transmission

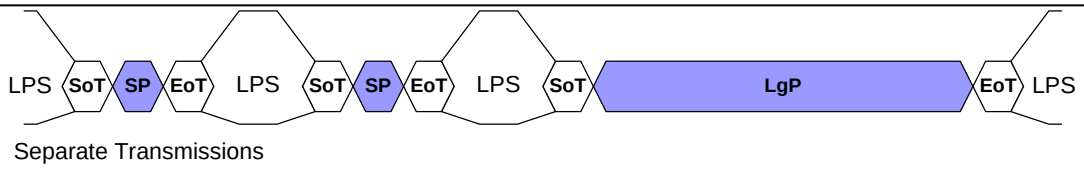
In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup.

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled. The method of enabling or disabling this capability is out of scope for this document.

The top diagram in Figure 7.7 illustrates a case where multiple packets are being sent separately with EoTp support disabled. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets. This constraint does not apply to LP transmissions. The bottom diagram in Figure 7.7 demonstrates a case where multiple packets are concatenated within a single HS transmission.

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KEY:

LPS - Low Power State
SoT - Start of Transmission
EoT - End of Transmission
SP – Short Packet
LgP – Long Packet

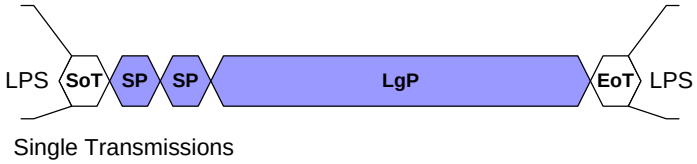
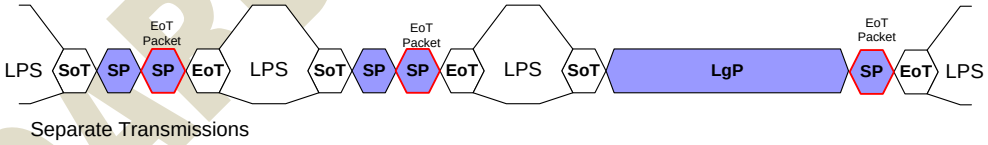


Figure 7.7: HS Transmission Examples with EoTp disabled

Figure 7.8 depicts HS transmission cases where EoTp generation is enabled. In the figure, EoT short packets are highlighted in red. The top diagram illustrates a case where a host is intending to send a short packet followed by a long packet using two separate transmissions. In this case, an additional EoT short packet is generated before each transmission ends. This mechanism provides a more robust environment, at the expense of increased overhead (four extra bytes per transmission) compared to cases where EoTp generation is disabled, i.e. the system only relies on the PHY layer EoT sequence for signaling the end of HS transmission. The overhead imposed by enabling EoTp can be minimized by sending multiple long and short packets within a single transmission as illustrated by the bottom diagram in Figure 7.8.



KEY:

LPS - Low Power State
SoT - Start of Transmission
EoT - End of Transmission
SP – Short Packet
LgP – Long Packet

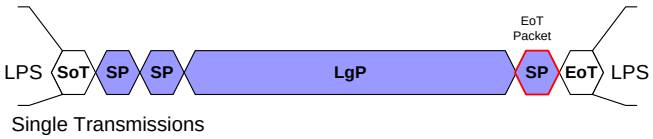


Figure 7.8: HS Transmission Examples with EoTp enabled

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7.1.6. Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure 7.9 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

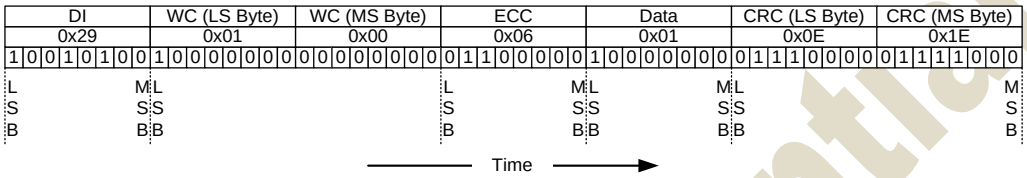


Figure 7.9: Endian Example (Long Packet)

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7.1.7. Packet Structure

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Packet sizes fall into two categories:

•**Long packets** specify the payload length using a two-byte Word Count field. Payloads may be from 0 to 216- 1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

•**Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

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7.1.8. Long Packet

Figure 7.10 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

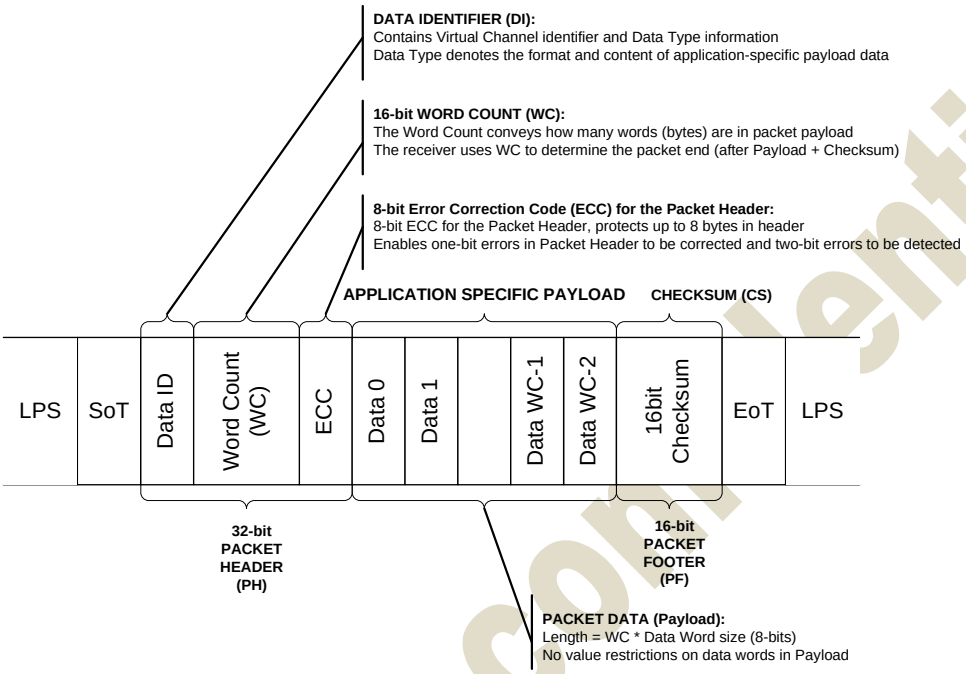


Figure 7.10: Long Packet Structure

The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data.

The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count.

The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields.

After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used.

Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the

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Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (0xFFFF). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0x0000). In the generic case, the length of the Data Payload shall be a multiple of bytes.

Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first.

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7.1.9. Short Packet

Figure 7.11 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

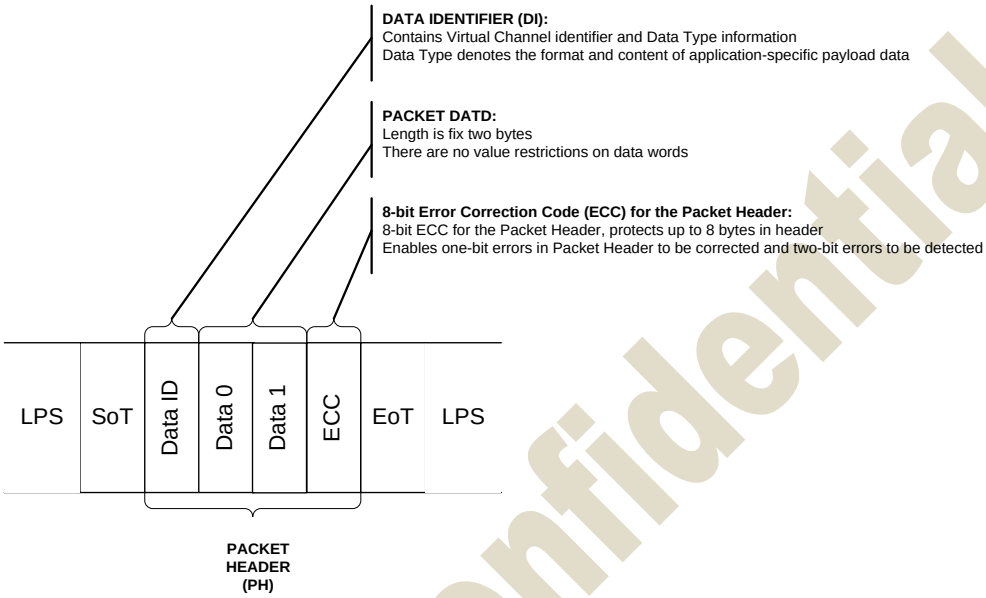


Figure 7.11: Short Packet Structure

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7.1.10.Common Packet Elements

Long and Short packets have several common elements that are described in this section.

7.1.11.Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 7.12 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels. DI[5:0]: These six bits specify the Data Type.

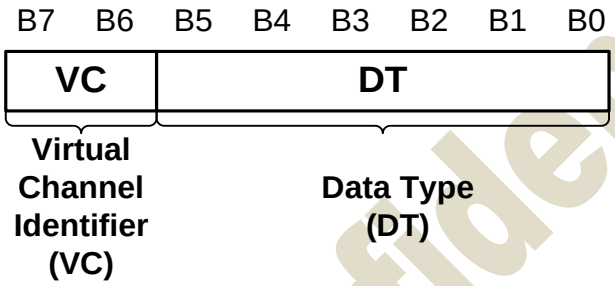


Figure 7.12: Data Identifier Byte

7.1.12.Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel.

7.1.13. Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

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7.1.14.ECC

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

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7.1.15.DSI packet

7.1.16.Processor-sourced Packets

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 7.1.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x02	00 0010	Color Mode (CM) Off Command	Short
0x12	01 0010	Color Mode (CM) On Command	Short
0x22	10 0010	Shut Down Peripheral Command	Short
0x32	11 0010	Turn On Peripheral Command	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write/write_LUT Command Packet	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
0xX0 and 0xXF unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Table 7.1: Data Types for supported Processor-sourced Packets

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7.1.17.Packed Pixel Stream, 16-bit Format, Long Packet

Packed Pixel Stream 16-Bit Format shown in Figure 7.13 is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Within a color component, the LSB is sent first, the MSB last. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

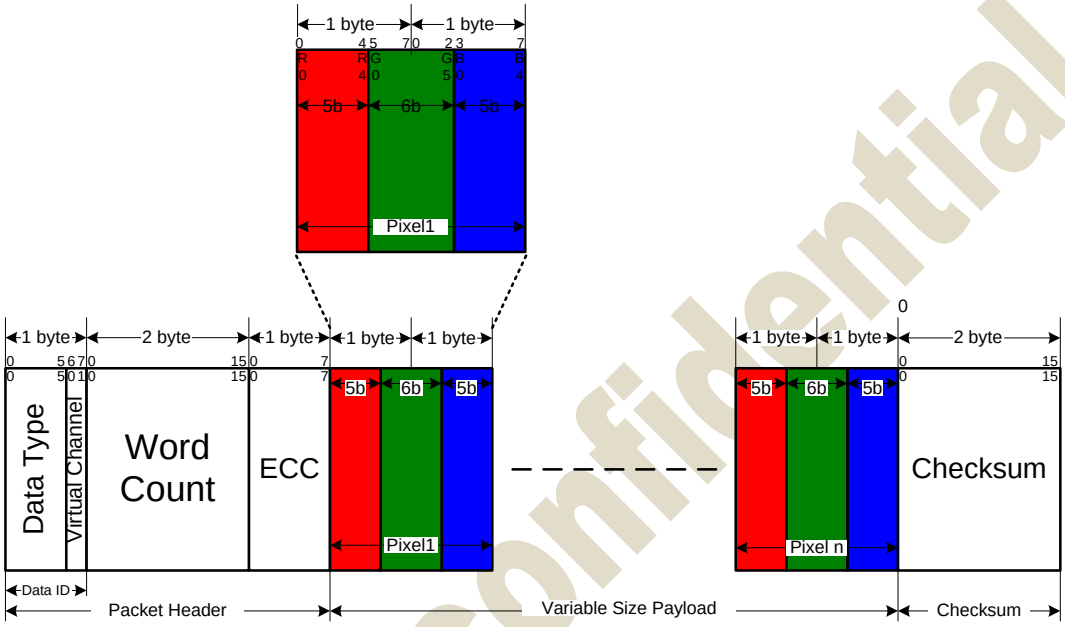


Figure 7.13: 16-bit per Pixel – RGB Color Format, Long Packet

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7.1.18.Packed Pixel Stream, 18-bit Format, Long Packet

Packed Pixel Stream 18-Bit Format (Packed) shown in Figure 7.14 is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. Peripheral will not display the fill pixels when refreshing the display device.

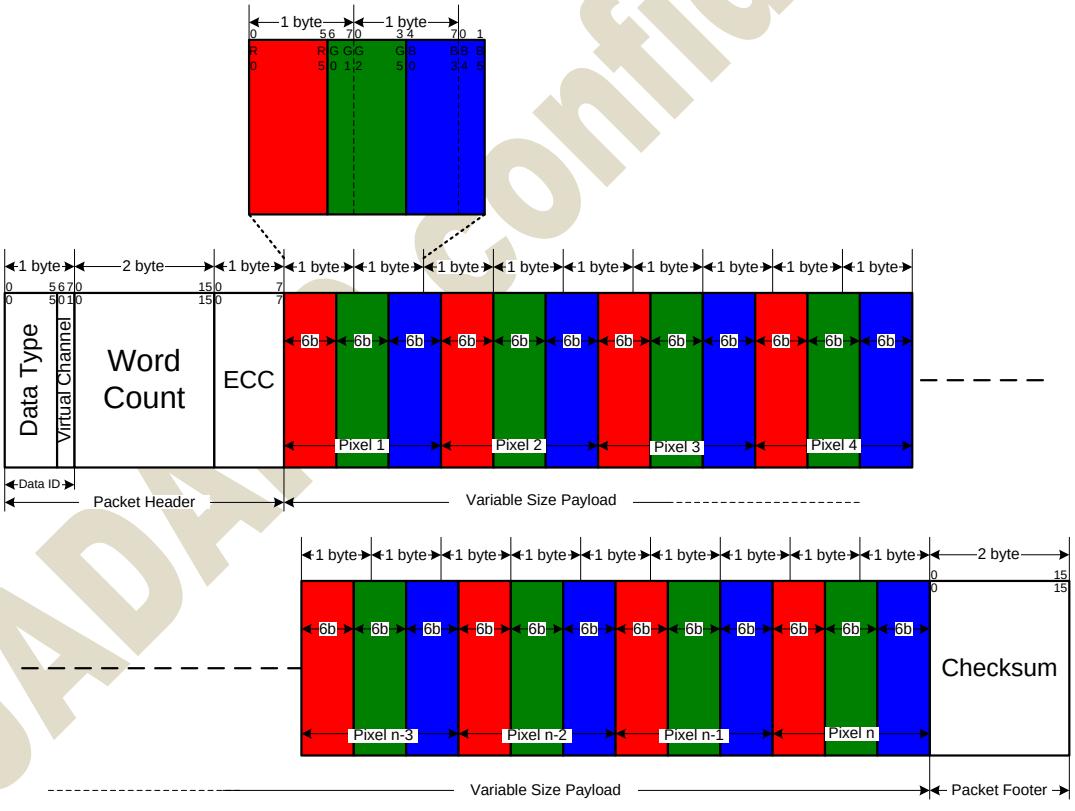


Figure 7.14: 18-bit per Pixel (Packed) – RGB Color Format, Long Packet

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7.1.19.Pixel Stream, 18-bit Loosely Format, Long Packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits, but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte as shown in Figure 7.15. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

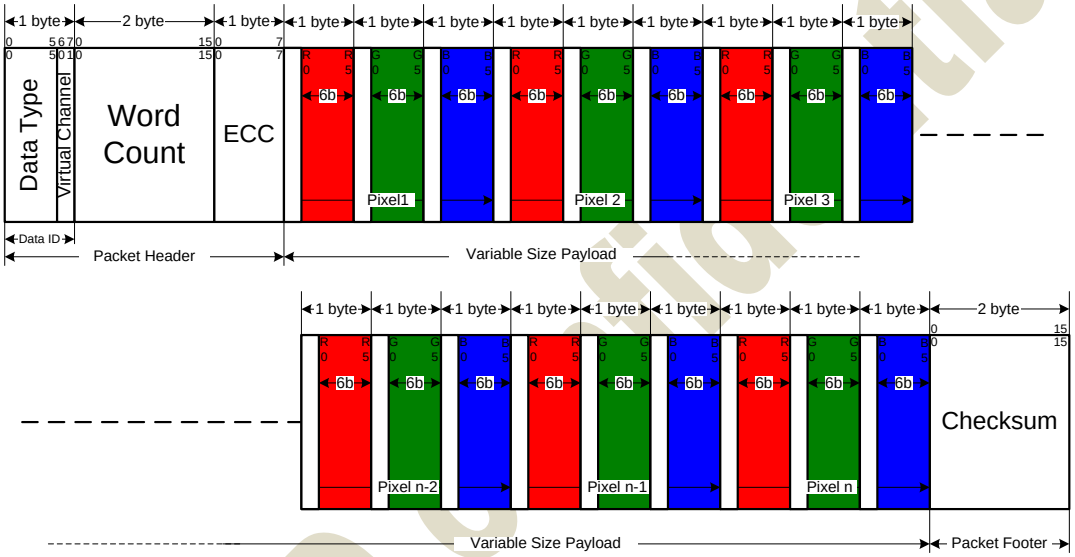


Figure 7.15: 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet

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7.1.20.Packed Pixel Stream, 24-bit Format, Long Packet

Packed Pixel Stream 24-Bit Format shown in Figure 7.16 is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

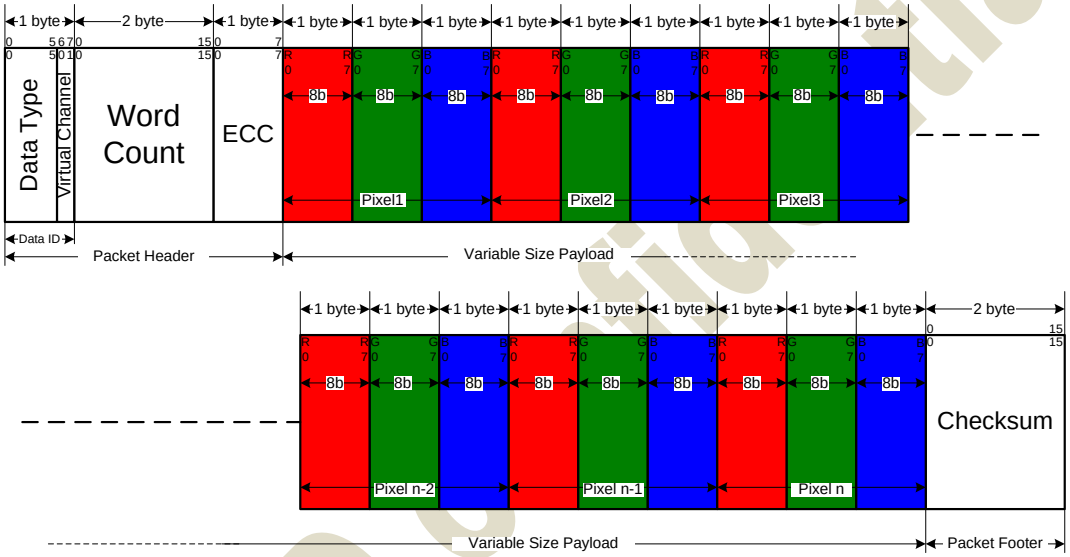


Figure 7.16: 24-bit per Pixel – RGB Color Format, Long Packet

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7.1.21.Peripheral to Processor Transmission

JD9365DA-H3 has bidirectional capability for returning READ data, acknowledge, or error information to the host processor. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.
Peripheral-to-processor transactions are of four basic types:

- **Tearing Effect (TE)** is a Trigger message sent to convey display timing information to the host processor. Trigger messages are single byte packets sent by a peripheral's PHY layer in response to a signal from the DSI protocol layer.

- **Acknowledge** is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, i.e. either triggers or packets, is received by the peripheral with no errors.

- **Acknowledge and Error Report** is a Short packet sent if any errors were detected in preceding transmissions from the host processor. Once reported, accumulated errors in the error register are cleared.

- **Response to Read Request** may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

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7.1.22. Appropriate Responses to Commands and ACK Requests

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

• Following a non-Read command, the peripheral shall respond with Acknowledge if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

• Following a Read request, the peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

• Following a Read request if only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte Acknowledge and Error Report packet in the same LP transmission. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

• Following a non-Read command if only a single-bit ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

• Following a Read request, if multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

• Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

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• Following any command, if SoT Error, SoT Sync Error or DSI VC ID Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response, with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication, in the two-byte error field. Only the Acknowledge and Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

• Following any command, if EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication. For a read command, only the Acknowledge and Error Report packet shall be transmitted; no read data shall be sent by the peripheral in response.

Once reported to the host processor, all errors documented in this section are cleared from the Error Register.

7.1.23.Peripheral-to-Processor Packet Description

Table7.2 presents the complete set of peripheral-to-processor Data Types.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x02	00 0010	Acknowledge and Error Report	Short
0x08	00 1000	End of Transmission packet	Short
0x1C	01 1100	DCS Long READ Response	Long

Table 7.2: Data Types for Peripheral-sourced Packets

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7.1.24.Format of Acknowledge and Error Report and Read Response Data Type

Acknowledge is sent using a Trigger message.

- Byte 0: 00100001 (shown here in first bit [left] to last bit [right] sequence)

Response to Read Request returns data requested by the preceding READ command from the processor. These may be short or Long packets. The format for short READ packet responses is:

- Byte 0: Data Identifier (Virtual Channel ID + Data Type)

- Bytes 1, 2: READ data, may be one or two bytes. For single byte parameters, the parameter shall be returned in Byte 1 and Byte 2 shall be set to 0x00.

- ECC byte covering the header

Acknowledge and Error Report confirms that the preceding command or data sent from the host processor to a peripheral was received, and indicates what types of error were detected on the transmission and any preceding transmissions. Note that if errors accumulate from multiple preceding transmissions, it may be difficult or impossible to identify which transmission contained the error. This message is a Short packet of four bytes, taking the form:

- Byte 0: Data Identifier (Virtual Channel ID + Acknowledge Data Type)

- Byte 1: Error Report bits 0-7

- Byte 2: Error Report bits 8-15

- ECC byte covering the header

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. Table 7.3 shows the bit assignment for all error reporting.

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Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, Single-bit (detected and corrected)
9	ECC Error, Multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Table 7.3: Error Report Bit Definitions

The first eight bits, bit 0 through bit 7, are related to the physical layer errors. Bits 8 and 9 are related to single-bit and multi-bit ECC errors. The remaining bits indicate DSI protocol-specific errors.

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7.1.25.Video Mode Interface Timing

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

7.1.26.Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- **Non-Burst Mode with Sync Pulses –** enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

- **Non-Burst Mode with Sync Events –** similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

- **Burst mode –** RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral.

To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. The host processor should return to LP state once per scanline during the horizontal blanking time.

During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX

- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode

- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

- If the previous processor-to-peripheral transmission ended with BTA, transmit one or

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more packets from the peripheral to the host processor using Escape Mode

・Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with VSE or HSS. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet.

Transmission packet components used in the figures in this section are defined in Figure 7.17 unless otherwise specified.

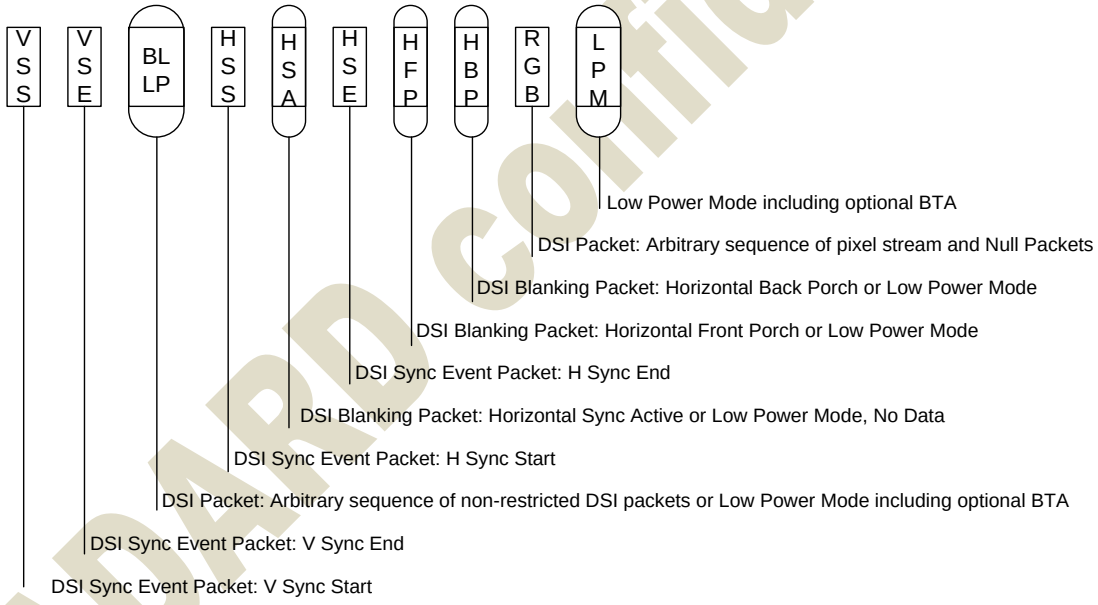


Figure 7.17: Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

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7.1.27.Non-Burst sync pulse mode

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure 7.18.

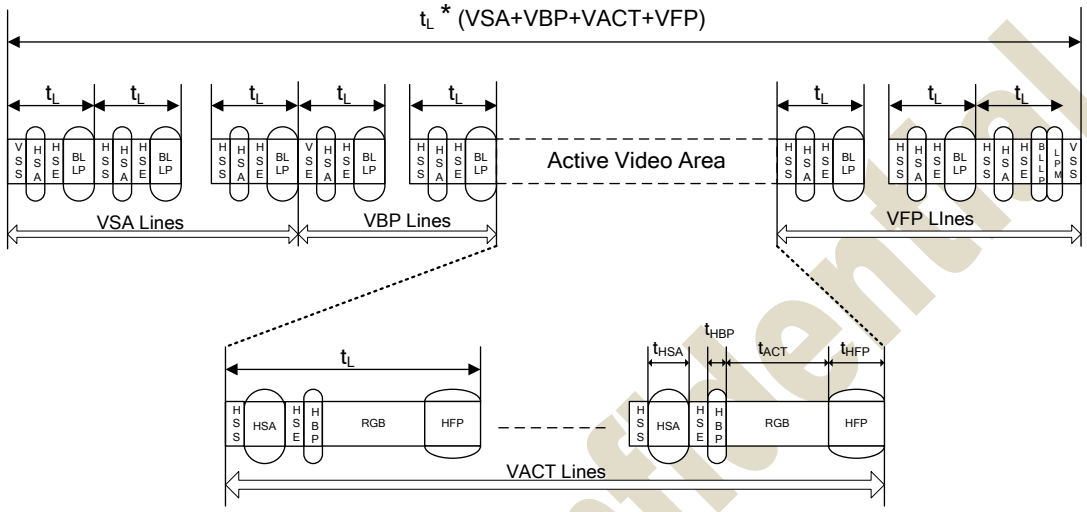


Figure 7.18: Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power. During HSA, HBP and HFP periods, the bus should stay in the LP-11 state.

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7.1.28.Non-Burst sync event mode

This mode is a simplification of the “Non-Burst Mode with Sync Pulses” format. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. An example of this mode is shown in Figure 7.19.

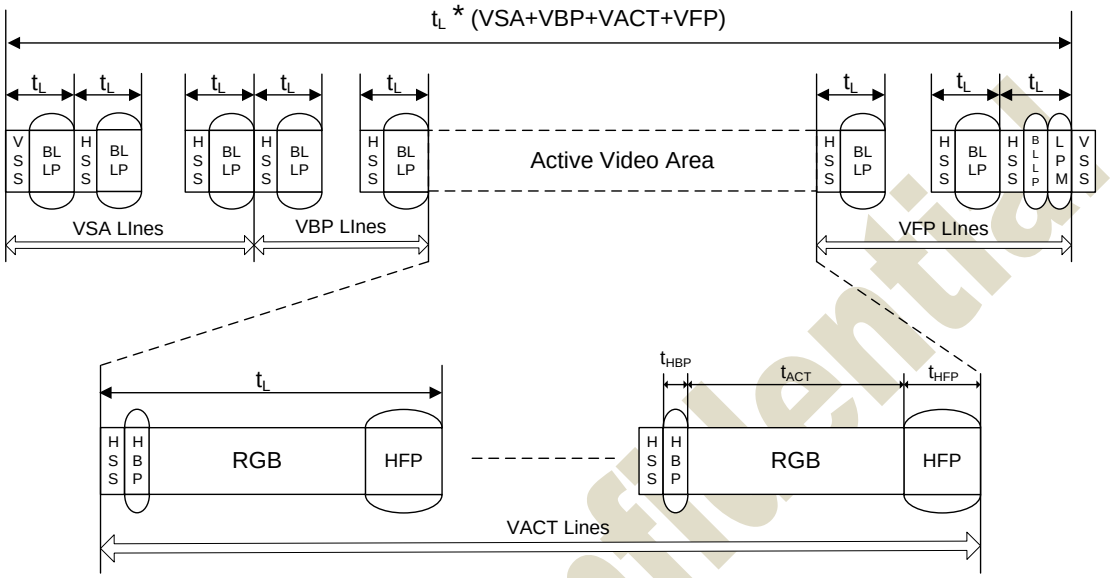


Figure 7.19: Video Mode Interface Timing: Non-burst Transmission with Sync Events

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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7.1.29.Burst mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

Following HS pixel data transmission, the bus may stay in HS Mode for sending blanking packets or go to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure 7.20.

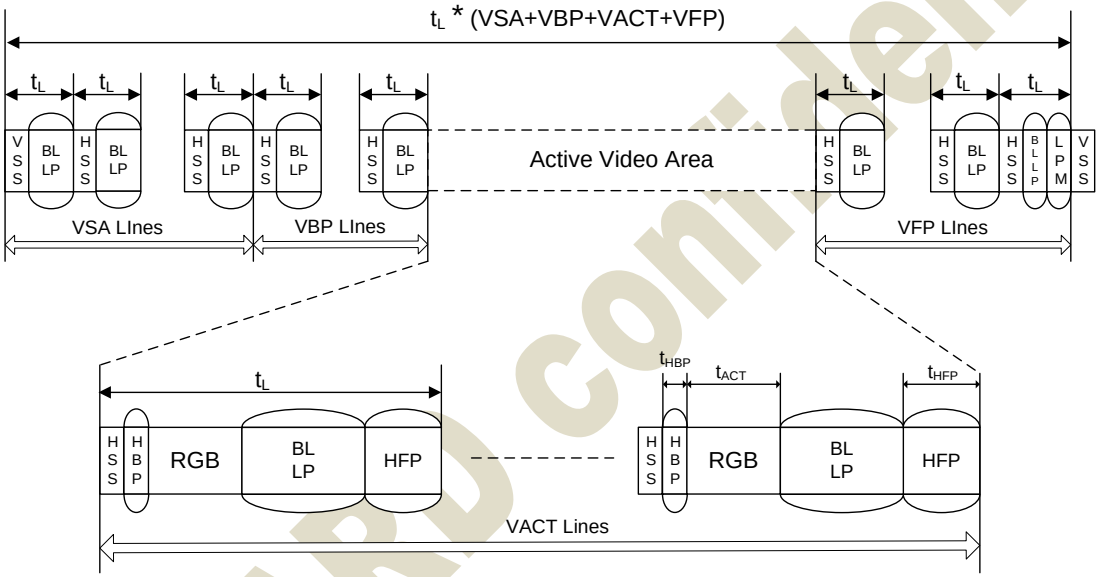


Figure 7.20: Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

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7.1.30.Error-Correcting Code and Checksum

7.1.31.Error-Correcting Code(ECC)

MIPI DSI uses Hamming Code Theory as ECC generate rule. The parity of each bits in ECC are showed as below.

P7=0

P6=0

P5=D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4=D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3=D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2=D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

P1=D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0=D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

ECC is generated from the twenty-four bits with in the Packet Header as illustrated in Figure 7.21, which also serves as an ECC calculation example.

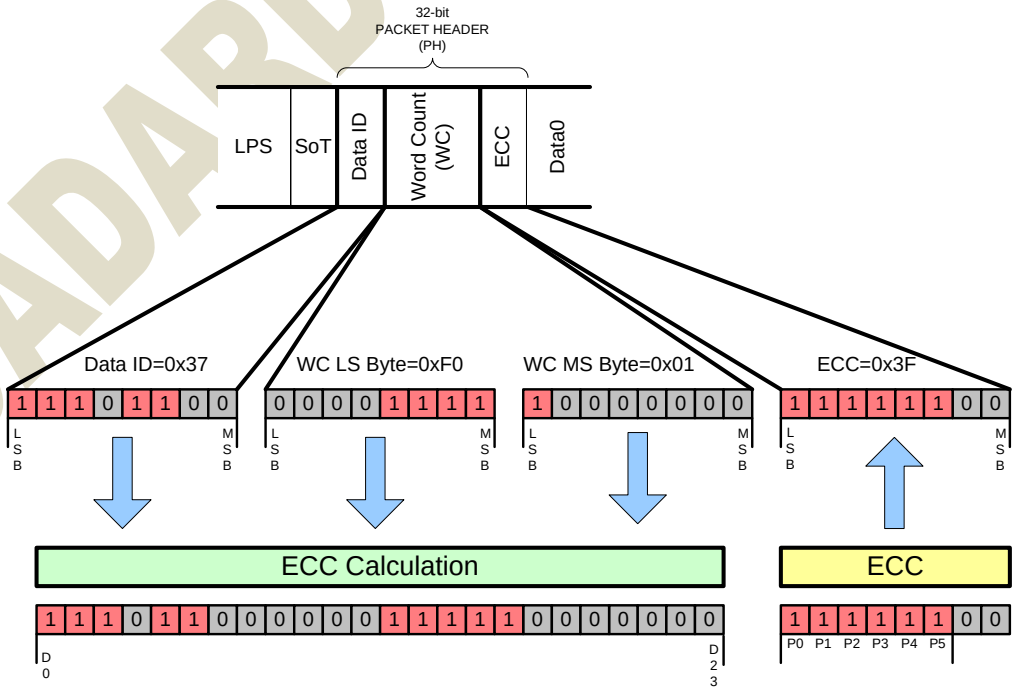


Figure 7.21: 24-bit ECC generation Example

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7.1.32.Checksum Generation for Long Packet Payloads

To detect errors in transmission of Long packets, a checksum is calculated over the payload portion of the data packet. Note that, for the special case of a zero- length payload, the 2-byte checksum is set to 0xFFFF. The checksum shall be realized as a 16-bit CRC with a generator polynomial of x^16+x^12+x^5+x^0

The transmission of the checksum is illustrated in Figure 7.22. The LS byte is sent first, followed by the MS byte. Note that within the byte, the LS bit is sent first.

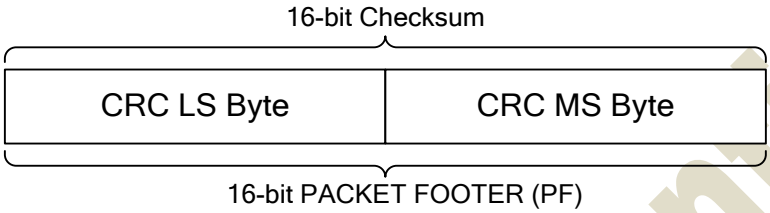


Figure 7.22: Checksum Transmission

The CRC implementation is presented in Figure 7.23. The CRC shift register shall be initialized to 0xFFFF before packet data enters. Packet data not including the Packet Header then enters as a bitwise data stream from the left, LS bit first. Each bit is fed through the CRC shift register before it is passed to the output for transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift register, the shift register contains the checksum. C15 contains the checksum's MSB and C0 the LSB of the 16-bit checksum. The checksum is then appended to the data stream and sent to the receiver. The receiver uses its own generated CRC to verify that no errors have occurred in transmission.

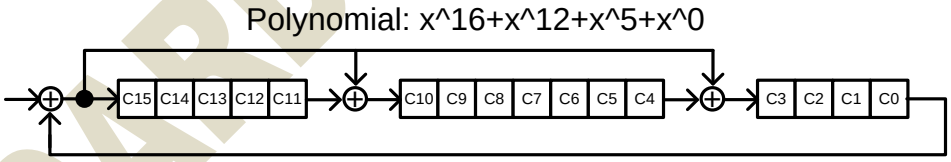


Figure 7.23: 16-bit CRC Generation Using a Shift Register

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7.1.33.DPHY

7.1.34.Lane Module

A PHY configuration contains a Clock Lane Module and one or more Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect wires simultaneously, one or more single-ended Low-Power functions operating on each of the interconnect wires individually, and control & interface logic. For proper operation, the set of functions in the Lane Modules on both sides of the Lane Interconnect has to be matched.

7.1.35.Lane Module Type of Clock Lane, Data0, Data1 and Data2

The required functions in a Lane Module depend on the Lane type and which side (master or slave) of the Lane Interconnect the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and Bi-directional Data Lane. Several PHY configurations can be constructed with these Lane types. In JD9365DA-H3 Below show the lane module architecture of each lane.

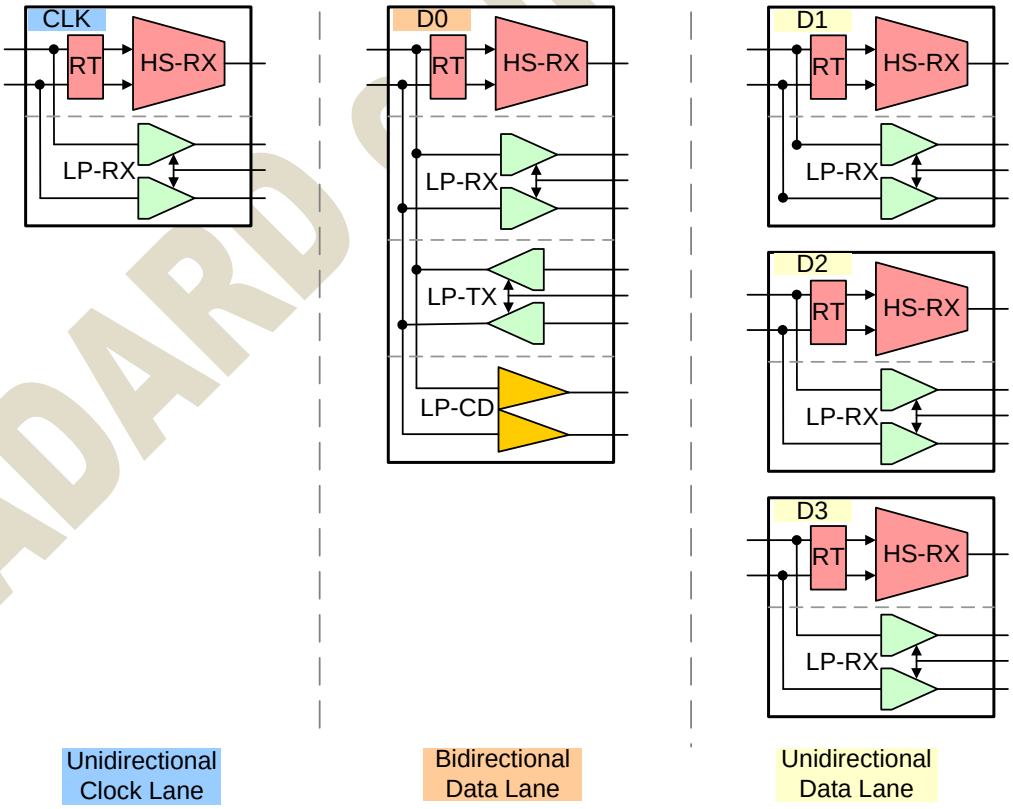


Figure 7.24: Lane Module Type

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7.1.36.Master and Slave

Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. The main direction of data communication, from source to sink, is denoted as the Forward direction. Data communication in the opposite direction is called Reverse transmission. Only bi-directional Data Lanes can transmit in the Reverse direction. In all cases, the Clock Lane remains in the Forward direction, but bi-directional Data Lane(s) can be turned around, sourcing data from the Slave side.

JD9365DA-H3 serves as Slave side.

7.1.37.Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High- Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential- 0 and Differential-1. The interpretation of Low-Power Lane states depends on the mode of operation. The LP-Receivers shall always interpret both High-Speed differential states as LP-00.

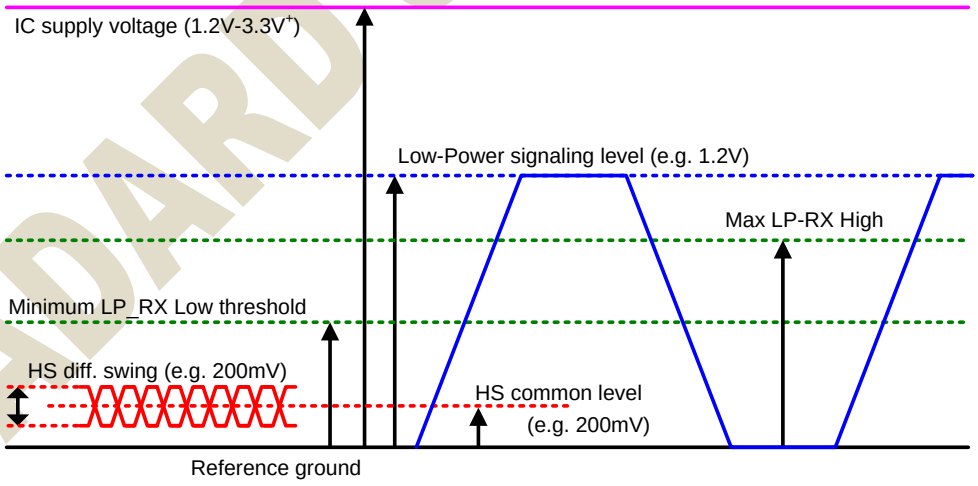


Figure 7.25: Line Levels

The Stop state has a very exclusive and central function. If the Line levels show a Stop state for the minimum required time, the PHY state machine shall return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. Table 7.4 lists all the states that can appear on a Lane during normal operation. All LP state periods shall be at least TLPX in duration. State

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transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines. Ideally, the reconstructed clock has a duration of at least 2*TLPX, but may have a duty cycle other than 50% due to signal slope and trip levels effects.

Start Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

Table 7.4: Lane State Descriptions

7.1.38.Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Notice that Master and Slave side shall not be changed by Turnaround.

Figure 7.26 shows the Turnaround procedure graphically.

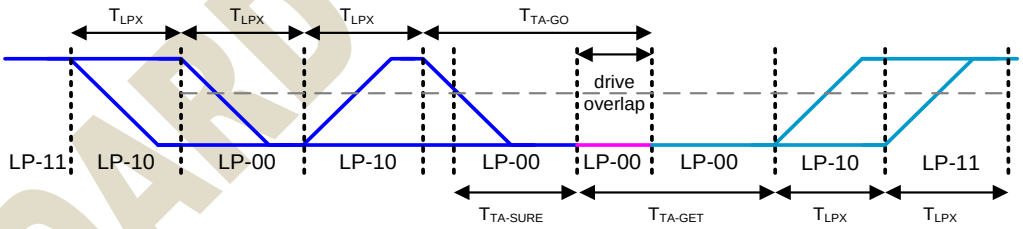


Figure 7.26: Turnaround Procedure

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7.1.39.Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command, by Spaced-One-Hot coding, to indicate the requested action. Table 7.5 lists all supported Escape mode commands and actions.

Spaced-One-Hot coding means that each Mark state is interleaved with a Space state. Each symbol consists therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0 followed by a Space to transmit a ‘zero-bit’ and it shall send a Mark-1 followed by a Space to transmit a ‘one-bit’. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not followed by a Space state.

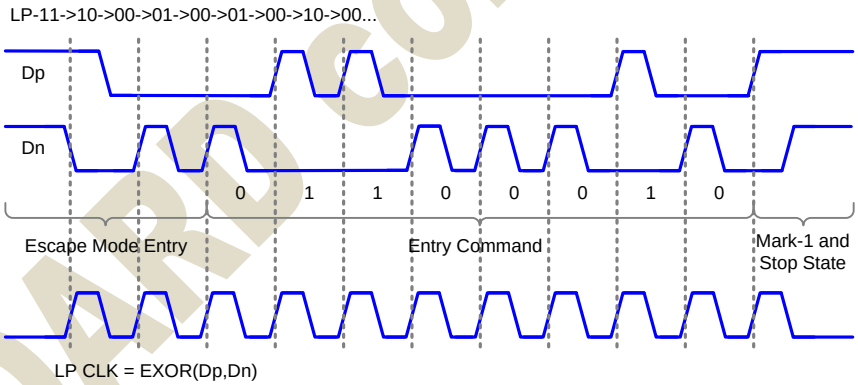


Figure 7.27: Trigger-Reset Command in Escape Mode

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low power State	mode	00011110
Reset-Trigger	Trigger	01100010
TE-Trigger	Trigger	01011101
Acknowledge	Trigger	00100001

Table 7.5: Escape Entry Codes

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7.1.40.Remote Trigger

Trigger signaling is the mechanism to send a flag to the protocol at the receiving side, on request of the protocol on the transmitting side. This can be either in the Forward or Reverse direction depending on the direction of operation and available Escape mode functionality. Trigger signaling requires Escape mode capability and at least one matching Trigger Escape Entry Command on both sides of the interface. Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

7.1.41.Low-Power Data Transmission(LPDT)

If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode. Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. The data is self-clocked by the applied bit encoding and does not rely on the Clock Lane. The Lane can pause while using LPDT by maintaining a Space state on the Lines. A Stop state on the Lines stops LPDT, exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a Mark-1 state, which does not represent a data-bit. At the end of LPDT the Lane shall return to the Stop state.

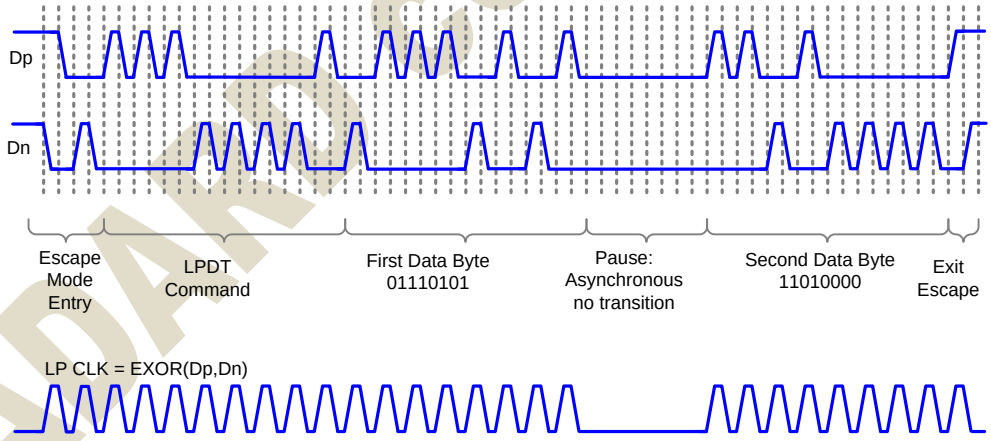


Figure 7.28: Two Data Byte Low-Power Data Transmission Example

7.1.42.Ultra-Low Power State(ULPS)

If the Ultra-Low Power State Entry Command is sent after an Escape mode Entry command, the Lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

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7.1.43.TE Trigger

A Command Mode display module has its own timing controller and local frame buffer for display refresh. In some cases the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bidirectional Data Lane.

For polling to the display module, the host processor shall detect the current scan line information with a DCS command such as get_scan_line to avoid Tearing Effects. For TE-reporting from the display module, the TE-reporting function is enabled and disabled by three DCS commands to the display module's controller: set_tear_on, set_tear_scanline, and set_tear_off.

set_tear_on and set_tear_scanline are sent to the display module as DSI Data Type 0x15 (DCS Short Write, one parameter) and DSI Data Type 0x39 (DCS Long Write/write_LUT), respectively. The host processor ends the transmission with Bus Turn-Around asserted, giving bus possession to the display module. Since the display module's DSI Protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with a normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession.

To enable TE-reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE reporting has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) Bus Turn-Around signal to its D-PHY functional block. The PHY layer will then initiate a Bus Turn-Around sequence in LP mode, which gives bus possession to the display module.

Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait for up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or requests to the display module, because it does not have bus possession.

When the TE event takes place the display module shall send TE event information in LP mode using a specified trigger message available with D-PHY protocol via the following sequence:

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・The display module shall send the LP Escape Mode sequence

・The display module shall then send the trigger message byte 01011101 (shown here in first bit to last bit sequence)

・The display module shall then return bus possession to the host processor

This Trigger Message is reserved by DSI for TE signaling only and shall not be used for any other purpose in a DSI-compliant interface.

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7.1.44.High Speed Transmission

7.1.45.Burst Payload Data

The payload data of a burst shall always represent an integer number of payload data bytes with a minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data. There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the practical BER will not be zero. Therefore, it is important to consider for every individual protocol what the best choice is for maximum burst length.

7.1.46.Start-of-Transmission

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure. Table 7.6 describes the sequence of events on TX and RX side.

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS-PREPARE}$	Observes transition from LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D-TERM-EN}$
Enables High-Speed driver and disables Low-Powerdrivers simultaneously.	
Drives HS-0 for a time $T_{HS-ZERO}$	Enables HS-RX and waits for timer $T_{HS-SETTLE}$ to expire in order to neglect transition effects
	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence ‘00011101’ beginning on a rising Clock edge	
	Synchronizes upon recognition of Leader Sequence ‘011101’
Continues to Transmit High-Speed payload data	
	Receives payload data

Table 7.6: Start-of-Transmission Sequence

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7.1.47.End-of-Transmission

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 7.7 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

TX Side	RX Side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS-SKIP}$ to hide transition effects
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

Table 7.7: End-of-Transmission Sequence

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7.1.48.High Speed Data Transmission

Figure 7.29 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane.

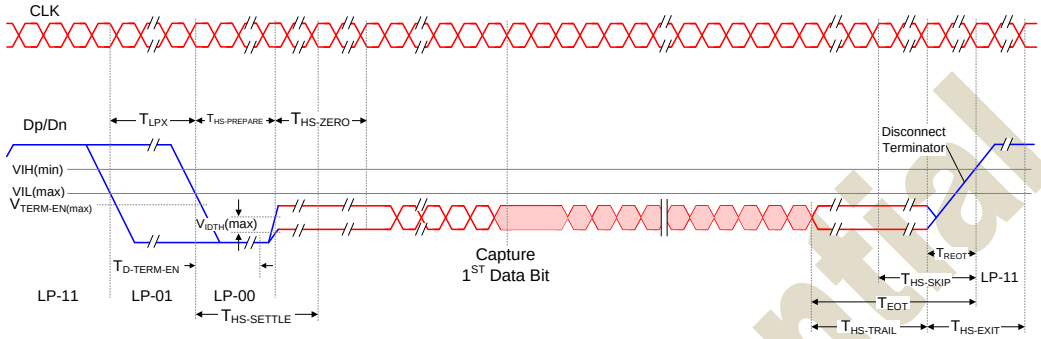


Figure 7.29: High-Speed Data Transmission in Bursts

7.1.49.High Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of the first transmitted bit of a burst. The detail Clock Start and Stop procedures are shown in Figure 7.30.

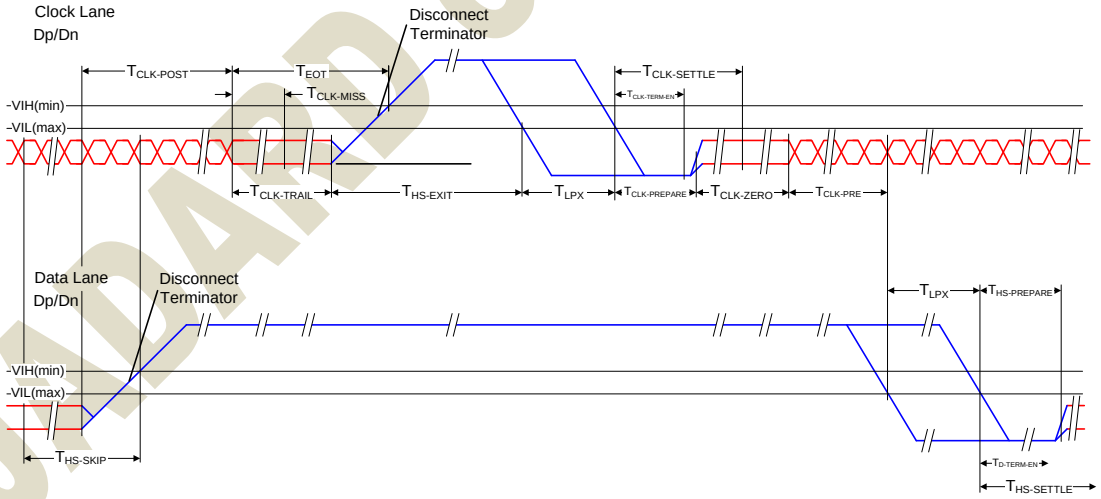


Figure 7.30: Switching the Clock Lane between Clock Transmission and Low-Power Mode

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7.1.50.System Power state

Each Lane within a PHY configuration, that is powered and enabled, has potentially three different power consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low Power State.

7.1.51.Initialization

After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer then TINIT. The first Stop state longer than the specified TINIT is called the Initialization period. The Master side shall ensure that a Stop State longer than TINIT does not occur on the Lines before the Master is initialized.

TINIT must larger than 500us.

7.1.52.Global Operation Flow Diagram

Figure 7.31 shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround, and Initialization.

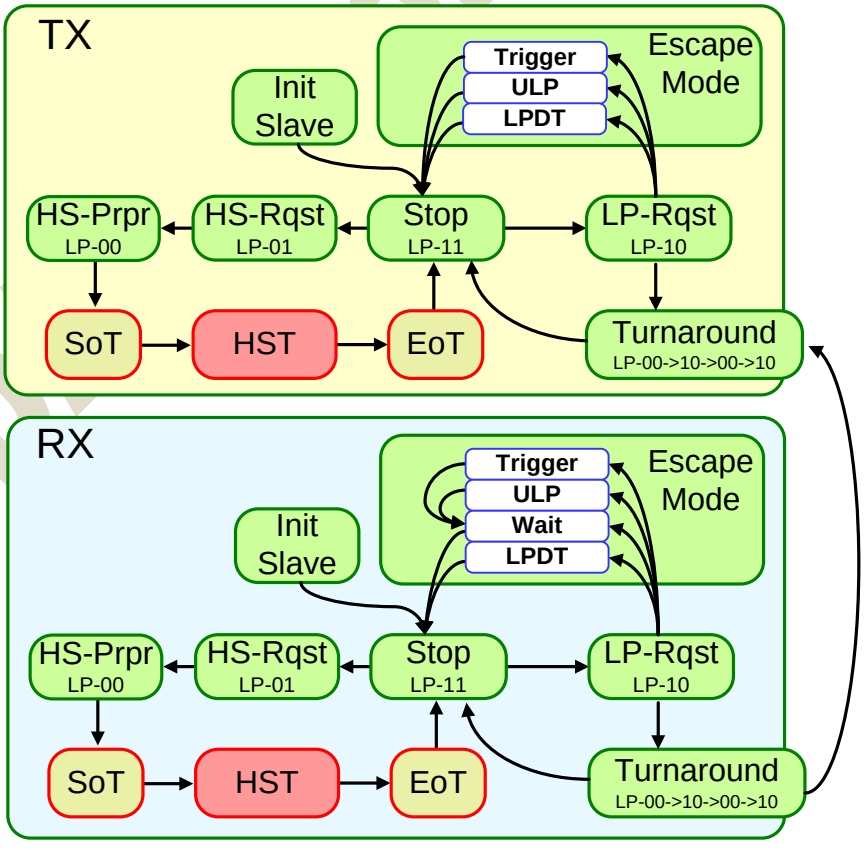


Figure 7.31: Data Lane Module State Diagram

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Figure 7.32 shows the state diagram for a Clock Lane Module. The Clock Lane Module has four major operational states: Init (of unspecified duration), Low-Power Stop state, Ultra-Low Power state, and High- Speed clock transmission.

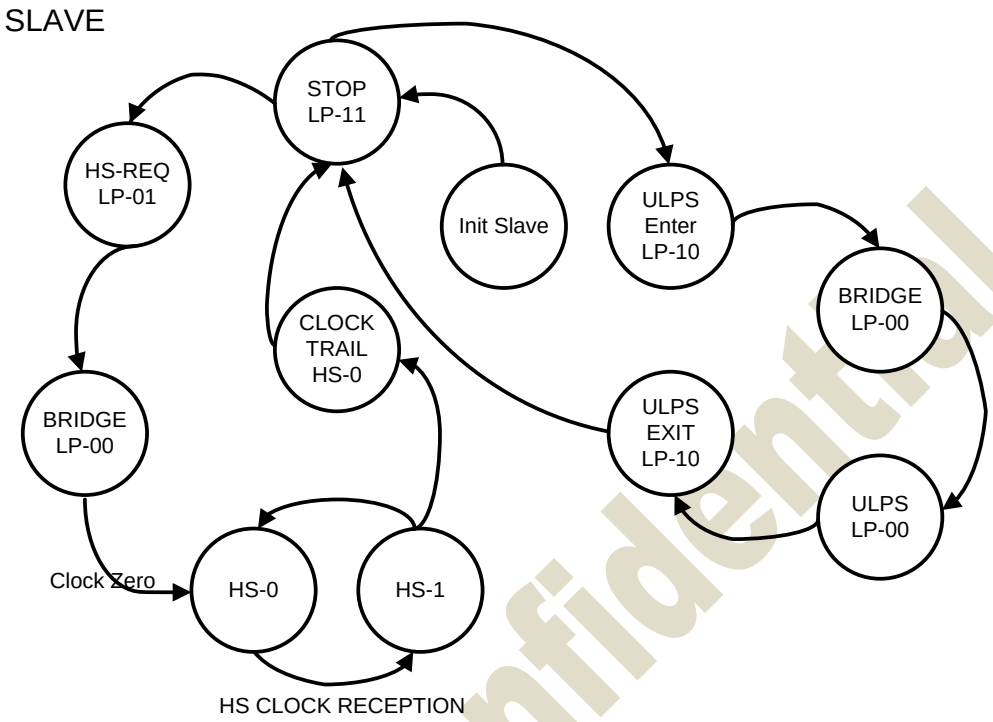


Figure 7.32: Clock Lane Module State Diagram

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8. The Power On/Off Sequence

8.1. Power on sequence for display initial code by FW

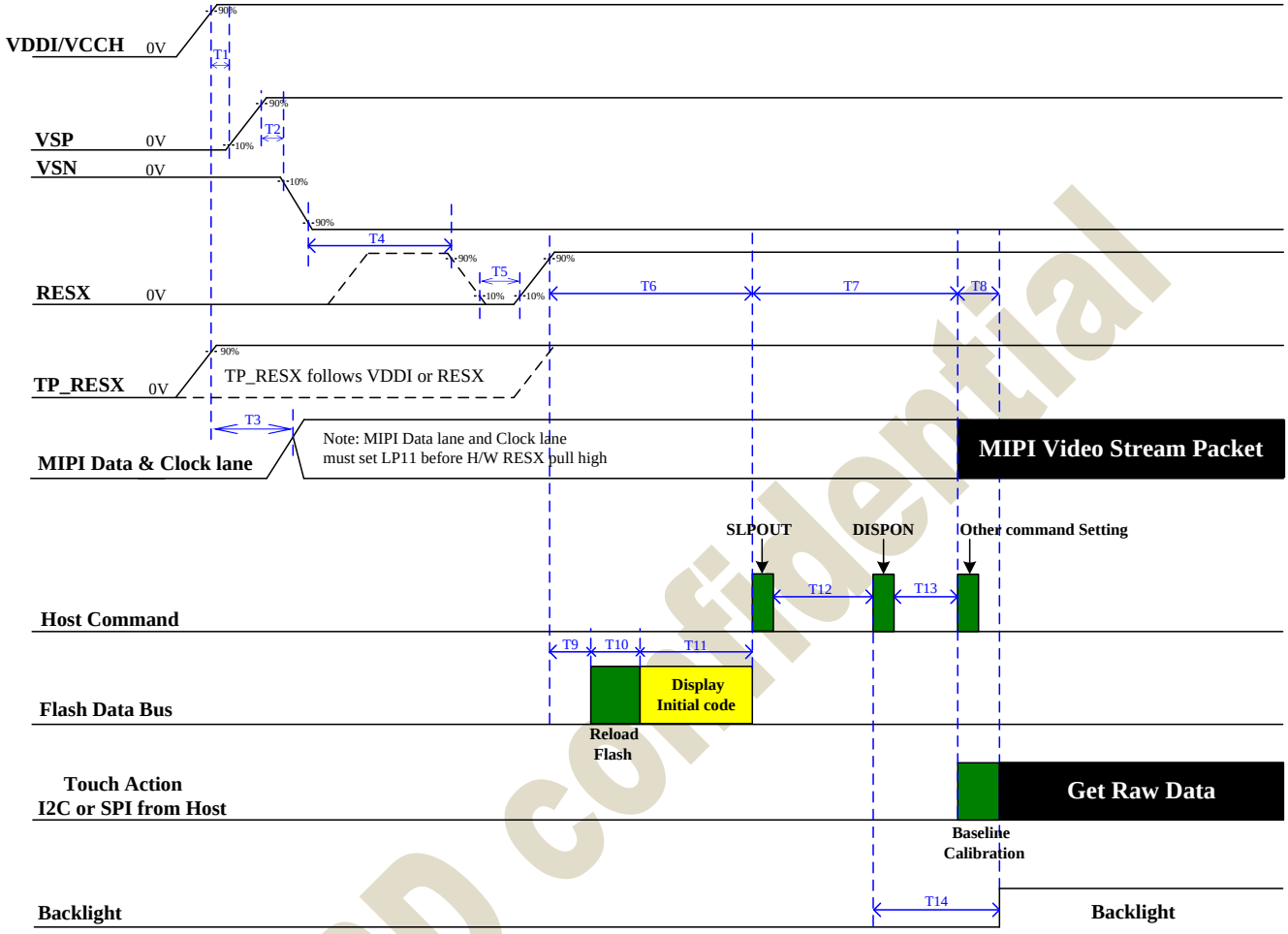


Figure 8.1: Power on sequence by FW

Symbol	Description	Min	Max	Unit	Note
T1	VDD1 to VSP	1	-	ms	
T2	VSP to VSN	1	-	ms	
T3	VDD1 to MIPI Lane	1	-	ms	
T4	Power Ready to Global Reset	1	-	ms	
T5	Global Reset Keep Low	15	-	us	TP Reset is the same
T6	Global Reset to Sleep Out	215	-	ms	
T7	Video Stream Start and Host TP Data Bus Active	140	-	ms	
T8	AP Start to Get Raw Data	30	-	ms	
T9	Reset to Flash Reload	-	5	ms	
T10	Flash Reload Time	-	115	ms	
T11	Display initial code by FW	-	100	ms	
T12	Sleep Out to Display On	10	-	ms	
T13	Display On to IC Ready	20	-	ms	
T14	Display On Command to BL On time	40	-	ms	

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8.2. Power on sequence for display initial code by Host

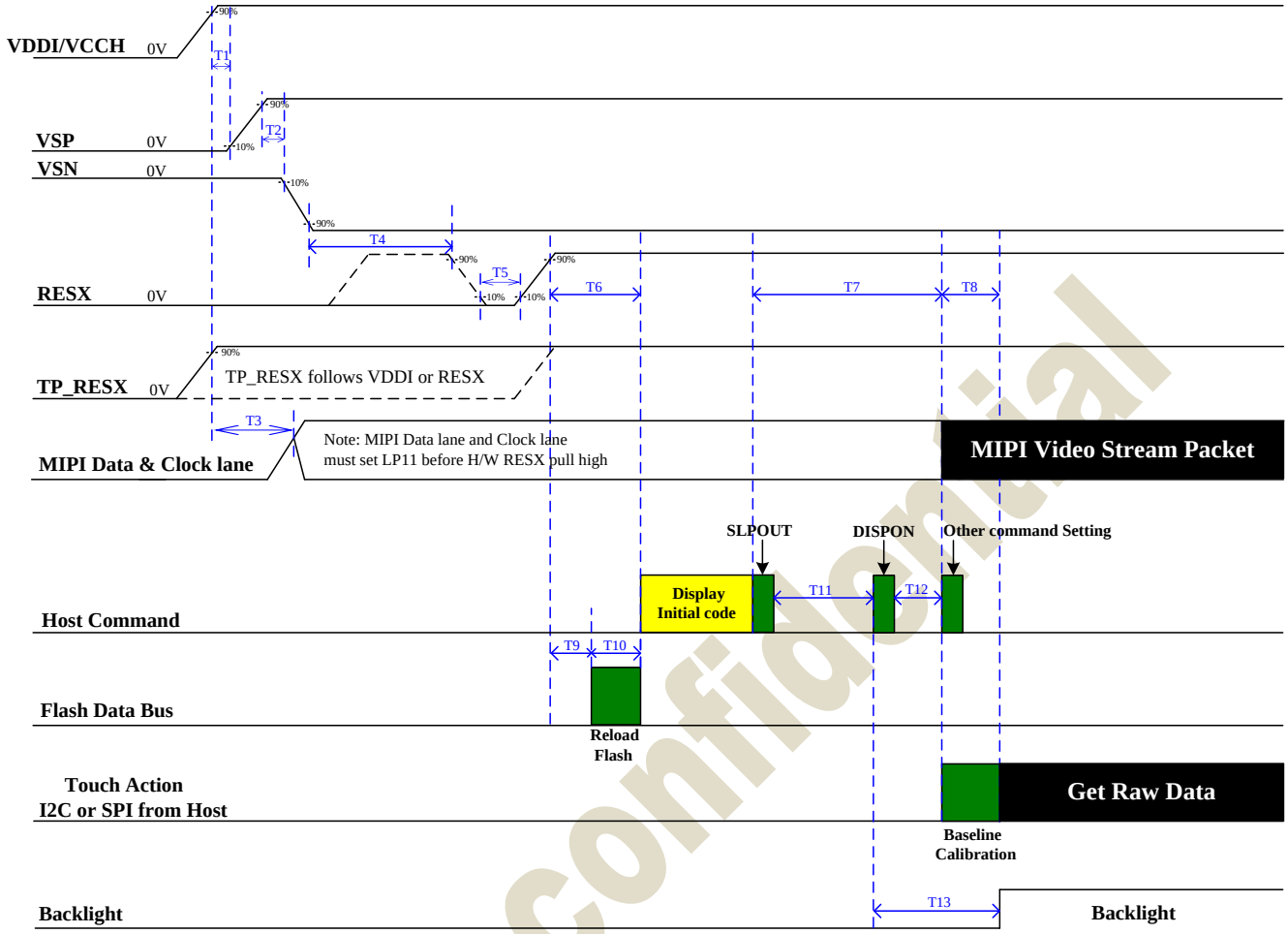


Figure 8.2: Power on sequence by Host

Symbol	Description	Min	Max	Unit	Note
T1	VDD1 to VSP	1	-	ms	
T2	VSP to VSN	1	-	ms	
T3	VDD1 to MIPI Lane	1	-	ms	
T4	Power Ready to Global Reset	1	-	ms	
T5	Global Reset Keep Low	15	-	us	TP Reset is the same
T6	Global Reset to Display Initial Code by Host	120	-	ms	
T7	Video Stream Start and Host TP Data Bus Active	140	-	ms	
T8	AP Start to Get Raw Data	30	-	ms	
T9	Reset to Flash Reload	-	5	ms	
T10	Flash Reload Time	-	115	ms	
T11	Sleep Out to Display On	10	-	ms	
T12	Display On to IC Ready	20	-	ms	
T13	Display On Command to BL On time	40	-	ms	

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8.3. Power off sequence for external power

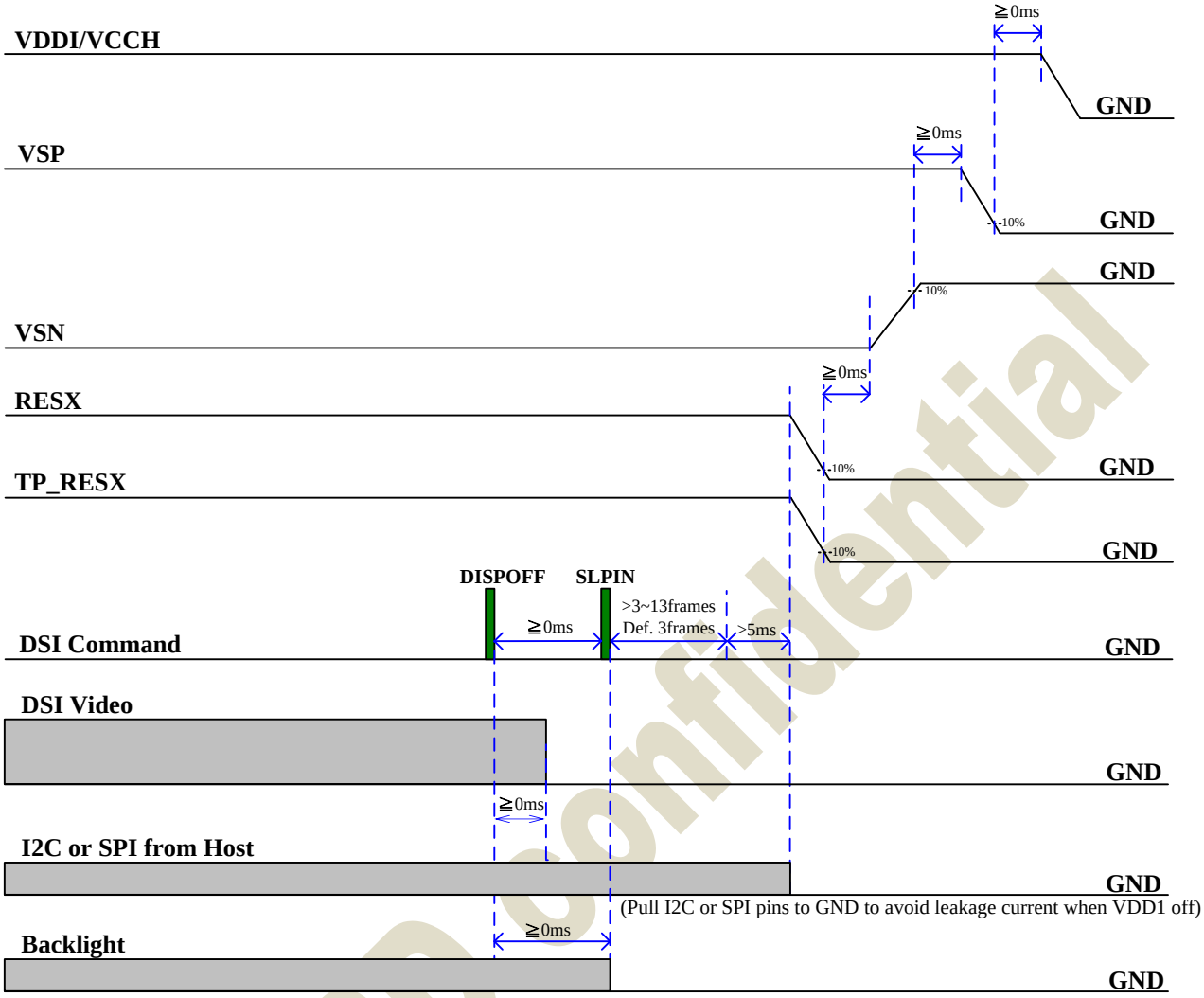


Figure 8.3: Power off sequence for external power

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8.4. Power on/off sequence for internal power

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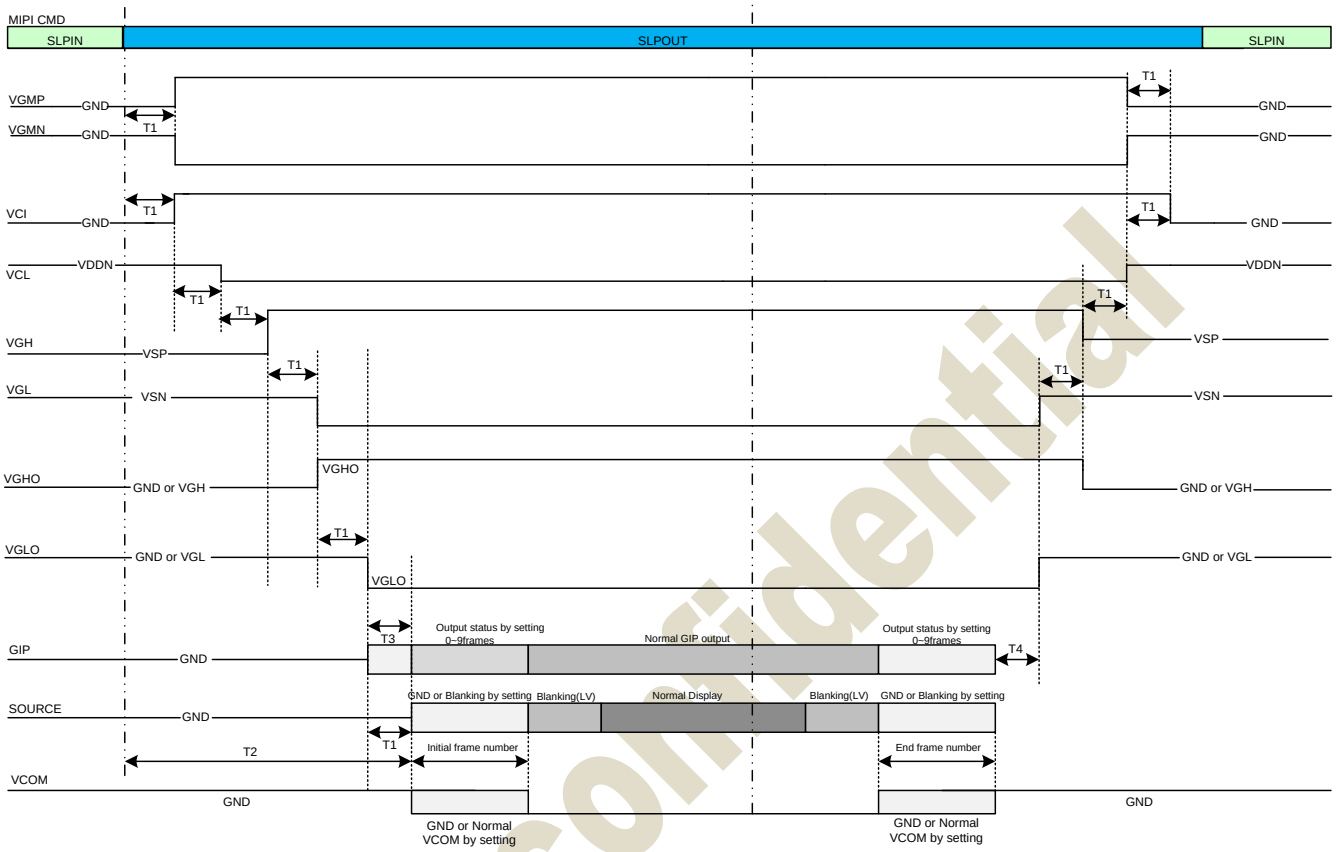


Figure 8.4: Power on/off sequence for internal power

Symbol	Description	Min	Max	Unit	Note
T1	SLPIN to VGMP/VGMN	0.5	-	frame	
T2	SLPIN to VCI	3	-	frame	
T3	Each power on step	1.5	-	frame	
T4	SLPIN to VCOM	1	-	frame	

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8.5. TP LPWUG sequence

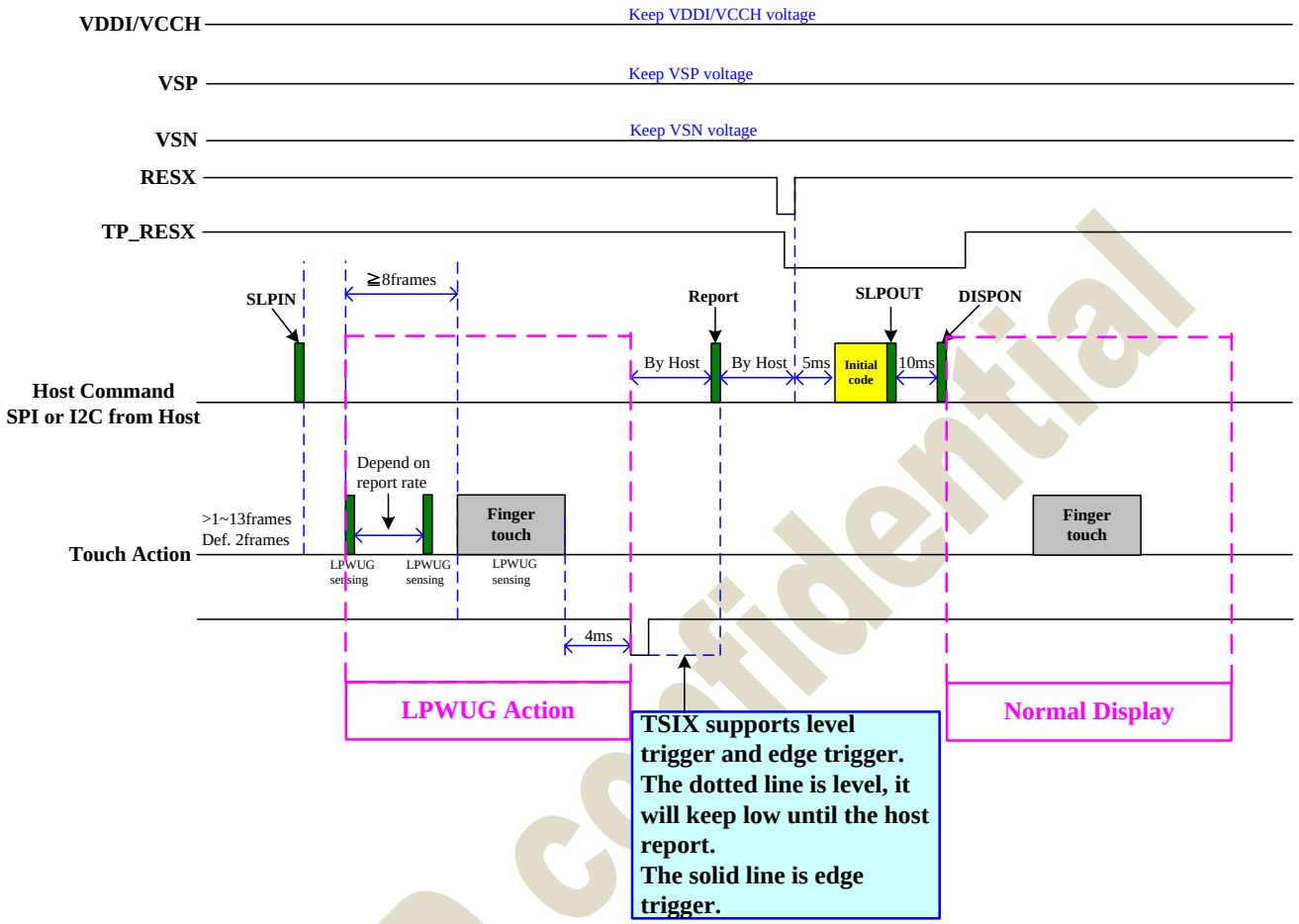


Figure 8.5: TP LPWUG sequence

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9. Panel Application

JD9366TC can support display resolution up to 1600RGB for horizontal active line, and 2560 vertical active line. It also can support 2 types of driving method for stripe and zigzag panel. When horizontal display resolution is over 800RGB, the chip cascade mode must be used. A cascade connection can synchronize signals between 2 chips. We are called master and slave.

JD9366TC can generate gate controller timing. These signals can support for GOA panel(Gate driver on Array).

9.1. Source output channel valid range

The channel of available output depends on the horizontal resolution, and non-available channel always locate at center channel numbers. The source output pin must be floating if don't used.

Horizontal resolution	Master IC			Slave IC		
	Enable channel	Disable channel	Enable channel	Enable channel	Disable channel	Enable channel
1600 RGB(1)	1 – 1200	X	1201 – 2400	1 – 1200	X	1201 – 2400
1536 RGB(2)	1 – 1152	1153 – 1248	1249 – 2400	1 – 1152	1153 – 1248	1249 – 2400
1440 RGB(3)	1 – 1080	1081 – 1320	1321 – 2400	1 – 1080	1081 – 1320	1321 – 2400
1200 RGB(4)	1 – 900	901 – 1500	1501 – 2400	1 – 900	901 – 1500	1501 – 2400
1080 RGB(5)	1 - 810	811 – 1590	1591 – 2400	1 - 810	811 – 1590	1591 – 2400
800 RGB(6)	1 – 1200	X	1201 – 2400	X		
768 RGB(7)	1 – 1152	1153 – 1248	1249 – 2400	X		
720 RGB(8)	1 – 1080	1081 – 1320	1321 – 2400	X		
600 RGB(9)	1 – 900	901 – 1500	1501 – 2400	X		

Note:(1)/(2)/(3)/(4)/(5) are used for cascade chips.

(6)/(7)/(8)/(9) are used for single chip.

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9.2. Cascade mode of synchronized signals

Synchronized signal is for synchronization with master and slave IC. Others function is touch control and gamma voltage
control signal.

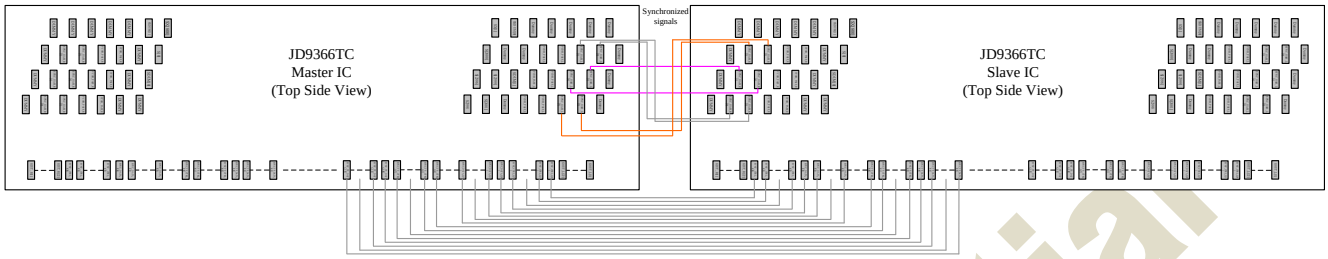


Figure 9.1: Cascade mode of synchronized signals

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9.3. Panel Structure

JD9366TC can support 2 types of driving method – stripe and zigzag . For zigzag panel type, the number 0 and 2401 of source output channel is used for zigzag panel type.

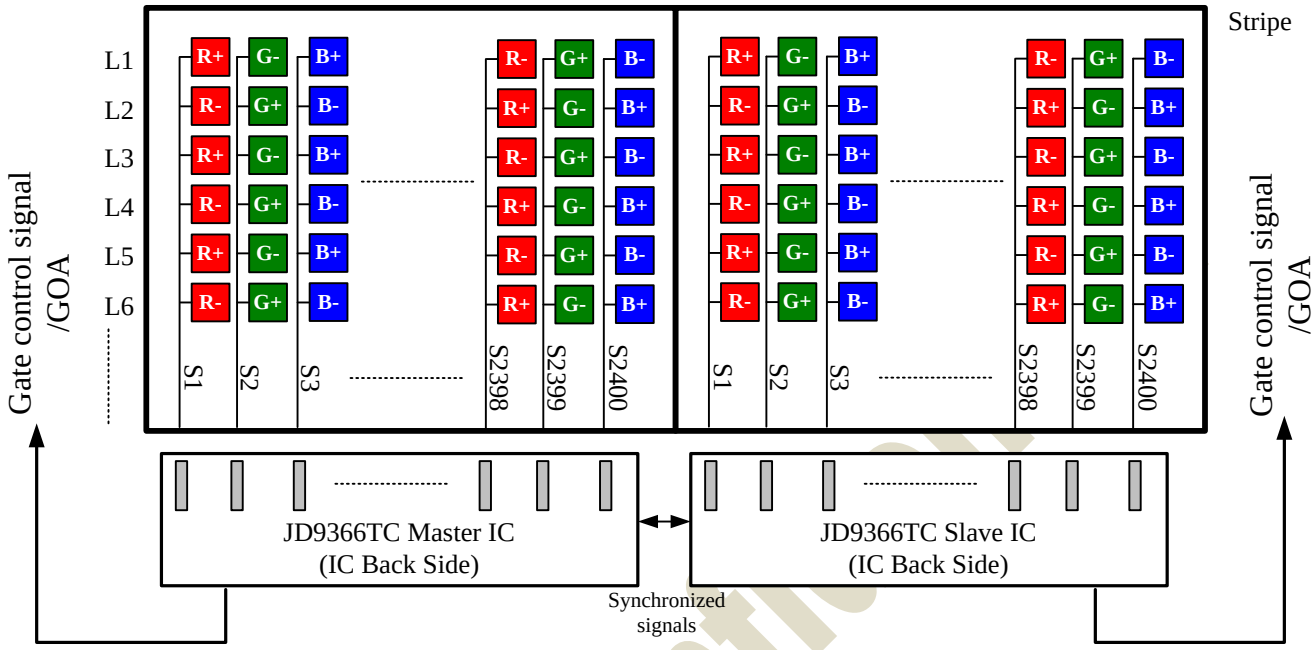


Figure 9.2: Stripe panel type

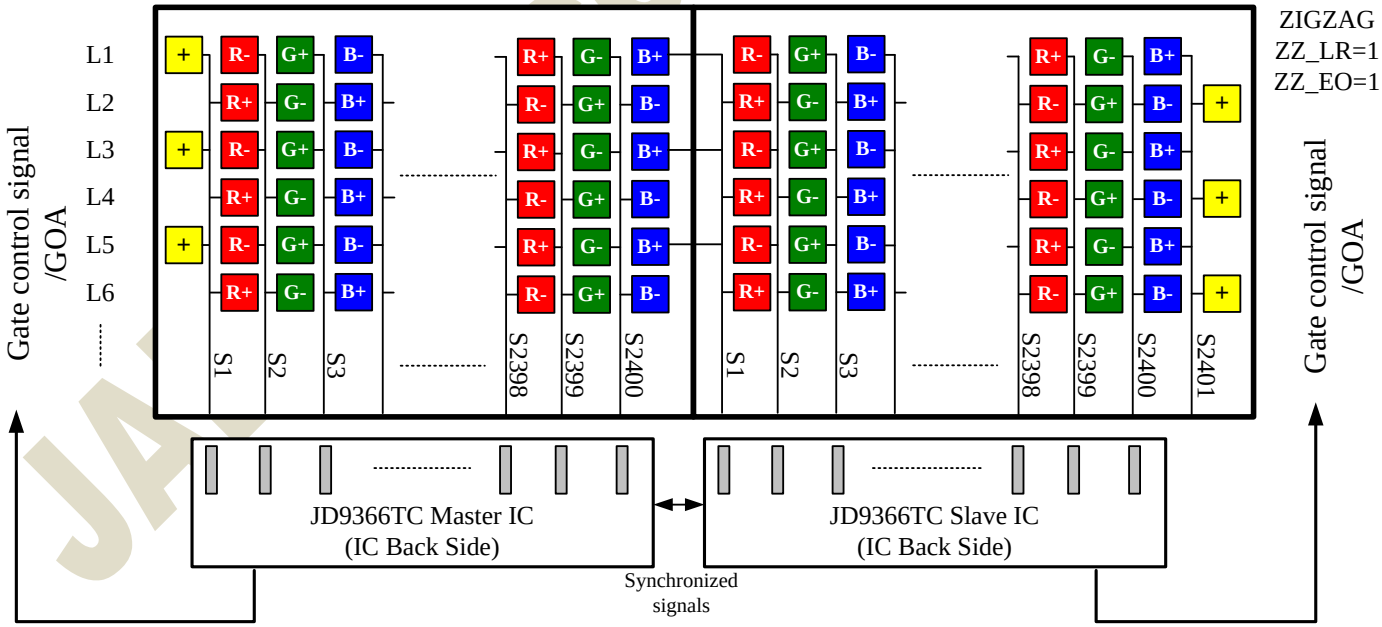


Figure 9.3: Zigzag type0 panel

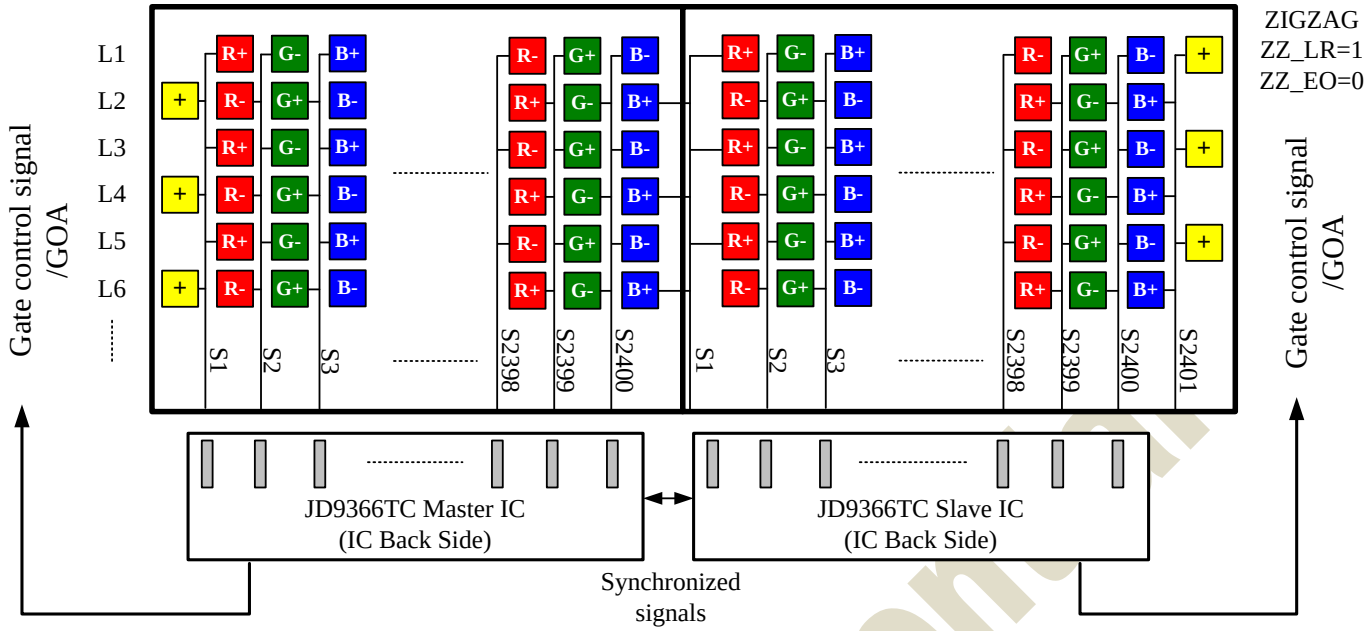


Figure 9.4: Zigzag type1 panel

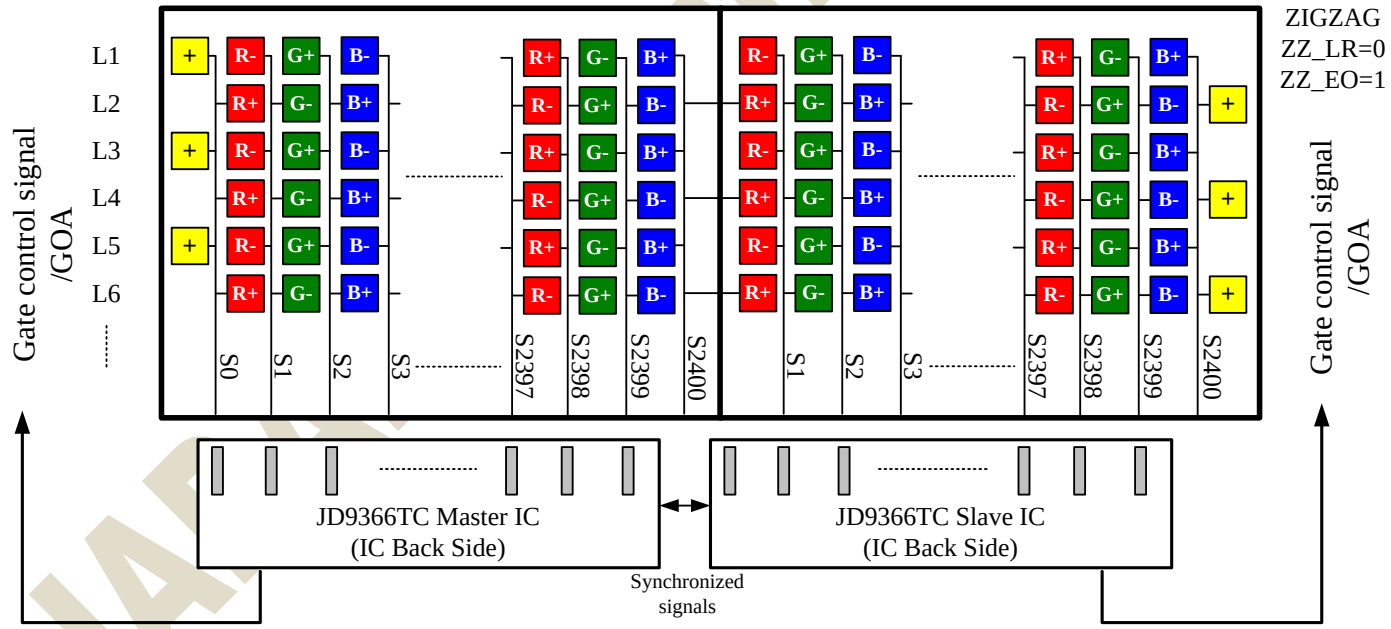


Figure 9.5: Zigzag type2 panel

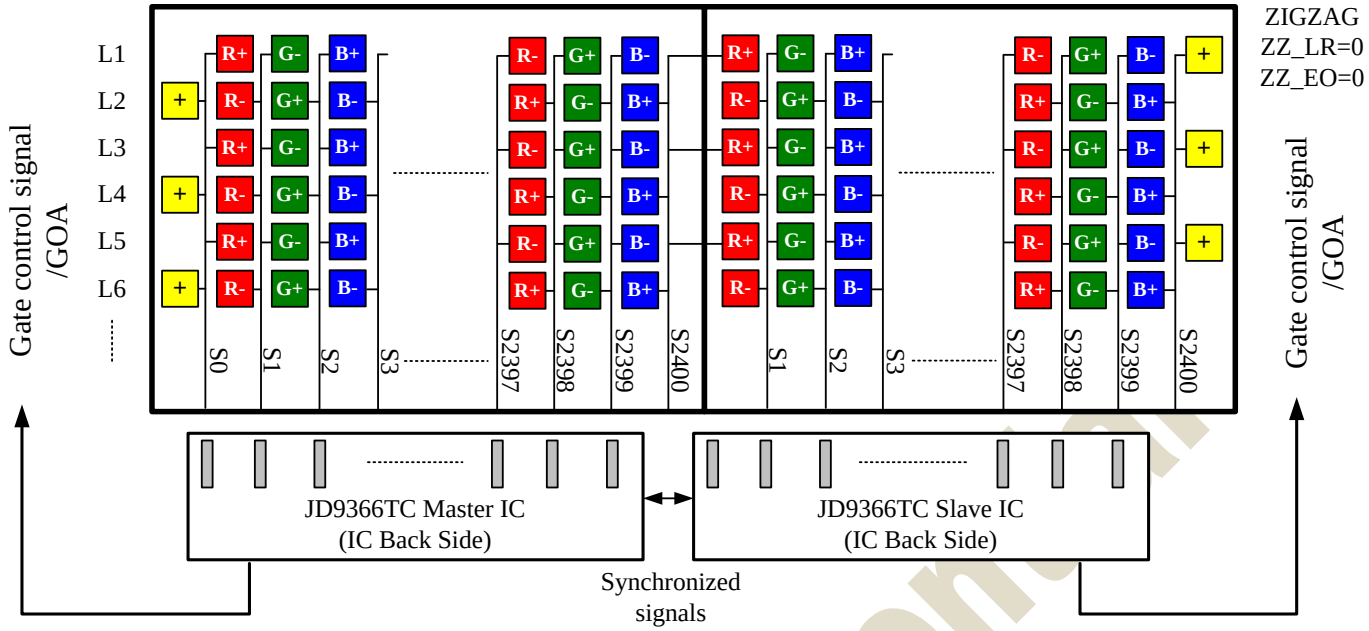


Figure 9.6: Zigzag type3 panel

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10. FUNCTION DESCRIPTION

10.1. Touch sensing cycle

The touch controller function supports up to 10 fingers. The firmware can provide the touch output which is consisted
of multiple sensing cycles and depends on the ADC scan setting in firmware.

The following timing block is showed the timing of display driving and touch ADC sensing. After display scanning, the touch controller is operated and ADC sensing data is received at the Vsync blanking period time.

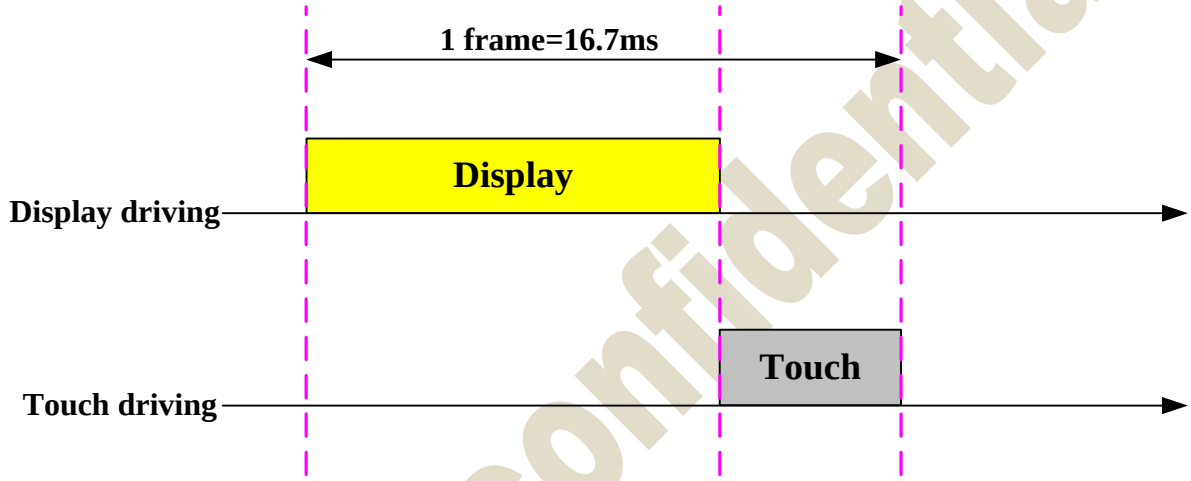


Figure 10.1: Display area and touch sensing area

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10.2. Touch part SPI Interface

JD9366TC would support 4-wire 4 modes (refer to the below picture). The SPI speed would support up to 16MHz.

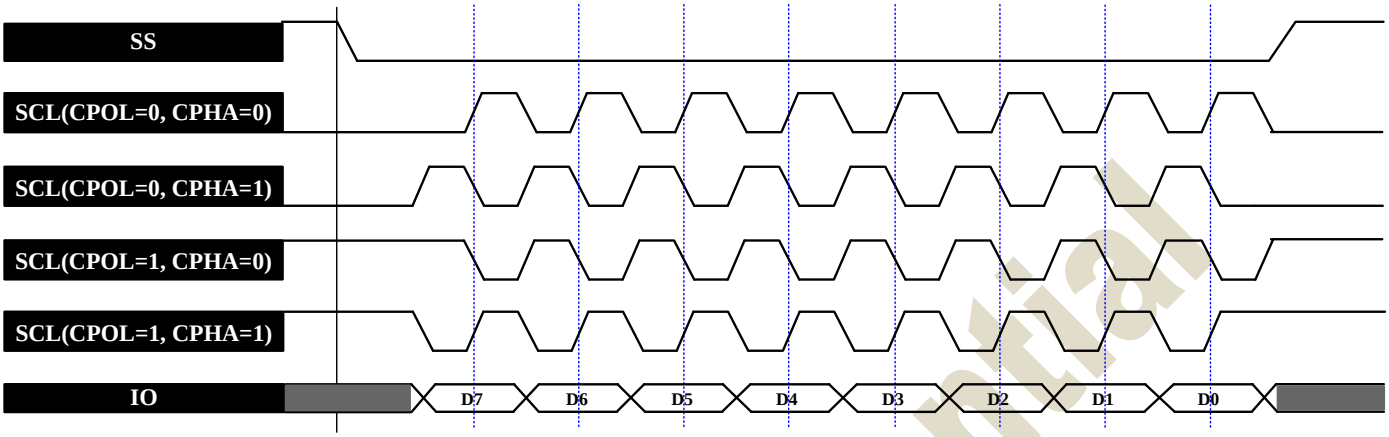


Figure 10.2: SPI with 4 modes

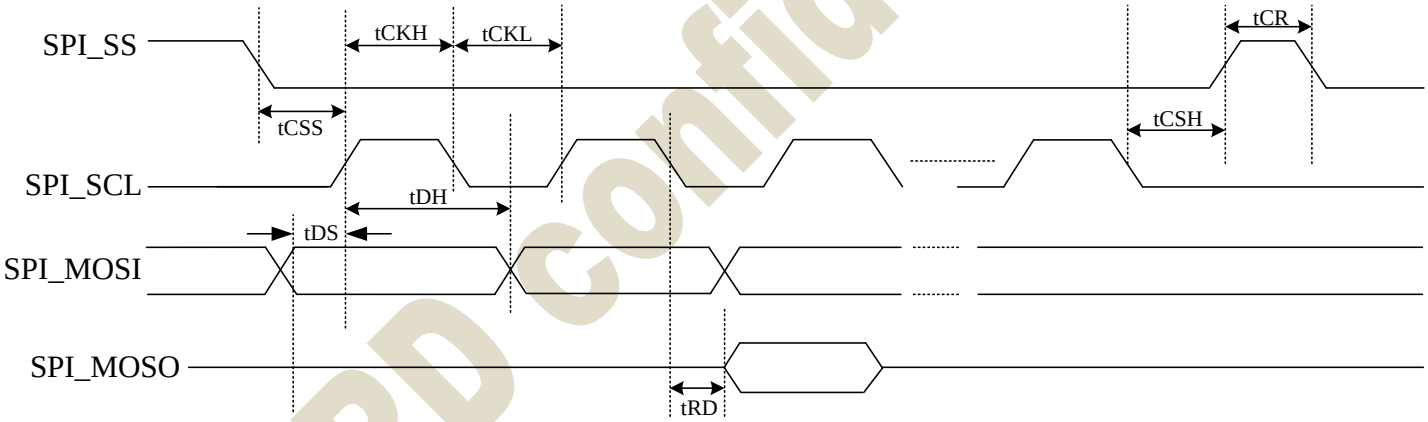


Figure 10.3: SPI Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL Frequence	fSCL	-	-	16	MHz
CS Set-up Time	tCSS	200	-	-	ns
CS Hold Time	tCSH	200	-	-	ns
CS Recovery Time	tCR	1	-	-	ns
SCL clock High Time	tCKH	31.25	-	-	ns
SCL clock Low Time	tCKL	31.25	-	-	ns
Data Output Delay Time (Test condition: C<50pF)	tRD	-	-	50	ns
Input Data Set-up Time	tDS	25	-	-	ns
Input Data Hold Time	tDH	25	-	-	ns

Table10.4: SPI Timing Table

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10.3. Touch part I2C Interface

JD9366TC supports register write sequence via I^2C-bus transfer. The register writing support single register write mode and multi-register write mode. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in below.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to “0” for WRITE.
(3) The slave issues an ACK to master.
(4) 7 bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) JD9366TC DA[6:0]=101_1010

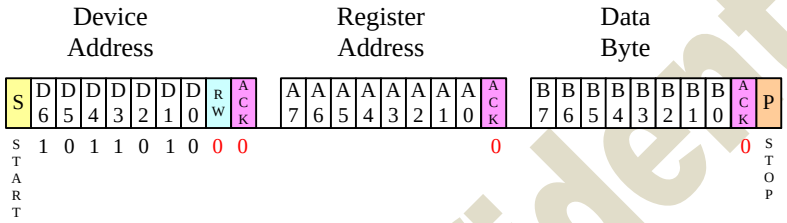


Figure 10.5: Single Writing operation

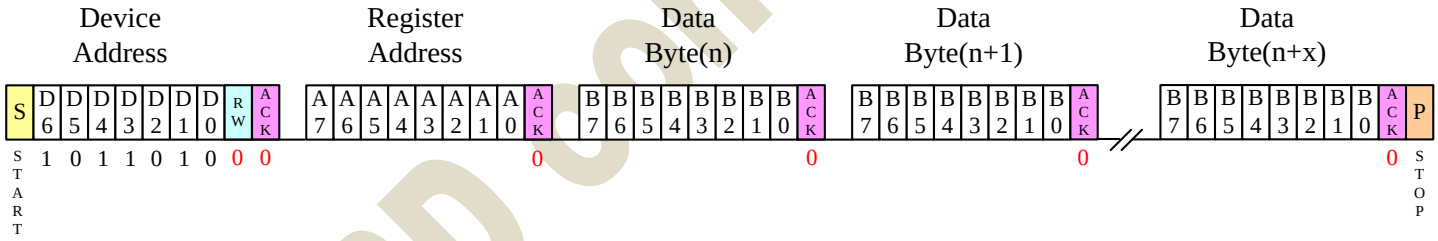


Figure 10.6: Multi Writing operation

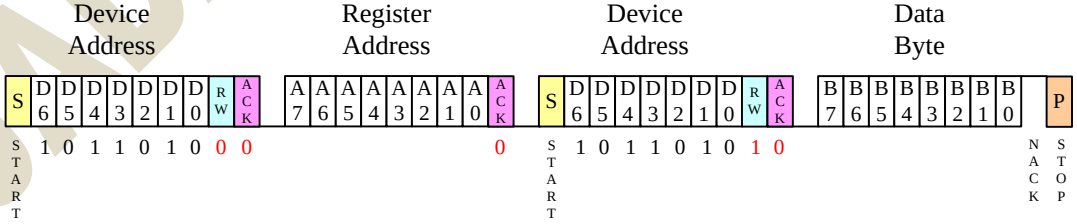


Figure 10.7: Single Reading operation

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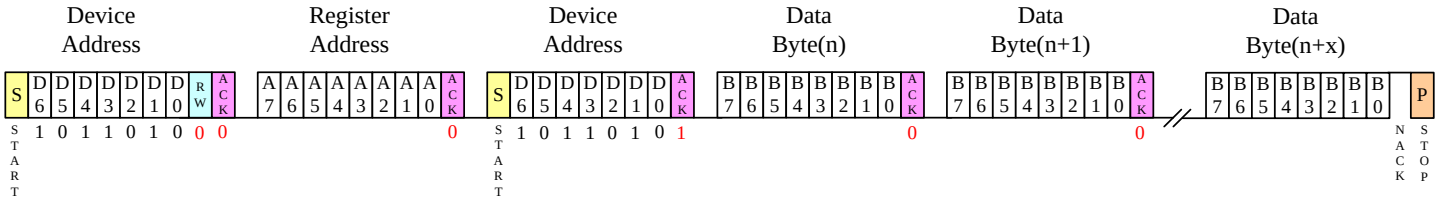


Figure 10.8: Multi Reading operation

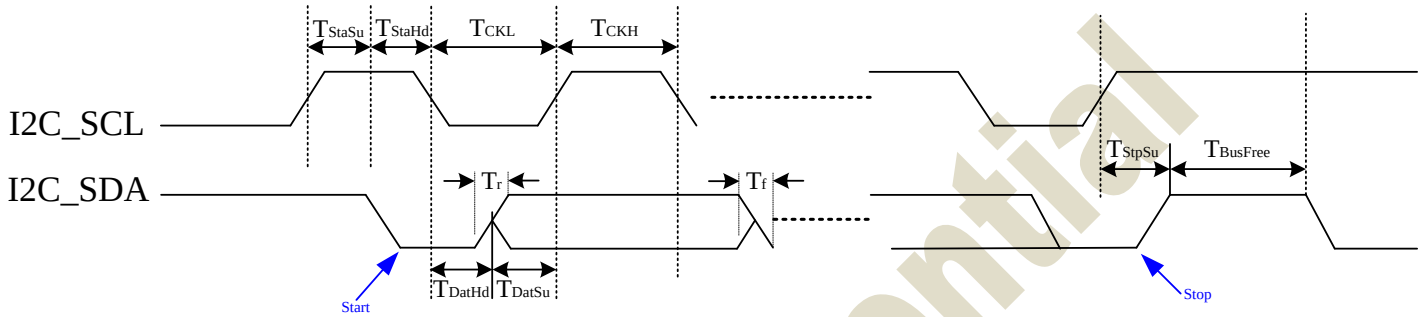


Figure 10.9: I2C Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Working Frequence	Fclk	0	-	400	KHz
I2C Clock Low	T_{CKL}	1300	-	-	ns
I2C Clock High	T_{CKH}	600	-	-	ns
I2C Clock and Data rising time	T_r	-	-	300	ns
I2C Clock and Data falling time	T_f	-	-	300	ns
I2C Data hold time	T_{DatHd}	0	-	-	ns
I2C Data setup time	T_{DatSu}	100	-	-	ns
I2C Start Condition hold time	T_{StaHd}	600	-	-	ns
I2C Start Condition setup time	T_{StaSu}	600	-	-	ns
I2C Stop Condition setup time	T_{StpSu}	600	-	-	ns
I2C Bus free time	$T_{BusFree}$	1300	-	-	ns

Table10.10: I2C Timing Table

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10.4. Driver part SPI Interface

The JD9366TC supports the 4-wire serial peripheral interface (SPI) to set internal register. The basic operation of SPI interface is shown below. The Host asserts the SPI_SS when it wants to initiate a read or write transaction. This is followed by the Host sending 16 pulses on the SPI clock (SPI_SCL). The 8th bit of SPI_SCL pulses is the read/write command. (0=Write, 1=Read). The Host de-asserts the SPI_SS to indicate end of transfer.

The typical SPI writes operation is shows following figure.

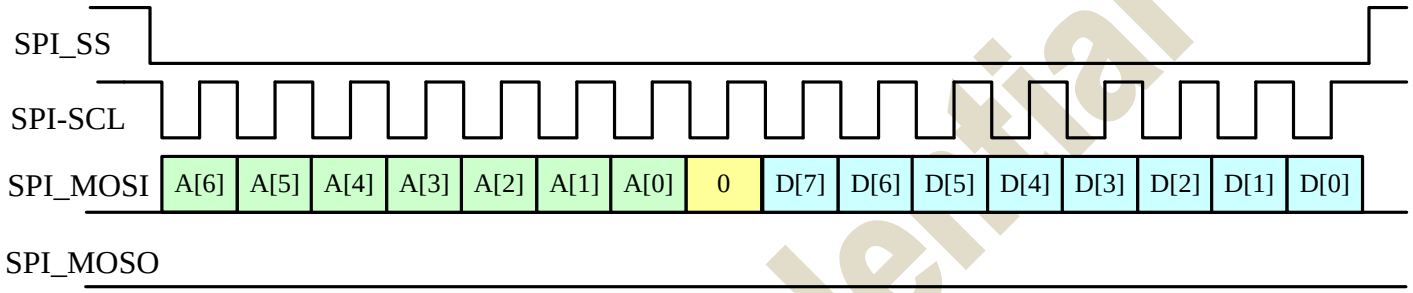


Figure 10.11: SPI single writing operation

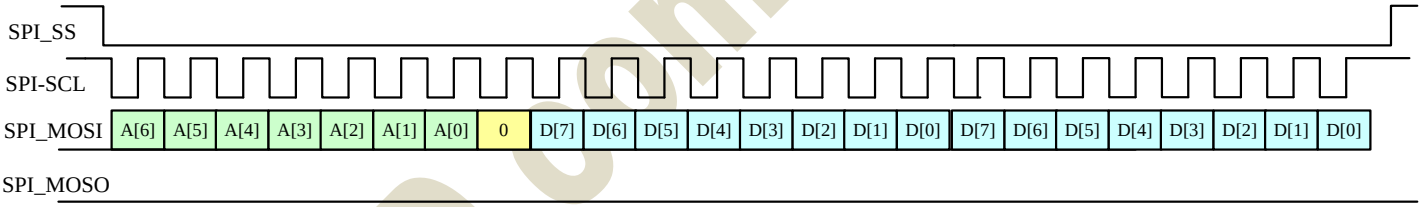


Figure 10.12: SPI Multi writing operation

The typical SPI reads operation is shows following figure.

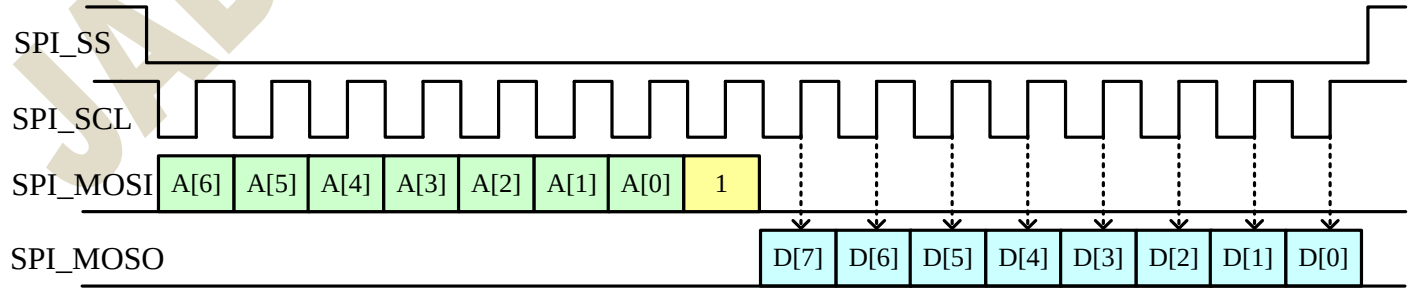


Figure 10.13: SPI Single read operation

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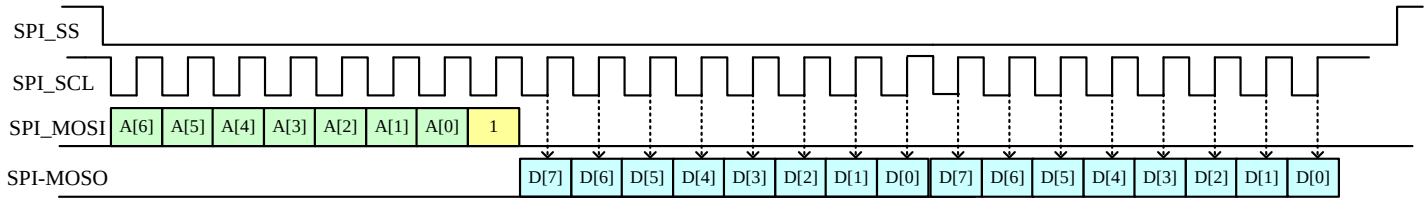


Figure 10.14: SPI Multi read operation

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10.5. GAS Function

When battery is removed from an electronic device, the image still keeps on the LCD panel for a long time. GAS function can speed the process that image disappears.

The GAS function is a voltage detector. By GAS circuit, JD9366TC can detect low voltage of VDDI/VSP/VSN and sent ideal GAS signal to discharge residual potential in LCD panel and removes image. The detect voltage could be selected by register setting.

When VDD recovers, power on procedure must be done to return normal mode.

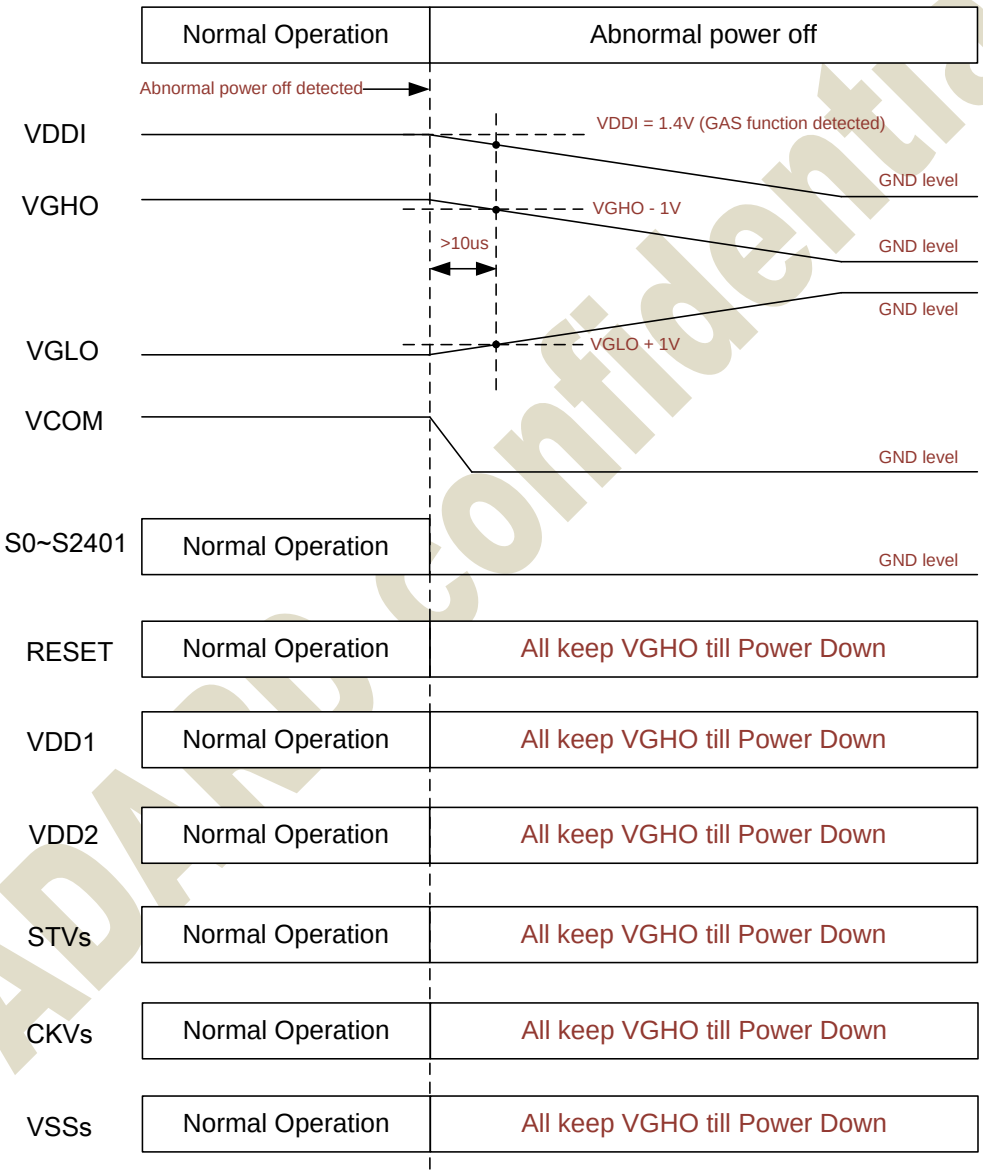


Figure 10.15: GAS discharge timing

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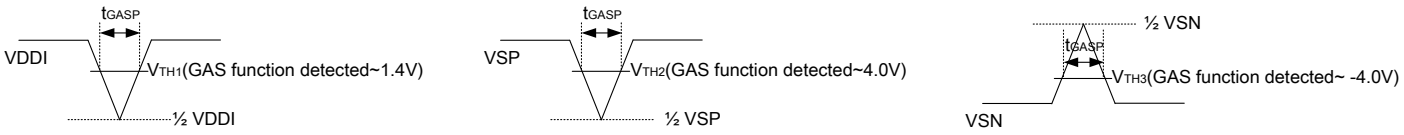


Figure 10.16: GAS v.s. VDDI/VSP/VSN

Parameter	Symbol	Step	Spec			Unit
			Min	Typ	Max	
VDDI/VSP/VSN power drop noise filter period.	T_{GASP}	-	100	-	-	ns
GAS function detection threshold voltage. VDDI lower than V_{TH1}, IC will execute GAS function	V_{TH1}	0.1	1.3	1.4	2.1	V
GAS function detection threshold voltage. VSP lower than V_{TH2}, IC will execute GAS function	V_{TH2}	0.4	2.8	4.0	4.0	V
GAS function detection threshold voltage. VSN lower than V_{TH3}, IC will execute GAS function	V_{TH3}	0.4	-4.0	-4.0	-2.8	V

Table10.17: GAS detect voltage

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10.6. Tearing effect Line

10.6.1. Tearing effect Line mode

The TE Effect line supplies to the MPU a Panel synchronization signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command.

Tearing Effect Line Modes
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

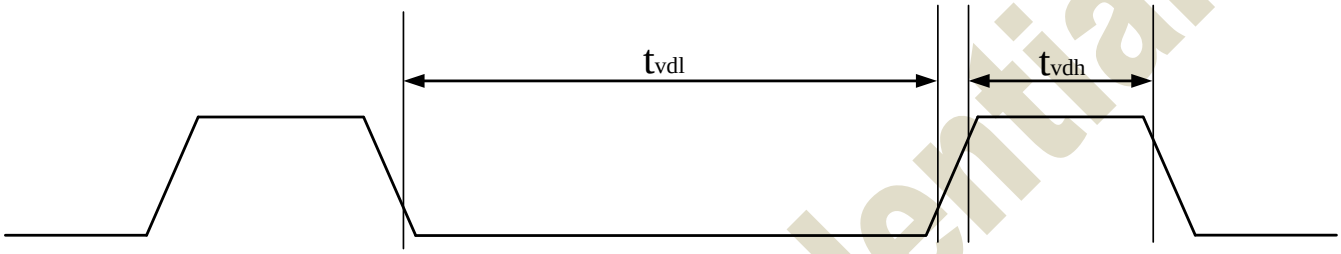


Figure 10.18:Tearing Effect Line mode 1

tvdh= The LCD display is not updated form the Frame Memory.
tvdl= The LCD display is updated form the Frame Memory.

Mode 2, the Tearing Effect Output signal consists of V-sync and H-sync Information, there is one V-sync and N H-sync pulses per field.
N: If the resolution is 1200RGB X 2000, the N=2000.

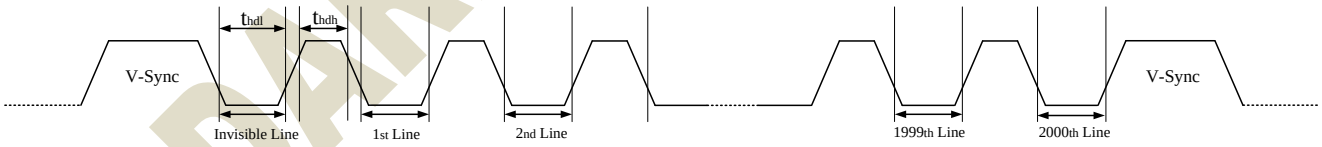


Figure 10.19: Tearing Effect Line mode 2

thdh= The LCD display is not updated form the Frame Memory
thdl= The LCD display is updated form the Frame Memory (except Invisible Line – see above)

The H-sync pulses output amount will be defined by TESL[15:0] setting under Mode 2.
Ex: 1. TESL[15:0]=0, then TE signal will the same as TE mode 1.
TESL[15:0]=1, then TE signal will output 2000 H-sync..

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TESL[15:0]=3, then TE signal will output 1998 H-sync.

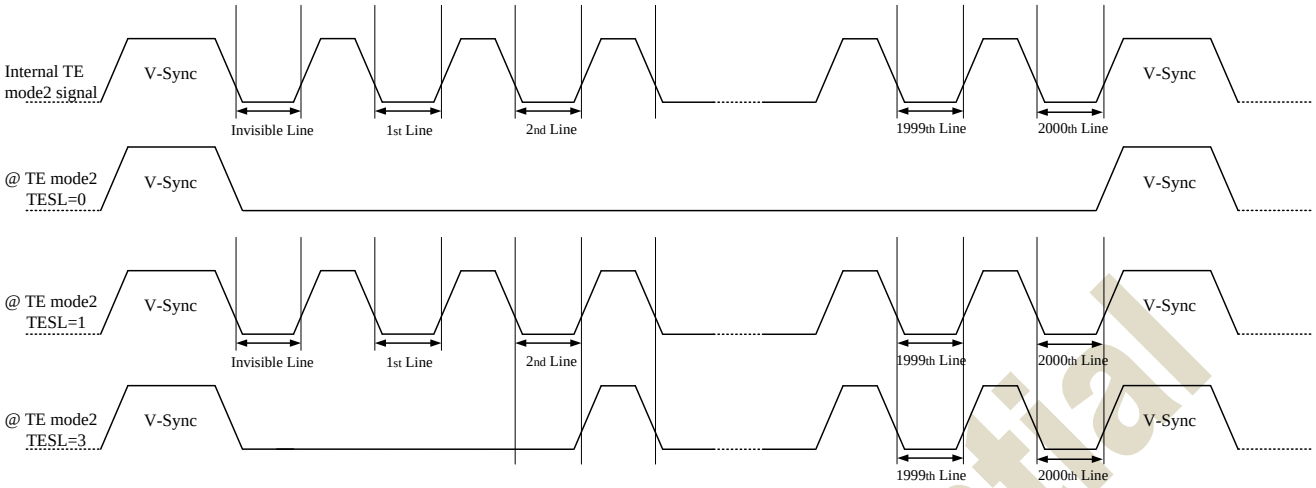


Figure 10.20: TE Line Output for TELINE setting

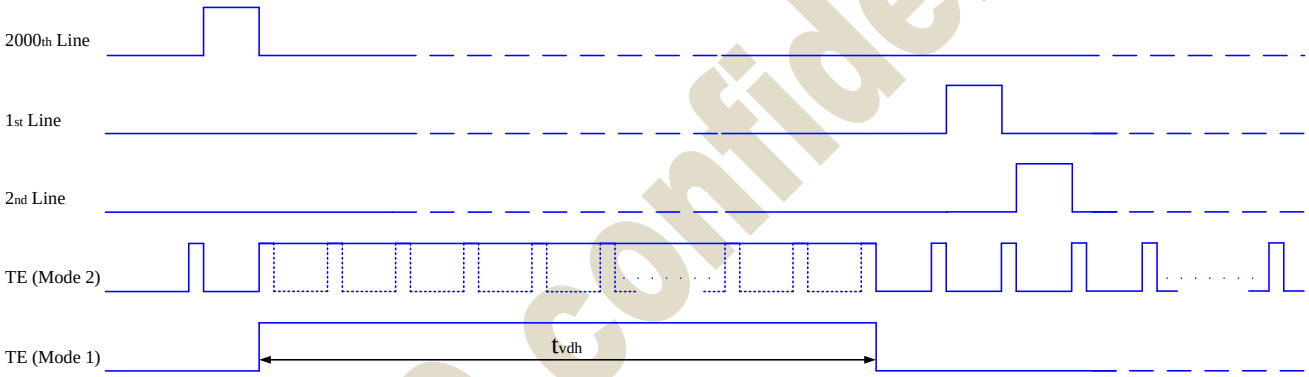


Figure 10.21: Tearing Effect Line Output signal

Note: During Sleep In Mode, the Tearing Output Pin is active Low.

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10.6.2.Tearing effect line timing

The Tearing Effect signal is described below:

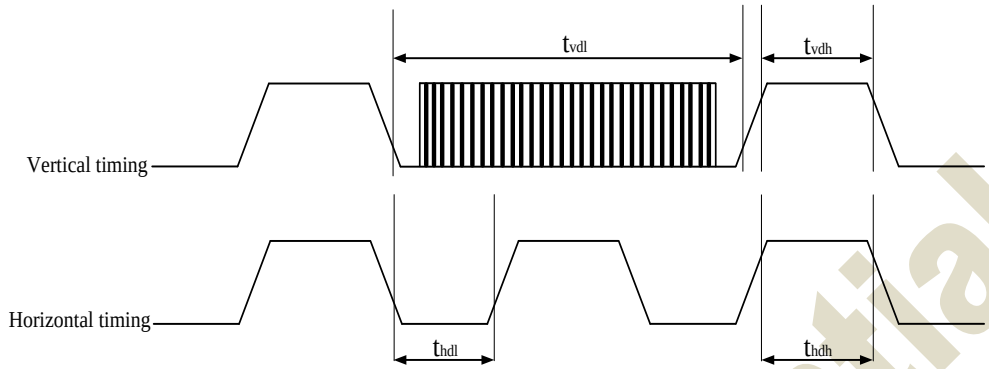


Figure 10.22: Tearing Effect Line timing

Idle Mode Off/On (Resolution 1200x2000RGB, Frame Rate=60 Hz)

Symbol	Parameter	Min.	Max.	Unit
tvdl	Vertical Timing Low Duration	Note1	-	ms
tvdh	Vertical Timing High Duration	Note2	-	us
thdl	Horizontal Timing Low Duration	Note3	-	us
thdh	Horizontal Timing High Duration	Note4	-	us
tr	Rise time	-	15 (Note5)	ns
tf	Fall time	-	15 (Note5)	ns

Table10.23: AC characteristics of Tearing Effect Line

Note: 1. tvdl = Vtotal- (VFP+VS+VBP)
2. tvdh = VFP+VS+VBP
3. thdl = Htotal- (HFP+HS+HBP)
4. thdh = HFP+HS+HBP
5. Base on panel loading C<30pF.

The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns.

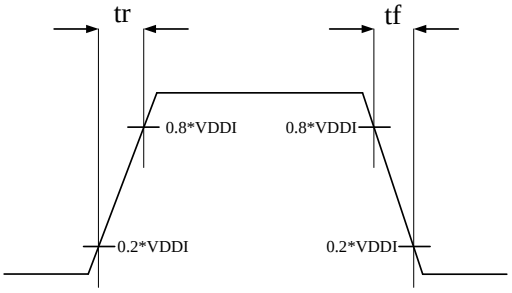


Figure 10.24: Tearing Effect Line definition of tr, tf

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10.7. Data Processing Circuit

The input data from external display interface will be fed to the data processing circuit, which contains the functions of contrast **(Gain)** control; brightness **(Offset)** control, and gamma control. See register descriptions for detail.

The contrast adjustment is done on RGB data with 3 sets of 8-bit registers. The 8-bit register represents gain value in the range of **0.5 ~ 1.496**. When output data of the gain multiplication exceeds 255, it will be clamped at 255. Default gain value is 1.0.

The brightness adjustment is done on RGB data with 3 sets of 8-bit registers. The 8-bit register represents offset value in the range of **-64 ~ +191**. When output data of the offset shifting exceeds the range of 0 to 255, it will be clamped to 0 and 255. Default offset is 0.

The digital gamma correction is done by 23-segment piecewise linear interpolation. The 23 segments are defined with 24 register values for level 0, 1, 3, 7, 11, 15, 23, 31, 47, 63, 95, 127, 128, 160, 192, 208, 224, 232, 240, 244, 248, 252, 254 and 255 for positive and negative polarity. The gamma correction output is then fed to 8-bit DAC and OP to drive the source lines on the panel.

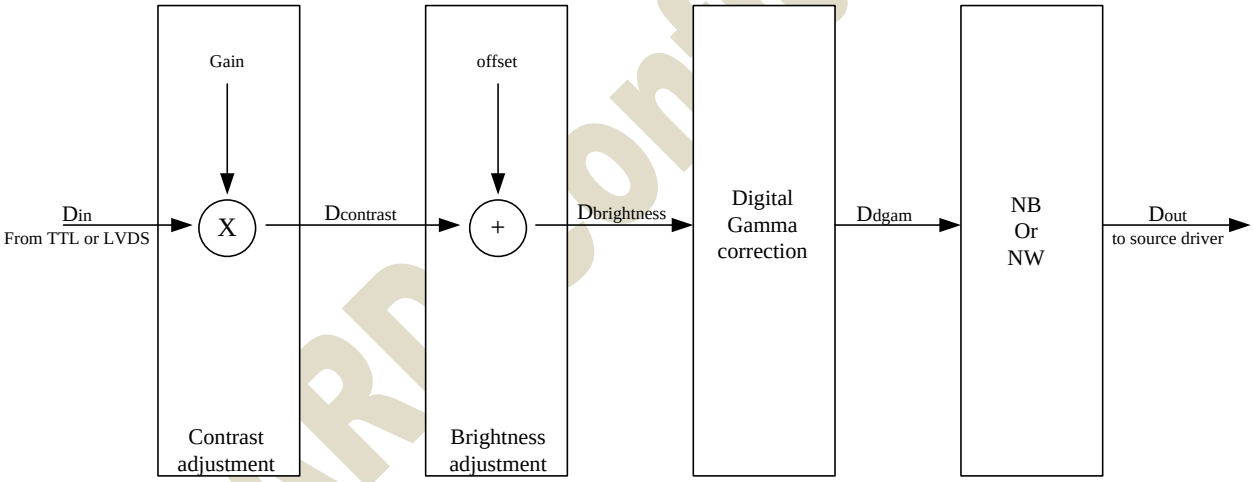


Figure 7.21: Data processing

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10.8. Contrast Adjustment

Contrast adjustment is done on RGB data separately by multiplying a gain ranging from 0.5 to 1.496. The gain for each color is set with 3 sets of 8-bit registers **(RGC [7:0], GGC[7:0], BGC[7:0])**. If the resulting output data exceeds 255, it will be clamped to 255. Default gain value is 1.0.

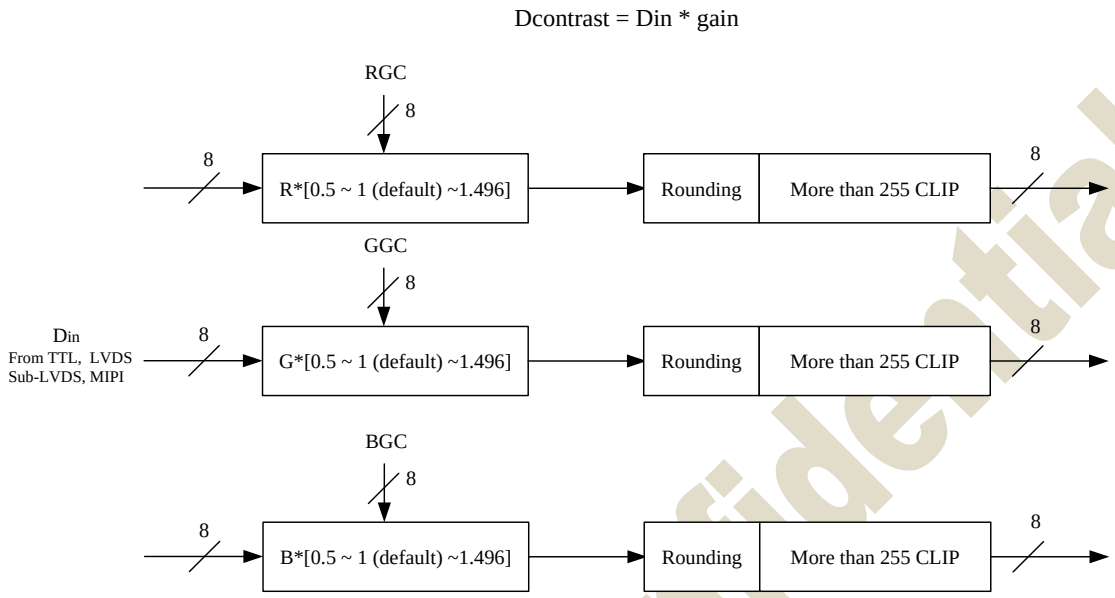


Figure 7.22: Contrast adjustment

10.9. Brightness Adjustment

Brightness adjustment is done on RGB data separately by adding an offset ranging from -64 to +191. The offset of each color is set with 3 sets of 8-bit registers **(ROB[7:0], GOB[7:0], BOB[7:0])**. If the resulting output data exceeds the range of 0 to 255, it will be clamped to 0 and 255. Default offset is 0.

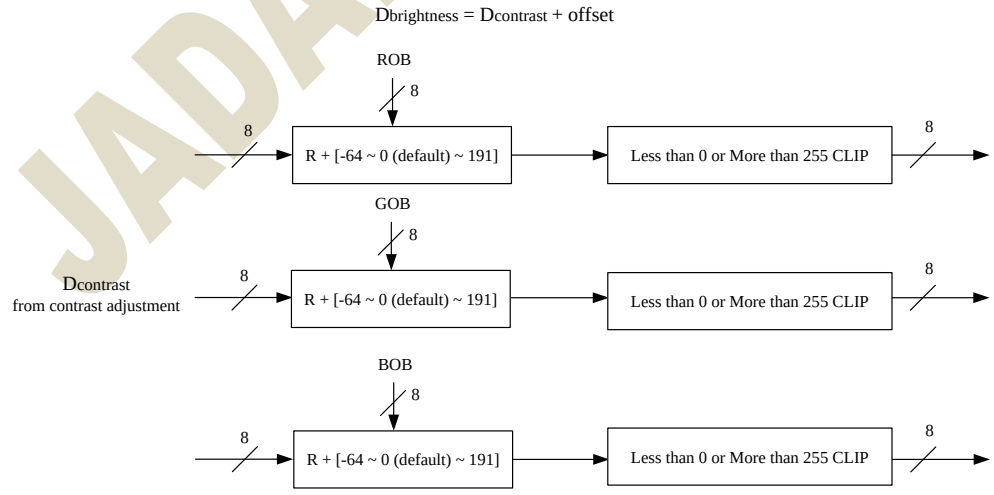


Figure 7.23: Brightness adjustment

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10.10. Digital Gamma Correction

The digital gamma correction is done on RGB data separately with 23-segment piecewise linear interpolation. The 23 segments are defined with 24 register values Y1~Y24 for level X1~X24 = 0, 1, 3, 7, 11, 15, 23, 31, 47, 63, 95, 127, 128, 160, 192, 208, 224, 232, 240, 244, 248, 252, 254 and 255. Y on X between Xn and Xn+1 is interpolated with the following equations.

$$Y = Yn + (Yn+1 - Yn) * (X-Xn) / (Xn+1-Xn)$$

The gamma correction output 10-bit data Ddgam is then fed to 8-bit DAC and OP to drive the source lines on the panel with dithering.

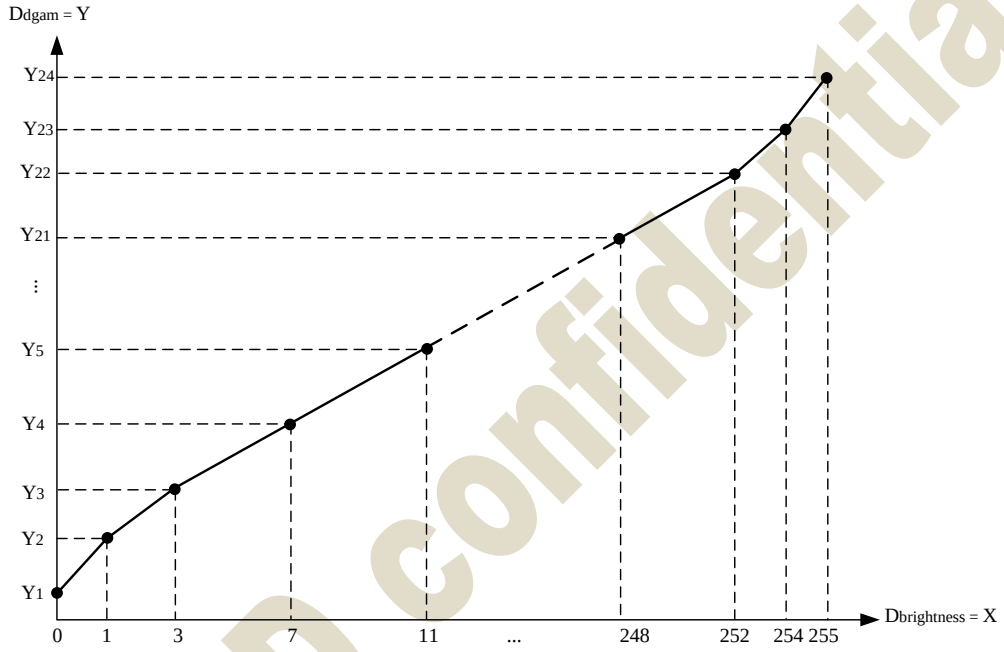


Figure 7.24: Digital gamma correction

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10.11. Analog Gamma Adjustmen

The JD9366TC has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The positive and negative polarity can be specified independently.

Register groups	Positive polarity	Negative polarity	Parameter
Up edge adjustment	VHP0 [6:0]	VHN0 [6:0]	128-to-1 selector (voltage level of grayscale 255)
	VHP1 [6:0]	VHN1 [6:0]	128-to-1 selector (voltage level of grayscale 254)
	VHP2 [6:0]	VHN2 [6:0]	128-to-1 selector (voltage level of grayscale 252)
	VHP3 [6:0]	VHN3 [6:0]	128-to-1 selector (voltage level of grayscale 250)
	VHP4 [6:0]	VHN4 [6:0]	128-to-1 selector (voltage level of grayscale 247)
Center adjustment	VMP0 [7:0]	VMN0 [7:0]	256-to-1 selector (voltage level of grayscale 243)
	VMP1 [7:0]	VMN1 [7:0]	256-to-1 selector (voltage level of grayscale 235)
	VMP2 [7:0]	VMN2 [7:0]	256-to-1 selector (voltage level of grayscale 227)
	VMP3 [7:0]	VMN3 [7:0]	256-to-1 selector (voltage level of grayscale 215)
	VMP4 [7:0]	VMN4 [7:0]	256-to-1 selector (voltage level of grayscale 203)
	VMP5 [7:0]	VMN5 [7:0]	256-to-1 selector (voltage level of grayscale 179)
	VMP6 [7:0]	VMN6 [7:0]	256-to-1 selector (voltage level of grayscale 155)
	VMP7 [7:0]	VMN7 [7:0]	256-to-1 selector (voltage level of grayscale 127)
	VMP8 [7:0]	VMN8 [7:0]	256-to-1 selector (voltage level of grayscale 99)
	VMP9 [7:0]	VMN9 [7:0]	256-to-1 selector (voltage level of grayscale 75)
	VMP10 [7:0]	VMN10 [7:0]	256-to-1 selector (voltage level of grayscale 51)

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	VMP11 [7:0]	VMN11 [7:0]	256-to-1 selector (voltage level of grayscale 39)
	VMP12 [7:0]	VMN12 [7:0]	256-to-1 selector (voltage level of grayscale 27)
	VMP13 [7:0]	VMN13 [7:0]	256-to-1 selector (voltage level of grayscale 19)
Down edge adjustment	VLP0 [6:0]	VLN0 [6:0]	128-to-1 selector (voltage level of grayscale 12)
	VLP1 [6:0]	VLN1 [6:0]	128-to-1 selector (voltage level of grayscale 8)
	VLP2 [6:0]	VLN2 [6:0]	128-to-1 selector (voltage level of grayscale 4)
	VLP3 [6:0]	VLN3 [6:0]	128-to-1 selector (voltage level of grayscale 0)

Table10.25: Gamma adjustment registers

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Gamma register stream and selector

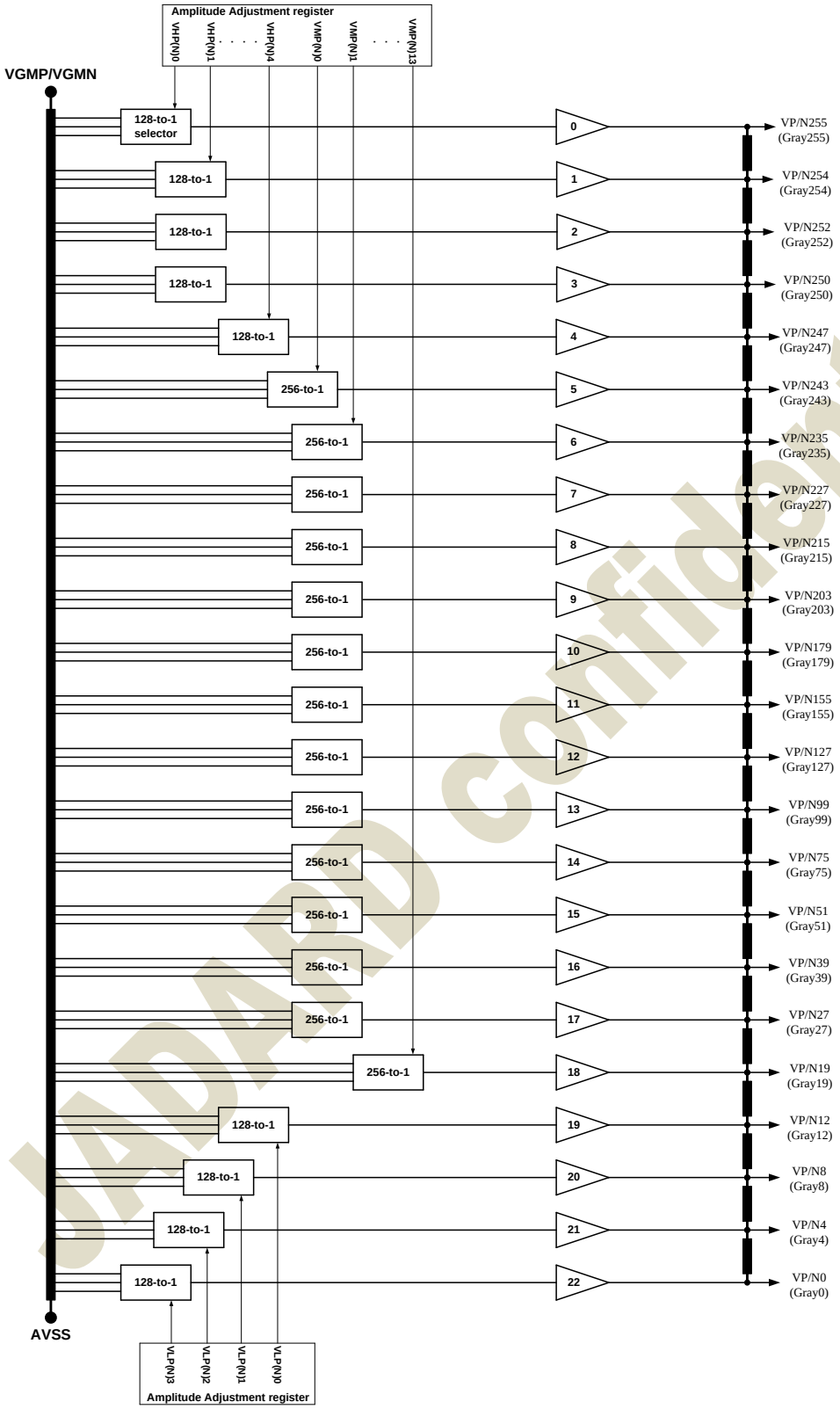


Figure 10.26: Gamma register stream and gamma reference voltage

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Variable register

The resistances of center and edge adjustment are decided by setting values in the below registers. The grayscale levels are determined by the following formulas:

Resistance mode	Reference voltage	Macro adjustment value	Formula
Up edge adjustment	VP[255]	VHP0 [6:0]	(300-VHP0[6:0])/300*VSPR
	VP[254]	VHP1 [6:0]	(298-VHP1[6:0])/300*VSPR
	VP[252]	VHP2 [6:0]	(296-VHP2[6:0])/300*VSPR
	VP[250]	VHP3 [6:0]	(294-VHP3[6:0])/300*VSPR
	VP[247]	VHP4 [6:0]	(290-VHP4[6:0])/300*VSPR
Center adjustment	VP[243]	VMP0 [7:0]	(548-VMP0[7:0])/600*VSPR
	VP[235]	VMP1 [7:0]	(548-VMP1[7:0])/600*VSPR
	VP[227]	VMP2 [7:0]	(548-VMP2[7:0])/600*VSPR
	VP[215]	VMP3 [7:0]	(536-VMP3[7:0])/600*VSPR
	VP[203]	VMP4 [7:0]	(516-VMP4[7:0])/600*VSPR
	VP[179]	VMP5 [7:0]	(492-VMP5[7:0])/600*VSPR
	VP[155]	VMP6 [7:0]	(464-VMP6[7:0])/600*VSPR
	VP[127]	VMP7 [7:0]	(452-VMP7[7:0])/600*VSPR
	VP[99]	VMP8 [7:0]	(428-VMP8[7:0])/600*VSPR
	VP[75]	VMP9 [7:0]	(404-VMP9[7:0])/600*VSPR
	VP[51]	VMP10 [7:0]	(391-VMP10[7:0])/600*VSPR
	VP[39]	VMP11 [7:0]	(363-VMP11[7:0])/600*VSPR
	VP[27]	VMP12 [7:0]	(339-VMP12[7:0])/600*VSPR
	VP[19]	VMP13 [7:0]	(295-VMP13[7:0])/600*VSPR
Down edge adjustment	VP[12]	VLP0 [6:0]	(133-VLP0[6:0])/300*VSPR
	VP[8]	VLP1 [6:0]	(131-VLP1[6:0])/300*VSPR
	VP[4]	VLP2 [6:0]	(129-VLP2[6:0])/300*VSPR
	VP[0]	VLP3 [6:0]	(127-VLP3[6:0])/300*VSPR

Table10.27: VP[255]-VP[0]

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Resistance mode	Reference voltage	Macro adjustment value	Formula
Up edge adjustment	VN[255]22	VHN0 [6:0]	(300-VHN0[6:0])/300*VSNR
	VN[254]21	VHN1 [6:0]	(298-VHN1[6:0])/300*VSNR
	VN[252]20	VHN2 [6:0]	(296-VHN2[6:0])/300*VSNR
	VN[250]19	VHN3 [6:0]	(294-VHN3[6:0])/300*VSNR
	VN[247]18	VHN4 [6:0]	(290-VHN4[6:0])/300*VSNR
Center adjustment	VN[243]17	VMN0 [7:0]	(548-VMN0[7:0])/600*VSNR
	VN[235]16	VMN1 [7:0]	(548-VMN1[7:0])/600*VSNR
	VN[227]15	VMN2 [7:0]	(548-VMN2[7:0])/600*VSNR
	VN[215]14	VMN3 [7:0]	(536-VMN3[7:0])/600*VSNR
	VN[203]13	VMN4 [7:0]	(516-VMN4[7:0])/600*VSNR
	VN[179]12	VMN5 [7:0]	(492-VMN5[7:0])/600*VSNR
	VN[155]11	VMN6 [7:0]	(464-VMN6[7:0])/600*VSNR
	VN[127]10	VMN7 [7:0]	(452-VMN7[7:0])/600*VSNR
	VN[99]9	VMN8 [7:0]	(428-VMN8[7:0])/600*VSNR
	VN[75]8	VMN9 [7:0]	(404-VMN9[7:0])/600*VSNR
	VN[51]7	VMN10 [7:0]	(391-VMN10[7:0])/600*VSNR
	VN[39]6	VMN11 [7:0]	(363-VMN11[7:0])/600*VSNR
	VN[27]5	VMN12 [7:0]	(339-VMN12[7:0])/600*VSNR
	VN[19]4	VMN13 [7:0]	(295-VMN13[7:0])/600*VSNR
Down edge adjustment	VN[12]3	VLN0 [6:0]	(133-VLN0[6:0])/300*VSNR
	VN[8]2	VLN1 [6:0]	(131-VLN1[6:0])/300*VSNR
	VN[4]1	VLN2 [6:0]	(129-VLN2[6:0])/300*VSNR
	VN[0]0	VLN3 [6:0]	(127-VLN3[6:0])/300*VSNR

Table10.28: VN[255]-VN[0]

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Grayscale voltage	Formula
Gray 0	VP/N[255]
Gray 1	VP/N[255]+1/4*(VP/N[254]-VP/N[255])
2	VP/N[255]+2/4*(VP/N[254]-VP/N[255])
3	VP/N[255]+3/4*(VP/N[254]-VP/N[255])
4	VP/N[254]
5	VP/N[254]+1/4*(VP/N[252]-VP/N[254])
6	VP/N[254]+2/4*(VP/N[252]-VP/N[254])
7	VP/N[254]+3/4*(VP/N[252]-VP/N[254])
8	VP/N[252]
9	VP/N[252]+1/4*(VP/N[250]-VP/N[252])
10	VP/N[252]+2/4*(VP/N[250]-VP/N[252])
11	VP/N[252]+3/4*(VP/N[250]-VP/N[252])
12	VP/N[250]
13	VP/N[250]+1/7*(VP/N[247]-VP/N[250])
14	VP/N[250]+2/7*(VP/N[247]-VP/N[250])
15	VP/N[250]+3/7*(VP/N[247]-VP/N[250])
16	VP/N[250]+4/7*(VP/N[247]-VP/N[250])
17	VP/N[250]+5/7*(VP/N[247]-VP/N[250])
18	VP/N[250]+6/7*(VP/N[247]-VP/N[250])
19	VP/N[247]
20	VP/N[247]+1/8*(VP/N[243]-VP/N[247])
21	VP/N[247]+2/8*(VP/N[243]-VP/N[247])
22	VP/N[247]+3/8*(VP/N[243]-VP/N[247])
23	VP/N[247]+4/8*(VP/N[243]-VP/N[247])
24	VP/N[247]+5/8*(VP/N[243]-VP/N[247])
25	VP/N[247]+6/8*(VP/N[243]-VP/N[247])
26	VP/N[247]+7/8*(VP/N[243]-VP/N[247])
27	VP/N[243]
28	VP/N[243]+1/12*(VP/N[235]-VP/N[243])
29	VP/N[243]+2/12*(VP/N[235]-VP/N[243])
30	VP/N[243]+3/12*(VP/N[235]-VP/N[243])
31	VP/N[243]+4/12*(VP/N[235]-VP/N[243])
32	VP/N[243]+5/12*(VP/N[235]-VP/N[243])
33	VP/N[243]+6/12*(VP/N[235]-VP/N[243])
34	VP/N[243]+7/12*(VP/N[235]-VP/N[243])
35	VP/N[243]+8/12*(VP/N[235]-VP/N[243])
36	VP/N[243]+9/12*(VP/N[235]-VP/N[243])
37	VP/N[243]+10/12*(VP/N[235]-VP/N[243])

Grayscale voltage	Formula
Gray 44	VP/N[235]+5/12*(VP/N[227]-VP/N[235])
Gray 45	VP/N[235]+6/12*(VP/N[227]-VP/N[235])
46	VP/N[235]+7/12*(VP/N[227]-VP/N[235])
47	VP/N[235]+8/12*(VP/N[227]-VP/N[235])
48	VP/N[235]+9/12*(VP/N[227]-VP/N[235])
49	VP/N[235]+10/12*(VP/N[227]-VP/N[235])
50	VP/N[235]+11/12*(VP/N[227]-VP/N[235])
51	VP/N[227]
52	VP/N[227]+1/24*(VP/N[215]-VP/N[227])
53	VP/N[227]+2/24*(VP/N[215]-VP/N[227])
54	VP/N[227]+3/24*(VP/N[215]-VP/N[227])
55	VP/N[227]+4/24*(VP/N[215]-VP/N[227])
56	VP/N[227]+5/24*(VP/N[215]-VP/N[227])
57	VP/N[227]+6/24*(VP/N[215]-VP/N[227])
58	VP/N[227]+7/24*(VP/N[215]-VP/N[227])
59	VP/N[227]+8/24*(VP/N[215]-VP/N[227])
60	VP/N[227]+9/24*(VP/N[215]-VP/N[227])
61	VP/N[227]+10/24*(VP/N[215]-VP/N[227])
62	VP/N[227]+11/24*(VP/N[215]-VP/N[227])
63	VP/N[227]+12/24*(VP/N[215]-VP/N[227])
64	VP/N[227]+13/24*(VP/N[215]-VP/N[227])
65	VP/N[227]+14/24*(VP/N[215]-VP/N[227])
66	VP/N[227]+15/24*(VP/N[215]-VP/N[227])
67	VP/N[227]+16/24*(VP/N[215]-VP/N[227])
68	VP/N[227]+17/24*(VP/N[215]-VP/N[227])
69	VP/N[227]+18/24*(VP/N[215]-VP/N[227])
70	VP/N[227]+19/24*(VP/N[215]-VP/N[227])
71	VP/N[227]+20/24*(VP/N[215]-VP/N[227])
72	VP/N[227]+21/24*(VP/N[215]-VP/N[227])
73	VP/N[227]+22/24*(VP/N[215]-VP/N[227])
74	VP/N[227]+23/24*(VP/N[215]-VP/N[227])
75	VP/N[215]
76	VP/N[215]+1/24*(VP/N[203]-VP/N[215])
77	VP/N[215]+2/24*(VP/N[203]-VP/N[215])
78	VP/N[215]+3/24*(VP/N[203]-VP/N[215])
79	VP/N[215]+4/24*(VP/N[203]-VP/N[215])
80	VP/N[215]+5/24*(VP/N[203]-VP/N[215])
81	VP/N[215]+6/24*(VP/N[203]-VP/N[215])

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38	VP/N[243]+11/12*(VP/N[235]-VP/N[243])
39	VP/N[235]
40	VP/N[235]+1/12*(VP/N[227]-VP/N[235])
41	VP/N[235]+2/12*(VP/N[227]-VP/N[235])
Gray 42	VP/N[235]+3/12*(VP/N[227]-VP/N[235])
Gray 43	VP/N[235]+4/12*(VP/N[227]-VP/N[235])

82	VP/N[215]+7/24*(VP/N[203]-VP/N[215])
83	VP/N[215]+8/24*(VP/N[203]-VP/N[215])
84	VP/N[215]+9/24*(VP/N[203]-VP/N[215])
85	VP/N[215]+10/24*(VP/N[203]-VP/N[215])
Gray 86	VP/N[215]+11/24*(VP/N[203]-VP/N[215])
Gray 87	VP/N[215]+12/24*(VP/N[203]-VP/N[215])

Grayscale voltage	Formula
Gray 88	VP/N[215]+13/24*(VP/N[203]-VP/N[215])
Gray 89	VP/N[215]+14/24*(VP/N[203]-VP/N[215])
90	VP/N[215]+15/24*(VP/N[203]-VP/N[215])
91	VP/N[215]+16/24*(VP/N[203]-VP/N[215])
92	VP/N[215]+17/24*(VP/N[203]-VP/N[215])
93	VP/N[215]+18/24*(VP/N[203]-VP/N[215])
94	VP/N[215]+19/24*(VP/N[203]-VP/N[215])
95	VP/N[215]+20/24*(VP/N[203]-VP/N[215])
96	VP/N[215]+21/24*(VP/N[203]-VP/N[215])
97	VP/N[215]+22/24*(VP/N[203]-VP/N[215])
98	VP/N[215]+23/24*(VP/N[203]-VP/N[215])
99	VP/N[203]
100	VP/N[203]+1/28*(VP/N[179]-VP/N[203])
101	VP/N[203]+2/28*(VP/N[179]-VP/N[203])
102	VP/N[203]+3/28*(VP/N[179]-VP/N[203])
103	VP/N[203]+4/28*(VP/N[179]-VP/N[203])
104	VP/N[203]+5/28*(VP/N[179]-VP/N[203])
105	VP/N[203]+6/28*(VP/N[179]-VP/N[203])
106	VP/N[203]+7/28*(VP/N[179]-VP/N[203])
107	VP/N[203]+8/28*(VP/N[179]-VP/N[203])
108	VP/N[203]+9/28*(VP/N[179]-VP/N[203])
109	VP/N[203]+10/28*(VP/N[179]-VP/N[203])
110	VP/N[203]+11/28*(VP/N[179]-VP/N[203])
111	VP/N[203]+12/28*(VP/N[179]-VP/N[203])
112	VP/N[203]+13/28*(VP/N[179]-VP/N[203])
113	VP/N[203]+14/28*(VP/N[179]-VP/N[203])
114	VP/N[203]+15/28*(VP/N[179]-VP/N[203])
115	VP/N[203]+16/28*(VP/N[179]-VP/N[203])
116	VP/N[203]+17/28*(VP/N[179]-VP/N[203])
117	VP/N[203]+18/28*(VP/N[179]-VP/N[203])
118	VP/N[203]+19/28*(VP/N[179]-VP/N[203])

Grayscale voltage	Formula
Gray 132	VP/N[179]+5/28*(VP/N[155]-VP/N[179])
Gray 133	VP/N[179]+6/28*(VP/N[155]-VP/N[179])
134	VP/N[179]+7/28*(VP/N[155]-VP/N[179])
135	VP/N[179]+8/28*(VP/N[155]-VP/N[179])
136	VP/N[179]+9/28*(VP/N[155]-VP/N[179])
137	VP/N[179]+10/28*(VP/N[155]-VP/N[179])
138	VP/N[179]+11/28*(VP/N[155]-VP/N[179])
139	VP/N[179]+12/28*(VP/N[155]-VP/N[179])
140	VP/N[179]+13/28*(VP/N[155]-VP/N[179])
141	VP/N[179]+14/28*(VP/N[155]-VP/N[179])
142	VP/N[179]+15/28*(VP/N[155]-VP/N[179])
143	VP/N[179]+16/28*(VP/N[155]-VP/N[179])
144	VP/N[179]+17/28*(VP/N[155]-VP/N[179])
145	VP/N[179]+18/28*(VP/N[155]-VP/N[179])
146	VP/N[179]+19/28*(VP/N[155]-VP/N[179])
147	VP/N[179]+20/28*(VP/N[155]-VP/N[179])
148	VP/N[179]+21/28*(VP/N[155]-VP/N[179])
149	VP/N[179]+22/28*(VP/N[155]-VP/N[179])
150	VP/N[179]+23/28*(VP/N[155]-VP/N[179])
151	VP/N[179]+24/28*(VP/N[155]-VP/N[179])
152	VP/N[179]+25/28*(VP/N[155]-VP/N[179])
153	VP/N[179]+26/28*(VP/N[155]-VP/N[179])
154	VP/N[179]+27/28*(VP/N[155]-VP/N[179])
155	VP/N[155]
156	VP/N[155]+1/24*(VP/N[127]-VP/N[155])
157	VP/N[155]+2/24*(VP/N[127]-VP/N[155])
158	VP/N[155]+3/24*(VP/N[127]-VP/N[155])
159	VP/N[155]+4/24*(VP/N[127]-VP/N[155])
160	VP/N[155]+5/24*(VP/N[127]-VP/N[155])
161	VP/N[155]+6/24*(VP/N[127]-VP/N[155])
162	VP/N[155]+7/24*(VP/N[127]-VP/N[155])

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119	VP/N[203]+20/28*(VP/N[179]-VP/N[203])
120	VP/N[203]+21/28*(VP/N[179]-VP/N[203])
121	VP/N[203]+22/28*(VP/N[179]-VP/N[203])
122	VP/N[203]+23/28*(VP/N[179]-VP/N[203])
123	VP/N[203]+24/28*(VP/N[179]-VP/N[203])
124	VP/N[203]+25/28*(VP/N[179]-VP/N[203])
125	VP/N[203]+26/28*(VP/N[179]-VP/N[203])
126	VP/N[203]+27/28*(VP/N[179]-VP/N[203])
127	VP/N[179]
128	VP/N[179]+1/28*(VP/N[155]-VP/N[179])
129	VP/N[179]+2/28*(VP/N[155]-VP/N[179])
Gray 130	VP/N[179]+3/28*(VP/N[155]-VP/N[179])
Gray 131	VP/N[179]+4/28*(VP/N[155]-VP/N[179])

163	VP/N[155]+8/24*(VP/N[127]-VP/N[155])
164	VP/N[155]+9/24*(VP/N[127]-VP/N[155])
165	VP/N[155]+10/24*(VP/N[127]-VP/N[155])
166	VP/N[155]+11/24*(VP/N[127]-VP/N[155])
167	VP/N[155]+12/24*(VP/N[127]-VP/N[155])
168	VP/N[155]+13/24*(VP/N[127]-VP/N[155])
169	VP/N[155]+14/24*(VP/N[127]-VP/N[155])
170	VP/N[155]+15/24*(VP/N[127]-VP/N[155])
171	VP/N[155]+16/24*(VP/N[127]-VP/N[155])
172	VP/N[155]+17/24*(VP/N[127]-VP/N[155])
173	VP/N[155]+18/24*(VP/N[127]-VP/N[155])
Gray 174	VP/N[155]+19/24*(VP/N[127]-VP/N[155])
Gray 175	VP/N[155]+20/24*(VP/N[127]-VP/N[155])

Grayscale voltage	Formula
Gray 176	VP/N[155]+21/24*(VP/N[127]-VP/N[155])
Gray 177	VP/N[155]+22/24*(VP/N[127]-VP/N[155])
178	VP/N[155]+23/24*(VP/N[127]-VP/N[155])
179	VP/N[127]
180	VP/N[127]+1/24*(VP/N[99]-VP/N[127])
181	VP/N[127]+2/24*(VP/N[99]-VP/N[127])
182	VP/N[127]+3/24*(VP/N[99]-VP/N[127])
183	VP/N[127]+4/24*(VP/N[99]-VP/N[127])
184	VP/N[127]+5/24*(VP/N[99]-VP/N[127])
185	VP/N[127]+6/24*(VP/N[99]-VP/N[127])
186	VP/N[127]+7/24*(VP/N[99]-VP/N[127])
187	VP/N[127]+8/24*(VP/N[99]-VP/N[127])
188	VP/N[127]+9/24*(VP/N[99]-VP/N[127])
189	VP/N[127]+10/24*(VP/N[99]-VP/N[127])
190	VP/N[127]+11/24*(VP/N[99]-VP/N[127])
191	VP/N[127]+12/24*(VP/N[99]-VP/N[127])
192	VP/N[127]+13/24*(VP/N[99]-VP/N[127])
193	VP/N[127]+14/24*(VP/N[99]-VP/N[127])
194	VP/N[127]+15/24*(VP/N[99]-VP/N[127])
195	VP/N[127]+16/24*(VP/N[99]-VP/N[127])
196	VP/N[127]+17/24*(VP/N[99]-VP/N[127])
197	VP/N[127]+18/24*(VP/N[99]-VP/N[127])
198	VP/N[127]+19/24*(VP/N[99]-VP/N[127])
199	VP/N[127]+20/24*(VP/N[99]-VP/N[127])

Grayscale voltage	Formula
Gray 216	VP/N[75]+1/12*(VP/N[51]-VP/N[75])
Gray 217	VP/N[75]+2/12*(VP/N[51]-VP/N[75])
218	VP/N[75]+3/12*(VP/N[51]-VP/N[75])
219	VP/N[75]+4/12*(VP/N[51]-VP/N[75])
220	VP/N[75]+5/12*(VP/N[51]-VP/N[75])
221	VP/N[75]+6/12*(VP/N[51]-VP/N[75])
222	VP/N[75]+7/12*(VP/N[51]-VP/N[75])
223	VP/N[75]+8/12*(VP/N[51]-VP/N[75])
224	VP/N[75]+9/12*(VP/N[51]-VP/N[75])
225	VP/N[75]+10/12*(VP/N[51]-VP/N[75])
226	VP/N[75]+11/12*(VP/N[51]-VP/N[75])
227	VP/N[51]
228	VP/N[51]+1/8*(VP/N[39]-VP/N[51])
229	VP/N[51]+2/8*(VP/N[39]-VP/N[51])
230	VP/N[51]+3/8*(VP/N[39]-VP/N[51])
231	VP/N[51]+4/8*(VP/N[39]-VP/N[51])
232	VP/N[51]+5/8*(VP/N[39]-VP/N[51])
233	VP/N[51]+6/8*(VP/N[39]-VP/N[51])
234	VP/N[51]+7/8*(VP/N[39]-VP/N[51])
235	VP/N[39]
236	VP/N[39]+1/8*(VP/N[27]-VP/N[39])
237	VP/N[39]+2/8*(VP/N[27]-VP/N[39])
238	VP/N[39]+3/8*(VP/N[27]-VP/N[39])
239	VP/N[39]+4/8*(VP/N[27]-VP/N[39])

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200	VP/N[127]+21/24*(VP/N[99]-VP/N[127])	240	VP/N[39]+5/8*(VP/N[27]-VP/N[39])
201	VP/N[127]+22/24*(VP/N[99]-VP/N[127])	241	VP/N[39]+6/8*(VP/N[27]-VP/N[39])
202	VP/N[127]+23/24*(VP/N[99]-VP/N[127])	242	VP/N[39]+7/8*(VP/N[27]-VP/N[39])
203	VP/N[99]	243	VP/N[27]
204	VP/N[99]+1/12*(VP/N[75]-VP/N[99])	244	VP/N[27]+1/4*(VP/N[19]-VP/N[27])
205	VP/N[99]+2/12*(VP/N[75]-VP/N[99])	245	VP/N[27]+2/4*(VP/N[19]-VP/N[27])
206	VP/N[99]+3/12*(VP/N[75]-VP/N[99])	246	VP/N[27]+3/4*(VP/N[19]-VP/N[27])
207	VP/N[99]+4/12*(VP/N[75]-VP/N[99])	247	VP/N[19]
208	VP/N[99]+5/12*(VP/N[75]-VP/N[99])	248	VP/N[19]+1/3*(VP/N[12]-VP/N[19])
209	VP/N[99]+6/12*(VP/N[75]-VP/N[99])	249	VP/N[19]+2//3*(VP/N[12]-VP/N[19])
210	VP/N[99]+7/12*(VP/N[75]-VP/N[99])	250	VP/N[12]
211	VP/N[99]+8/12*(VP/N[75]-VP/N[99])	251	1/2* VP/N[12]+1/2* VP/N[8]
212	VP/N[99]+9/12*(VP/N[75]-VP/N[99])	252	VP/N[8]
213	VP/N[99]+10/12*(VP/N[75]-VP/N[99])	253	1/2* VP/N[8]+1/2* VP/N[4]
Gray 214	VP/N[99]+11/12*(VP/N[75]-VP/N[99])	Gray 254	VP/N[4]
Gray 215	VP/N[75]	Gray 255	VP/N[0]

Table10.29: Voltage calculation formula of 256-grayscale voltage (positive/negative polarity)

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10.12. OTP programming Flow

When OTP programming must display off and TP_RESX pull GND.

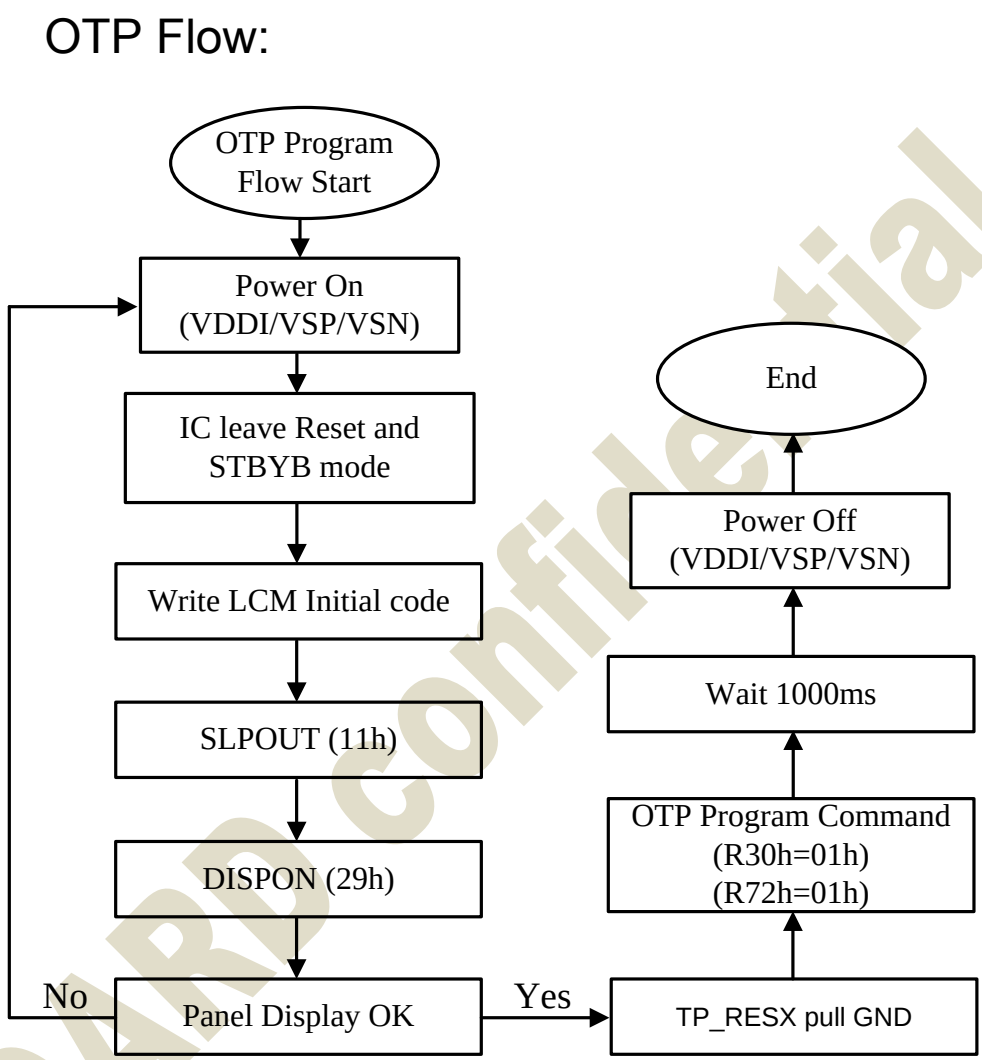


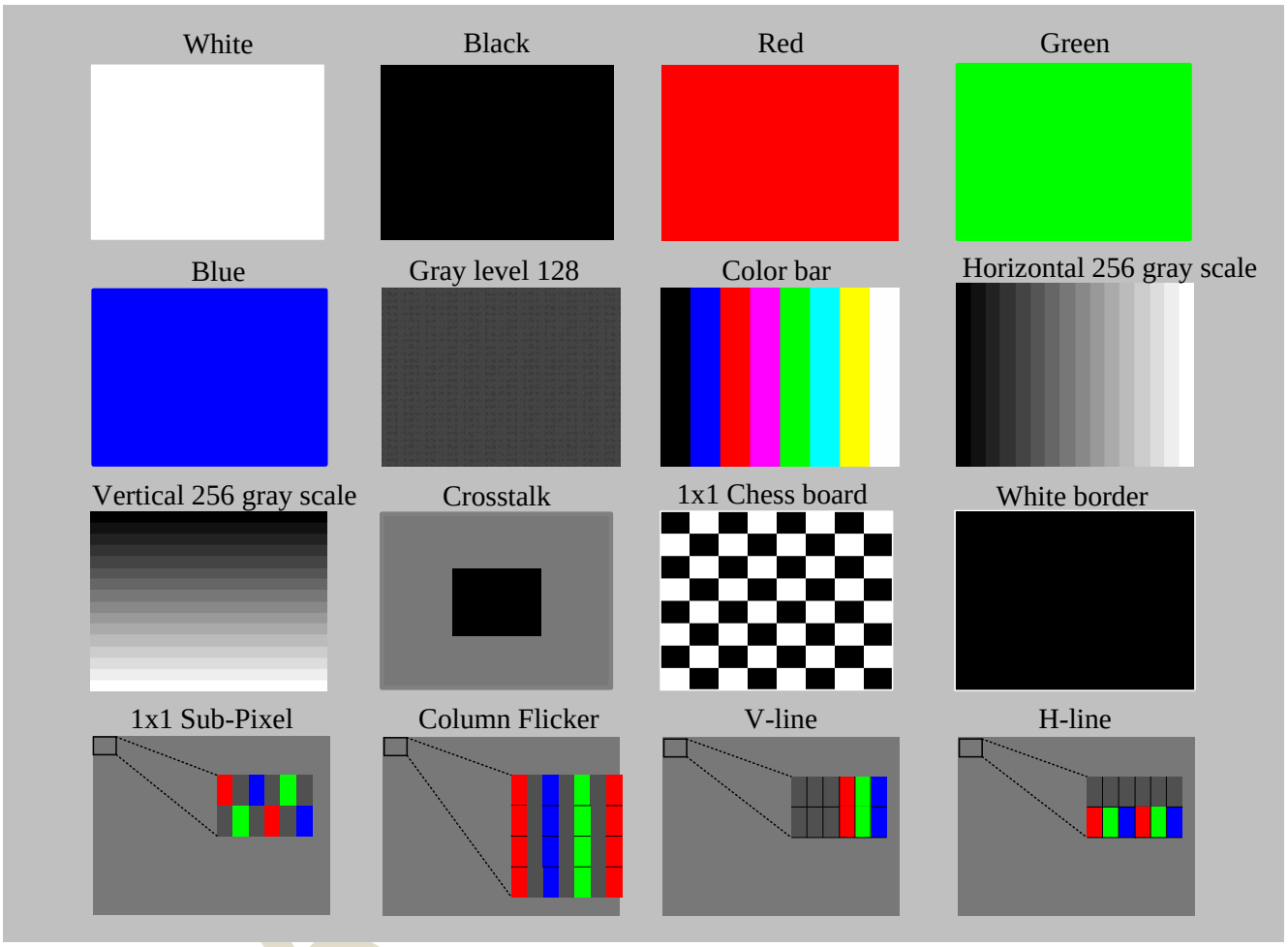
Figure 7.26: OTP timing chart

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10.13. BIST Fuction

When BIST_EN is trigger to high, then JD9366TC will leave normal operation mode and starts to generate the BIST pattern to LCD panel without TX input signals.

BIST Pattern



White → Black → Red → Green → Blue → Gray level 128 → Color Bar→ Horizontal 256 gray scale → Vertical 256 gray scale → Crosstalk → 1x1 Chess board → White border → 1x1 Sub-Pixel → Column Flicker → V-line → H-line.

11. Command

11.1. Command List

11.1.1. Standard command

Address	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function
00	NOP	W	0	0	0	0	0	0	0	0	No Operation
01	SWRESET	W	0	0	0	0	0	0	0	1	Software Reset
04	RDDIDIF	W	0	0	0	0	0	1	0	0	Read Display Identification Information
		R	ID1[7:0]								
		R	ID2[7:0]								
		R	ID3[7:0]								
05	RDNUMPE	W	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error
		R	P[7:0]								
06	RDRED	W	0	0	0	0	0	1	1	0	Read Red Color
		R	R[7:0]								
07	RDGREEN	W	0	0	0	0	0	1	1	1	Read Green Color
		R	G[7:0]								
08	RDBLUE	W	0	0	0	0	1	0	0	0	Read Blue Color
		R	B[7:0]								
09	RDDST	W	0	0	0	0	1	0	0	1	Read Display Status
		R	D[31:24]								
		R	D[23:16]								
		R	D[15:8]								
		R	D[7:0]								
0A	RDDPM	W	0	0	0	0	1	0	1	0	Read display power mode
		R	D7	D6	D5	D4	D3	D2	0	0	
0B	RDDMADCTL	W	0	0	0	0	1	0	1	1	Read display MADCTL
		R	D7	D6	D5	D4	D3	D2	D1	D0	
0C	RDDCOLMOD	W	0	0	0	0	1	1	0	0	Read display pixel format
		R	0	D6	D5	D4	0	D2	D1	D0	
0D	RDDIM	W	0	0	0	0	1	1	0	1	Read display image mode
		R	D7	D6	D5	D4	D3	D2	D1	D0	
0E	RDDSM	W	0	0	0	0	1	1	1	0	Read display signal mode
		R	D7	D6	D5	D4	D3	D2	D1	D0	
0F	RDDSDR	W	0	0	0	0	1	1	1	1	Read display self-diagnostic result
		R	D7	D6	D5	D4	0	0	0	0	
10	SLPIN	W	0	0	0	1	0	0	0	0	Sleep In
11	SLPOUT	R	0	0	0	1	0	0	0	1	Sleep Out
13	NORON	W	0	0	0	1	0	0	1	1	Normal display mode on
20	INVOFF	W	0	0	1	0	0	0	0	0	Display inversion off
21	INVON	W	0	0	1	0	0	0	0	1	Display inversion on

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22	ALLPOFF	W	0	0	1	0	0	0	1	0	All Pixel Off
23	ALLPON	W	0	0	1	0	0	0	1	1	All Pixel On
26	GAMSET	W	0	0	1	0	0	1	1	0	Gamma set-
		W	CG[7:0]								
28	DISPOFF	W	0	0	1	0	1	0	0	0	Display off
29	DISPON	W	0	0	1	0	1	0	0	1	Display on
34	TEOFF	W	0	0	1	1	0	1	0	0	Tearing Effect Line OFF
35	TEON	W	0	0	1	1	0	1	0	1	Tearing Effect Line ON
		W	X	X	X	X	X	X	X	M	
36	MADCTL	W	0	0	1	1	0	1	1	0	Memory Access Control
		W	B7	B6	B5	B4	B3	B2	X	X	
38	IDMOFF	W	0	0	1	1	1	0	0	0	Idle mode off
39	IDMON	W	0	0	1	1	1	0	0	1	Idle mode on
3A	COLMOD	W	0	0	1	1	1	0	1	0	Interface Pixel Format
		W	X	D6	D5	D4	X	D2	D1	D0	
44	TESL	W	0	1	0	0	0	1	0	0	Set Tear Effect Scan Lines
		W	TELINE[15:8]								
		W	TELINE[7:0]								
45	GETSCAN	W	0	1	0	0	0	1	0	1	Return the current scanline
		R	SLN[15:8]								
		R	SLN[7:0]								
51	WRDISBV	W	0	1	0	1	0	0	0	1	Write Display Brightness
		W	DBV[7:0]								-
52	RDDISBV	W	0	1	0	1	0	0	1	0	Read Display Brightness Value
		R	DBV[7:0]								
53	WRCTRLD	W	0	1	0	1	0	0	1	1	Write CTRL Display
		W	X	X	BCTRL	X	DD	BL	X	X	
54	RDCTRLD	W	0	1	0	1	0	0	1	1	Read Control Value Display-
		R	0	0	BCTRL	0	DD	BL	0	0	
55	WRCABC	W	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control
		W	IEC[3:0]				X	X	CABC[1:0]		
56	RDCABC	W	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content
		R	IEC[3:0]				0	0	CABC[1:0]		
5E	WRCABCMB	W	0	1	0	1	1	1	1	0	Write CABC minimum brightness
		W	CMB[7:0]								
5F	RDCABCMB	W	0	1	0	1	1	1	1	1	Read CABC minimum brightness
		R	CMB[7:0]								
68	RDABCSDR	W	0	1	1	0	1	0	0	0	Read ABC Self-Diagnostic Result
		R	D[7:6]		0	0	0	0	0	0	
DA	RDID1	W	1	1	0	1	1	0	1	0	Read ID1
		R	module's manufacturer[7:0]								

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DB	RDID2	W	1	1	0	1	1	0	1	1	Read ID2
		R	LCD module/driver version [7:0]								
DC	RDID3	W	1	1	0	1	1	1	0	0	Read ID3
		R	LCD module/driver ID[7:0]								
A1	RDDDB	W	1	0	1	0	0	0	0	1	Read the DDB from the provided location.
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
A8	RDDDBCON	W	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
AA	RDFCS	W	1	0	1	0	1	0	1	0	Read First Checksum
		R	FCS[7:0]								
AF	RDCCS	W	1	0	1	0	1	1	1	1	Read Continue Checksum
		R	CCS[7:0]								

Table 11.1: Standard command list

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11.1.2.Standard Command Accessibility

Hex Code	Operation code	Normal Mode On, Idle Mode Off, Sleep Mode Off	Normal Mode On, Idle Mode On, Sleep Mode Off	Partial Mode On, Idle Mode Off, Sleep Mode Off	Partial Mode On, Idle Mode On, Sleep Mode Off	Sleep Mode On
00	NOP	Yes	Yes	Yes	Yes	Yes
01	SWRESET	Yes	Yes	Yes	Yes	Yes
04	RDDIDIF	Yes	Yes	Yes	Yes	Yes
05	RDNUMPE	Yes	Yes	N/A	N/A	Yes
06	RDRED	Yes	Yes	N/A	N/A	Yes
07	RDGREEN	Yes	Yes	N/A	N/A	Yes
08	RDBLUE	Yes	Yes	N/A	N/A	Yes
09	RDDST	Yes	Yes	N/A	N/A	Yes
0A	RDDPM	Yes	Yes	Yes	Yes	Yes
0B	RDDMADCTL	Yes	Yes	Yes	Yes	Yes
0C	RDDCOLMOD	Yes	Yes	Yes	Yes	Yes
0D	RDDIM	Yes	Yes	Yes	Yes	Yes
0E	RDDSM	Yes	Yes	Yes	Yes	Yes
0F	RDDSDR	Yes	Yes	Yes	Yes	Yes
10	SLPIN	Yes	Yes	Yes	Yes	Yes
11	SLPOUT	Yes	Yes	Yes	Yes	Yes
13	NORON	Yes	Yes	Yes	Yes	Yes
20	INVOFF	Yes	Yes	Yes	Yes	Yes
21	INVON	Yes	Yes	Yes	Yes	Yes
22	ALLPOFF	Yes	Yes	N/A	N/A	Yes
23	ALLPON	Yes	Yes	N/A	N/A	Yes
26	GAMSET	Yes	Yes	Yes	Yes	Yes
28	DISPOFF	Yes	Yes	Yes	Yes	Yes
29	DISPON	Yes	Yes	Yes	Yes	Yes
34	TEOFF	Yes	Yes	Yes	Yes	Yes
35	TEON	Yes	Yes	Yes	Yes	Yes
36	MADCTL	Yes	Yes	Yes	Yes	Yes
38	IDMOFF	Yes	Yes	Yes	Yes	Yes
39	IDMON	Yes	Yes	Yes	Yes	Yes
3A	COLMOD	Yes	Yes	Yes	Yes	Yes
44	TESL	Yes	Yes	Yes	Yes	Yes
45	GETSCAN	Yes	Yes	Yes	Yes	Yes
51	WRDISBV	Yes	Yes	Yes	Yes	Yes
52	RDDISBV	Yes	Yes	Yes	Yes	Yes
53	WRCTRLD	Yes	Yes	Yes	Yes	Yes
54	RDCTRLD	Yes	Yes	Yes	Yes	Yes
55	WRCABC	Yes	Yes	Yes	Yes	Yes
56	RDCABC	Yes	Yes	Yes	Yes	Yes
5E	WRCABCMB	Yes	Yes	Yes	Yes	Yes
5F	RDCABCMB	Yes	Yes	Yes	Yes	Yes
DA	RDID1	Yes	Yes	Yes	Yes	Yes
DB	RDID2	Yes	Yes	Yes	Yes	Yes
DC	RDID3	Yes	Yes	Yes	Yes	Yes
A1	RDDDB	Yes	Yes	Yes	Yes	Yes
A8	RDDDBCON	Yes	Yes	Yes	Yes	Yes
AA	RDFCS	Yes	Yes	Yes	Yes	Yes
AF	RDCCS	Yes	Yes	Yes	Yes	Yes

Table 11.2: Standard Command Accessibility

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11.1.3.Standard Command Default Modes and Values

Hex Code	Operation code	Parameters	Power-on Sequence	SW Reset	HW Reset
00	NOP	None	N/A	N/A	N/A
01	SWRESET	None	N/A	N/A	N/A
04	RDDIDIF	3	OTP Value	OTP Value	OTP Value
05	RDNUMPE	1	00h	00h	00h
06	RDRED	1	00h	00h	00h
07	RDGREEN	1	00h	00h	00h
08	RDBLUE	1	00h	00h	00h
09	RDDST	1	Refer to corresponding command parameters	Refer to corresponding command parameters	Refer to corresponding command parameters
0A	RDDPM	1	08h	08h	08h
0B	RDDMADCTL	1	00h	Refer to corresponding command parameters	00h
0C	RDDCOLMOD	1	07h	07h	07h
0D	RDDIM	1	00h	00h	00h
0E	RDDSM	1	00h	00h	00h
0F	RDDSDR	1	00h	00h	00h
10	SLPIN	None	Sleep In Mode	Sleep In Mode	Sleep In Mode
11	SLPOUT	None	Sleep In Mode	Sleep In Mode	Sleep In Mode
13	NORON	None	Normal Display mode On	Normal Display mode On	Normal Display mode On
20	INVOFF	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
21	INVON	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
22	ALLPOFF	None	All Pixel Off	All Pixel Off	All Pixel Off
23	ALLPON	None	All Pixel Off	All Pixel Off	All Pixel Off
26	GAMSET	1	01h	01h	01h
28	DISPOFF	None	Display Off	Display Off	Display Off
29	DISPON	None	Display Off	Display Off	Display Off
34	TEOFF	None	TE Off	TE Off	TE Off
35	TEON	1	TE Off	TE Off	TE Off
36	MADCTL	1	00h	No Change	00h
37	VSCRSADD	2	0000h	0000h	0000h
38	IDMOFF	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
39	IDMON	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
3A	COLMOD	1	07h	No Change	07h
44	TESL	2	0000h	0000h	0000h
45	GETSCAN	2	0000h	0000h	0000h
51	WRDISBV	1	00h	00h	00h
52	RDDISBV	1	00h	00h	00h
53	WRCTRLD	1	00h	00h	00h
54	RDCTRLD	1	00h	00h	00h
55	WRCABC	1	00h	00h	00h
56	RDCABC	1	00h	00h	00h
5E	WRCABCMB	1	00h	00h	00h
5F	RDCABCMB	1	00h	00h	00h
DA	RDID1	1	OTP Value	OTP Value	OTP Value
DB	RDID2	1	OTP Value	OTP Value	OTP Value
DC	RDID3	1	OTP Value	OTP Value	OTP Value
A1	RDDDB	All	OTP Value	OTP Value	OTP Value
A8	RDDDBCON	All	OTP Value	OTP Value	OTP Value
AA	RDFCS	1	00h	00h	00h
AF	RDCCS	1	00h	00h	00h

Table 11.3: Standard Command Default Modes and Value

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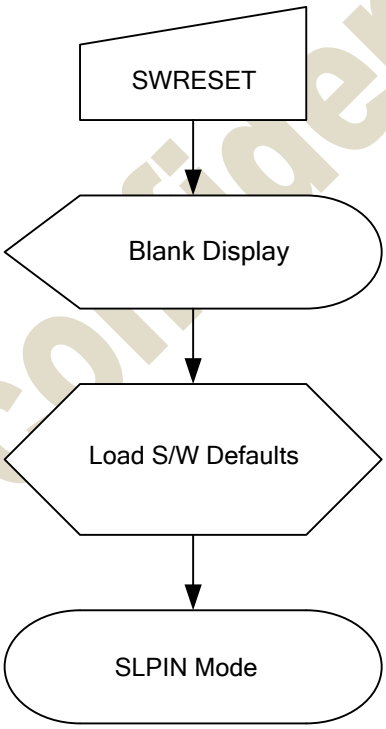
11.2. Command Description

11.2.1.NOP (00h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	0	0	0	0	00
Description	This command does not have any effect on the display module. The NOP command may be used to terminate a Frame Memory Read or Frame Memory Write.									
Restriction	-									
Flow Chart	-									

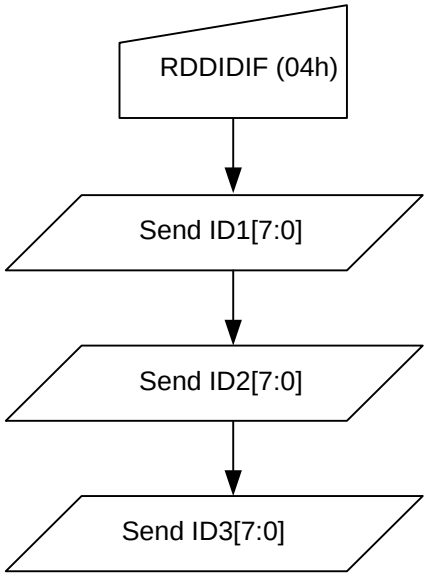
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11.2.2.SWRESET: Software Reset (01h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	0	0	0	1	01
Description	The display module performs a software reset. Registers are written with their SW Reset default values. The Frame Memory contents are unaffected by this command									
Restriction	The host processor must wait 5 milliseconds before sending any new commands to a display module following this command. The display module updates the registers during this time. If a SWRESET is sent when the display module is in SLPIN Mode, the host processor must wait 120 milliseconds before sending an SLPOUT command. SWRESET should not be sent when the display module is not in SLPIN mode.									
Flow Chart										

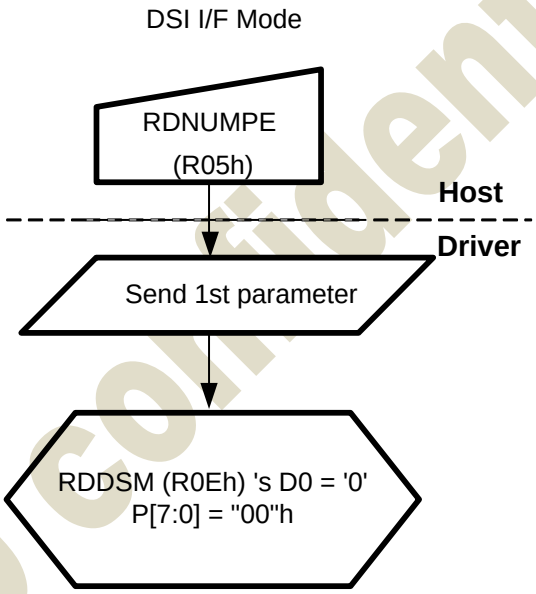
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11.2.3.RDDIDIF: Read Display Identification Information (04h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04</td></tr>
<tr><td>Parameter 1</td><td>R</td><td colspan="8">ID1[7:0]</td><td></td></tr>
<tr><td>Parameter 2</td><td>R</td><td colspan="8">ID2[7:0]</td><td></td></tr>
<tr><td>Parameter 3</td><td>R</td><td colspan="8">ID3[7:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns 24-bit display identification information.
The 1st Parameter identifies the LCD module’s manufacturer. It is specified by display supplier and for xx is defined as xxHEX.
The 2nd Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Color). Bits 6~0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:
<table>
<tr><th>ID Byte Value V[7:0]</th><th>Version</th><th>Changes</th></tr>
<tr><td>80h</td><td></td><td></td></tr>
<tr><td>81h</td><td></td><td></td></tr>
<tr><td>82h</td><td></td><td></td></tr>
<tr><td>83h</td><td></td><td></td></tr>
<tr><td>84h</td><td></td><td></td></tr>
<tr><td>85h</td><td></td><td></td></tr>
</table>
The 3rd parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10">
</td></tr>
</table>

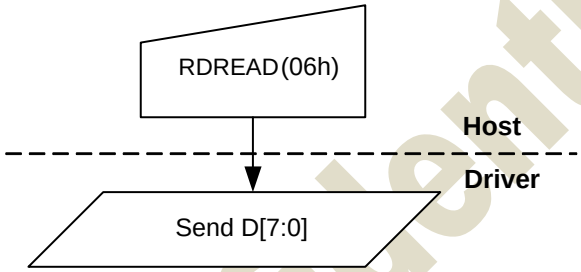
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11.2.4.RDNUMPE: Read number of the parity errors (05h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	0	1	0	1	05
Parameter 1	**R**	P7	P6	P5	P4	P3	P2	P1	P0	
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6:0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6..0] bits. P[7:0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (=The read function is completed).									
Restriction	-									
Flow Chart										

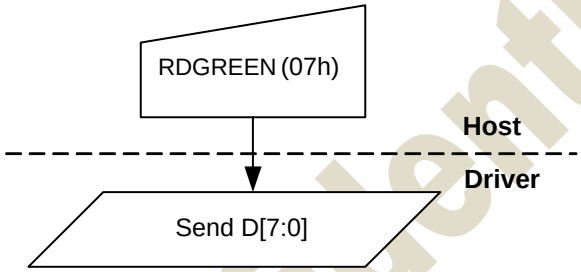
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11.2.5.REDRD: Read Red Color (06h)

CMD/PAs	R/W	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	-	0	0	0	0	0	1	1	0	06
Parameter 1	**R**	-	R7	R6	R5	R4	R3	R2	R1	R0	
Description	The first parameter is telling red color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'. 24 bit format: R7 is MSB and R0 is LSB. All bits are used.										
Restriction	-										
Flow Chart											

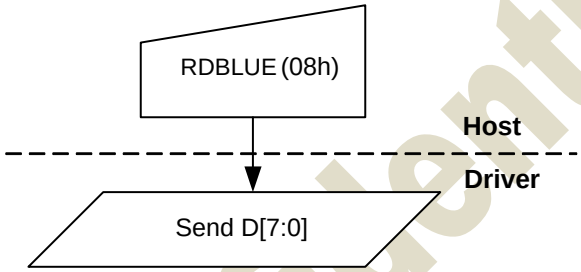
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11.2.6.REDGREEN: Read Green Color (07h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	0	1	1	1	07
Parameter 1	**R**	G7	G6	G5	G4	G3	G2	G1	G0	
Description	The first parameter is telling green color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. 18 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. 24 bit format: G7 is MSB and G0 is LSB. All bits are used.									
Restriction	-									
Flow Chart										

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11.2.7.REDBLUE: Read Blue Color (08h)

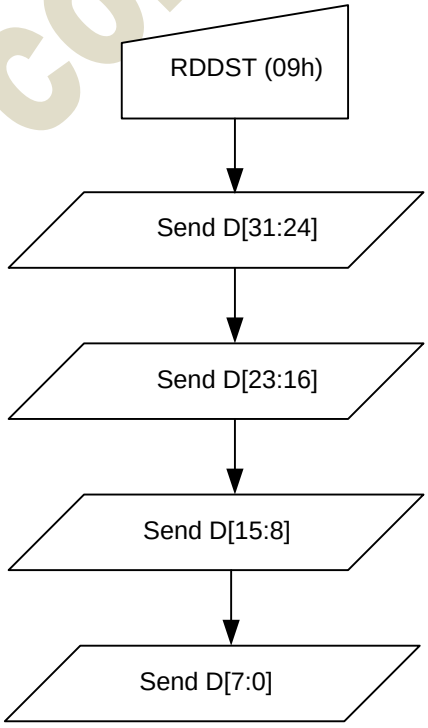
CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	1	0	0	0	08
Parameter 1	**R**	B7	B6	B5	B4	B3	B2	B1	B0	
Description	The first parameter is telling blue color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'. 24 bit format: B7 is MSB and B0 is LSB. All bits are used.									
Restriction	-									
Flow Chart										

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11.2.8.RDDST: Read Display Status (09h)

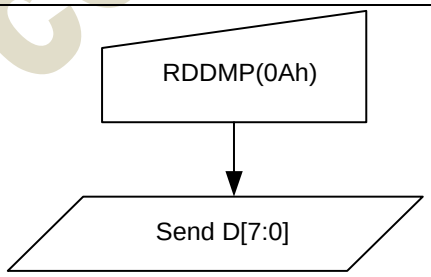
<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>09</td></tr>
<tr><td>Parameter 1</td><td>R</td><td colspan="8">D[31:24]</td><td></td></tr>
<tr><td>Parameter 2</td><td>R</td><td colspan="8">D[23:16]</td><td></td></tr>
<tr><td>Parameter 3</td><td>R</td><td colspan="8">D[15:8]</td><td></td></tr>
<tr><td>Parameter 4</td><td>R</td><td colspan="8">D[7:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D31</td><td>Booster Voltage Status</td><td>‘0’ = Booster Off.
‘1’ = Booster On.</td></tr>
<tr><td>D30</td><td>Page Address Order</td><td>‘0’ = Top to Bottom (MADCTL B7=’0’).
‘1’ = Bottom to Top (MADCTL B7=’1’).</td></tr>
<tr><td>D29</td><td>Column Address Order</td><td>‘0’ = Left to Right (MADCTL B6=’0’).
‘1’ = Right to Left (MADCTL B6=’1’)</td></tr>
<tr><td>D28</td><td>Page/Column Order</td><td>‘0’ = Normal (MADCTL B5=’0’).
‘1’ = Rotation (MADCTL B5=’1’).</td></tr>
<tr><td>D27</td><td>Display Device Line Refresh Order</td><td>‘0’ = Refresh Top to Bottom (MADCTL B4=’0’).
‘1’ = Refresh Bottom to Top (MADCTL B4=’1’).</td></tr>
<tr><td>D26</td><td>RGB/BGR Order</td><td>‘0’ = RGB (MADCTL B3=’0’).
‘1’ = BGR (MADCTL B3=’1’).</td></tr>
<tr><td>D25</td><td>Display Data Latch Data Order</td><td>‘0’ = Refresh Left to Right (MADCTL B2=’0’).
‘1’ = Refresh Right to Left (MADCTL B2=’1’).</td></tr>
<tr><td>D24</td><td>Source san sequence</td><td>‘0’ = Source output Left to Right (MADCTL B1=’0’).
‘1’ = Source output Right to Left (MADCTL B1=’1’)</td></tr>
<tr><td>D23</td><td>Gate san sequence</td><td>‘0’ = Gate output Top to Bottom (MADCTL B0=’0’).
‘1’ = Gate output Bottom to Top (MADCTL B0=’1’)</td></tr>
<tr><td>D22
D21
D20</td><td>Interface Colo
Pixel Format Definition</td><td>
<table>
<tr><th>Interface Format</th><th>D22</th><th>D21</th><th>D20</th></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 Bit/Pixel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 Bit/Pixel</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>24 Bit/Pixel</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>D19</td><td>Idle Mode On/Off</td><td>‘0’ = Idle Mode Off. ‘1’ = Idle Mode On.</td></tr>
<tr><td>D18</td><td>Partial Mode On/Off</td><td>‘0’ = Partial Mode Off, ‘1’ = Partial Mode On.</td></tr>
<tr><td>D17</td><td>Sleep In/Out</td><td>‘0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.</td></tr>
<tr><td>D16</td><td>Display Normal Mode On/Off</td><td>‘0’ = Partial or Scrolling Mode.
‘1’ = Normal Mode.</td></tr>
<tr><td>D15</td><td>Vertical Scrolling Status</td><td>‘0’ = Vertical Scrolling is Off.
‘1’ = Vertical Scrolling is On.</td></tr>
<tr><td>D14</td><td>Horizontal Scrolling Status</td><td>This bit is not applicable for this project, so it is set to ‘0’</td></tr>
<tr><td>D13</td><td>Inversion Status</td><td>‘0’ = Inversion is Off.
‘1’ = Inversion is On.</td></tr>
<tr><td>D12</td><td>All Pixels On</td><td>‘0’ = Normal mode.
‘1’ = All Pixels On.</td></tr>
<tr><td>D11</td><td>All Pixels Off</td><td>0’ = Normal mode.
‘1’ = All Pixels Off.</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><td></td><td>
<table>
<tr><td>D10</td><td>Display On/Off</td><td>‘0’ = Display is Off.
‘1’ = Display is On.</td></tr>
<tr><td>D9</td><td>Tearing Effect Line On/Off</td><td>‘0’ =Tearing Effect Line Off.
‘1’ = Tearing Effect On.</td></tr>
<tr><td>D8
D7
D6</td><td>Gamma Curve Selection</td><td>
<table>
<tr><td>Gamma Curve Selected</td><td>B8</td><td>B7</td><td>B6</td></tr>
<tr><td>Gamma Curve 1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Gamma Curve 2</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Gamma Curve 3</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Gamma Curve 4</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>D5</td><td>Tearing Effect
Output Line Mode</td><td>‘0’ = Mode 1, V-Blanking only.
‘1’ = Mode 2, both H-Blanking and V-Blanking.</td></tr>
<tr><td>D4</td><td>Horizontal Sync.
(HSYNC, DPI I/F)</td><td>‘0’ = Horizontal Sync. line is Off (“Low”).
‘1’ = Horizontal Sync. line is On (“High”).</td></tr>
<tr><td>D3</td><td>Vertical Sync.
(VSYNC, DPI I/F)</td><td>‘0’ = Vertical Sync. line is Off (“Low”).
‘1’ = Vertical Sync. line is On (“High”).</td></tr>
<tr><td>D2</td><td>Pixel Clock
(DCK, DPI I/F)</td><td>‘0’ = PCLK line is Off (“Low”).
‘1’ = PCLK line is On (“High”).</td></tr>
<tr><td>D1</td><td>Reserved</td><td>Always = ‘0’</td></tr>
<tr><td>D0</td><td>Parity Error on DSI</td><td>‘0’=No Parity Error.
‘1’=Parity Error.</td></tr>
</table>
Note: This bit indicates current status of the line when this command has been sent.
</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Flow Chart</td><td>
</td></tr>
</table>

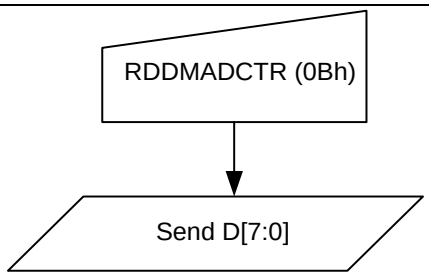
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11.2.9.RDDPM: Read Display Power Mode (0Ah)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Booster Voltage Status</td><td>‘0’ = Booster Off.
‘1’ = Booster On.</td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td>‘0’ = Idle Mode Off.
‘1’ = Idle Mode On.</td></tr>
<tr><td>D5</td><td>Partial Mode On/Off</td><td>‘0’ = Partial Mode Off.
‘1’ = Partial Mode On.</td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td>0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.</td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td>‘0’ = Display Normal Mode Off.
‘1’ = Display Normal Mode On.</td></tr>
<tr><td>D2</td><td>Display On/Off</td><td>‘0’ = Display is Off.
‘1’ = Display is On.</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10">
</td></tr>
</table>

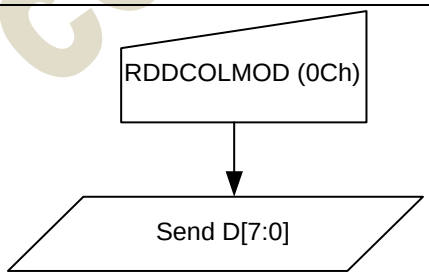
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11.2.10. RDDMATCDL: Read Display MADCTL (0Bh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td>‘0’ = Top to Bottom (When MADCTL B7=’0’).
‘1’ = Bottom to Top (When MADCTL B7=’1’).</td></tr>
<tr><td>D6</td><td>Column Address Order</td><td>‘0’ = Left to Right (When MADCTL B6=’0’).
‘1’ = Right to Left (When MADCTL B6=’1’).</td></tr>
<tr><td>D5</td><td>Page/Column Order</td><td>‘0’ = Normal (When MADCTL B5=’0’).
‘1’ = Rotation (When MADCTL B5=’1’).</td></tr>
<tr><td>D4</td><td>Line Address Order</td><td>‘0’ = Refresh Top to Bottom (When MADCTL B4=’0’).
‘1’ = Refresh Bottom to Top (When MADCTL B4=’1’).</td></tr>
<tr><td>D3</td><td>RGB/BGR Order</td><td>‘0’ = RGB (When MADCTL B3=’0’).
‘1’ = BGR (When MADCTL B3=’1’).</td></tr>
<tr><td>D2</td><td>Display Data Latch Order</td><td>‘0’ = LCD Refresh Left to Right (When MADCTL B2=’0’).
‘1’ = LCD Refresh Right to Left (When MADCTL B2=’1’).</td></tr>
<tr><td>D1</td><td>Source san sequence</td><td>‘0’ = Source output Left to Right (When MADCTL B1=’0’).
‘1’ = Source output Right to Left (When MADCTL B1=’1’).</td></tr>
<tr><td>D0</td><td>Gate san sequence</td><td>‘0’ = Gate output Top to Bottom (When MADCTL B0=’0’).
‘1’ = Gate output Bottom to Top (When MADCTL B0=’1’).</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10">
</td></tr>
</table>

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11.2.11. RDDCOLMOD: Read Display COLMOD (0Ch)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	1	1	0	0	0C
Parameter 1	**R**	-	D6	D5	D4	-	D2	D1	D0	
Description	This command gets the pixel format for the RGB image data used by the interface. D[6:4] – DPI Interface Color Pixel Format Definition, fixed @111 D[2:0] – DBI Interface Color Pixel Format Definition, fixed @000. If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module are undefined. Therefore, for a DBI display module, the Host shall ignore D[6:4] and for a DPI display module, the Host shall ignore D[2:0].									
Restriction	-									
Flow Chart										

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11.2.12. Read Display Image Mode (0Dh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	1	1	0	1	0D
Parameter 1	**R**	D7	D6	D5	D4	D3	D2	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

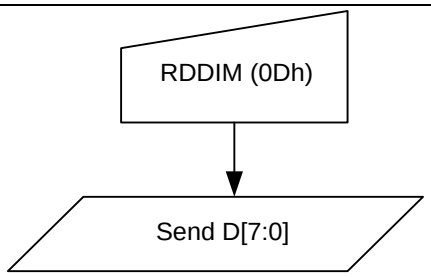
Bit	Description	Value
D7	Vertical Scrolling On/Off	'0' = Vertical Scrolling is Off. '1' = Vertical Scrolling is On.
D6	Horizontal Scrolling Status	This bit is not applicable for this project, set it to '0'
D5	Inversion On/Off	'0' = Inversion is Off. '1' = Inversion is On.
D4	All Pixels On	'0' = Normal Display '1' = White Display
D3	All Pixels Off	'0' = Normal Display '1' = Black Display
D2 D1 D0	Gamma Curve Selection	See table below

Gamma Curve Selected	D2	D1	D0	Gamma Set (26h)
Gamma Curve 1	0	0	0	CG0
Gamma Curve 2	0	0	1	CG1
Gamma Curve 3	0	1	0	CG2
Gamma Curve 4	0	1	1	CG3
Not Defined	1	0	0	
Not Defined	1	0	1	
Not Defined	1	1	0	
Not Defined	1	1	1	

Restriction

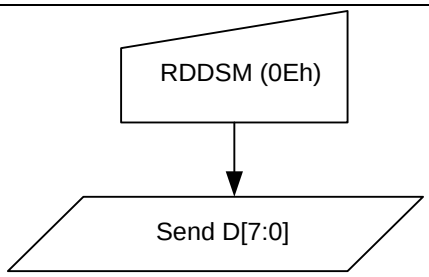
-

Flow Chart



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11.2.13. RDDSM: Read Display Signal Mode (0Eh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0E</td></tr>
<tr><td>Parameter 1</td><td>R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>‘0’ = Tearing Effect Line Off.
‘1’ = Tearing Effect On.</td></tr>
<tr><td>D6</td><td>Tearing Effect Line Output Mode</td><td>‘0’ = Mode 1.
‘1’ = Mode 2.</td></tr>
<tr><td>D5</td><td>Horizontal Sync. (RGB I/F) On/Off.</td><td>‘0’ = Horizontal Sync. Line is Off (“Low”).
‘1’ = Horizontal Sync. Line is On (“High”).</td></tr>
<tr><td>D4</td><td>Vertical Sync. (RGB I/F) On/Off.</td><td>‘0’ = Vertical Sync. Line is Off (“Low”).
‘1’ = Vertical Sync. Line is On (“High”).</td></tr>
<tr><td>D3</td><td>Pixel Clock (PCLK, RGB I/F) On/Off.</td><td>‘0’ = PCLK line is Off (“Low”).
‘1’ = PCLK line is On (“High”).</td></tr>
<tr><td>D2</td><td>Data Enable (DE, RGB I/F)) On/Off.</td><td>‘0’ = DE line is Off (“Low”).
‘1’ = DE line is On (“High”).</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>for future use and are set to ‘0’.</td></tr>
<tr><td>D0</td><td>Parity Error on DSI</td><td>‘0’=No Parity Error.
‘1’=Parity Error.</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10">
</td></tr>
</table>

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11.2.14. RDDSDR: Read Display Self-Diagnostic Result (0Fh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	0	1	1	1	1	0F
Parameter 1	**R**	D7	D6	D5	D4	0	0	0	0	

Description

The display module returns the self-diagnostic results following a SLPOUT command.

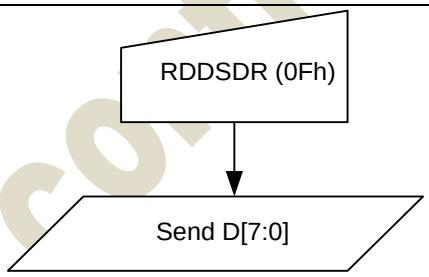
See section “錯誤! 找不到參照來源。 錯誤! 找不到參照來源。” for a description

Bit	Description	Value
D7	Register Loading Detection	See section “Sleep Out –command and self-diagnostic functions of the display module”
D6	Functionality Detection	
D5	Chip Attachment Detection	Set to ‘0’ if feature unimplemented.
D4	Display Glass Break Detection	Set to ‘0’ if feature unimplemented.
D3	Reserved	Set to ‘0’.
D2		Set to ‘0’.
D1		Set to ‘0’.
D0		Set to ‘0’.

Restriction

-

Flow Chart



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11.2.15. SLPIN: Enter Sleep In Mode (10h)

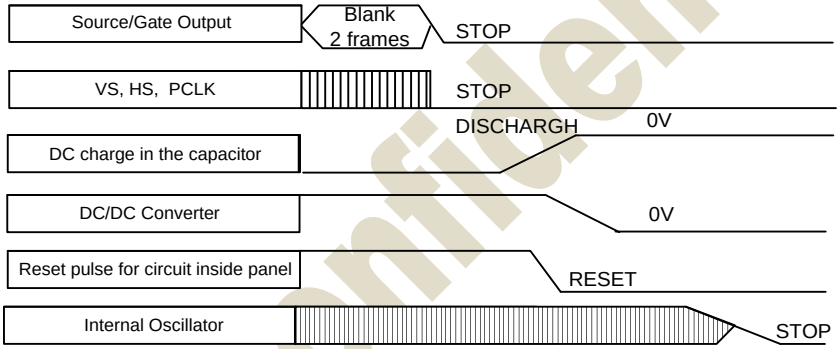
CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	1	0	0	0	0	10

Description

This command causes the LCD module to enter the minimum power consumption mode. In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports.

DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to DPI IF for two frames after this command is sent when the display module is in Normal mode.

In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.

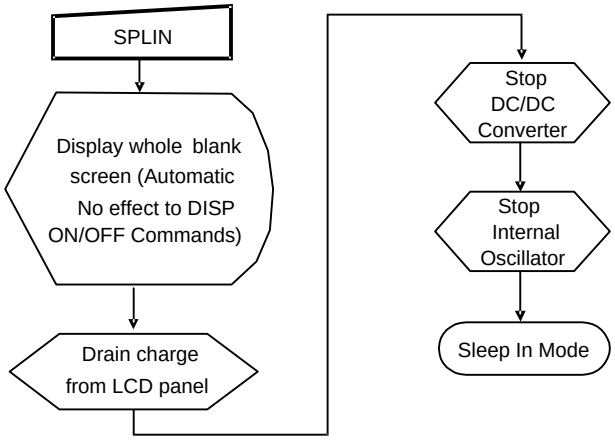


Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



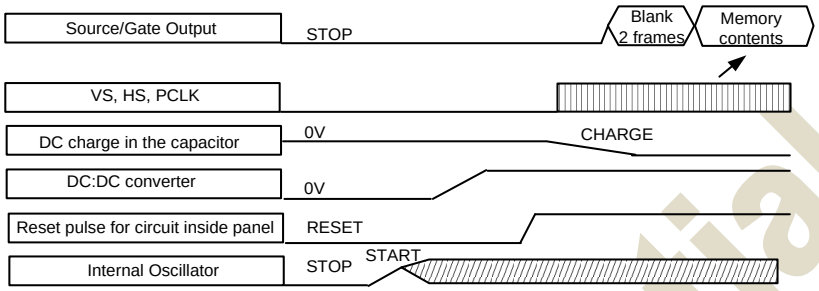
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11.2.16. SLPOUT: Exit Sleep In Mode (11h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	1	0	0	0	1	11

Description

This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.



User can start to send PCLK, HS and VS information on DPI IF before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In -mode to Sleep Out-mode in Normal Mode On. There is used an internal oscillator for blank display.

Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).

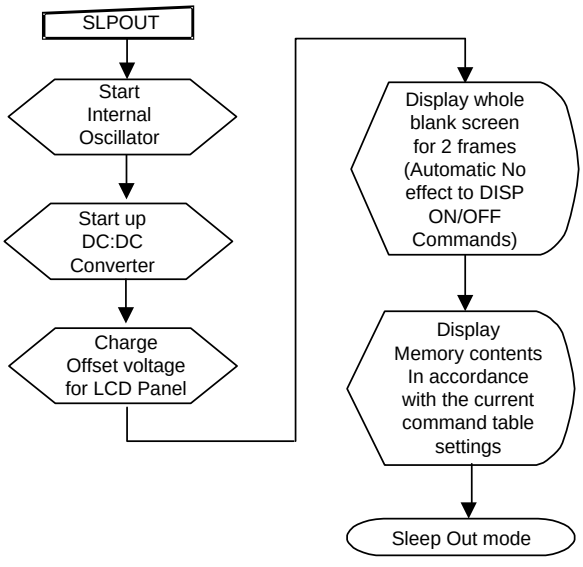
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.

The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



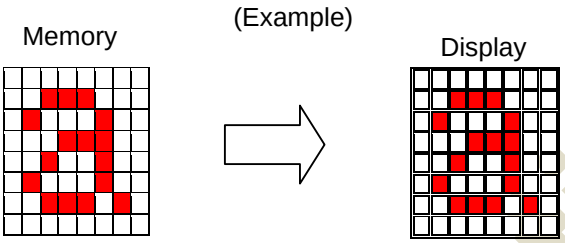
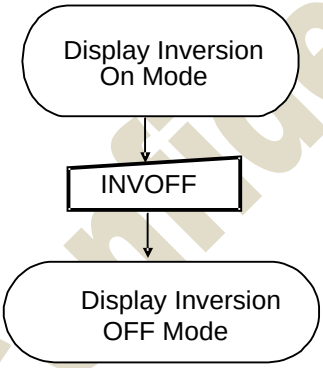
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11.2.17. NORON: Enter Normal Mode (13h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	0	1	0	0	1	1	13
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off. There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.									
Restriction	This command has no effect when Normal Display mode is active.									
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.									

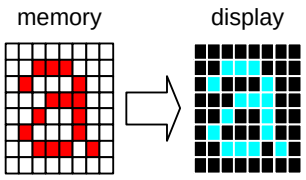
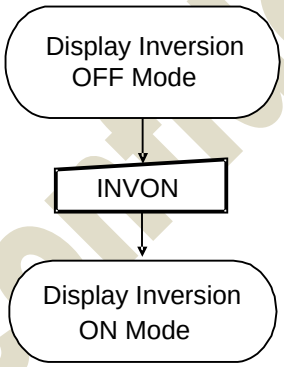
JADARD confidential

11.2.18. INVOFF: Display Inversion Off (20h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	0	0	0	0	20
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. 									
Restriction	This command has no effect when module is already in inversion off mode.									
Flow Chart										

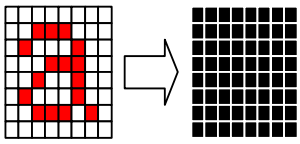
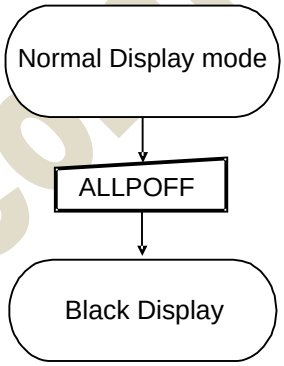
JADARD confidential

11.2.19. INVON: Display Inversion On (21h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	0	0	0	1	21
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in inversion on mode.									
Flow Chart										

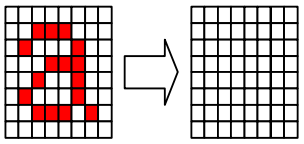
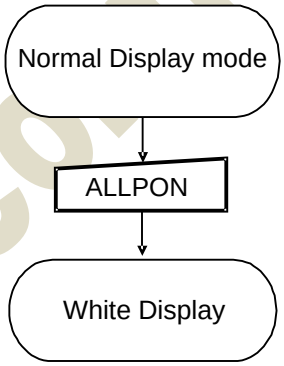
JADARD confidential

11.2.20. ALLPOFF: All Pixel Off (22h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	0	0	1	0	22
Description	This command turns the display panel black in ‘Sleep Out’ –mode and a status of the ‘Display On/Off’ –register can be ‘on’ or ‘off’. This command makes no change of contents of frame memory. This command does not change any other status (Example) memory display  ‘All Pixels On’, ’Normal Display Mode On’ or ’Partial Mode On’ – commands are used to leave this mode. The display panel is showing the content of the frame memory after ‘Normal Display Mode On’ and ‘Partial Mode On’ -commands.									
Restriction	This command has no effect when module is already in All Pixel Off mode.									
Flow Chart										

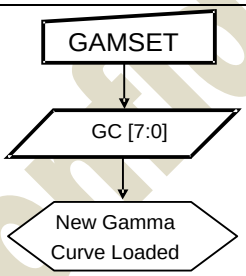
JADARD confidential

11.2.21. ALLPON: All Pixel On (23h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	0	0	1	1	23
Description	This command turns the display panel white in 'Sleep out ' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display  'All Pixels Off', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' –commands.									
Restriction	This command has no effect when module is already in all Pixel On mode.									
Flow Chart										

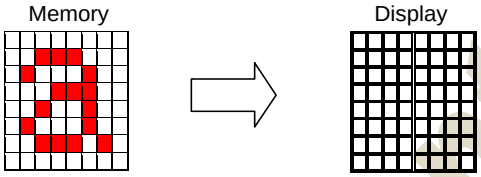
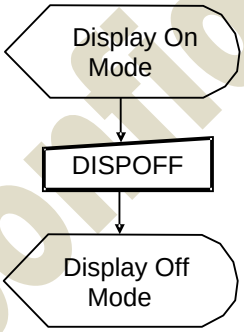
JADARD confidential

11.2.22. GAMSET: Gamma Set (26h)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>26</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:
<table>
<tr><th>GC[7..0]</th><th>Parameter</th><th>Curve selected</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr>
<tr><td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr>
<tr><td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr>
<tr><td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr>
</table>
Note: All other values are undefined.</td></tr>
<tr><td>Restriction</td><td colspan="10">Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</td></tr>
<tr><td>Flow Chart</td><td colspan="10">
</td></tr>
</table>

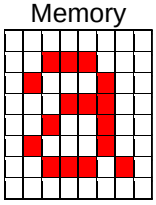
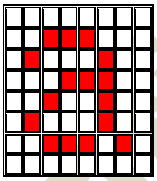
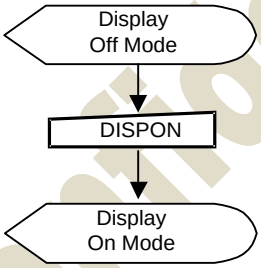
JADARD confidential

11.2.23. DISPOFF: Display Off (28h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	1	0	0	0	28
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Example 									
Restriction	This command has no effect when module is already in display off mode.									
Flow Chart										

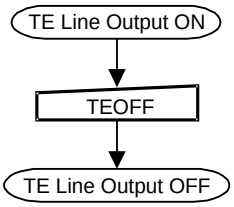
JADARD confidential

11.2.24. DISPON: Display On (29h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	0	1	0	0	1	29
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory  Display 									
Restriction	This command has no effect when module is already in display on mode.									
Flow Chart										

JADARD confidential

11.2.25. TEOFF: Tearing Effect Line OFF (34h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	0	1	0	0	34
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									
Flow Chart										

JADARD confidential

11.2.26. TEON: Tearing Effect Line ON (35h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	0	1	0	1	35
Parameter 1	**W**	X	X	X	X	X	X	X	M	

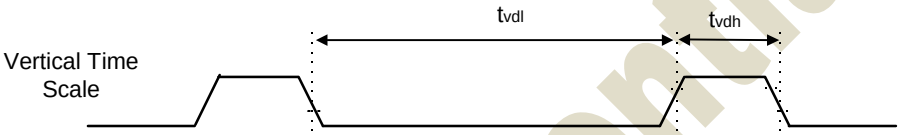
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

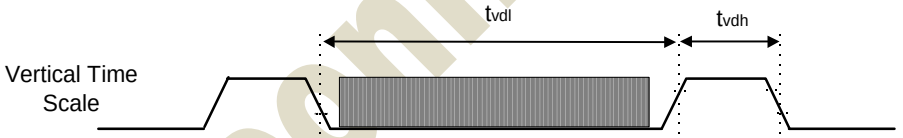
When M=0:

The Tearing Effect Output line consists of V-Blanking information only:



When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

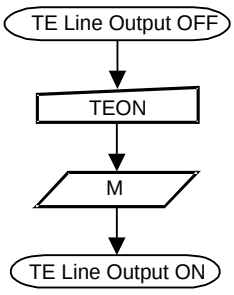


Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

Flow Chart



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11.2.27. MADCTL: Memory Access Control(36h)

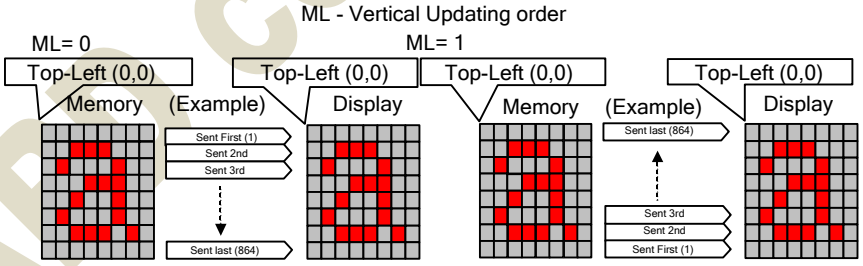
CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	0	1	1	0	36
Parameter 1	**W**	B7	B6	B5	B4	B3	B2	B1	B0	

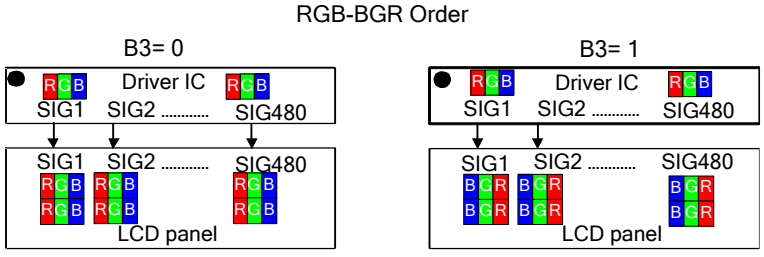
Description

This command defines read/write scanning direction of frame memory.

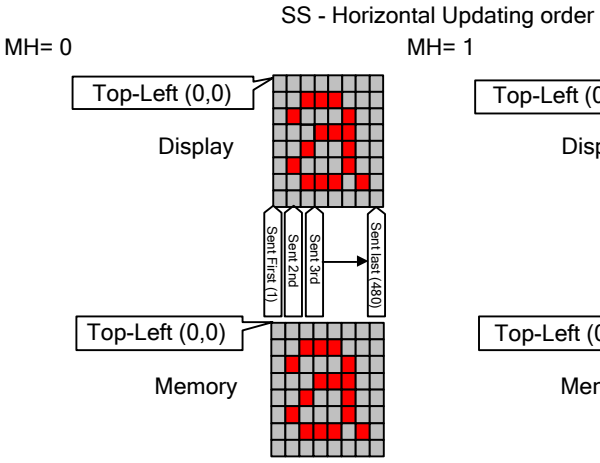
This command makes no change on the other driver status.

Bit	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Vertical ORDER (ML)	LCD vertical refresh direction control
B3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
B2	Horizontal ORDER (MH)	LCD horizontal refresh direction control
B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module
B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module

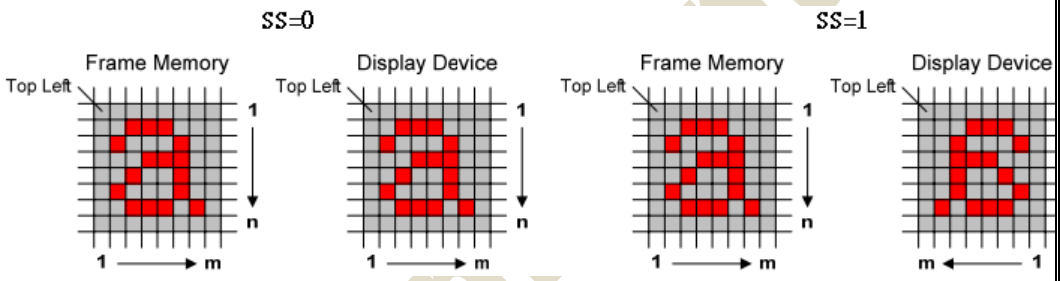




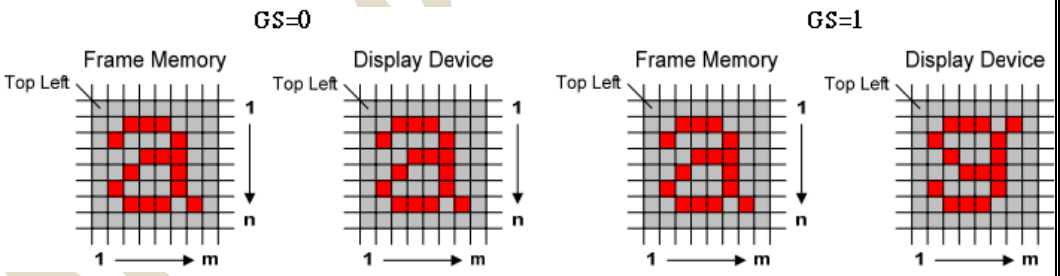
JADARD confidential



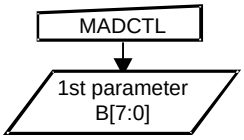
Source scan sequence (SS)



Gate scan sequence (GS)

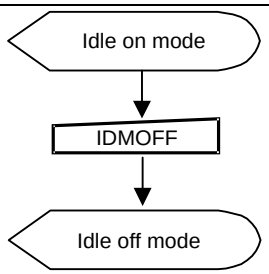


Note: Top-Left (0,0) means a physical memory location.

Restriction	-
Flow Chart	

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11.2.28. IDMOFF: Idle Mode Off (38h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	1	0	0	0	38
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors.									
Restriction	This command has no effect when module is already in idle off mode.									
Flow Chart										

JADARD confidential

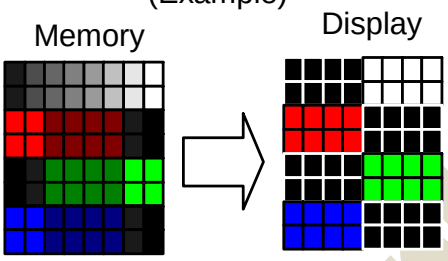
11.2.29. IDMON: Idle Mode On (39h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	1	0	0	0	38

Description

This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

(Example)



Memory contents vs. Display Color

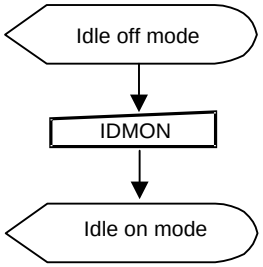
	R7 - R0	G7 - G0	B7 - B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magent	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X=don't care

Restriction

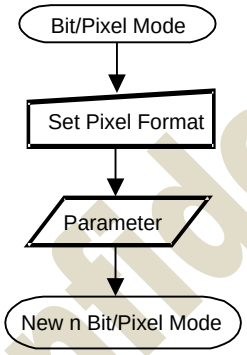
This command has no effect when module is already in idle on mode.

Flow Chart



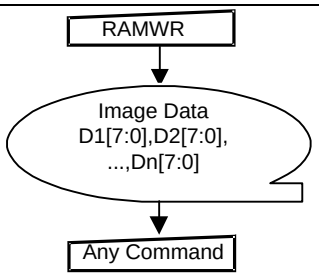
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11.2.30. COLMOD: Interface Pixel Format (3Ah)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	1	0	1	0	3A
Parameter 1	**W**	X	D6	D5	D4	X	D2	D1	D0	
Description	This command is used to define the format of RGB picture data. D6~D4 : DPI Pixel format Definition, fixed @111. D2~D0 : DBI Pixel format Definition, fixed @000. If a particular interface, enter DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module undefined.									
Restriction	There is no visible effect until the Frame Memory is written to.									
Flow Chart										

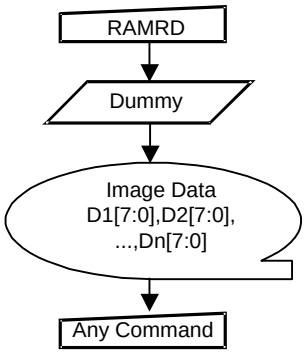
JADARD confidential

11.2.31. Write Memory Continue (3Ch)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	1	1	0	0	3C
Parameter 1	**W**	D1[7:0]								
:	**W**	Dx[7:0]								
Parameter n	**W**	Dn[7:0]								
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous Write Memory Continue (3Ch) or Memory Write Start (2Ch) command. Sending any other command can stop frame Write. If MATCDL MV = 0: Data is written continuing from the pixel location after the write range of the previous Memory Write Start (2Ch) or Write Memory Continue (3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MATCDL MV = 1: Data is written continuing from the pixel location after the write range of the previous Memory Write Start (2Ch) or Write Memory Continue (3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.									
Restriction	In all color modes, there is no restriction on length of parameters. The transfer pixel number must can be divisible by 2.									
Flow Chart										

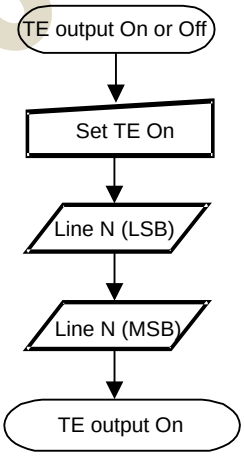
JADARD confidential

11.2.32. RAMRDCON: Read Memory Continue (3Eh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	0	1	1	1	1	1	0	3E
Parameter 1	**R**	D1[7:0]								
:	**R**	Dx[7:0]								
Parameter n	**R**	Dn[7:0]								
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous Read Memory Continue (3Eh) or Memory Read Start (2Eh) command. If MATCDL MV=0: Pixels are read continuing from the pixel location after the read range of the previous Memory Read Start (2Eh) or Read Memory Continue (3Eh). The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MATCDL MV=1: Pixels are read continuing from the pixel location after the read range of the previous Memory Read Start (2Eh) or Read Memory Continue (3Eh). The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.									
Restriction	Regardless of the color mode set in Interface Pixel Format (3Ah), the pixel format returned by Read Memory Continue (3Eh) is always 24-bit so there is no restriction on the length of data. A Memory Read Start (2Eh) should follow a Column Address Set (2Ah), Page Address Set (2Bh) or Memory Access Control (36h) to define the read location. Otherwise, data read with Read Memory Continue (3Eh) is undefined.									
Flow Chart										

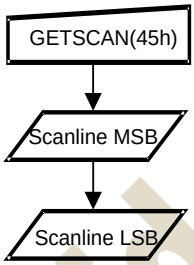
JADARD confidential

11.2.33. TESL: Set Tear Effect Scanline (44h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	0	0	1	0	0	44
Parameter 1	**W**	TELINE[15:8]								
Parameter 2	**W**	TELINE[7:0]								
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only:  **Note**: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.									
Restriction	The command has no effect when Tearing Effect output is already ON.									
Flow Chart	 									

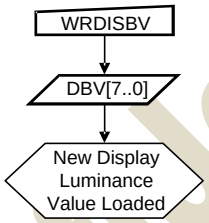
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11.2.34. GETSCAN: Get the Current Scanline (45h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	0	0	1	0	1	45
Parameter 1	**W**	SLN[15:8](8'b0)								
Parameter 2	**W**	SLN[7:0](8'b0)								
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get scanline is undefined.									
Restriction	-									
Flow Chart										

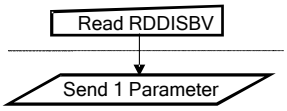
JADARD confidential

11.2.35. WRDISBV: Write Display Brightness (51h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	0	0	1	51
Parameter 1	**W**	DBV[7:0]								
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “Brightness Control Block”.									
Restriction	-									
Flow Chart										

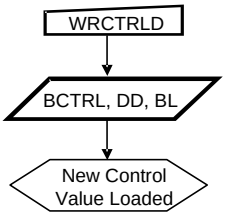
JADARD confidential

11.2.36. RDDISBV: Read Display Brightness Value (52h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	0	1	0	52
Parameter 1	**R**	DBV[7:0]								
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapters: “10.7 Content Adaptive Brightness Control (CABC)” and “11.2.43 WRDISBV: Write Display Brightness (51h)”. DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is ‘0’ when bit BCTRL of “11.2.45 WRCTRLD: Write CTRL Display (53h)” command is ‘0’. DBV[7:0] is manual set brightness specified with “11.2.45 WRCTRLD: Write CTRL Display (53h)” command when bit BCTRL is ‘1’. When bit BCTRL of “11.2.45 WRCTRLD: Write CTRL Display (53h)” command is ‘1’ and bit C1/C0 of “ WRCABC: Write Content Adaptive Brightness Control (55h)” are ‘0’, DBV[7:0] output is the brightness value specified with “11.2.43 WRDISBV: Write Display Brightness (51h)” command.									
Restriction	-									
Flow Chart										

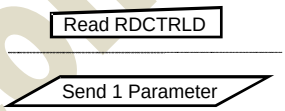
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11.2.37. WRCTRLD: Write CTRL Display (53h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	0	1	1	53
Parameter 1	**W**	x	x	BCTRL	x	DD	BL	x	x	
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don’t care.									
Restriction	-									
Flow Chart										

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11.2.38. RDCTRLD: Read CTRL Value Display (54h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	1	0	0	54
Parameter 1	**R**	0	0	BCTRL	0	DD	BL	0	0	
Description	This command returns ambient light and brightness control values, see chapter: “11.2.45 WRCTRLD: Write CTRL Display (53h)”. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On									
Restriction	-									
Flow Chart										

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11.2.39. WRCABC: Write Content Adaptive Brightness Control (55h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	1	0	1	55
Parameter 1	**W**	IEC[3:0]				X	X	CABC[1:0]		

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter “10.7 Content Adaptive Brightness Control (CABC)”.

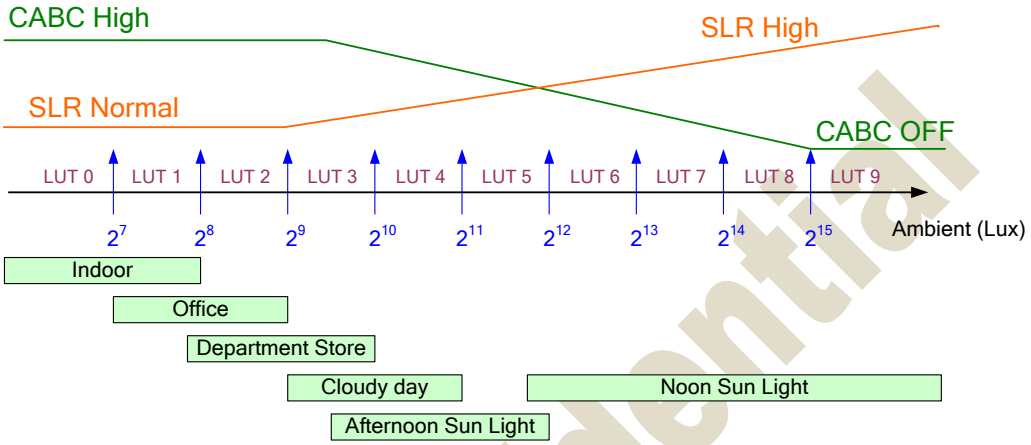
C[1:0]		Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

IEC[3:0] : Image Enhancement Control;

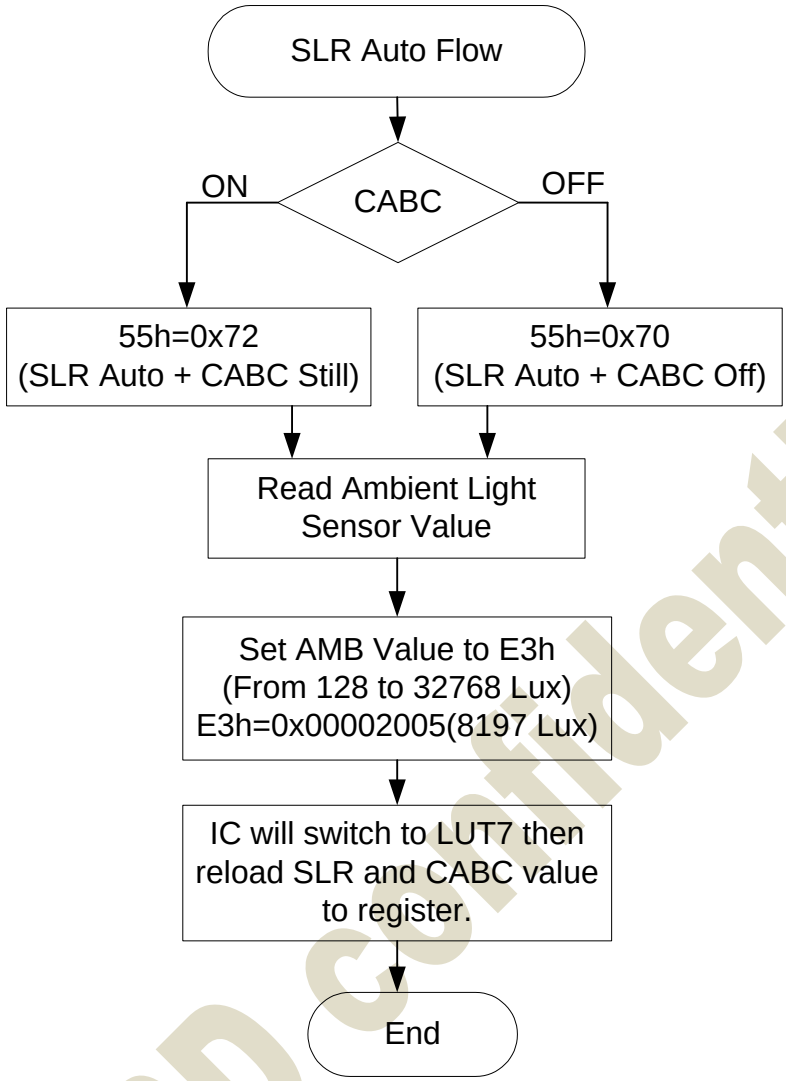
IEC[3:0]				CE	SLR
0	0	0	0	Off	Off
0	0	1	0	Low	Low
0	0	1	1	Low	Medium
0	1	0	0	Off	Low
0	1	0	1	Off	Medium
0	1	1	0	Off	High
0	1	1	1	Low	Auto
1	0	0	0	Low	Off
1	0	0	1	Medium	Off
1	0	1	0	Medium	High
1	0	1	1	High	Off
1	1	0	0	Low	Off
1	1	0	1	Medium	Low
1	1	1	0	High	Medium
others				reserved	

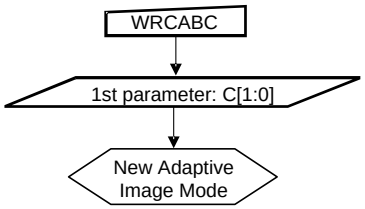
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1. Important: If IEC is set as 0x7 (SLR Auto), CE strength will always set as low.
2. If CABC is enable, CABC _PWM_WT= AMB_CABC_PWM <<2.
3. SLR_STR = AMB_SLRH_STR <<3.
4. In indoor situation, CABC should open to get power saving.



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Restriction	-
Flow Chart	

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11.2.40. RDCABC: Read Content Adaptive Brightness Control (56h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	1	1	0	56
Parameter 1	**R**	IEC[3:0]				X	X	CABC[1:0]		

Description

This command is used to get parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter “10.7 Content Adaptive Brightness Control (CABC)”.

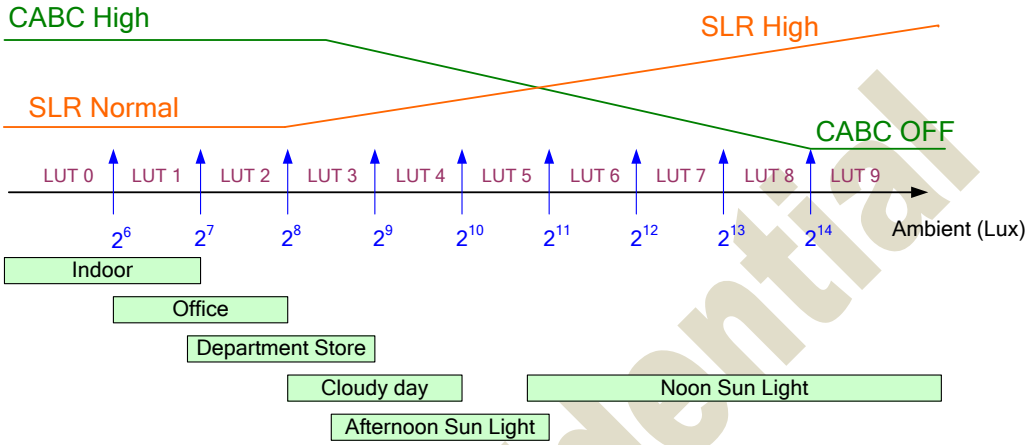
C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

IEC[3:0] : Image Enhancement Control;

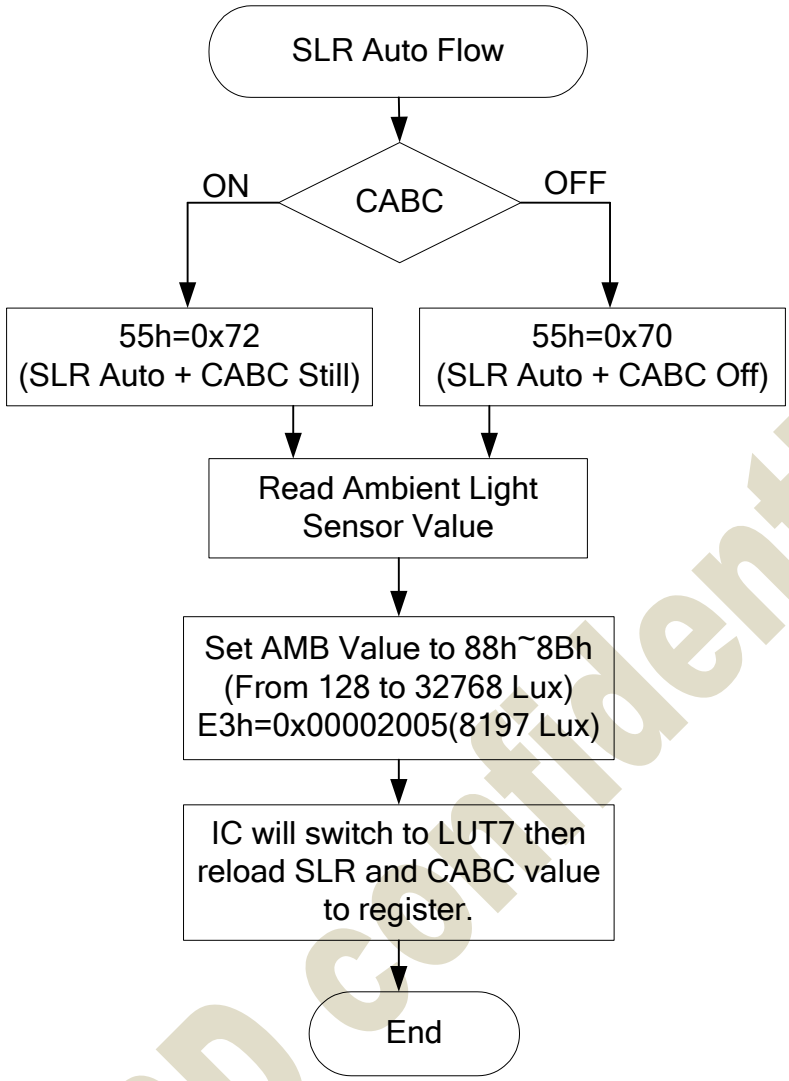
IEC[3:0]				CE	SLR
0	0	0	0	Off	Off
0	0	1	0	Low	Low
0	0	1	1	Low	Medium
0	1	0	0	Off	Low
0	1	0	1	Off	Medium
0	1	1	0	Off	High
0	1	1	1	Low	Auto
1	0	0	0	Low	Off
1	0	0	1	Medium	Off
1	0	1	0	Medium	High
1	0	1	1	High	Off
1	1	0	0	Low	Off
1	1	0	1	Medium	Low
1	1	1	0	High	Medium
others				reserved	

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1. Important: If IEC is set as 0x7 (SLR Auto), CE strength will always set as low.
2. If CABC is enable, CABC _PWM_WT= AMB_CABC_PWM <<2.
3. SLR_STR = AMB_SLRH_STR <<3.
4. In indoor situation, CABC should open to get power saving.



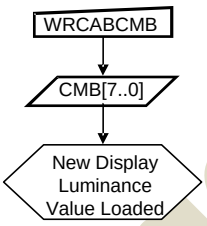
JADARD confidential



Restriction	-
Flow Chart	Read RDCABC Send 1 Parameter

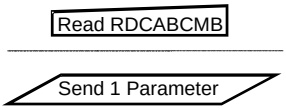
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11.2.41. WRCABCMB: Write CABC Minimum Brightness (5Eh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	1	1	1	0	5E
Parameter 1	**W**	CMB[7:0]								
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter " 10.7.3 Minimum brightness setting of CABC function".									
Restriction	-									
Flow Chart										

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11.2.42. RDCABCMB: Read CABC Minimum Brightness (5Fh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	0	1	0	1	0	1	1	1	5F
Parameter 1	**R**	CMB[7:0]								
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “10.7.3 Minimum brightness setting of CABC function”									
Restriction	-									
Flow Chart										

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11.2.43. RDDDB: Read DDB Start (A1h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	0	1	0	0	0	0	1	A1
Parameter 1	**R**	X	X	X	X	X	X	X	X	
:	**R**	X	X	X	X	X	X	X	X	
Parameter n	**R**	X	X	X	X	X	X	X	X	

Description

This command reads identifying and descriptive information from the peripheral.
This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data.

The format of returned data is as follows:
Parameter 1: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.

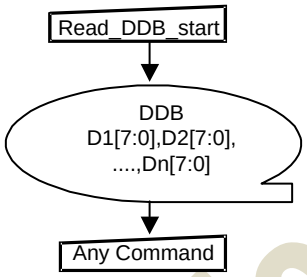
Parameter 2: MS (most significant) byte of Supplier ID.

Parameter 3: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.

Parameter 4: MS (most significant) byte of Supplier Elective Data
Parameter 5: single-byte *Escape or Exit Code* (EEC). The code is interpreted as follows:
- FFh - Exit code – there is no more data in the Descriptor Block
- 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard)
- Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in *MIPI Alliance Standard for Device Descriptor Block (DDB)*.

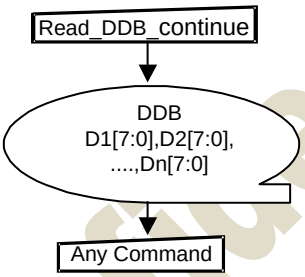
DDBs may contain many more data fields providing information about the peripheral.
In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command RDDDB: Read DDB Start (A1h) from host processor to peripheral, which includes the bus turn-around token.
The peripheral then takes control of the bus and returns the requested data. The peripheral response to RDDDB: Read DDB Start (A1h) is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command.
The response to a RDDDB: Read DDB Start (A1h)command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a RDDDBCON: Read DDB

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	Continue (A8h) command to access the next portion of the DDB. A RDDDBCON: Read DDB Continue (A8h) command begins the next read at the location following the last byte of the previous data read from the DDB. Subsequent RDDDBCON: Read DDB Continue (A8h) commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any **Read DDB xxx** command.
Restriction	-
Flow Chart	

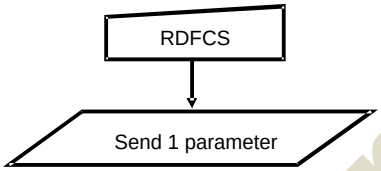
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11.2.44. RDDDBCON: Read DDB Continue (A8h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	0	1	0	1	0	0	0	A8
Parameter 1	**R**	X	X	X	X	X	X	X	X	
:	**R**	X	X	X	X	X	X	X	X	
Parameter n	**R**	X	X	X	X	X	X	X	X	
Description	A RDDDB: Read DDB Start (A1h) command should be executed at least once before a RDDDBCON: Read DDB Continue (A8h) command to define the read location. Otherwise, data read with a RDDDBCON: Read DDB Continue (A8h) command is undefined.									
Restriction	-									
Flow Chart										

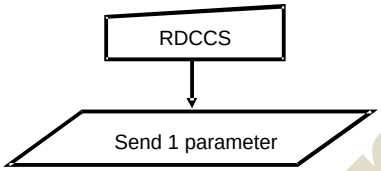
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11.2.45. RDFCS: Read First Checksum (AAh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	0	1	0	1	0	1	0	AA
Parameter 1	**R**	FCS7:0]								
Description	This command returns the first checksum what has been calculated from Nokia's area registers and the frame memory after the write access to those registers and/or frame memory has been done.									
Restriction	-It will be necessary to wait 150ms after there is the last write access on Nokia area registers before there can read this checksum value.									
Flow Chart										

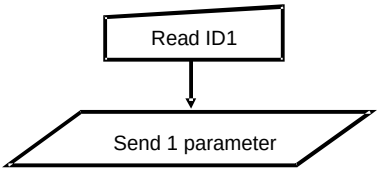
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11.2.46. RDCCS: Read Continue Checksum (AFh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	0	1	0	1	1	1	1	AF
Parameter 1	**R**	CCS[7:0]								
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from Nokia area registers and the frame memory after the write access to those registers and/or frame memory has been done.									
Restriction	-it will be necessary to wait 300ms after there is the last write access on Nokia area registers before there can read this checksum value in the first time.									
Flow Chart										

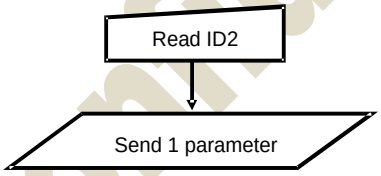
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11.2.47. RDID1: Read ID1 (DAh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	1	0	1	1	0	1	0	DA
Paameter 1	**R**	module's manufacturer[7:0]								
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.									
Restriction	-									
Flow Chart										

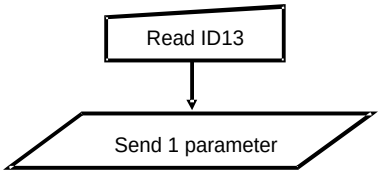
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11.2.48. RDID2: Read ID2 (DBh)

<table>
<tr><th>CMD/PAs</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>W</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DB</td></tr>
<tr><td>Parameter 1</td><td>R</td><td colspan="8">LCD module/driver version [7:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="10">This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:
<table>
<tr><th>ID Byte Value V[7:0]</th><th>Version</th><th>Changes</th></tr>
<tr><td>80h</td><td></td><td></td></tr>
<tr><td>81h</td><td></td><td></td></tr>
<tr><td>82h</td><td></td><td></td></tr>
<tr><td>83h</td><td></td><td></td></tr>
<tr><td>84h</td><td></td><td></td></tr>
<tr><td>85h</td><td></td><td></td></tr>
</table>
X= Don't care</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Flow Chart</td><td colspan="10">
</td></tr>
</table>

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11.2.49. RDID3: Read ID3 (DCh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	**W**	1	1	0	1	1	1	0	0	DC
Parameter 1	**R**	LCD module/driver ID[7:0]								
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.									
Restriction	-									
Flow Chart										

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12. Electrical Specifications

12.1. Absolute maximum ratings

Symbol	Parameter	Unit	Value	Note
VCCH/VDDI/VDDI_PLL	Interface Supply Voltage	V	-0.3 to +1.95	Note(3),(4)
VSP	Positive Voltage input	V	-0.3 to +6.6	Note(8)
VSN	Negative Voltage input	V	0 to -6.6	Note(9)
VGH	Power Supply Voltage	V	-0.3 to +20	Note(10)
VGL	Power Supply Voltage	V	0 to -18	Note(11)
Top	Operating Temperature	°C	-40 to +85	Note(12)
Tstg	Storage Temperature	°C	-55 to +110	Note(13)

Note: (1) Permanent device damage may occur if absolute maximum conditions are exceeded.
(2) Functional operation should be restricted to the conditions described under DC Characteristics.
(3) VCCD/IOVCC, VSSD must be maintained.
(4) To make sure VCCD/IOVCC ≥ VSSD.
(5) To make sure VCIP≥ AVSS.
(6) To make sure VCI≥ AVSS.
(7) To make sure VCCH ≥ VSSH.
(8) To make sure AVDD ≥ AVSS.
(9) To make sure AVSS ≥ AVEE
(10) To make sure VGH ≥ AVSS.
(11) To make sure AVSS ≥ VGL
VGH +|VGL| < 32V
(12) For die and wafer products, specified up to +85℃.
(13) This temperature specifications apply to the COG package.

Table 12.1: Absolute maximum ratings

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12.2. DC characteristics

(T_A=-40 ~ 85 °C)

Parameter		Symbol	Spec.			Unit	Note
			Min.	Typ.	Max.		
Input high level voltage		V_{IH}	0.7VDDI	-	VDDI	V	1.65V≦VDDI≦1.95V
Input low level voltage		V_{IL}	0	-	0.3VDDI	V	
Output high level voltage		V_{OH}	VDD-0.2V	-	VDDI	V	1.65V≦VDDI≦1.95V
Output low level voltage		V_{OL}	0	-	0.2V	V	
Input leakage current		I_{L1}	-1	-	+1	uA	-
VDDI output voltage		VDDI	1.65	-	1.95	V	-
VCCH output voltage		VCCH	1.65	-	1.95	V	-
VSP output voltage		VSP	4.5	-	6.2	V	-
VSN output voltage		VSN	-6.2	-	-4.5	V	-
VDDD output voltage		VDDD	1.19	1.32	1.45	V	-
VDDH output voltage		VDDH	1.19	1.32	1.45	V	-
VGMP output voltage		VGMP	3.1	4.8	6	V	-
VGMN output voltage		VGMN	-6	-4.8	-3.1	V	-
VCOM output voltage		VCOM	-3	-1	-0.08	V	-
VCI output voltage		VCI	2.3	2.6	3	V	-
VCL output voltage		VCL	-3	-2.6	-2.3	V	-
VGH output voltage		VGH	VGHO+1	16	20	V	-
VGL output voltage		VGL	-15	-12	-6.7	V	-
VGHO output voltage		VGHO	7.3	15	VGH-1	V	-
VGLO output voltage		VGLO	VGL+1	-10	-5.3	V	-
TPVDD output voltage		TPVDD	4.6	4.7	4.9	V	-
VPP output voltage (OTP power)		VPP	8	8.25	8.5	V	-
Source output current	VSO=5V at positive, VOUT=4V	IOSH	-	-	200	uA	-
	VSO=-5V at negative, VOUT=-4V	IOSL	-	-	200	uA	-
Source output offset deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255	-	50	-	-	mV	Graycode 0 limit: GP23R>GND+0.4V GN23R<GND-0.4V
	Graycode = 15 ~ 31 Graycode = 208 ~ 240	-	40	-	-	mV	
	Graycode = 32 ~ 207	-	30	-	-	mV	
VDDI current consumption	Standby mode	-	-	-	450	uA	VDD1 = 1.8V VSP = 5.5V VSN = -5.5V TA = 25℃
VSP current consumption		-	-	-	150	uA	
VSN current consumption		-	-	-	55	uA	
VDDI current consumption	Normal mode		-	-	TBD	uA	VDD1 = 1.8V VSP = 5.5V VSN = -5.5V TA = 25℃
VSP current consumption			-	-	TBD	uA	
VSN current consumption			-	-	TBD	uA	
VOTP operation current		VOTP	-	-	8	mA	TA = 25℃
Oscillator tolerance		△OSC	-3	-	3	%	TA = 25℃

Table 12.2: DC characteristic

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12.3. AC characteristics

12.3.1. Reset input timings

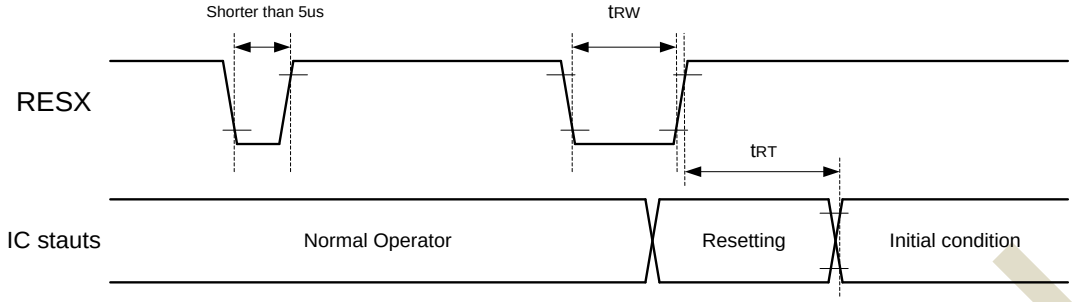


Figure 12.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	20	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

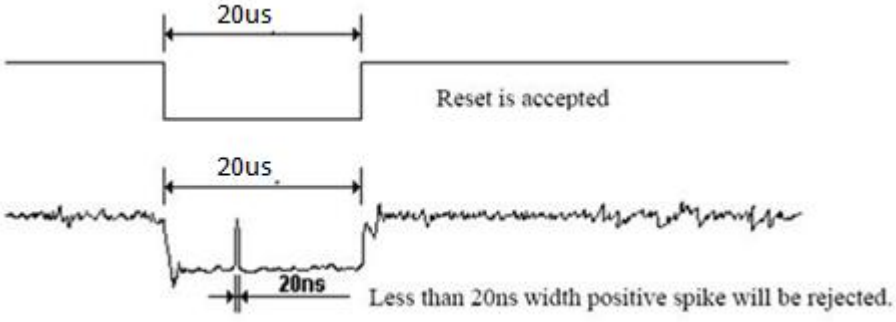
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

Table 12.3: Reset timings

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12.3.2.DSI D-PHY electronic characteristics

The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 13.2 shows the complete set of electronic functions required for a fully featured PHY transceiver.

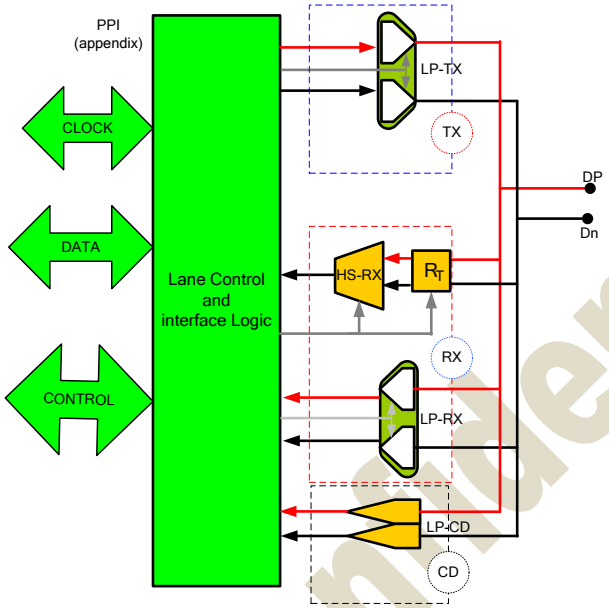


Figure 12.2: Electronic functions of a D-PHY transceiver

Figure13.3 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

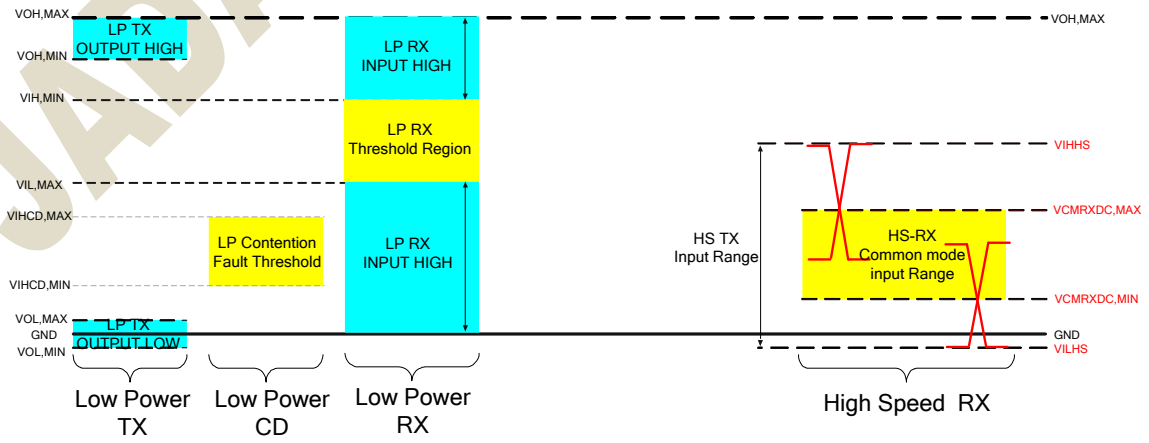


Figure 12.3: HS and LP signal levels

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The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 12.4: LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

Table 12.5: LP-TX AC Specifications

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The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 13.4 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.

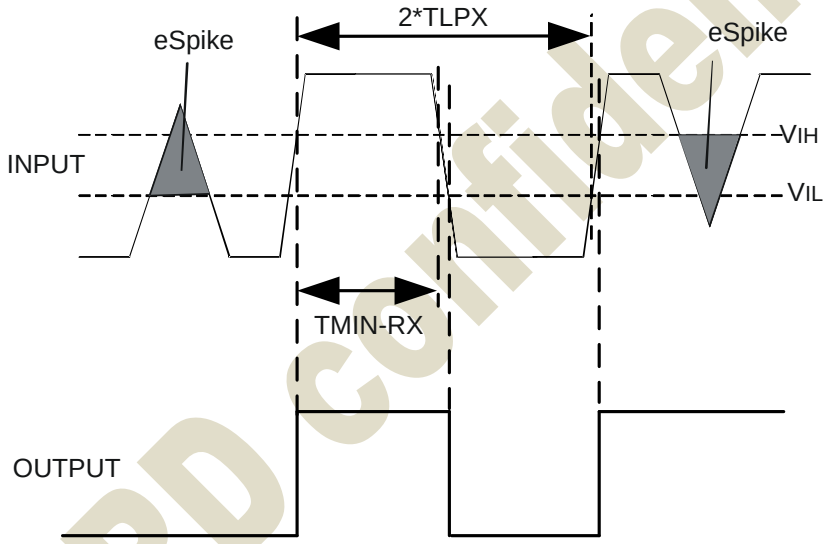


Figure 12.4: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Table 12.6: LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

Table 12.7: LP-RX AC Specifications

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Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.

2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 12.8: Contention Detector DC Specifications

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High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 12.9: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 12.10: HS Receiver AC Specifications

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High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.

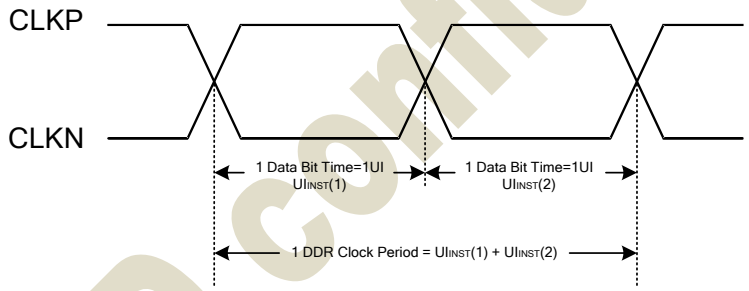


Figure 12.5: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

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The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Base on resolution 800x1280, HS=20, HBP=40, HFP=40, VS=2, VBP=8, VFP=20 and frame rate = 60HZ.
- The total bit rate is about **850Mbps** of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.**(The max. limitation lane speed=1Gbps/ lane)**

- The total bit rate is about **1.7Gbps** of 2 data lane 24-bit data format/ 1.275Gbps of 2 data lane 18-bit data format/1.133Gbps of 2 data lane 16-bit data format.**(The max. limitation lane speed=1Gbps/ lane)**

- The total bit rate is **1.7Gbps** of 3 data lane 24-bit data format/ 1.275G bps of 3 data lane 18-bit data format/1.133Gbps of 3 data lane 16-bit data format.**(The max. limitation lane speed=800Mbps/ lane)**

- The total bit rate is **1.7Gbps** of 4 data lane 24-bit data format/ 1.275Gbps of 4 data lane 18-bit data format/ 560Mbps of 4 data lane 16-bit data format.**(The max. limitation lane speed=600Mbps/ lane)**

Table 12.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.
The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.
All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.
Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

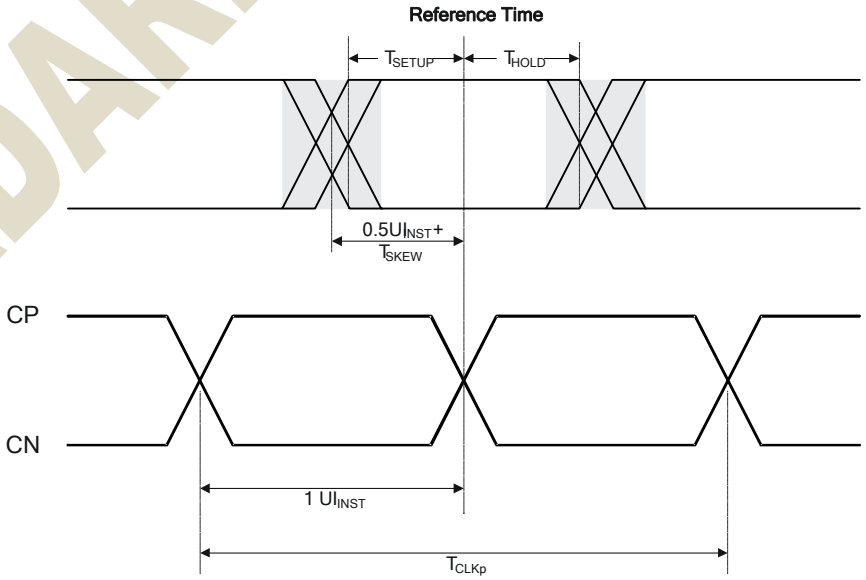


Figure 12.6: Data to Clock Timing Definitions

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Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Table 12.12: Data to Clock Timing Specifications

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Burst Mode Data Transmission

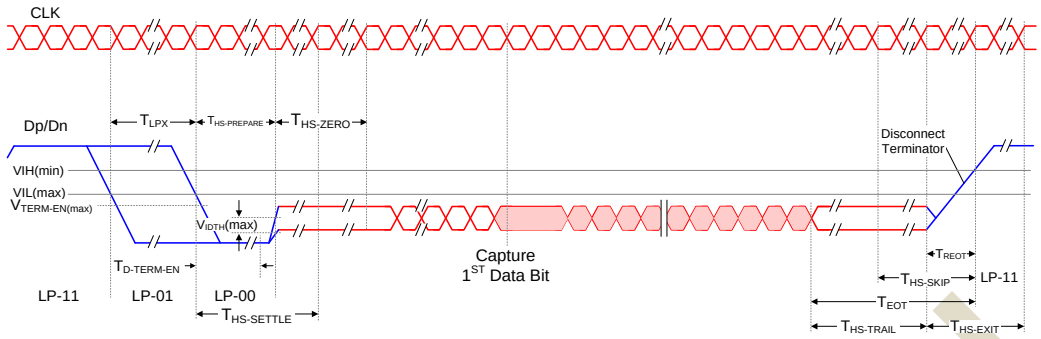


Figure 12.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

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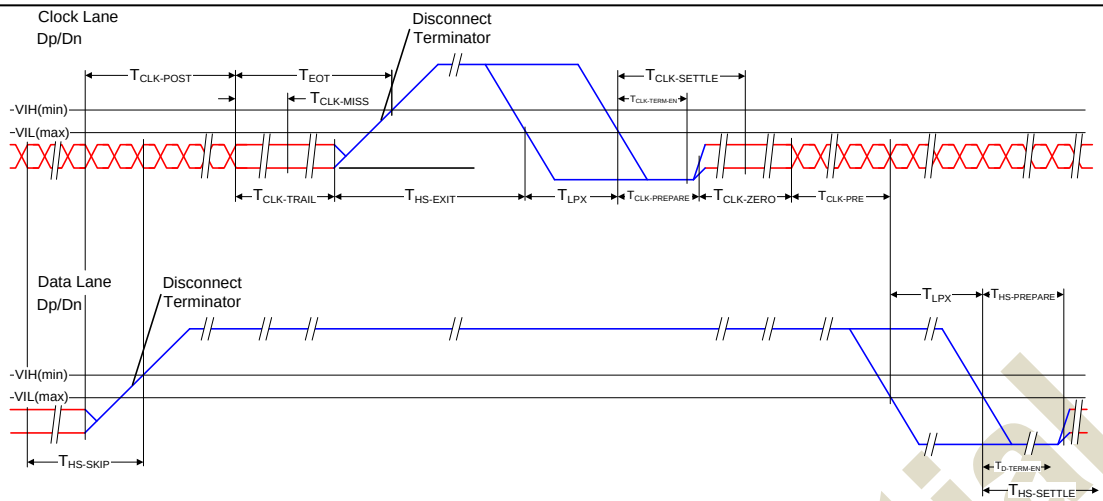


Figure 12.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

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12.3.3.Timings for DSI Video mode

Vertical Timings

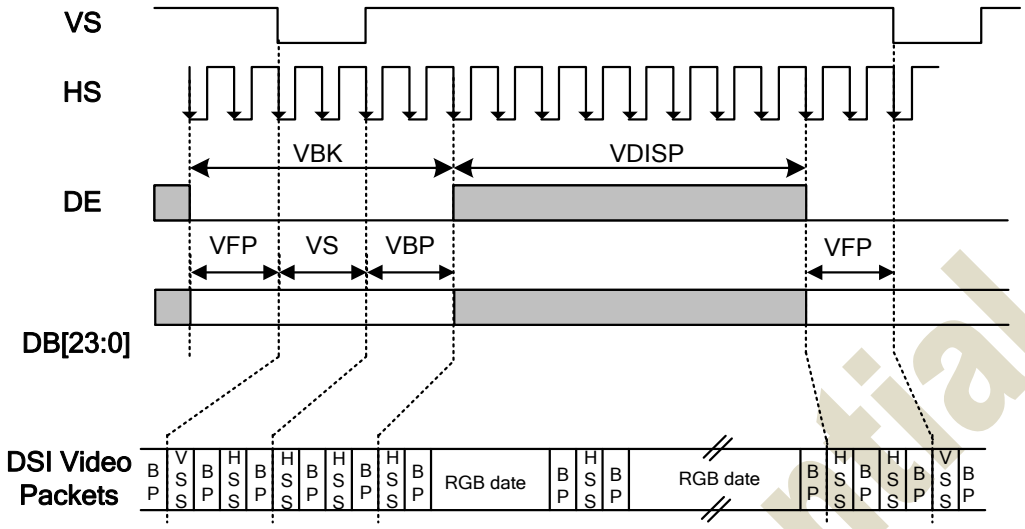


Figure 12.9: Vertical Timings for DPI I/F

Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	4	200 Note(1)	Line
Vertical front porch	VFP	-	4	20	200	Line
Vertical back porch	VBP	-	2	10	200 Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	8	34	250	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Table 12.13: Vertical Timings for RGB I/F

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Horizontal Timings

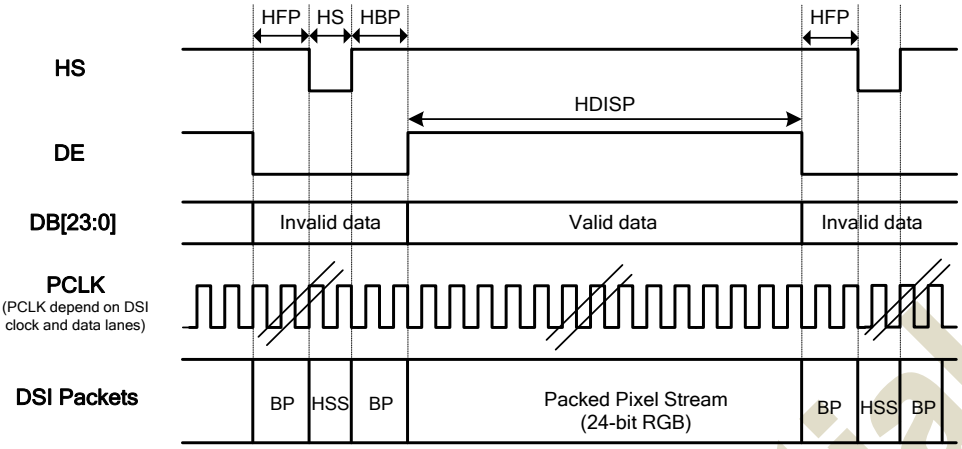


Figure 12.10: Horizontal Timing for DSI Video mode I/F

Resolution=800x1280 (T_A=25°C, IOVCC=1.8V, VCIP=VCI=VCCH=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	18	-	DCK
Horizontal back porch	HBP	-	5	18	-	DCK
Horizontal front porch	HFP	-	5	18	-	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	54 (Note1)	-	DCK
Horizontal active area	HDISP	-	-	800	-	DCK
Pixel Clock	PCLK	-	63.06 (Note2)	67.33 (Note2)	-	MHz

Note 1: HS+HBP > 0.5us.
Note 2: Pixel Clock = (HBLK+HDISP) * (VBK+VDISP) * Frame rate, Frame rate=60Hz.

Table 12.14: Horizontal Timings for DSI Video mode I/F

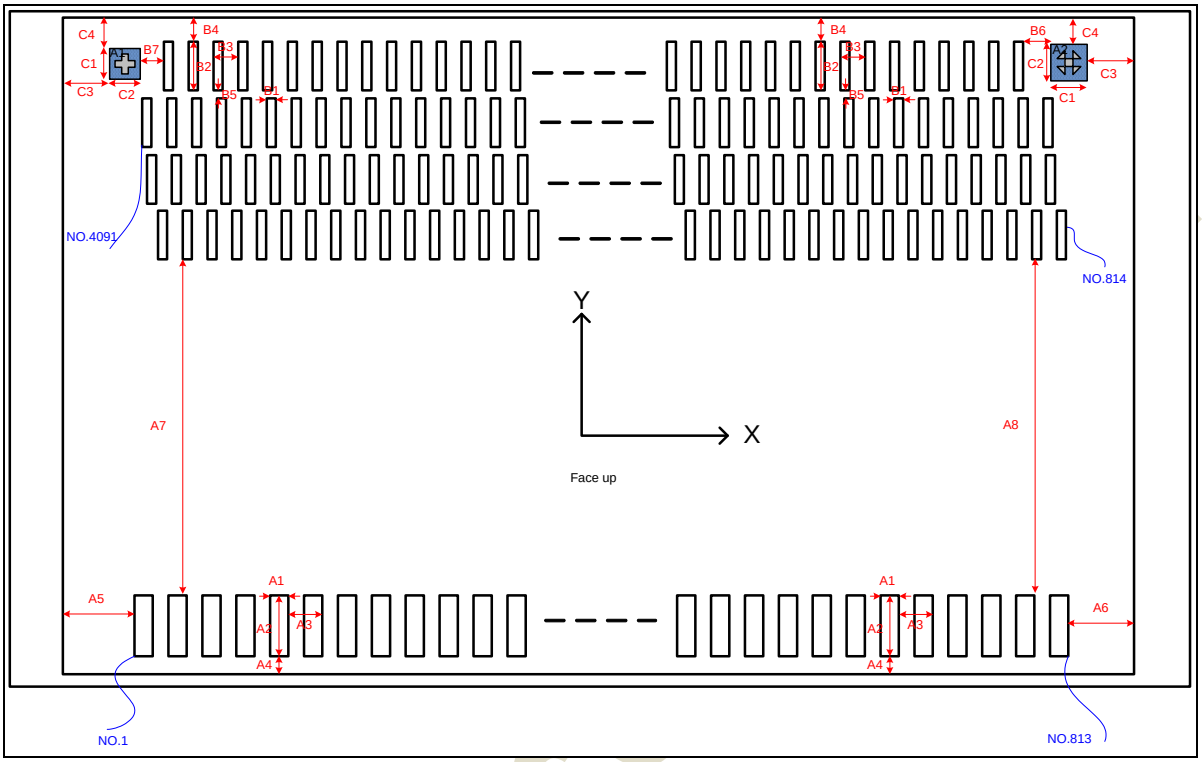
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13. Chip information

13.1. PAD assignment

IC chip size: 32233um*1155um (Include Scribe-Line and Seal-Ring)

Overview (Simple view)



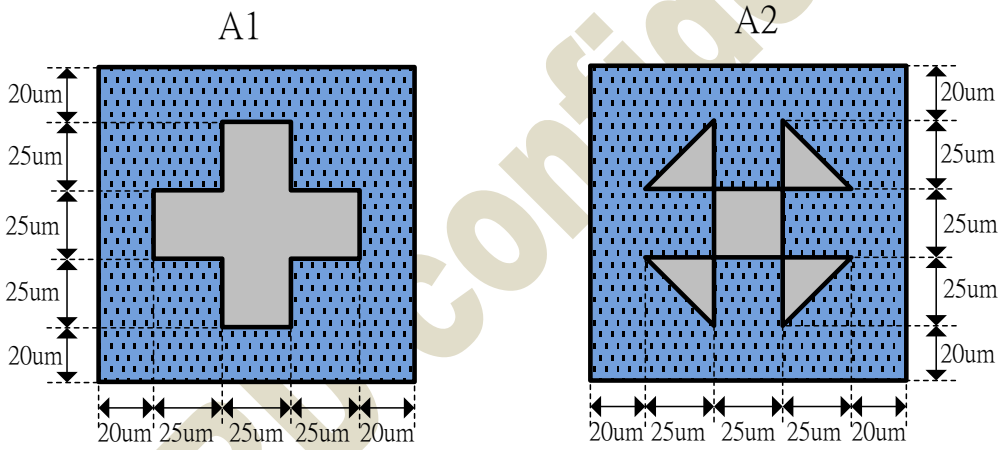
Pad with temperature compensation (Pad with Shift)

INPUT PAD (NO.1 ~ NO.813)			OUTPUT PAD (NO814 ~ NO.4091)			ARMARK		
Symbol	Size	Tolerance	Symbol	Size	Tolerance	Symbol	Size	Tolerance
A1	24	±3	B1	15	±3	C1	115	±3
A2	65	±3	B2	100	±3	C2	115	±3
A3	39	±3	B3	38.8	±3	C3	89.6	±3
A4	98	±3	B4	95	±3	C4	60	±3
A5	269	±3	B5	20	±3			
A6	280	±3	B6	82.85	±3			
A7	437	±3	B7	34.35	±3			

Pad without temperature compensation (Pad without Shift)

INPUT PAD (NO.1 ~ NO.813)			OUTPUT PAD (NO814 ~ NO.4091)			ARMARK		
Symbol	Size	Tolerance	Symbol	Size	Tolerance	Symbol	Size	Tolerance
A1	24	±3	B1	15	±3	C1	115	±3
A2	65	±3	B2	100	±3	C2	115	±3
A3	39	±3	B3	38.8	±3	C3	89.6	±3
A4	98	±3	B4	95	±3	C4	60	±3
A5	265	±3	B5	20	±3			
A6	276	±3	B6	78.85	±3			
A7	437	±3	B7	30.35	±3			

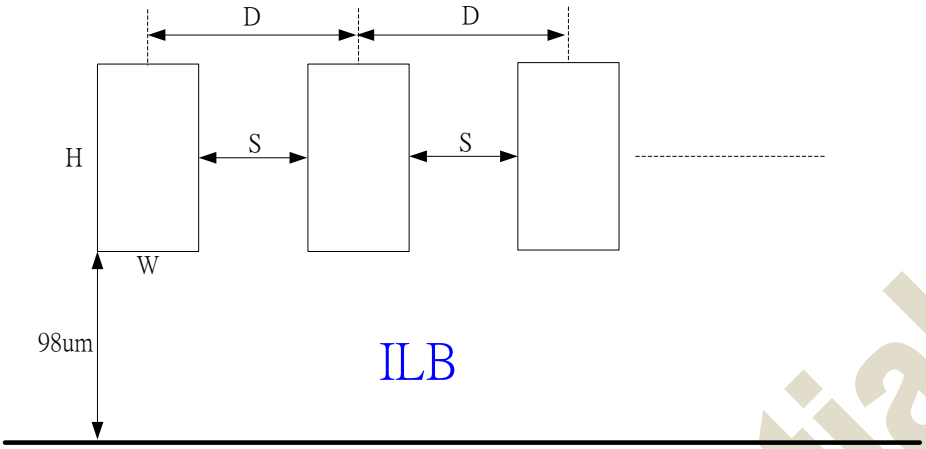
Alignment mark



Symbol	Name	X-axis	XY-axis	W	H
A1	Alienment_Mark	-15969.4	460	115	115
A2	Alienment_Mark	15969.4	460	115	115

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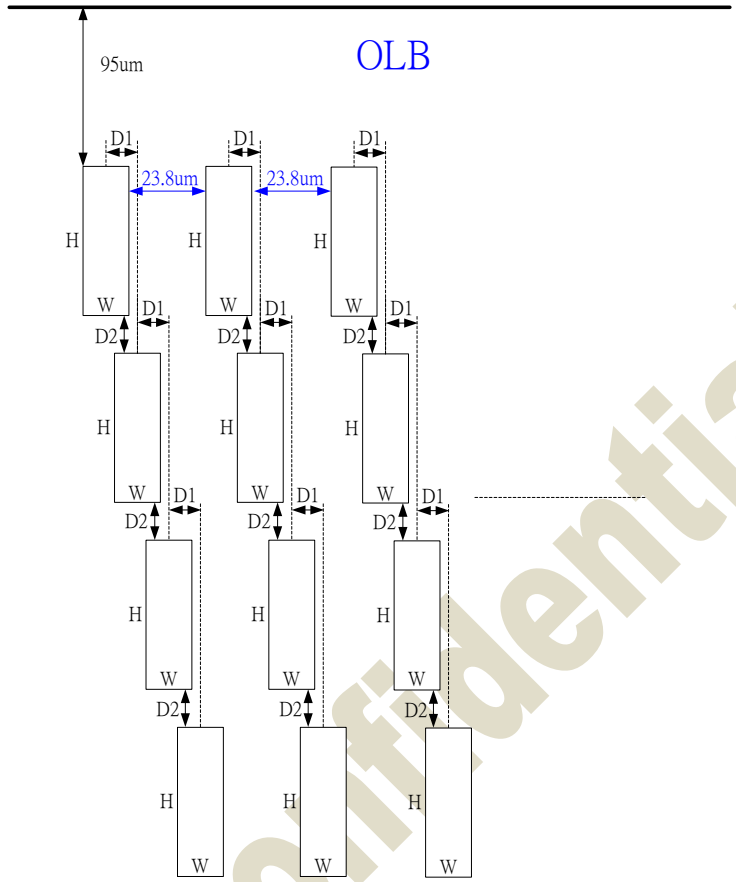
Input Pad: NO.1~NO.813



Description	Symbol	Unit (um)
Height	H	65
Width	W	24
Pitch	D	39
Space	S	15

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Output Pad: NO.814~NO.4091



Description	Symbol	Unit (um)
Height	H	100
Width	W	15
Pitch	D1	9.7
Distance	D2	20

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14. Ordering Information

TBD

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