PRODUCT SPECIFICATION

CDTECH Model: **S101QWX98NP-FC104-AF**

CUSTOMER Model: **119.03.0179**

Description: **10.1” a-Si TFT with Touch sensor IN Display with LENS**

Version: **1.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2025.10.23	2025.10.23	2025.10.23

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
1.0	2025-10-23	First Release	-

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1. General Specifications

1.1 LCM General Information

Item	Specification	Unit
LCD Size	10.1	inch
Number of Pixels	800 (H) RGB x 1280 (V)	pixels
Display Mode	Normally Black	-
Viewing Direction	Free	-
Interface	MIPI	-
Display Colors	16.7M	colors
Outline Dimension	152.96 (H) x 238.58 (V) x 3.77 (D)	mm
Active Area	135.36 (H) x 216.58 (V)	mm
Pixel Pitch	0.1692 (H) x 0.1692 (V)	mm
Driver IC	JD9366TC	-
Operation Temperature	-10~60	℃
Storage Temperature	-20~70	℃

Note1:Requirements on environmental protection RoHS compliant.

1.2 Touch Panel Information

Item	Specification
Touch Structure	-
Bonding Type with LCM	OCA Optical Bonding
Driver IC	-
Interface	I²C
Touch Count Max	TBD Points
Surface treatment	-
Surface hardness	6H
Origin of coordinate	Top Right Corner

Note1:Requirements on environmental protection RoHS compliant.

2. Absolute Maximum Ratings

Item	Symbol	MIN.	MAX.	Unit	Note
Analog Supply voltage	LCM_VDD	-0.3	1.95	V	Note 1
Power Voltage	AVDD(+5.8V)	-0.3	6.6	V	
	AVDD(-5.8V)	-6.6	0	V	

Note 1:Permanent damage may occur to the LCD module if beyond this specification.
Functional operation should be restricted to the conditions described under normal operating conditions.

3. Elecrical Characteristics

3.1 Recommended Operating Condition for TFT LCD

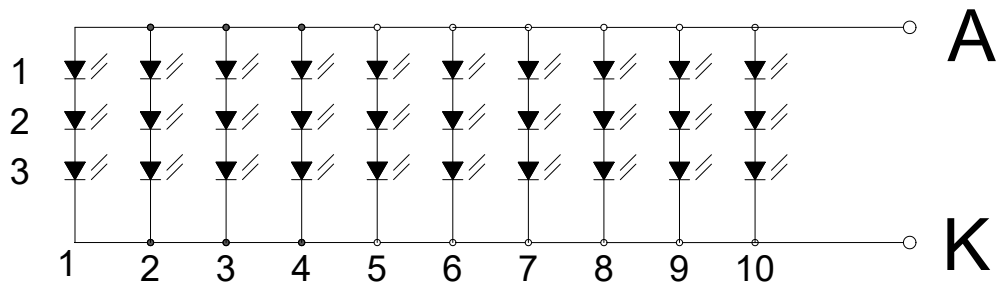
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	LCM_VDD	1.65	1.8	1.95	V	
Analog supply current	I_{LCM_VDD}	-	TBD	-	mA	LCM_VDD=1.8V
Power supply for LCD	AVDD(+5.8V)	4.5	5.8	6.0	V	
	AVDD(-5.8V)	-6.0	-5.8	-4.5	V	
Logic input voltage	VIH	0.7*LCM_VDD	-	LCM_VDD	V	
	VIL	GND	-	0.3*LCM_VDD	V	

3.2 Recommended Driving Condition for Backlight

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Driving Current	I_F	-	200	-	mA	
Driving Voltage	V_F	8.4	-	9.6	V	
Power consumption	W_{BL}	1.68	-	1.92	W	
LED Life-Time	N/A	-	30,000	-	Hours	Ta=25℃ Note 1

Note 1:LED lifetime is defined as the module brightness decay 50% of original brightness at Ta=25 degree, typical current.

Note 2:LED circuit :



4. Interface Pin Assignment

4.1 LCM Pin Assignment

No.	Symbol	Description
1	LCM_VDD(1.8V)	Power supply(1.8V)
2	GND	Ground
3	LCM_VDD(1.8V)	Power supply(1.8V)
4	D0P	MIPI Positive data signal(+)
5	LCM_VDD(1.8V)	Power supply(1.8V)
6	D0N	MIPI Negative data signal(-)
7	ID	LCM_ID
8	GND	Ground
9	LEDA	Power for LED backlight (Anode)
10	D1P	MIPI Positive data signal(+)
11	LEDA	Power for LED backlight (Anode)
12	D1N	MIPI Negative data signal(-)
13	LEDK	Power for LED backlight (Cathode)
14	GND	Ground
15	LEDK	Power for LED backlight (Cathode)
16	CLKP	MIPI Positive clock signal(+)
17	AVDD(+5.8V)	Positive Voltage for Analog Circuit(+5.8V)
18	CLKN	MIPI Negative clock signal(-)
19	AVDD(-5.8V)	Negative Voltage for Analog Circuit(-5.8V)
20	GND	Ground
21	GND	Ground
22	D2P	MIPI Positive data signal(+)
23	GND	Ground
24	D2N	MIPI Negative data signal(-)

25	GND	Ground
26	GND	Ground
27	CTP-EINT(1.8V)	Interrupt signal for Touch(1.8V)
28	D3P	MIPI Positive data signal(+)
29	GND	Ground
30	D3N	MIPI Negative data signal(-)
31	CTP-RST(1.8V)	Reset Pin for Touch(1.8V)
32	GND	Ground
33	CTP-SCL(1.8V)	I2C clock input for Touch(1.8V)
34	GND	Ground
35	CTP-SDA(1.8V)	I2C data input and output for Touch(1.8V)
36	RESET(1.8V)	Global reset pin(1.8V)
37	NC	No connection
38	GND	Ground
39	NC	No connection

5. Interface Characteristics

5.1 Power Sequence

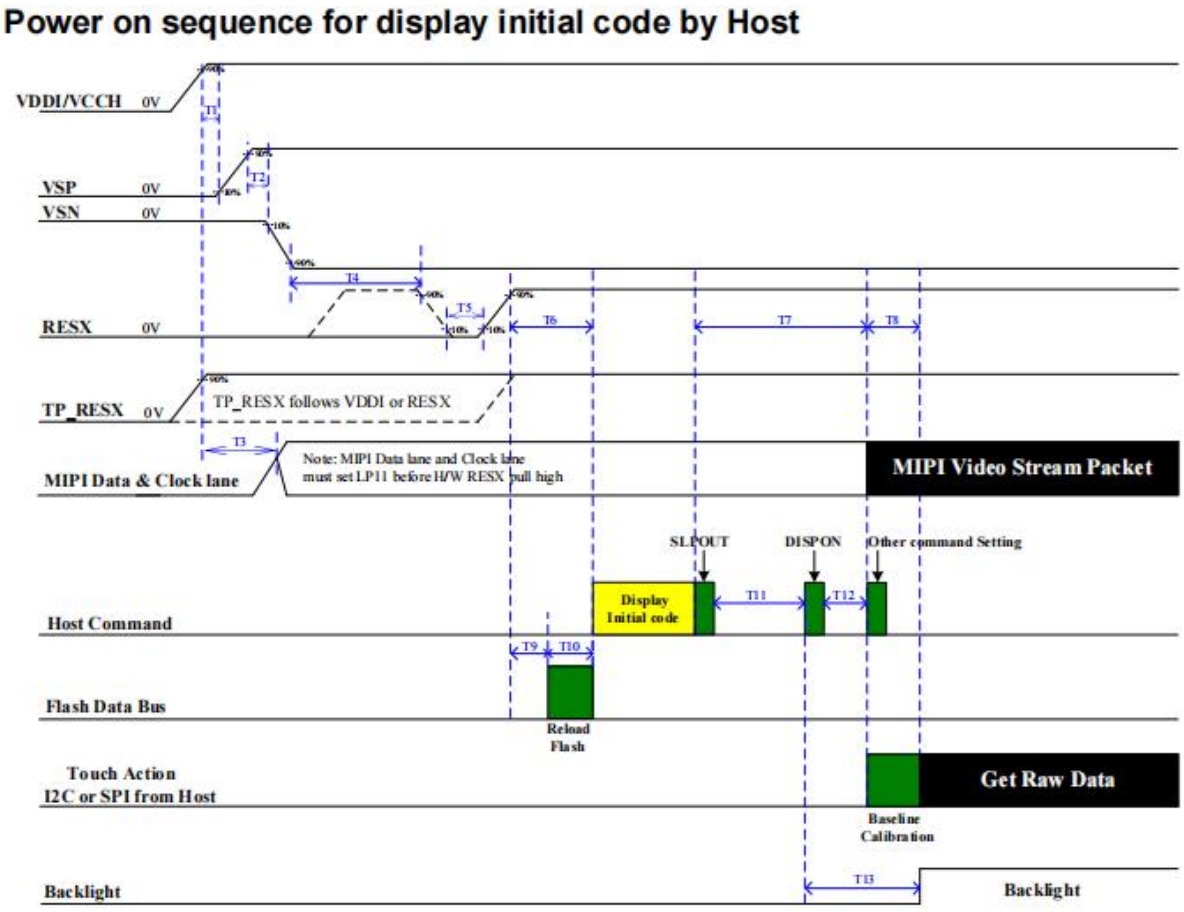


Figure 8.2: Power on sequence by Host

Symbol	Description	Min	Max	Unit	Note
T1	VDD1 to VSP	1	-	ms	
T2	VSP to VSN	1	-	ms	
T3	VDD1 to MIPI Lane	1	-	ms	
T4	Power Ready to Global Reset	1	-	ms	
T5	Global Reset Keep Low	15	-	us	TP Reset is the same
T6	Global Reset to Display Initial Code by Host	120	-	ms	
T7	Video Stream Start and Host TP Data Bus Active	140	-	ms	
T8	AP Start to Get Raw Data	30	-	ms	
T9	Reset to Flash Reload	-	5	ms	
T10	Flash Reload Time	-	115	ms	
T11	Sleep Out to Display On	10	-	ms	
T12	Display On to IC Ready	20	-	ms	
T13	Display On Command to BL On time	40	-	ms	

Power off sequence for external power

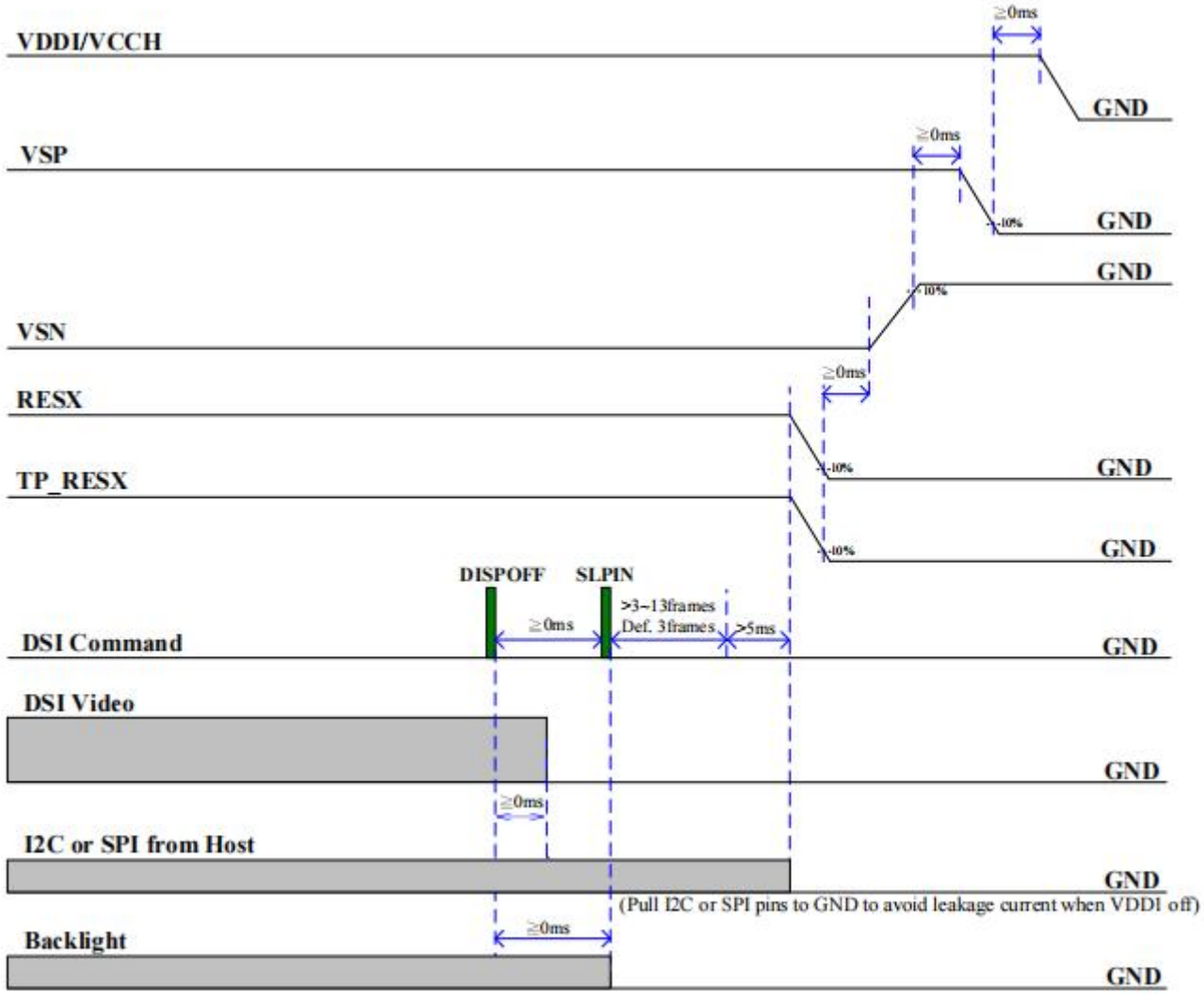


Figure 8.3: Power off sequence for external power

5.2 DC Characteristics

Parameter		Symbol	Spec.			Unit	Note
			Min.	Typ.	Max.		
Input high level voltage		V_{IH}	0.7VDDI	-	VDDI	V	1.65V≦VDDI≦1.95V
Input low level voltage		V_{IL}	0	-	0.3VDDI	V	
Output high level voltage		V_{OH}	VDD-0.2V	-	VDDI	V	1.65V≦VDDI≦1.95V
Output low level voltage		V_{OL}	0	-	0.2V	V	
Input leakage current		I_{IL1}	-1	-	+1	uA	-
VDDI output voltage		VDDI	1.65	-	1.95	V	-
VCCH output voltage		VCCH	1.65	-	1.95	V	-
VSP output voltage		VSP	4.5	-	6.2	V	-
VSN output voltage		VSN	-6.2	-	-4.5	V	-
VDDD output voltage		VDDD	1.19	1.32	1.45	V	-
VDDH output voltage		VDDH	1.19	1.32	1.45	V	-
VGMP output voltage		VGMP	3.1	4.8	6	V	-
VGMN output voltage		VGMN	-6	-4.8	-3.1	V	-
VCOM output voltage		VCOM	-3	-1	-0.08	V	-
VCI output voltage		VCI	2.3	2.6	3	V	-
VCL output voltage		VCL	-3	-2.6	-2.3	V	-
VGH output voltage		VGH	VGHO+1	16	20	V	-
VGL output voltage		VGL	-15	-12	-6.7	V	-
VGHO output voltage		VGHO	7.3	15	VGH-1	V	-
VGLO output voltage		VGLO	VGL+1	-10	-5.3	V	-
TPVDD output voltage		TPVDD	4.6	4.7	4.9	V	-
VPP output voltage (OTP power)		VPP	8	8.25	8.5	V	-
Source output current	VSO=5V at positive, VOUT=4V	IOSH	-	-	200	uA	-
	VSO=-5V at negative, VOUT=-4V	IOSL	-	-	200	uA	-
Source output offset deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255	-	50	-	-	mV	Graycode 0 limit: GP23R>GND+0.4V GN23R<GND-0.4V
	Graycode = 15 ~ 31 Graycode = 208 ~ 240	-	40	-	-	mV	
	Graycode = 32 ~ 207	-	30	-	-	mV	
VDDI current consumption	Standby mode	-	-	-	450	uA	VDD1 = 1.8V VSP = 5.5V VSN = -5.5V TA = 25℃
VSP current consumption		-	-	-	150	uA	
VSN current consumption		-	-	-	55	uA	
VDDI current consumption	Normal mode		-	-	TBD	uA	VDD1 = 1.8V VSP = 5.5V VSN = -5.5V TA = 25℃
VSP current consumption			-	-	TBD	uA	
VSN current consumption			-	-	TBD	uA	
VOTP operation current		VOTP	-	-	8	mA	TA = 25℃
Oscillator tolerance		△OSC	-3	-	3	%	TA = 25℃

Table 12.2: DC characteristic

5.3 AC Characteristics

Reset input timings

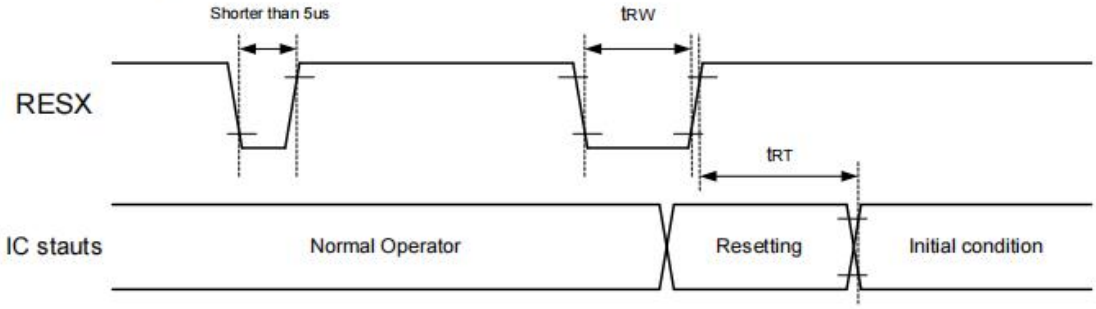


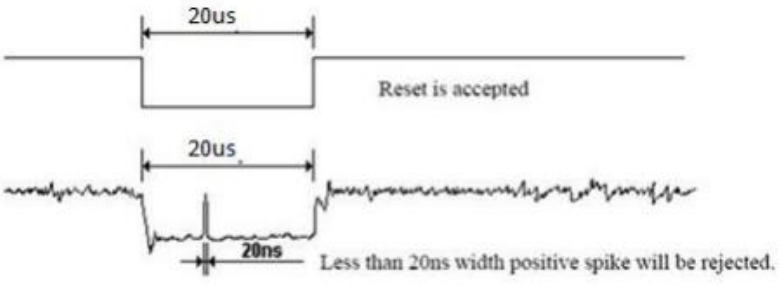
Figure 12.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	20	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for HW reset.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.
(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

Table 12.3: Reset timings

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.

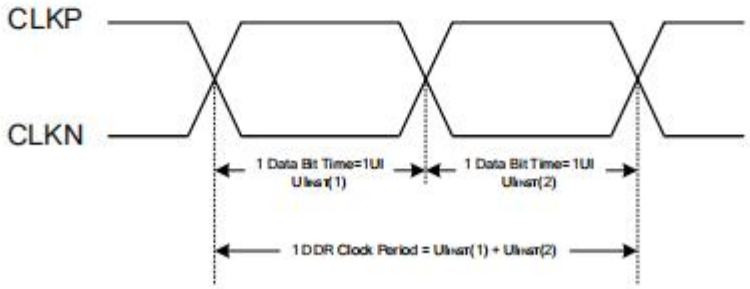


Figure 12.5: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Base on resolution 800x1280, HS=20, HBP=40, HFP=40, VS=2, VBP=8, VFP=20 and frame rate = 60HZ.
- The total bit rate is about **850Mbps** of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.**(The max. limitation lane speed=1Gbps/ lane)**

- The total bit rate is about **1.7Gbps** of 2 data lane 24-bit data format/ 1.275Gbps of 2 data lane 18-bit data format/1.133Gbps of 2 data lane 16-bit data format.**(The max. limitation lane speed=1Gbps/ lane)**

- The total bit rate is **1.7Gbps** of 3 data lane 24-bit data format/ 1.275G bps of 3 data lane 18-bit data format/1.133Gbps of 3 data lane 16-bit data format.**(The max. limitation lane speed=800Mbps/ lane)**

- The total bit rate is **1.7Gbps** of 4 data lane 24-bit data format/ 1.275Gbps of 4 data lane 18-bit data format/ 560Mbps of 4 data lane 16-bit data format.**(The max. limitation lane speed=600Mbps/ lane)**

Table 12.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.
The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.
All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.
Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

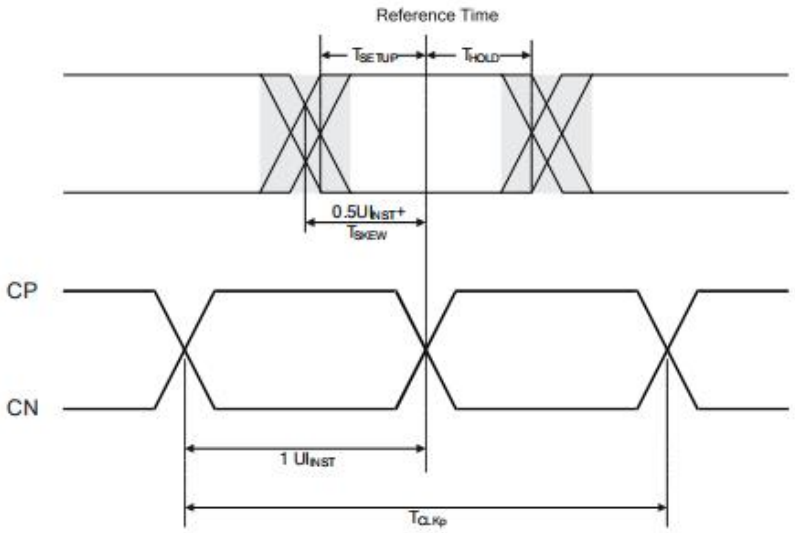


Figure 12.6: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Table 12.12: Data to Clock Timing Specifications

Burst Mode Data Transmission

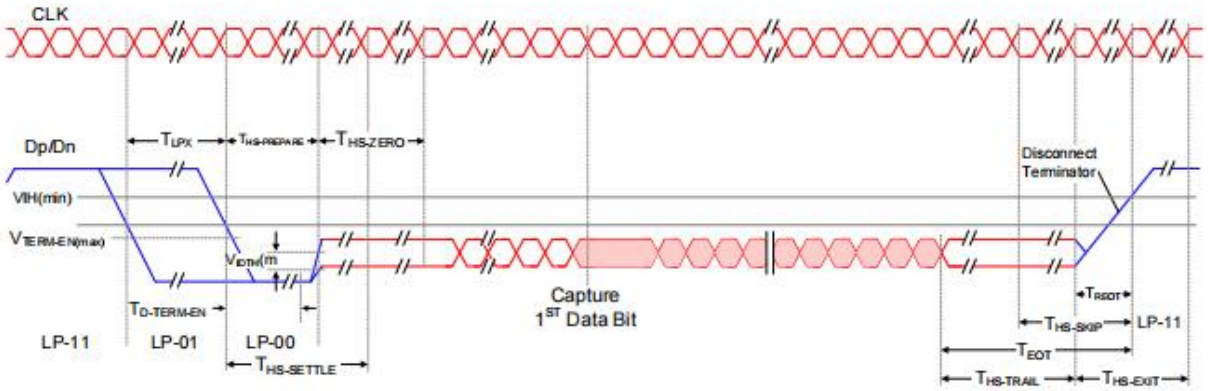


Figure 12.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

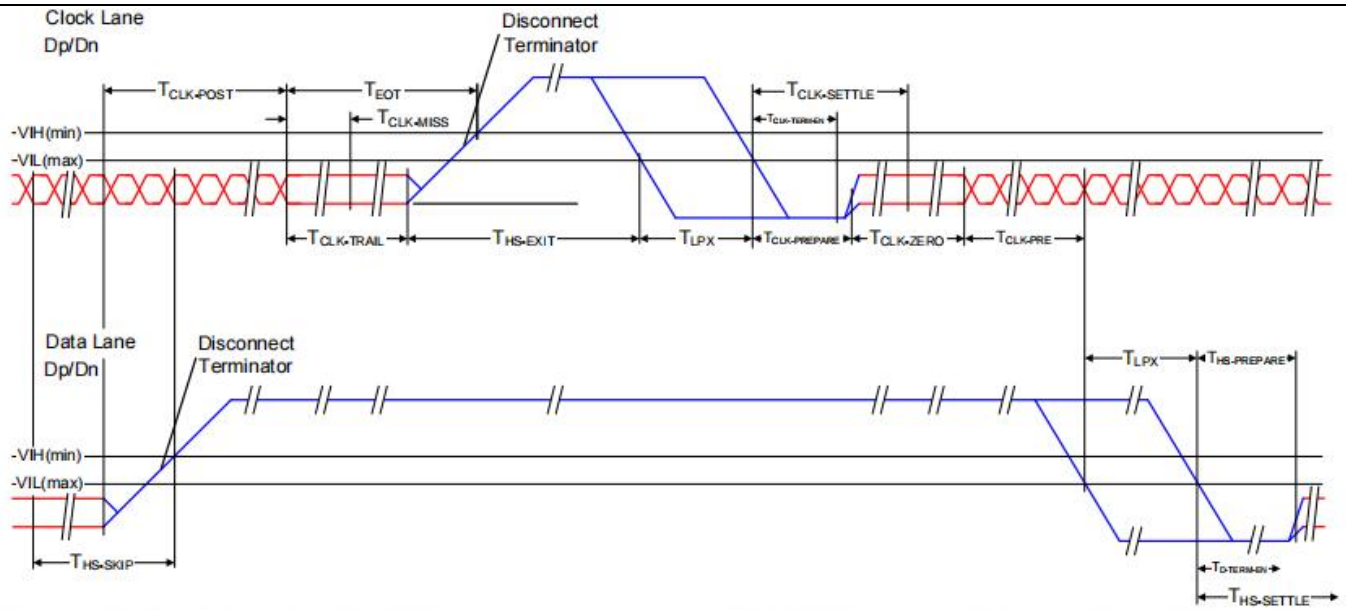


Figure 12.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Timings for DSI Video mode

Vertical Timings

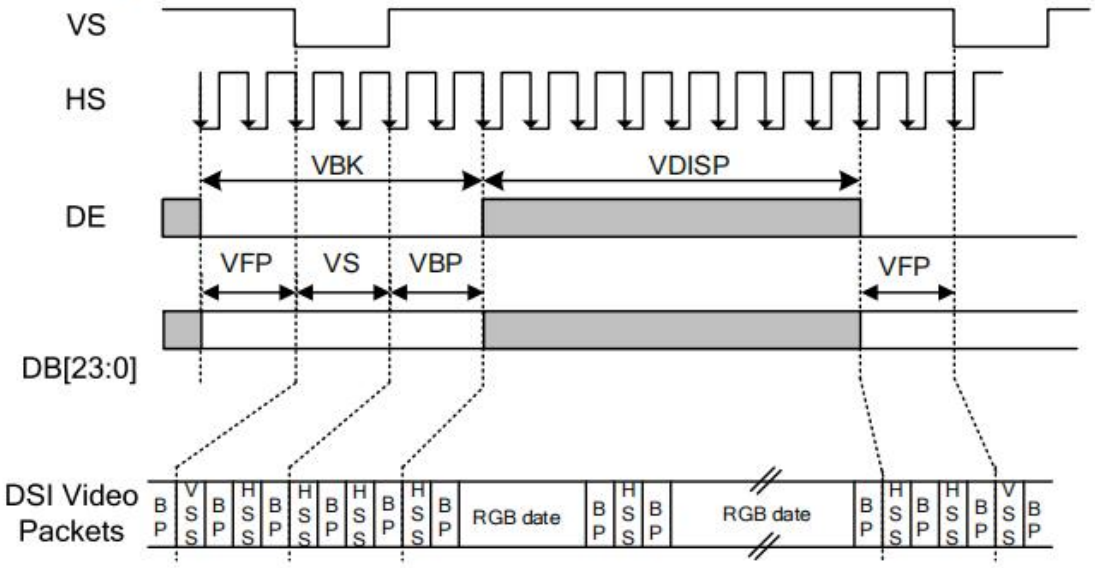


Figure 12.9: Vertical Timings for DPI I/F

Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	4	200 Note(1)	Line
Vertical front porch	VFP	-	4	20	200	Line
Vertical back porch	VBP	-	2	10	200 Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	8	34	250	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Table 12.13: Vertical Timings for RGB I/F

Horizontal Timings

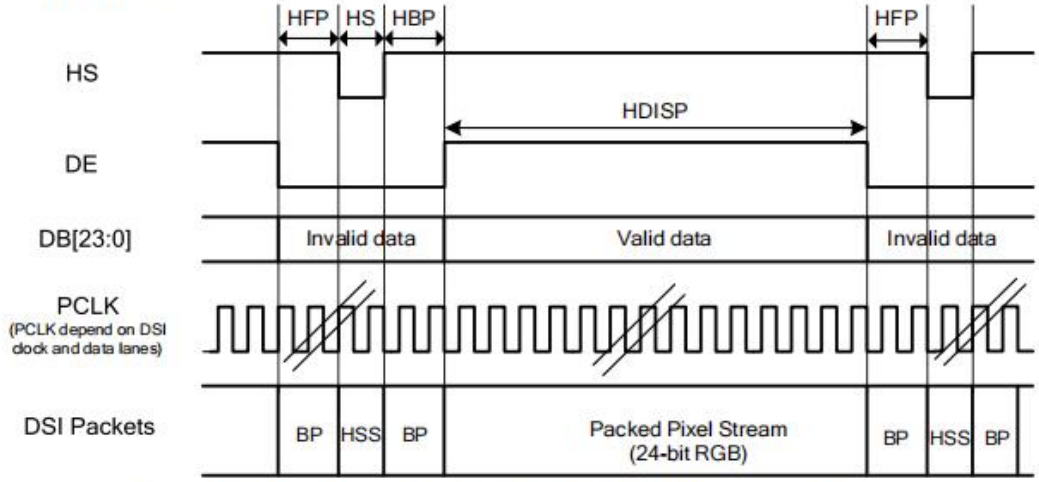


Figure 12.10: Horizontal Timing for DSI Video mode I/F

Resolution=800x1280 (T_A=25°C, IOVCC=1.8V, VCIP=VCI=VCCH=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	18	-	DCK
Horizontal back porch	HBP	-	5	18	-	DCK
Horizontal front porch	HFP	-	5	18	-	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	54 (Note1)	-	DCK
Horizontal active area	HDISP	-	-	800	-	DCK
Pixel Clock	PCLK	-	63.06 (Note2)	67.33 (Note2)	-	MHz

Note 1: HS+HBP > 0.5us.
Note 2: Pixel Clock = (HBLK+HDISP) * (VBK+VDISP) * Frame rate, Frame rate=60Hz.

Table 12.14: Horizontal Timings for DSI Video mode I/F

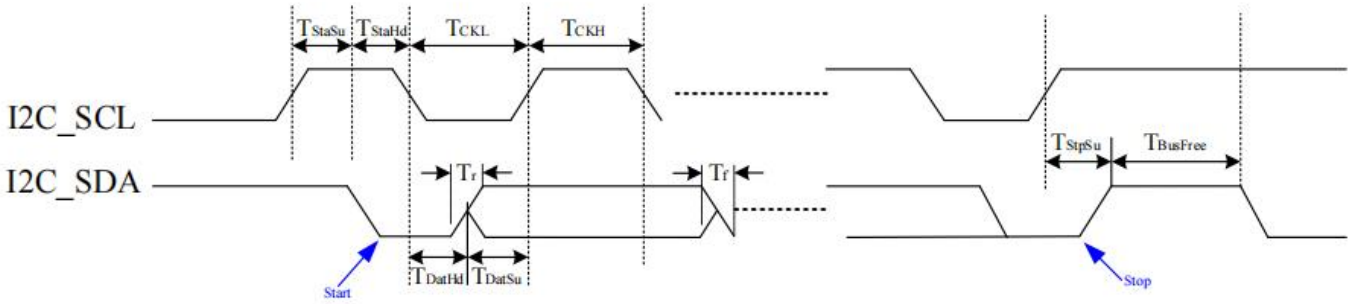


Figure 10.9: I2C Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Working Frequence	Fclk	0	-	400	KHz
I2C Clock Low	T_{CKL}	1300	-	-	ns
I2C Clock High	T_{CKH}	600	-	-	ns
I2C Clock and Data rising time	T_r	-	-	300	ns
I2C Clock and Data falling time	T_f	-	-	300	ns
I2C Data hold time	T_{DatHd}	0	-	-	ns
I2C Data setup time	T_{DatSu}	100	-	-	ns
I2C Start Condition hold time	T_{StaHd}	600	-	-	ns
I2C Start Condition setup time	T_{StaSu}	600	-	-	ns
I2C Stop Condition setup time	T_{StpSu}	600	-	-	ns
I2C Bus free time	$T_{BusFree}$	1300	-	-	ns

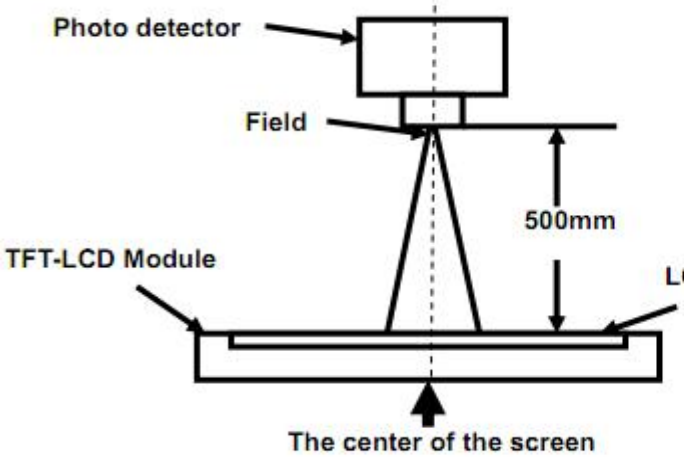
Table10.10: I2C Timing Table

6. Optical Specifications

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10) B/L ON	θ_T	Φ=90°(12 o'clock)	75	80	-	deg	Note2
	θ_B	Φ=270°(6 o'clock)	75	80	-	deg	Note2
	θ_L	Φ=180°(9 o'clock)	75	80	-	deg	Note2
	θ_R	Φ=0°(3 o'clock)	75	80	-	deg	Note2
Response Time	T_{ON}	Normal θ=Φ=0°	-	15	17	msec	Note4
	T_{OFF}		-	15	17	msec	Note4
Contrast Ratio	CR		1000	1500	-	-	Note1 Note3
Color Chromaticity	W_X		TBD	TBD	TBD	-	Note1 Note5
	W_Y		TBD	TBD	TBD	-	Note1 Note5
Luminance	L		220	270	-	cd/m²	Note1 Note7
Luminance Uniformity	Y_U		75	80	-	%	Note1 Note6
NTSC	-		55	60	-	%	-

Note 1:Definition of optical measurement system

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Fig 1

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

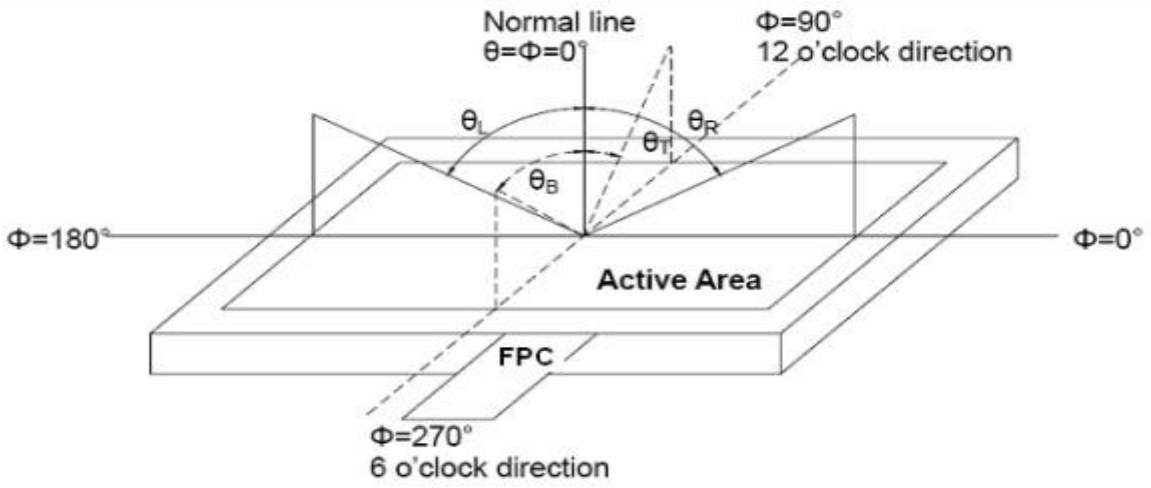


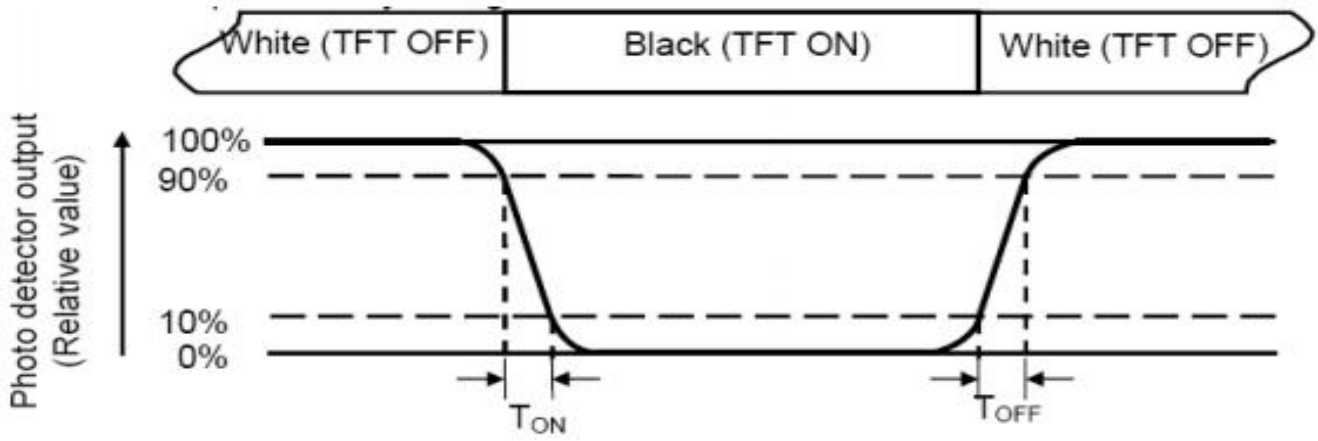
Fig 2 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.3-a/b

Note 7:Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

For more information see FIG.3-a/b

Note 8:

H,V : Active area(see Figure b)

Light spot size ⌀ =5mm(BM-5) or ⌀ =7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens. test spot position : see Figure b.

measurement instrument : TOPCON's luminance meter SR-3A or BM-7 or compatible (see Figure 1).

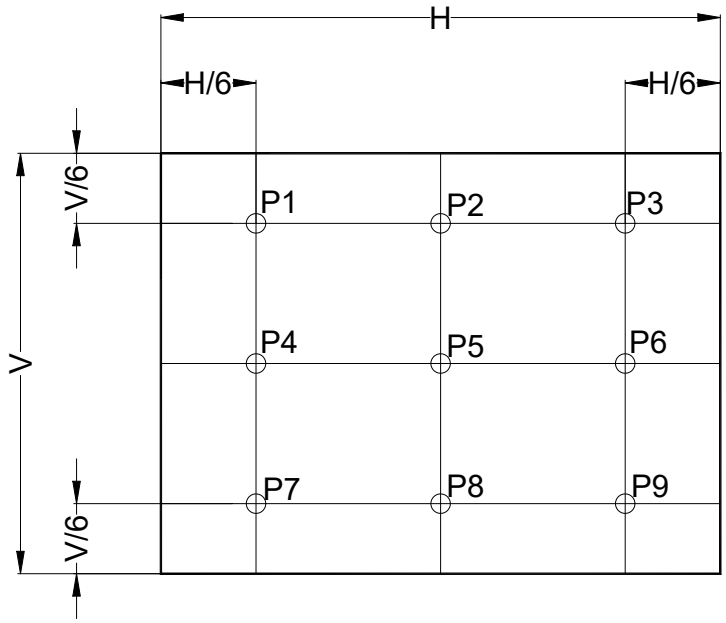


Fig. 3-b Definition of points

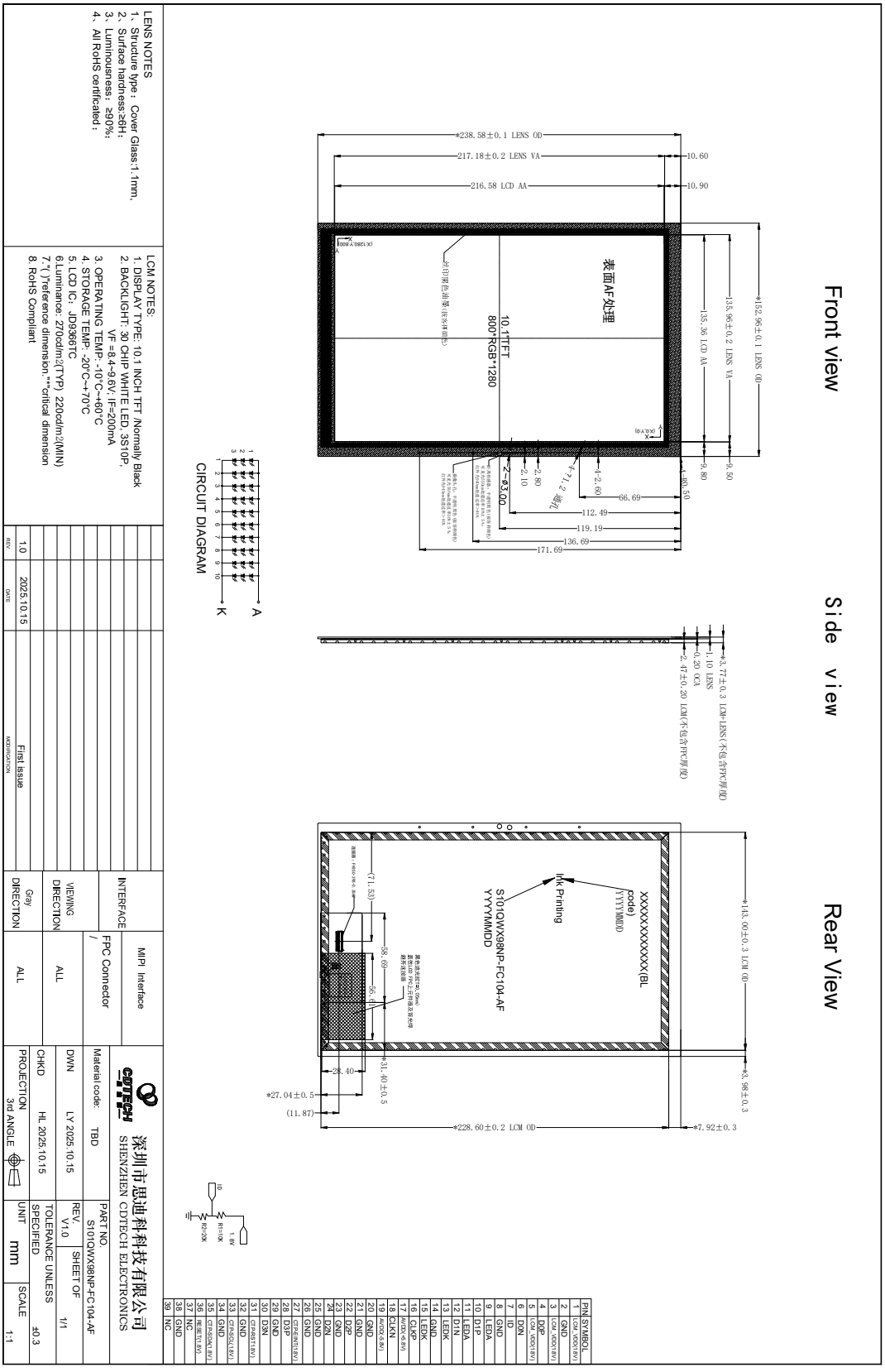
7. Reliability Test Items

Test Item	Test Conditions	
High Temperature Storage	Ta= +70℃	96hrs
Low Temperature Storage	Ta= -20℃	96hrs
High Temperature Operation	Ta= +60℃	96hrs
Low Temperature Operation	Ta= -10℃	96hrs
High Temperature and Humidity Storage	Ta= +60℃, 90% RH	96hrs
Thermal Shock (Non-operation)	-10℃/30 min ~ +60℃/30 min for 20 cycles Start with cold temperature end with high temperature	
Electro Static Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B R=330Ω,C=150pF	
Vibration	Sweep: 10Hz~55Hz~10Hz Stroke: 1.5mm 2 hrs for each direction of X .Y. Z.	
Mechanical Shock	60G 6ms,±X,±Y,±Z 3 times for each direction	
Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

Notes: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample will not be accepted if appear these defects:

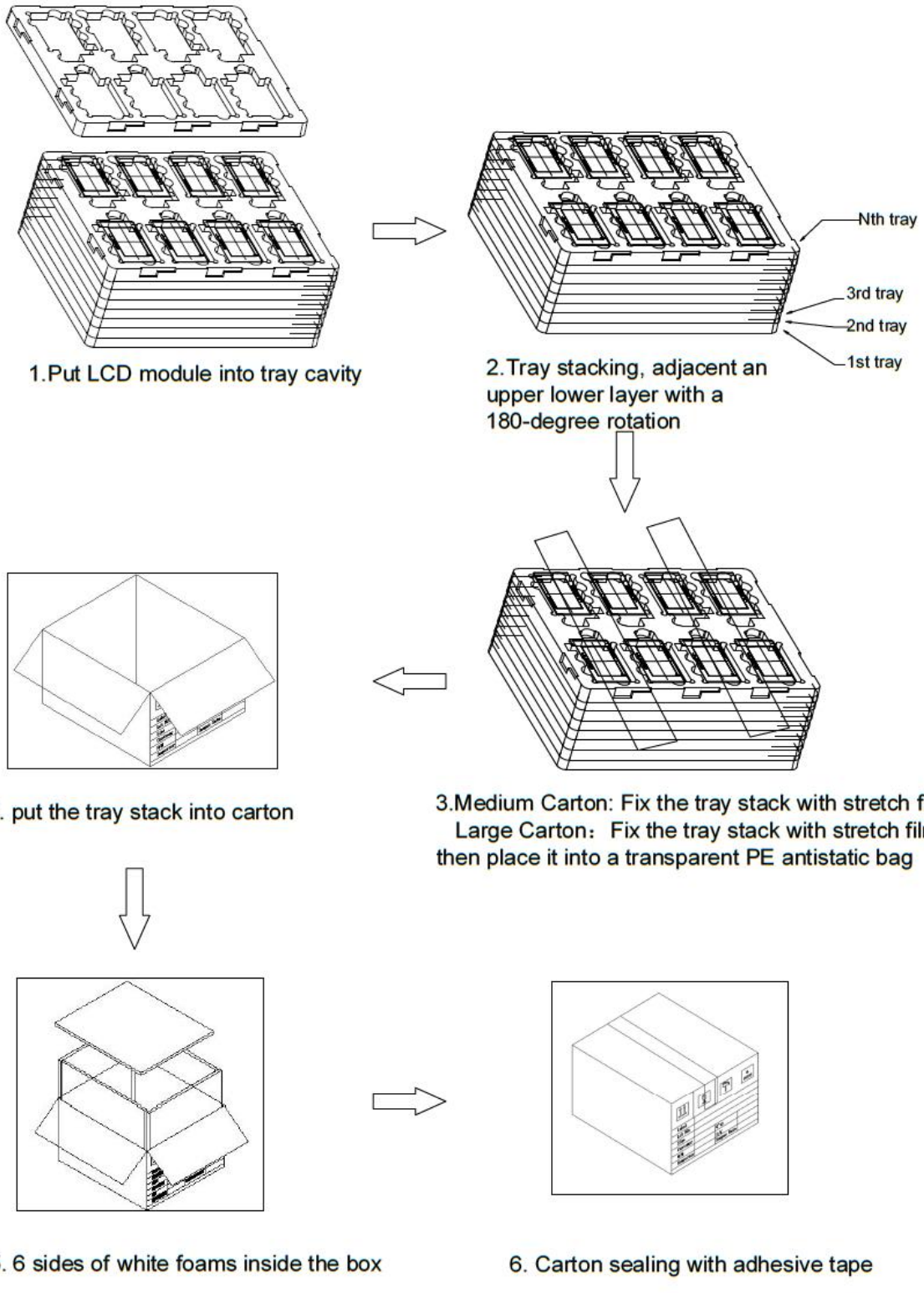
1). Air bubble in the LCD
2). Seal leak or Glass crack
3). Non display or abnormal display
4). Brightness reduction >50%

8. Mechanical Drawing



9. Packing

Packing Method



10. Precautions for Use of LCD modules

10.1 Handling Precautions

10.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketene
- Aromatic solvents

10.1.6. Do not attempt to disassemble the LCD Module.

10.1.7. If the logic circuit power is off, do not apply the input signals.

10.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1. Be sure to ground the body when handling the LCD Modules.

10.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1.When storing the LCD modules,avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2.The LCD modules should be stored under the storage temperature range if the LCD modules will be stored for a long time,the recommend condition is :

Temperature : 0℃ ~40℃ Relatively humidity: ≤80%

10.2.3.The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

10.4 Packaging instructions

When the customers using trays, they have to stack the adjacent trays in a 180° staggered to prevent pressure that could cause product damage.